MCM60256A
MCM60L256A

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Advance Information

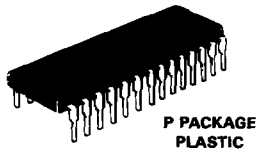
32K x 8 Bit CMOS Static Random Access Memory

The MCM60256A is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the minimum cycle time is 85 ns.

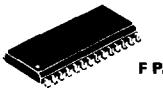
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current for MCM60L256A is 2 μA (T_A = 25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 45 ns (MCM60256A-85). Thus the MCM60256A is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

The MCM60256A is offered in a 600 mil, 28 pin plastic dual-in-line package as well as the 330 mil, 28 pin plastic small outline gullwing package.

- Single 5 V Supply, ±10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L256A)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM60256A-85 and MCM60L256A-85 = 85 ns (Max)
  MCM60256A-10 and MCM60L256A-10 = 100 ns (Max)
  MCM60256A-12 and MCM60L256A-12 = 120 ns (Max)

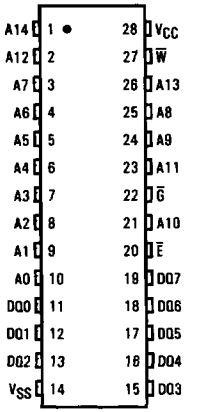


P PACKAGE
PLASTIC
CASE 710

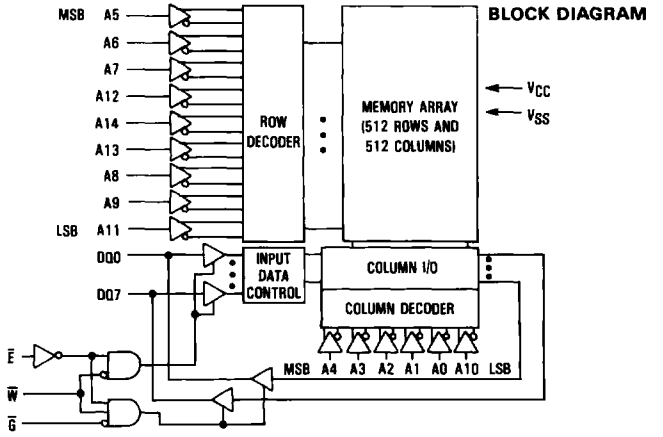


F PACKAGE
SOG
CASE 751H

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to 7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED *OPERATING CONDITIONS*. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA)	I_{CCA1}				mA
MCM60256A, MCM60L256A: t_{AVAV} = 1 μs		–	10	–	
MCM60256A, MCM60L256A-85: t_{AVAV} = 85 ns		–	–	70	
MCM60256A, MCM60L256A-10: t_{AVAV} = 100 ns		–	–	70	
MCM60256A, MCM60L256A-12: t_{AVAV} = 120 ns		–	–	70	
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA) MCM60256A, MCM60L256A: t_{AVAV} = 1 μs	I_{CCA2}	–	5	–	
MCM60256A, MCM60L256A-85: t_{AVAV} = 85 ns		–	–	60	
MCM60256A, MCM60L256A-10: t_{AVAV} = 100 ns		–	–	60	
MCM60256A, MCM60L256A-12: t_{AVAV} = 120 ns		–	–	60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	–	–	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) MCM60256A	I_{SB2}	–	2	100	μA
MCM60L256A		–	–	30	
MCM60L256A (T_A = 25°C)		–	–	2	
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	–	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	–	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

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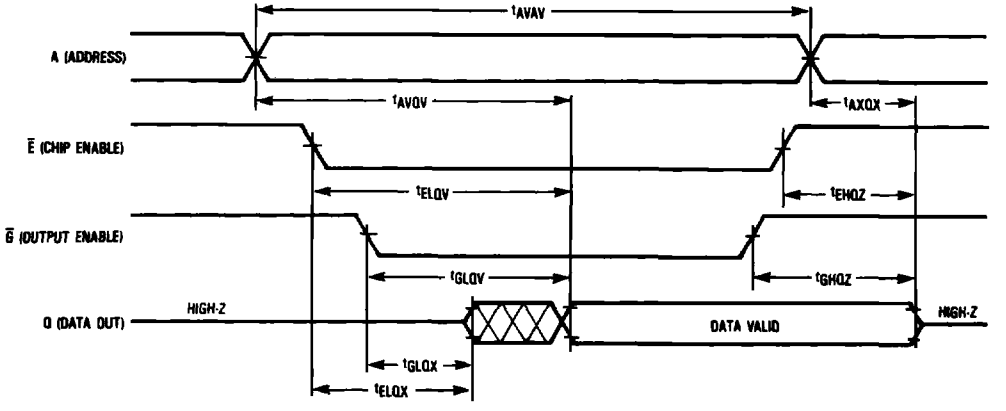
READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60256A-85 MCM60L256A-85		MCM60256A-10 MCM60L256A-10		MCM60256A-12 MCM60L256A-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	85	–	100	–	120	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	85	–	100	–	120	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	85	–	100	–	120	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	45	–	50	–	60	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	10	–	10	–	ns	–
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	10	–	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	5	–	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	30	0	50	0	60	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	30	0	40	0	50	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



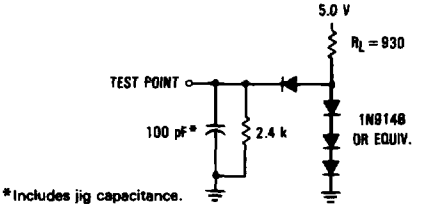


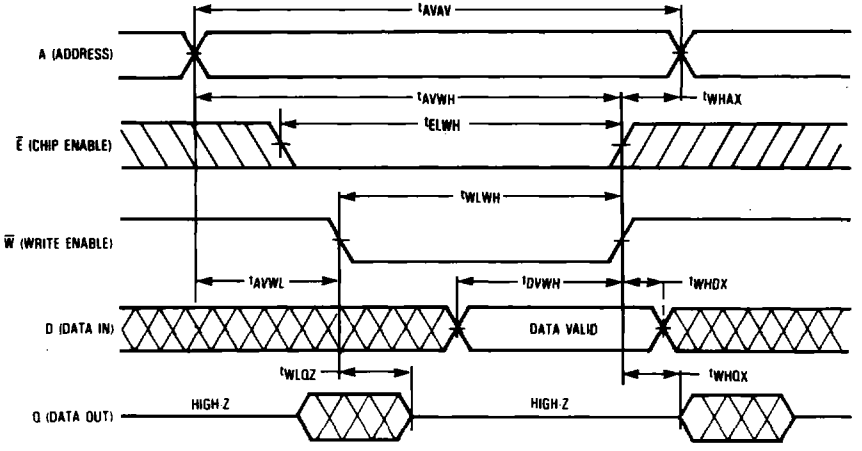
Figure 1. AC Test Load

WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60256A-85 MCM60L256A-85		MCM60256A-10 MCM60L256A-10		MCM60256A-12 MCM60L256A-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	85	–	100	–	120	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	80	–	95	–	115	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	70	–	80	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	40	–	40	–	50	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	30	0	50	0	60	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	10	–	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	5	–	5	–	5	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	65	–	90	–	100	–	ns	–

NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. *These parameters are periodically sampled and not 100% tested.*
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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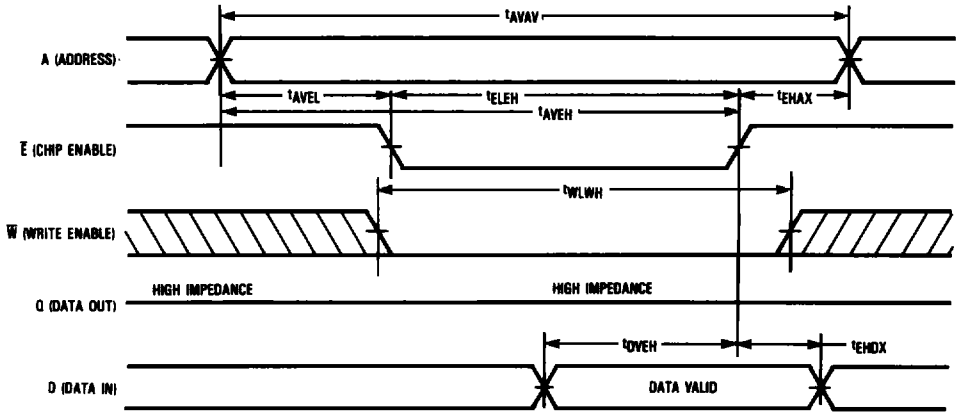
WRITE CYCLE 2 ($\overline{E}$ Controlled)

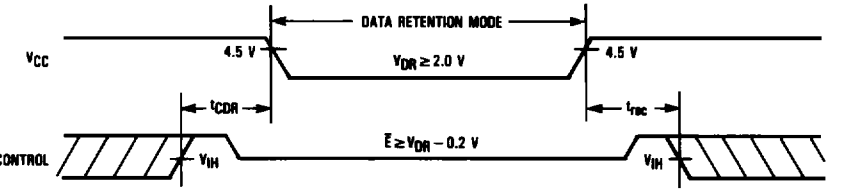


DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	MCM60256A : V_{CC} = 3.0 V	I_{CCDR}	–	–	50	µA
	V_{CC} = 5.5 V		–	–	100	
	MCM60L256A: V_{CC} = 3.0 V		–	–	20	
	V_{CC} = 5.5 V		–	–	30	
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

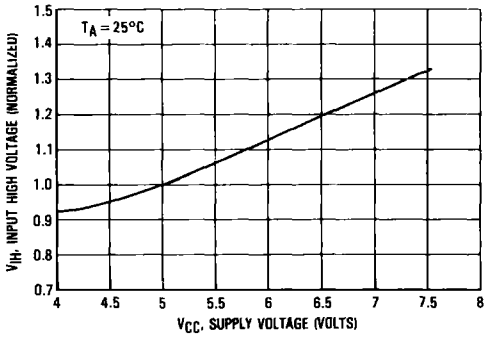


Figure 1. Input High Voltage versus Supply Voltage

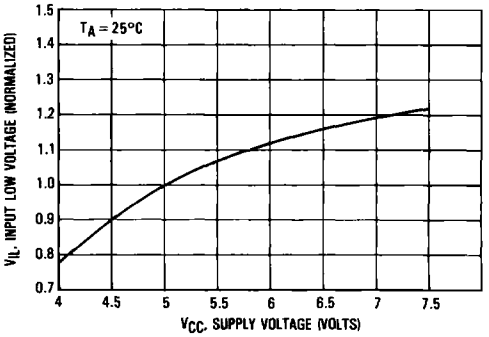


Figure 2. Input Low Voltage versus Supply Voltage

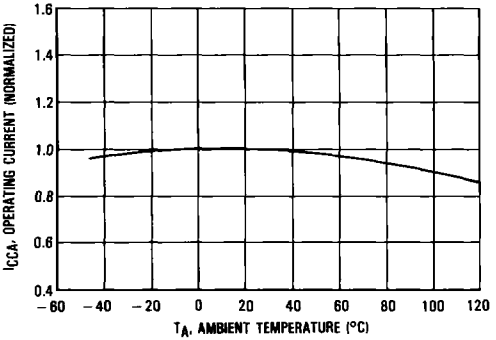


Figure 3. Operating Current versus Ambient Temperature

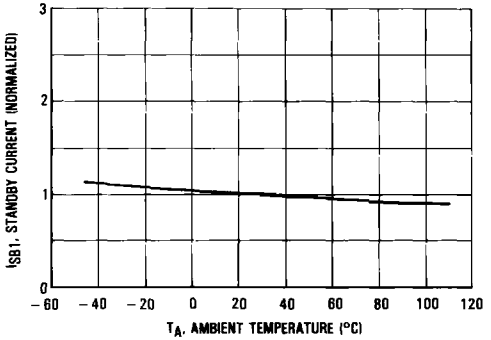


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

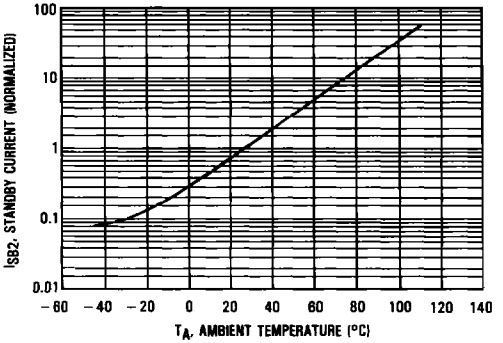


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

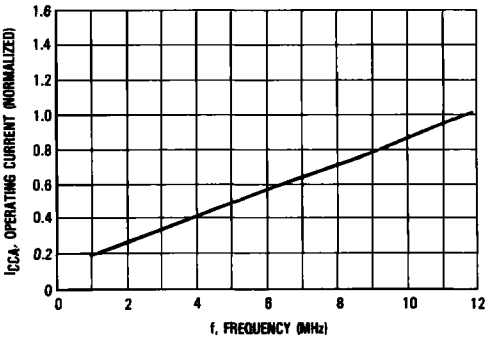


Figure 6. Operating Current versus Frequency (Read)

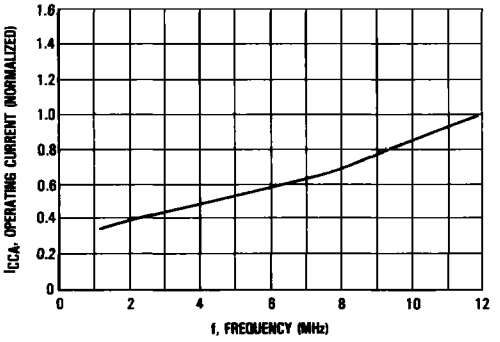


Figure 7. Operating Current versus Frequency (Write)

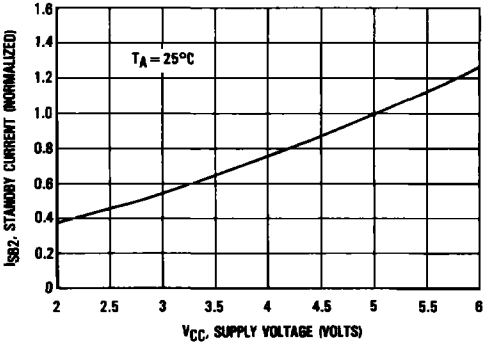


Figure 8. I_{SB2} Standby Current versus Supply Voltage

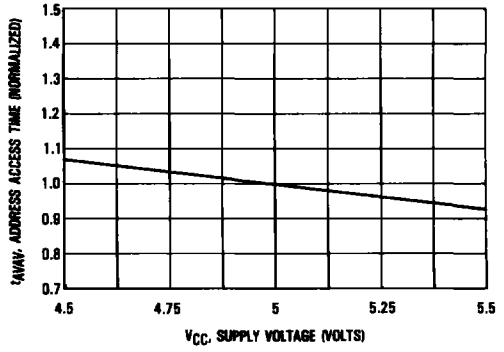


Figure 9. Access Time versus Supply Voltage

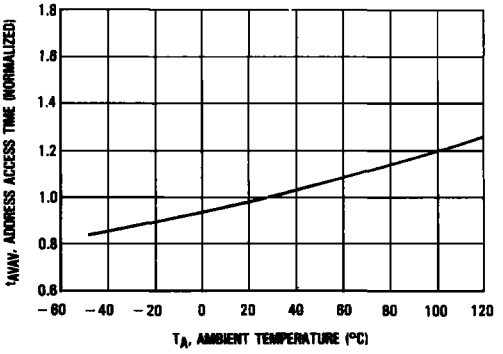
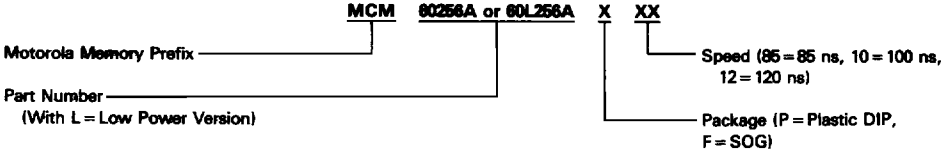


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—		
	MCM60256AP85	MCM60L256AP85
	MCM60256AP10	MCM60L256AP10
	MCM60256AP12	MCM60L256AP12
	MCM60256AF85	MCM60L256AF85
	MCM60256AF10	MCM60L256AF10
	MCM60256AF12	MCM60L256AF12

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