Features

- High Performance, High Density Programmable Logic Device
  - Typical 9 ns Pin-to-Pin Delay
  - Fully Connected Logic Array With 416 Product Terms
- Flexible Output Macrocell
  - 48 Flip-Flops - Two per Macrocell
  - 72 Sum Terms
  - All Flip-Flops, I/O Pins Feed In Independently
  - Achieves Over 80% Gate Utilization
- Enhanced Macrocell Configuration Selections
  - D- or T-Type Flip-Flops
  - Product Term or Direct Input Pin Clocking
  - Registered or Combinatorial Internal Feedback
- Low Power ATV2500BL and ATV2500BVL - 0.5 mA Stand-By (Typical)
- Backward Compatible With ATV2500H/L Software
- Proven and Reliable High Speed UV EPROM Process
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- 40-Pin Dual-In-Line and 44-Lead Surface Mount Packages
- 3.3-Volt Operation for ATV2500BV and ATV2500BVL

Temperature	ATV2500BV		ATV2500BVL	
	Com.	Ind./Mil.	Com.	Ind./Mil.
Icc (mA) at Vcc = 3.6 V	110	120	1.0	1.5

High Speed High Density UV Erasable Programmable Logic Device

2

## Preliminary

Block Diagram
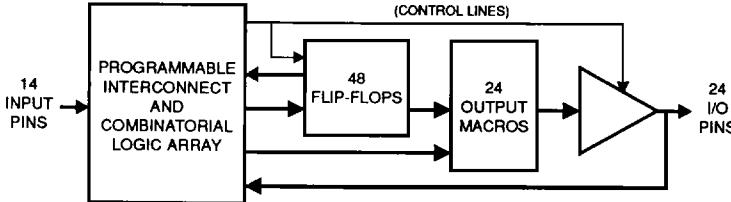
Description

The ATV2500Bs are the highest density PLDs available in a 40-pin package. With their fully connected logic array and flexible macrocell structure, high gate utilization is easily obtainable.

The ATV2500Bs are organized around a single universal input bus. All pin and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop. *(continued)*

## Pin Configurations

Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bidirectional Buffers
I/O 0,2,4..	"Even" I/O Buffers
I/O 1,3,5..	"Odd" I/O Buffers

Functional Logic Diagram ATV2500B/BV
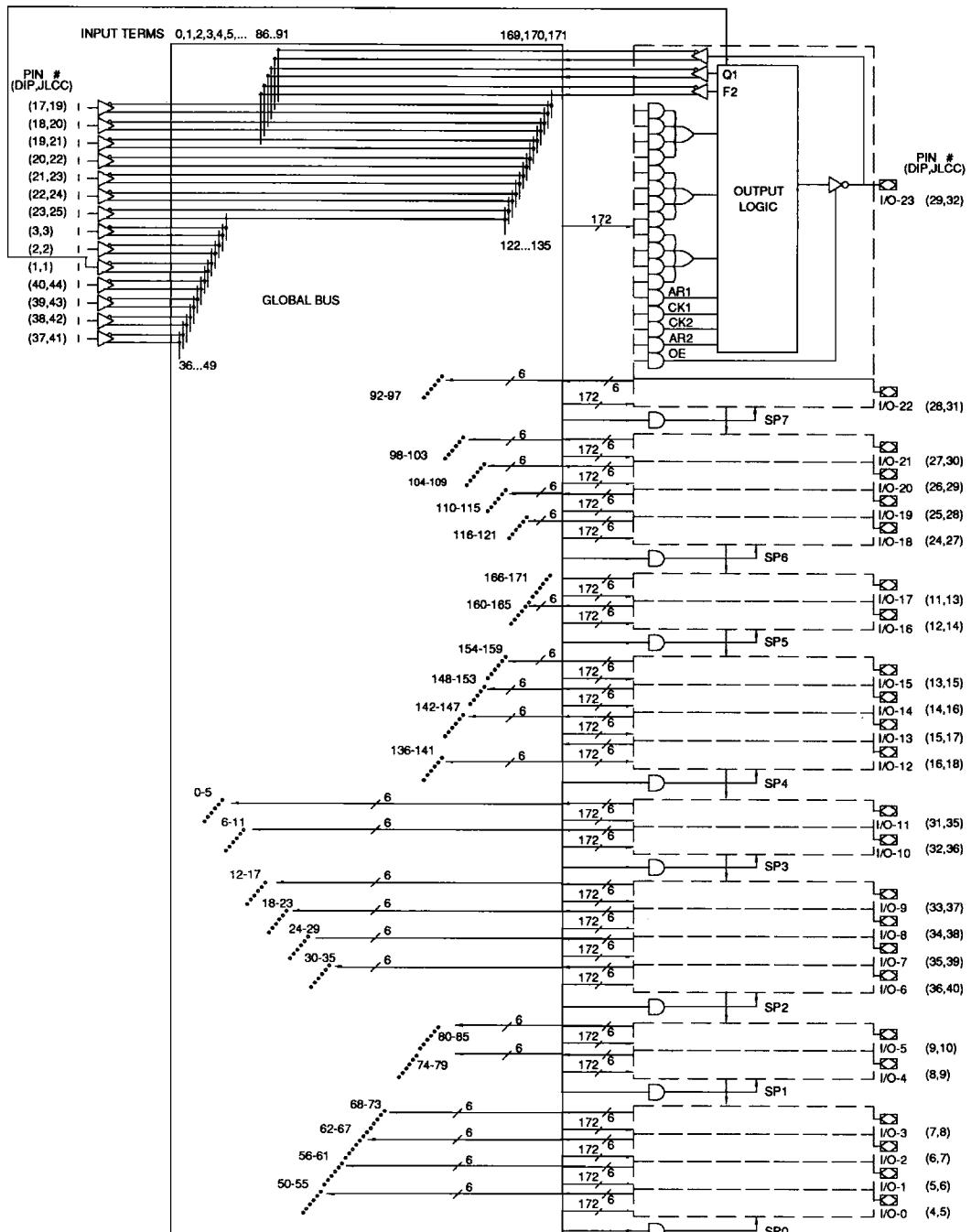
Description (Continued)

In the ATV2500Bs, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with no performance penalty. Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power up.

The ATV2500BV and ATV2500BVL are low voltage compatible devices with speeds as fast as 20 ns. Power dissipation is as low as 2.5 mW at 3.6 volts. All performance parameters are specified over the 3.0 V to 5.5 V range. These devices provide the optimum low power PLD solution with full CMOS output levels. They significantly reduce total system power, allowing battery-powered operation.

Functional Logic Diagram Description

The ATV2500B functional logic diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the single global bus.

The ATV2500Bs are straightforward and uniform PLDs. The 24 macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) feedback F2[1] true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

Note: 1. Either the flip-flop input (D/T2) or output (Q2) may be fed back in the ATV2500Bs.

Operating Modes

Mode	40-Pin DIP	21	2	38	23	20	V$_{CC}$(10)	Odd I/Os	Even I/Os
	44-Lead SMD	23	2	42	25	22	V$_{CC}$(11,12)	Odd I/Os	Even I/Os
"PLD"		X[1]	X	X	X	X	4.5 V - 5.5 V[3]	I/O	I/O
Program		V$_{PP}$	X	X	X	V$_H$ [2]	6 V	D$_{IN}$	N.C.
PGM Verify		V$_{PP}$	X	X	X	V$_{IL}$	6 V	D$_{OUT}$	V$_{OH}$
PGM Inhibit		V$_{PP}$	X	X	X	V$_{IH}$	6 V	High Z	High Z
Preload Q1		⊓	X	V$_H$	V$_{IL}$/V$_{IH}$	V$_{IL}$	4.5 V - 5.5 V[3]	D$_{IN}$(Even/Odd)	V$_{IH}$
Preload Q2		⊓	X	V$_H$	V$_{IL}$/V$_{IH}$	V$_{IH}$	4.5 V - 5.5 V[3]	D$_{IN}$(Even/Odd)	V$_{IH}$
Observe Q2		X	V$_H$	X	X	X	4.5 V - 5.5 V[3]	D$_{OUT}$	D$_{OUT}$

Notes: 1. X can be V$_{IL}$ or V$_{IH}$.
2. V$_H$ = 11.0 V to 14.0 V.
3. 3.0 V to 5.5 V for ATV2500BV, ATV2500BVL.

Absolute Maximum Ratings*

Temperature Under Bias.................-55°C to +125°C

Storage Temperature......................-65°C to +150°C

Voltage on Any Pin with
Respect to Ground.........................-2.0 V to +7.0 V[1]

Voltage on Input Pins
with Respect to Ground
During Programming...................-2.0 V to +14.0 V[1]

Programming Voltage with
Respect to Ground......................-2.0 V to +14.0 V[1]

Integrated UV Erase Dose .... 7258 W·sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

		ATV2500B	ATV2500BL	ATV2500BV	ATV2500BVL
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	3.0 V - 5.5 V	3.0 V - 5.5 V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Output Logic, Registered [1]
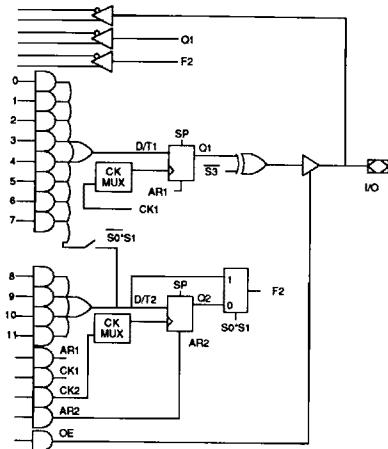
Output Logic, Combinatorial [1]
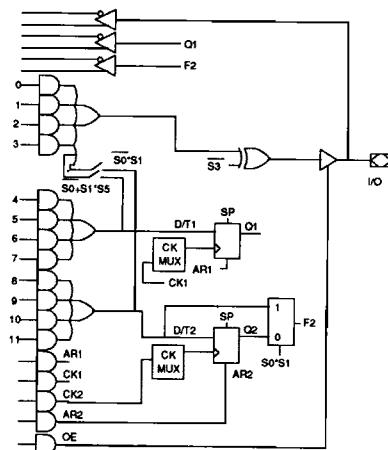
Note: 1. These diagrams shows equivalent logic functions, not necessarily the actual circuit implementation.

S2 = 0		Terms In		
S1	S0	D/T1	D/T2	Output Configuration
0	0	8	4	Registered (Q1); Q2 FB
1	0	12	4[1]	Registered (Q1); Q2 FB
1	1	8	4	Registered (Q1); D/T2 FB

Note: 1. These four terms are shared with D/T1.

S2 = 1			Terms In		
S5	S1	S0	D/T1	D/T2	Output Configuration
X	0	0	4[1]	4	Combinatorial (8 Terms); Q2 FB
X	0	1	4	4	Combinatorial (4 Terms); Q2 FB
X	1	0	4[1]	4[1]	Combinatorial (12 Terms); Q2 FB
1	1	1	4[1]	4	Combinatorial (8 Terms); D/T2 FB
0	1	1	4	4	Combinatorial (4 Terms); D/T2 FB

Note: 1. These four terms are shared with D/T1.

S3	Output Configuration
0	Active Low
1	Active High

S4	Register 1 Type
0	D
1	T

S5	Register 2 Type
0	D
1	T

S6	Q1 CLOCK
0	CK1
1	CK1 · PIN1

S7	Q2 CLOCK
0	CK2
1	CK2 · PIN1

Clock Option
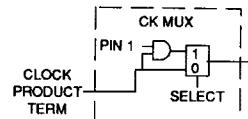
D.C. Characteristics

| Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = 5.5 V, V_{IN} = GND or V_{CC} f = 0 MHz, Outputs Open	ATV2500BL, ATV2500BVL	Com.		0.5	2 [2]	mA
				Ind.,Mil.		0.5	3 [2]	mA
			ATV2500B, ATV2500BV	Com.		80	160	mA
				Ind.,Mil.		80	180	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = 5.5 V Outputs Open V_{IN} = GND or V_{CC}	ATV2500BL, ATV2500BVL	Com.		10	15	mA/MHz
				Ind.,Mil.		10	20	mA/MHz
I_{CC3}	Power Supply Current, 3-Volt Standby	V_{CC} = 3.6 V, V_{IN} = GND or V_{CC}, f = 0 MHz, Outputs Open	ATV2500BVL	Com.		0.3	1	mA
				Ind.,Mil.		0.4	1.5	mA
			ATV2500BV	Com.		60	110	mA
				Ind.,Mil.		70	120	mA
I_{CC4}	Clocked Power Supply Current, 3-Volt	V_{CC} = 3.6 V, V_{IN} = GND or V_{CC}, Outputs Open	ATV2500BVL	Com.		5	10	mA/MHz
				Ind.,Mil.		5	15	mA/MHz
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL1}	Input Low Voltage	4.5 ≤ V_{CC} ≤ 5.5 V			-0.6		0.8	V
V_{IL2}	Input Low Voltage	3.0 ≤ V_{CC} < 4.5 V	ATV2500BV, ATV2500BVL		-0.6		0.6	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL1}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 4.5 V;	I_{OL} = 8 mA Com,Ind				0.5	V
			I_{OL} = 6 mA Mil.				0.5	V
V_{OL2}	Output Low Voltage	V_{CC} = 3.0 V, ATV2500BV, ATV2500BVL	I_{OL} = 4 mA Com.,Ind.				0.35	V
			I_{OL} = 3 mA Mil.				0.35	V
V_{OH1}	Output High Voltage	V_{CC} = 4.5 V	I_{OH} = -100 µA			V_{CC}-0.3		V
			I_{OH} = -4.0 mA			2.4		V
V_{OH2}	Output High Voltage	V_{CC} = 3.0 V, ATV2500BV, ATV2500BVL	I_{OH} = -0.4 mA			2.4		V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

2. I_{CC} Standby is 5.0 mA (max) for ATV2500BL in Cerdip and PDIP packages.

A.C. Waveforms [1]
Input Pin Clock
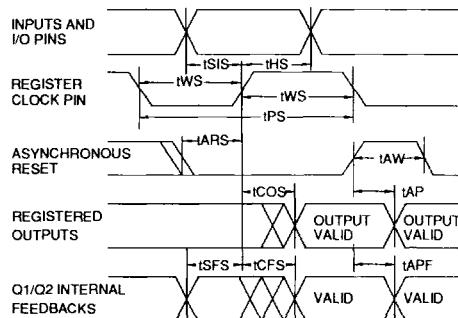
A.C. Waveforms [1]
Product Term Clock
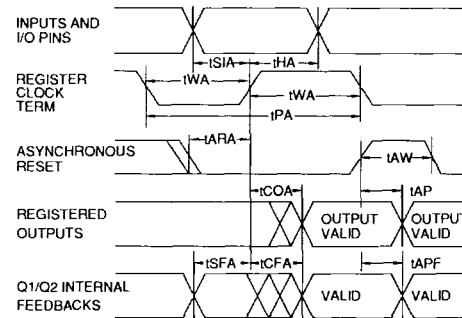
Notes: 1. Timing measurement reference is 1.5 V Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	ATV2500B -15		ATV2500B,BV/ ATV2500BL -20		ATV2500B,BV/ ATV2500BL,BVL -25		ATV2500BV/ ATV2500BL,BVL -30		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{COS}	Clock to Output		10		13/10		15/13		15	ns
t_{CFS}	Clock to Feedback	0	5	0	7/5	0	9/7	0	9	ns
t_{SIS}	Input Setup Time	9		11/13		13/15		17		ns
t_{SFS}	Feedback Setup Time	9		11/9		13/11		13		ns
t_{HS}	Hold Time	0		0		0		0		ns
t_{WS}	Clock Width	4		5/4		6/5		6		ns
t_{PS}	Clock Period	8		10/8		12/10		12		ns
F_{MAXS}	Maximum Frequency (1/t_{PS})		125		100/125		83/100		83	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	12		15		18		21		ns

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	ATV2500B -15		ATV2500B,BV/ ATV2500BL -20		ATV2500B,BV/ ATV2500BL,BVL -25		ATV2500BV/ ATV2500BL,BVL -30		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{COA}	Clock to Output		15		20		25	5	30	ns
t_{CFA}	Clock to Feedback	5	12	7/5	16	9/7	18	9	20	ns
t_{SIA}	Input Setup Time	5		7/9		9/11		20		ns
t_{SFA}	Feedback Setup Time	5		6		7		10		ns
t_{HA}	Hold Time	5		7/9		9		10		ns
t_{WA}	Clock Width	6		8/10		10/12		12		ns
t_{PA}	Clock Period	12		16/20		20/24		30		ns
F_{MAXA}	Maximum Frequency (1/t_{PA})		83		62.5/41		50/41		33	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	8		12		15		18		ns

2

A.C. Waveforms [1]
Combinatorial Outputs and Feedback
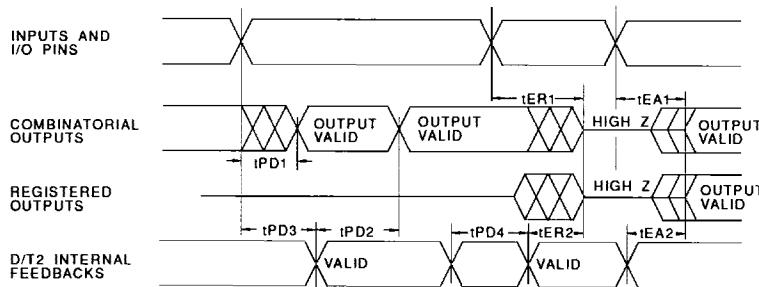
```
INPUTS AND
I/O PINS

                                                    tER1      tEA1
COMBINATORIAL          OUTPUT    OUTPUT              HIGH Z    OUTPUT
OUTPUTS                VALID     VALID                         VALID
          tPD1

REGISTERED                                          HIGH Z    OUTPUT
OUTPUTS                                                        VALID
          tPD3    tPD2            tPD4  tER2         tEA2

D/T2 INTERNAL          VALID            VALID
FEEDBACKS
```

Notes: 1. Timing measurement reference is 1.5 V Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	ATV2500B -15		ATV2500B,BV/ ATV2500BL -20		ATV2500B,BV/ ATV2500BL,BVL -25		ATV2500BV/ ATV2500BL,BVL -30		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to Non-Registered Output		15		20		25		30	ns
t_{PD2}	Feedback to Non-Registered Output		15		20/15		25/20		25	ns
t_{PD3}	Input to Non-Registered Feedback		10		15		20		25	ns
t_{PD4}	Feedback to Non-Registered Feedback		10		15/10		20/15		20	ns
t_{EA1}	Input to Output Enable		15		20		25		30	ns
t_{ER1}	Input to Output Disable		15		20		25		30	ns
t_{EA2}	Feedback to Output Enable		15		20/15		25/20		25	ns
t_{ER2}	Feedback to Output Disable		15		20/15		25/20		25	ns
t_{AW}	Asynchronous Reset/Preset Width	8		10		15		18		ns
t_{AP}	Asynchronous Reset/ Preset to Registered Output		18		22		25		30	ns
t_{APF}	Asynchronous Reset/ Preset to Registered Feedback		15		19		22		27	ns

Input Test Waveforms and Measurement Levels

```
            3.0V
AC                        AC
DRIVING     1.5V          MEASUREMENT
LEVELS                    LEVEL
            0.0V
```
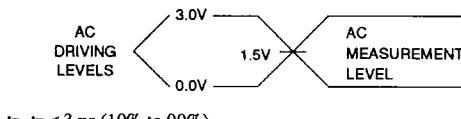
t_R, t_F < 3 ns (10% to 90%)

Output Test Load

```
R = 167 (200 MIL.)
              W        2.0 V
          C_L = 50 pF
```
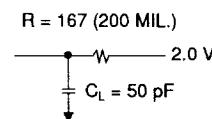
Preload and Observability of Registered Outputs

The ATV2500Bs registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 11 V to 14 V signal on DIP pin 38 (SMP lead 42). When the preload clock DIP pin 21 (SMP lead 23) is pulsed high, the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 11 V to 14 V signal on pin/lead 2. In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.
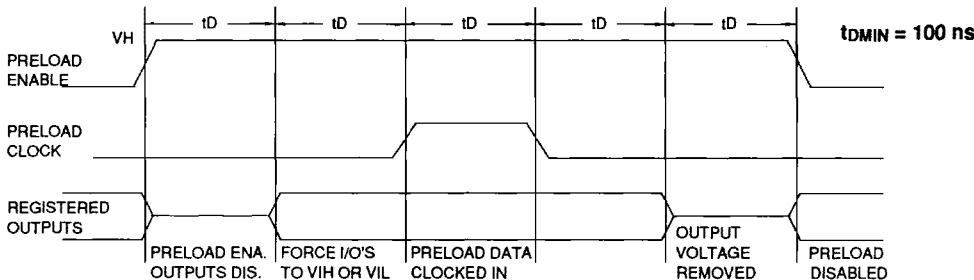

Level forced on Odd I/O pin during PRELOAD cycle.	Q Select Pin State	Even/ Odd Select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}	Low	Low	High	X	X	X
V_{IL}	Low	Low	Low	X	X	X
V_{IH}	High	Low	X	High	X	X
V_{IL}	High	Low	X	Low	X	X
V_{IH}	Low	High	X	X	High	X
V_{IL}	Low	High	X	X	Low	X
V_{IH}	High	High	X	X	X	High
V_{IL}	High	High	X	X	X	Low

Power Up Reset

The registers in the ATV2500Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.
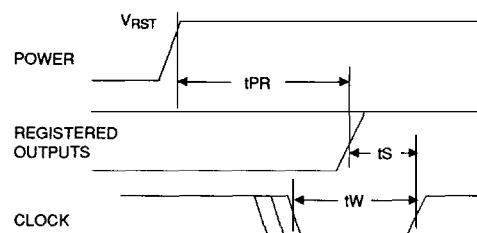
Para-meter	Description		Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns
V_{RST}	Power-Up Reset Voltage	ATV2500B/BL	3.8	4.5	V
		ATV2500BV/BVL	2.5	3.0	V

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of ATV2500B fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

Atmel CMOS PLDs

The ATV2500Bs utilize an advanced 0.8-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.

Using the ATV2500Bs Many Advanced Features

The ATV2500Bs advanced flexibility packs more usable gates into 44 leads than other PLDs. Some of the ATV2500Bs key features are:

- Fully Connected Logic Array -

Each array input is always available to every product term. This makes logic placement a breeze.

- Selectable D- and T-Type Registers -

Each ATV2500B flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.

- Buried Combinatorial Feedback -

Each macrocell's Q2 register may be bypassed to feed its input (D/T2) directly back to the logic array. This provides further logic expansion capability without using precious pin resources.

- Selectable Synchronous/Asynchronous Clocking -

Each of the ATV2500Bs flip-flops has a dedicated clock product term. This removes the constraint that all registers use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks.

Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.

- A Total of 48 Registers -

The ATV2500B provides two flip-flops per macrocell - a total of 48. Each register has its own clock and reset terms, as well as its own sum term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500B has a dedicated input path. Each of the 48 registers has its own feedback term into the array as well. These features, combined with individual product terms for each I/O's output enable, facilitate true bi-directional I/O design.

- Combinable Sum Terms -

Each output macrocell's three sum terms may be combined into a single term. This provides a fan in of up to 12 product terms per sum term with no speed penalty.

Programming Software Support

As with all other Atmel PLDs, several third party PLD development software products and programmers will support the ATV2500Bs. Atmel-Abel-5.0, Abel 5.0 and Cupl software will fully support all ATV2500B features. Also, any software which supports the ATV2500H/L will automatically support the same features on the ATV2500B. This includes Atmel-Abel-4, Abel 4.0 and above, as well as Cupl 3.0 and above.

Several third party programmers will support the ATV2500B as well. Additionally, the ATV2500B may be programmed to perform the ATV2500H/Ls functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATV2500H/L algorithm. In this case, the ATV2500B becomes a direct replacement or speed upgrade for the ATV2500H/L.

Erasure Characteristics

The entire memory array of an ATV2500B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

ATV2500B/BV

ATV2500B/BV

Ordering Information

tPD (ns)	tCOS (ns)	fMAXS (MHz)	Ordering Code	Package	Operation Range
15	10	125	ATV2500B-15JC ATV2500B-15KC ATV2500B-15LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500B-15JI ATV2500B-15KI ATV2500B-15LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500B-15KM ATV2500B-15LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500B-15KM/883 ATV2500B-15LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	13	100	ATV2500B-20JC ATV2500B-20KC ATV2500B-20LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500B-20JI ATV2500B-20KI ATV2500B-20LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500B-20KM ATV2500B-20LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500B-20KM/883 ATV2500B-20LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	83	ATV2500B-25DC ATV2500B-25JC ATV2500B-25KC ATV2500B-25LC ATV2500B-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500B-25DI ATV2500B-25JI ATV2500B-25KI ATV2500B-25LI ATV2500B-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500B-25DM ATV2500B-25KM ATV2500B-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500B-25DM/883 ATV2500B-25KM/883 ATV2500B-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

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AIMEL

Ordering Information

tPD (ns)	tCOS (ns)	fMAXS (MHz)	Ordering Code	Package	Operation Range
20	10	125	ATV2500BL-20JC ATV2500BL-20KC ATV2500BL-20LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500BL-20JI ATV2500BL-20KI ATV2500BL-20LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500BL-20KM ATV2500BL-20LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BL-20KM/883 ATV2500BL-20LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	13	100	ATV2500BL-25JC ATV2500BL-25KC ATV2500BL-25LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500BL-25JI ATV2500BL-25KI ATV2500BL-25LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500BL-25KM ATV2500BL-25LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BL-25KM/883 ATV2500BL-25LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	15	83	ATV2500BL-30DC ATV2500BL-30JC ATV2500BL-30KC ATV2500BL-30LC ATV2500BL-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500BL-30DI ATV2500BL-30JI ATV2500BL-30KI ATV2500BL-30LI ATV2500BL-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500BL-30DM ATV2500BL-30KM ATV2500BL-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500BL-30DM/883 ATV2500BL-30KM/883 ATV2500BL-30LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
20	13	100	ATV2500BV-20JC ATV2500BV-20KC ATV2500BV-20LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500BV-20JI ATV2500BV-20KI ATV2500BV-20LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500BV-20KM ATV2500BV-20LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BV-20KM/883 ATV2500BV-20LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	83	ATV2500BV-25JC ATV2500BV-25KC ATV2500BV-25LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500BV-25JI ATV2500BV-25KI ATV2500BV-25LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500BV-25KM ATV2500BV-25LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BV-25KM/883 ATV2500BV-25LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	15	83	ATV2500BV-30JC ATV2500BV-30KC ATV2500BV-30LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500BV-30JI ATV2500BV-30KI ATV2500BV-30LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500BV-30KM ATV2500BV-30LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BV-30KM/883 ATV2500BV-30LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

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Ordering Information

tPD (ns)	tCOS (ns)	fMAXS (MHz)	Ordering Code	Package	Operation Range
25	13	100	ATV2500BVL-25JC ATV2500BVL-25KC ATV2500BVL-25LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500BVL-25JI ATV2500BVL-25KI ATV2500BVL-25LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500BVL-25KM ATV2500BVL-25LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BVL-25KM/883 ATV2500BVL-25LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	15	83	ATV2500BVL-30JC ATV2500BVL-30KC ATV2500BVL-30LC	44J 44KW 44LW	Commercial (0°C to 70°C)
			ATV2500BVL-30JI ATV2500BVL-30KI ATV2500BVL-30LI	44J 44KW 44LW	Industrial (-40°C to 85°C)
			ATV2500BVL-30KM ATV2500BVL-30LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BVL-30KM/883 ATV2500BVL-30LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

ATV2500B/BV