NZF220DFT1

EMI Filter with ESD Protection

Features:

- 2 EMI/RFI Bi–directional “Pi” Low–Pass Filters
- ESD Protection Meets IEC6000–4–2, ±8 kV Contact Discharge
- Diode Capacitance: 7 – 10 pF
- Zener/Resistor Line Capacitance: 22 ±20% pF
- Low Zener Diode Leakage: 1 μA Maximum
- Zener Breakdown Voltage; 6 – 8 Volts

Benefits:

- Designed to suppress EMI/RFI Noise in Systems Subjected to Electromagnetic Interference
- Nominal Cutoff Frequency of 220 MHz (per Figure 2)
- Small Package Size Minimizes Parasitic Inductance, Thus a More “Ideal” Low Pass Filtering Response

Typical Applications:

- Cellular Phones
- Communication Systems
- Computers
- Portable Products with Input/Output Conductors

MAXIMUM RATINGS

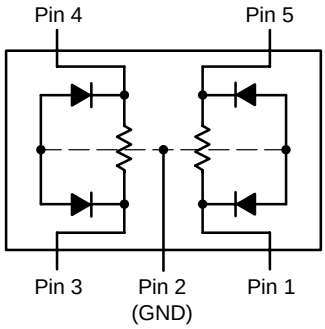
Rating	Symbol	Value	Unit
Peak Power Dissipation (Note 1.) 8 × 20 μs Pulse	P_{PK}	14	Watts
IEC6100–4–2 Contact Discharge	ESD	±8.0	kV
Maximum Junction Temperature	T_J	150	°C

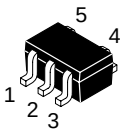
1. Between I/O Pins

ON Semiconductor™

http://onsemi.com

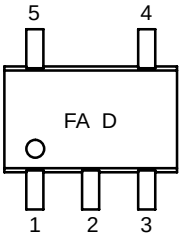
CIRCUIT DESCRIPTION





SC–88A
CASE 419A
DF SUFFIX

MARKING DIAGRAM



FA = Specific Device Code
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping
NZF220DFT1	SC–88A	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Unit
V_Z	Zener Breakdown Voltage, @ I_{ZT} = 1 mA	6.0	–	8.0	V
I_r	Zener Leakage Current, @ V_R = 3 V	N/A	–	1.0	μA
V_F	Zener Forward Voltage, @ I_F = 50 mA	N/A	–	1.5	V
Capacitance	Zener Internal Capacitance, @ 0 V Bias	7.0	–	10	pF
Capacitance	Zener/Resistor Array Line Capacitance	17.6	–	26.4	pF
Resistor	Resistance	90	–	110	Ω
F_C (Note 2.)	Cutoff Frequency	–	220	–	MHz

2. 50 Ω Source and 50 Ω Lead Termination per Figure 2

Applications Information

Suppressing Noise at the Source

- Filter all I/O signals leaving the noisy environment
- Locate I/O driver circuits close to the connector
- Use the longest rise/fall times possible for all digital signals

Reducing Noise at the Receiver

- Filter all I/O signals entering the unit
- Locate the I/O filters as close as possible to the connector

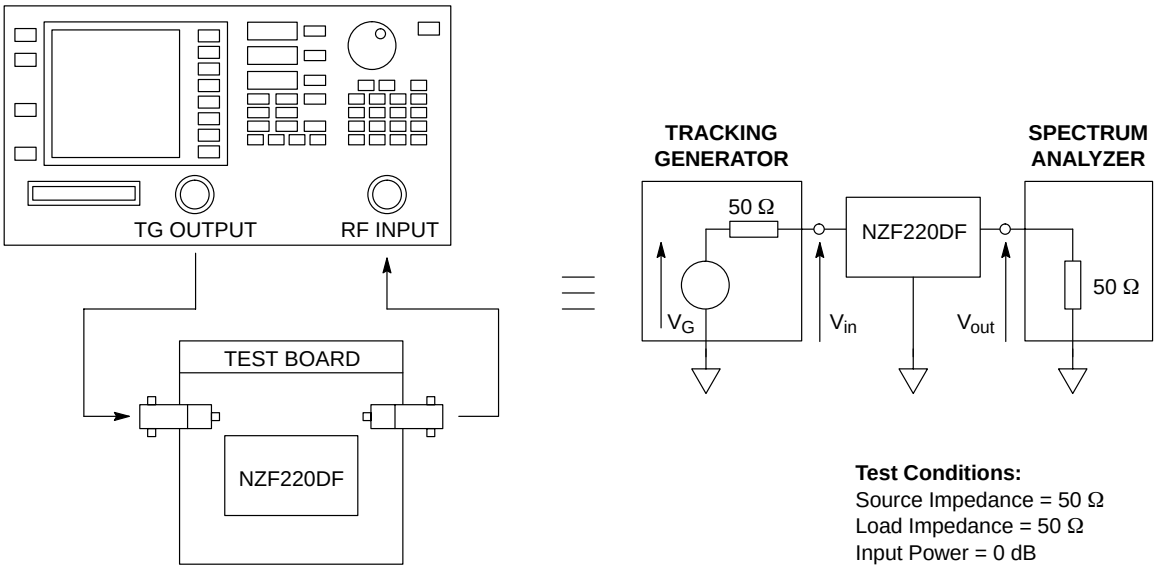
Minimizing Noise Coupling

- Use multilayer PCBs to minimize power and ground inductance
- Keep clock circuits away from the I/O connector
- Ground planes should be used whenever possible
- Minimize the loop area for all high speed signals
- Provide for adequate power decoupling

ESD Protection

- Locate the suppression devices as close to the I/O connector as possible
- Minimize the PCB trace length to the suppression device
- Minimize the PCB trace length for the ground return for the suppression device

Frequency Response Specification



Test Conditions:
Source Impedance = 50 Ω
Load Impedance = 50 Ω
Input Power = 0 dB

Figure 1. Measurement Conditions

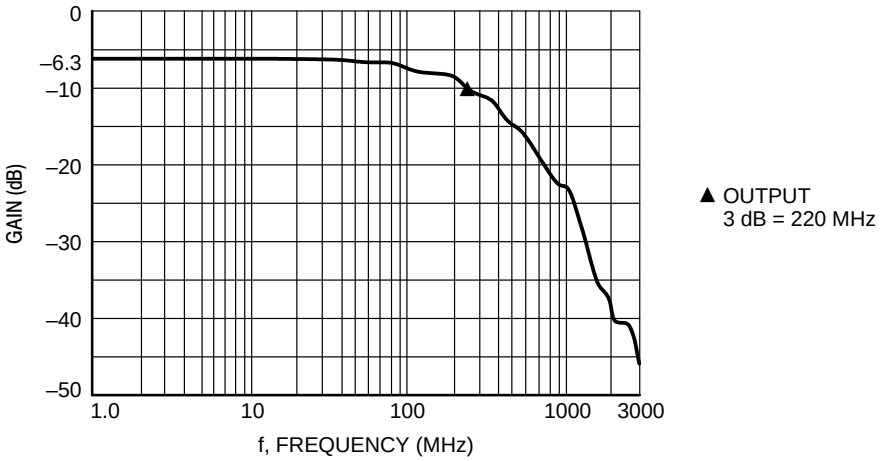
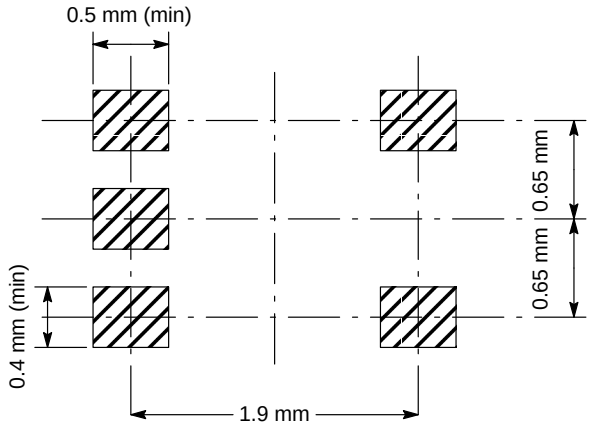


Figure 2. Typical EMI Filter Response (50 Ω Source and 50 Ω Lead Termination)

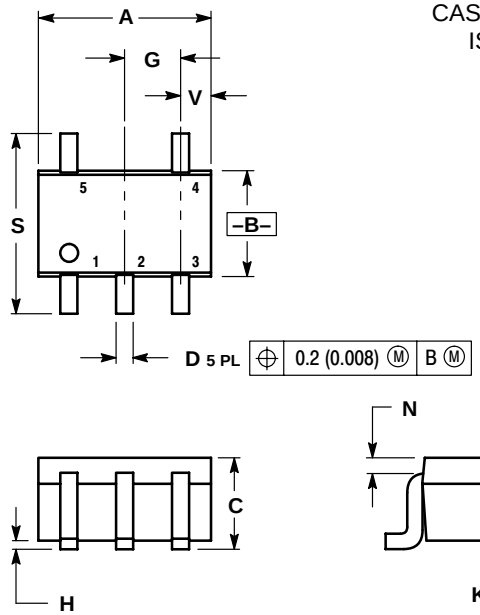
Footprint



OUTLINE DIMENSIONS

EMI Filter with ESD Protection

SC–88A/SOT–323
CASE 419A–01
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR
5. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

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