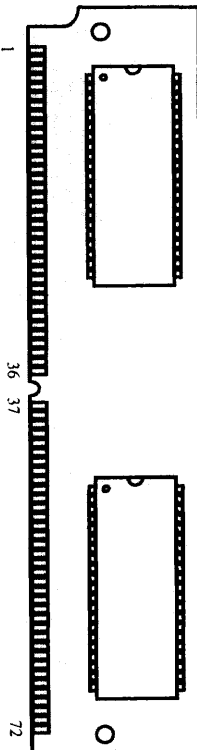




**Description**

The GMM7321000CNS/SG is an 1M x 32 bits Dynamic RAM MODULE which is assembled 2 pieces of 1M x 16bit DRAMs in 42 pin SOJ package on single sides the printed circuit board with decoupling capacitors. The GMM7321000CNS/SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. The GMM7321000CNS/SG provides common data inputs and outputs.

- GMM7321000CNS/SG (Single Side)



**Features**

- 72 pins Single In-Line Package
  - GMM7321000CNS : Solder plating
  - GMM7321000CNSG : Gold plating
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

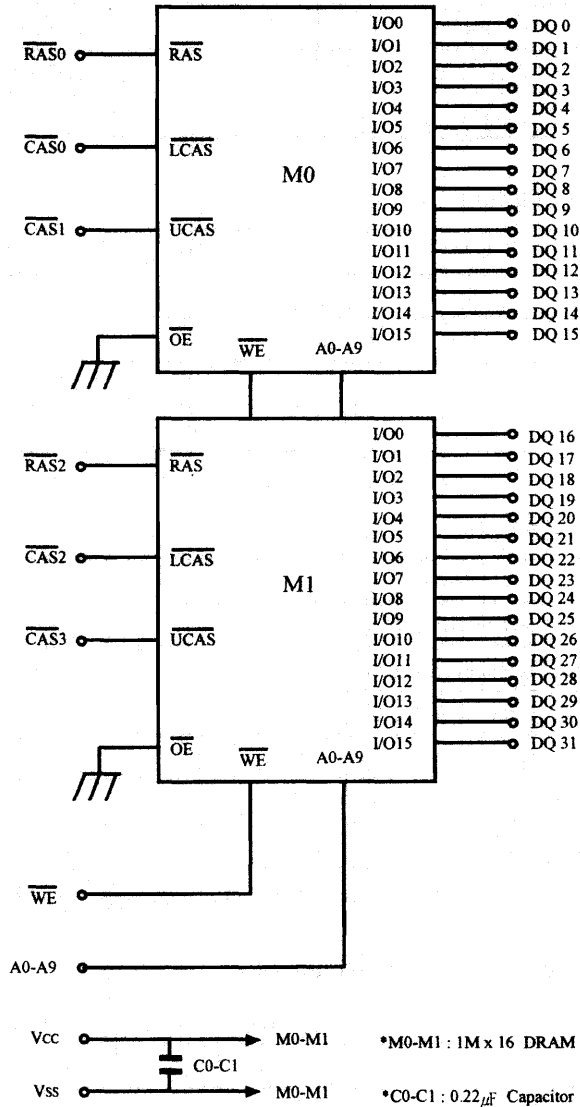
	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>
GMM7321000CNS/SG-6	60	15	110	40
GMM7321000CNS/SG-7	70	18	130	45
GMM7321000CNS/SG-8	80	20	150	50

- Low Power
  - Active : 1,870/1,650/1,430 mW (MAX)
  - Standby : 11mW (CMOS level : MAX)
- RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms

**Pin Configuration (Top View)**

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V <sub>SS</sub>	19	NC	37	NC	55	DQ <sub>11</sub>
2	DQ <sub>0</sub>	20	DQ <sub>4</sub>	38	NC	56	DQ <sub>27</sub>
3	DQ <sub>16</sub>	21	DQ <sub>20</sub>	39	V <sub>SS</sub>	57	DQ <sub>12</sub>
4	DQ <sub>1</sub>	22	DQ <sub>5</sub>	40	CAS <sub>0</sub>	58	DQ <sub>28</sub>
5	DQ <sub>17</sub>	23	DQ <sub>21</sub>	41	CAS <sub>2</sub>	59	V <sub>CC</sub>
6	DQ <sub>2</sub>	24	DQ <sub>6</sub>	42	CAS <sub>3</sub>	60	DQ <sub>29</sub>
7	DQ <sub>18</sub>	25	DQ <sub>22</sub>	43	CAS <sub>1</sub>	61	DQ <sub>13</sub>
8	DQ <sub>3</sub>	26	DQ <sub>7</sub>	44	RAS <sub>0</sub>	62	DQ <sub>30</sub>
9	DQ <sub>19</sub>	27	DQ <sub>23</sub>	45	NC	63	DQ <sub>14</sub>
10	V <sub>CC</sub>	28	A <sub>7</sub>	46	NC	64	DQ <sub>31</sub>
11	NC	29	NC	47	WE	65	DQ <sub>15</sub>
12	A <sub>0</sub>	30	V <sub>CC</sub>	48	NC	66	NC
13	A <sub>1</sub>	31	A <sub>8</sub>	49	DQ <sub>8</sub>	67	PD <sub>1</sub>
14	A <sub>2</sub>	32	A <sub>9</sub>	50	DQ <sub>24</sub>	68	PD <sub>2</sub>
15	A <sub>3</sub>	33	NC	51	DQ <sub>9</sub>	69	PD <sub>3</sub>
16	A <sub>4</sub>	34	RAS <sub>2</sub>	52	DQ <sub>25</sub>	70	PD <sub>4</sub>
17	A <sub>5</sub>	35	NC	53	DQ <sub>10</sub>	71	NC
18	A <sub>6</sub>	36	NC	54	DQ <sub>26</sub>	72	V <sub>SS</sub>

Block Diagram



**Pin Description**

Pin	Function	Pin	Function
A0-A9	Address Inputs	PD1-PD4	Presence Detect
DQ0-DQ31	Data Input/Output	V <sub>CC</sub>	Power (+5V)
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe	V <sub>SS</sub>	Ground
$\overline{\text{CAS0}}, \overline{\text{CAS3}}$	Column Address Strobe	NC	No Connection
$\overline{\text{WE}}$	Read/Write Enable		

**Presence Detect Pins (Optional)**

Pin	60ns	70ns	80ns
PD1	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
PD2	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
PD3	NC	V <sub>SS</sub>	NC
PD4	NC	NC	V <sub>SS</sub>

**Absolute Maximum Ratings\***

Symbol	Parameter	Rating	Unit
T <sub>A</sub>	Ambient Temperature under Bias	0 ~ 70	°C
T <sub>STG</sub>	Storage Temperature (Plastic)	-55 ~ 125	°C
V <sub>IN/VOUT</sub>	Voltage on any Pin Relative to V <sub>SS</sub>	-1.0 ~ 7.0	V
V <sub>CC</sub>	Power Supply Voltage	-1.0 ~ 7.0	V
I <sub>OUT</sub>	Short Circuit Output Current	50	mA
P <sub>D</sub>	Power Dissipation	2	W

\*Note: 1. Stress greater than above Absolute Maximum Ratings may cause permanent damage to the device.

**Recommended DC Operating Conditions (T<sub>A</sub> = 0 ~ 70 °C)**

Symbol	Parameter	Min	Typ	Max	Unit	Note
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	1
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	1
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	1

\*Note: 1. All voltages referenced to V<sub>SS</sub>.

DC Electrical Characteristics ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ C$ )

Symbol	Parameter	Min	Max	Unit	Note	
$V_{OH}$	Output Level Output $\square$ Level Voltage ( $I_{OUT} = -5mA$ )	2.4	$V_{CC}$	V		
$V_{OL}$	Output Level Output $\square$ Level Voltage ( $I_{OUT} = 4.2mA$ )	0	0.4	V		
$I_{CC1}$	Operating Current Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC} = t_{RC\ min}$ )	60ns	-	340	mA	1, 2
		70ns	-	300		
		80ns	-	260		
$I_{CC2}$	Standby Current (TTL) Power Supply Standby Current ( $\overline{RAS}$ , $\overline{CAS} = V_{IH}$ )	-	4	mA		
$I_{CC3}$	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = t_{RC\ min}$ )	60ns	-	340	mA	2
		70ns	-	300		
		80ns	-	260		
$I_{CC4}$	Fast Page Mode Current Average Power Supply Current Fast Page Mode ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t_{RC} = t_{RC\ min}$ )	60ns	-	340	mA	1, 3
		70ns	-	300		
		80ns	-	260		
$I_{CC5}$	Standby Current (CMOS) Power Supply Standby Current ( $\overline{RAS}$ , $\overline{CAS} \geq V_{CC} - 0.2V$ )	-	2	mA		
$I_{CC6}$	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current ( $t_{RC} = t_{RC\ min}$ )	60ns	-	340	mA	
		70ns	-	300		
		80ns	-	260		
$I_{CC7}$	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = Enable$	-	10	mA	1	
$I_{IL}$	Input Leakage Current Any Input ( $0V \leq V_{IN} \leq 7V$ ) All Other Pins Not Under Test = 0V	-10	10	$\mu A$		
$I_{OL}$	Output Leakage Current ( $D_{OUT}$ is Disabled, $0V \leq V_{OUT} \leq 7V$ )	-10	10	$\mu A$		

Note: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC(max)}$  is specified at the output open condition.

2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

**Capacitance** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 25^\circ C$ ,  $f = 1MHz$ )

Symbol	Parameter	Min	Max	Unit	Note
C <sub>11</sub>	Input Capacitance (A0~A9)	-	35	pF	1
C <sub>12</sub>	Input Capacitance ( $\overline{WE}$ )	-	34	pF	1, 2
C <sub>13</sub>	Input Capacitance ( $\overline{RAS0}, \overline{RAS2}$ )	-	27	pF	1, 2
C <sub>14</sub>	Input Capacitance ( $\overline{CAS0} \sim \overline{CAS3}$ )	-	27	pF	1, 2
C <sub>10</sub>	I/O Capacitance (DQ0~DQ31)	-	20	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{CAS} = V_{IH}$  to disable DOUT.

**AC Electrical Characteristics** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ C$ , Notes 1, 15)

The GMM7321000CNS/SG writes data only in early write cycle ( $twcs \geq twcs(min)$ ).  
 Delayed write cycle is not available because of I/O common.

**Read, Write and Refresh Cycle** (Common Parameters)

Symbol	Parameter	GMM7321000 CNS/SG-6		GMM7321000 CNS/SG-7		GMM7321000 CNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t <sub>RC</sub>	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t <sub>RP</sub>	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t <sub>RAS</sub>	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t <sub>CAS</sub>	$\overline{CAS}$ Pulse Width	15	10,000	18	10,000	20	10,000	ns	
t <sub>ASR</sub>	Row Address Setup Time	0	-	0	-	0	-	ns	
t <sub>RAH</sub>	Row Address Hold Time	10	-	10	-	10	-	ns	
t <sub>ASC</sub>	Column Address Setup Time	0	-	0	-	0	-	ns	
t <sub>CAH</sub>	Column Address Hold Time	10	-	15	-	15	-	ns	
t <sub>RCD</sub>	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	20	60	ns	9
t <sub>RAD</sub>	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
t <sub>RSH</sub>	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
t <sub>CSH</sub>	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t <sub>CRP</sub>	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t <sub>REF</sub>	Refresh Period (1024 Cycles)	-	16	-	16	-	16	ms	

**Read Cycle**

Symbol	Parameter	GMM7321000 CNS/SG-6		GMM7321000 CNS/SG-7		GMM7321000 CNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	-	60	-	70	-	80	ns	2, 3
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$	-	15	-	18	-	20	ns	3, 4
t <sub>AA</sub>	Access Time from Column Address	-	30	-	35	-	40	ns	3, 5, 14
t <sub>RCS</sub>	Read Command Setup Time	0	-	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	6
t <sub>RRH</sub>	Read Command Hold Time to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	6
t <sub>RAL</sub>	Column Address to $\overline{\text{RAS}}$ Lead Time	30	-	35	-	40	-	ns	
t <sub>OFF</sub>	Output Buffer Turn-off Time	-	15	-	15	-	15	ns	7

**Write Cycle**

Symbol	Parameter	GMM7321000 CNS/SG-6		GMM7321000 CNS/SG-7		GMM7321000 CNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t <sub>WCS</sub>	Write Command Setup Time	0	-	0	-	0	-	ns	11
t <sub>WCH</sub>	Write Command Hold Time	10	-	15	-	15	-	ns	
t <sub>WP</sub>	Write Command Pulse Width	10	-	10	-	10	-	ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	15	-	18	-	20	-	ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	15	-	18	-	20	-	ns	
t <sub>DS</sub>	Data-in Setup Time	0	-	0	-	0	-	ns	12
t <sub>DH</sub>	Data-in Hold Time	10	-	15	-	15	-	ns	12

**Refresh Cycle**

Symbol	Parameter	GMM7321000 CNS/SG-6		GMM7321000 CNS/SG-7		GMM7321000 CNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t <sub>CSR</sub>	$\overline{\text{CAS}}$ Setup Time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t <sub>RPC</sub>	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	5	-	ns	

**Fast Page Mode Cycle**

Symbol	Parameter	GMM7321000 CNS/SG-6		GMM7321000 CNS/SG-7		GMM7321000 CNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t <sub>PC</sub>	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
t <sub>CP</sub>	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	10	-	10	-	10	-	ns	
t <sub>RASP</sub>	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	60	100,000	70	100,000	80	100,000	ns	13
t <sub>ACP</sub>	Access Time from $\overline{\text{CAS}}$ Precharge	-	35	-	40	-	45	ns	14
t <sub>RHCP</sub>	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	35	-	40	-	45	-	ns	

**Notes:**

1. AC measurements assume  $t_r = 5\text{ns}$ .
2. Assumes that  $t_{rCD} \leq t_{rCD}(\text{max})$  and  $t_{rAD} \leq t_{rAD}(\text{max})$ . If  $t_{rCD}$  or  $t_{rAD}$  is greater than the maximum recommended value shown in this table,  $t_{rAC}$  exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that  $t_{rCD} \geq t_{rCD}(\text{max})$  and  $t_{rAD} \leq t_{rAD}(\text{max})$ .
5. Assumes that  $t_{rCD} \leq t_{rCD}(\text{max})$  and  $t_{rAD} \geq t_{rAD}(\text{max})$ .
6. Either  $t_{rCH}$  or  $t_{rRH}$  must be satisfied for a read cycles.
7.  $t_{off}(\text{max})$  defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
8.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
9. Operation with the  $t_{rCD}(\text{max})$  limit insures that  $t_{rAC}(\text{max})$  can be met,  $t_{rCD}(\text{max})$  is specified as a reference point only, if  $t_{rCD}$  is greater than the specified  $t_{rCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
10. Operation with the  $t_{rAD}(\text{max})$  limit insures that  $t_{rAC}(\text{max})$  can be met,  $t_{rAD}(\text{max})$  is specified as a reference point only, if  $t_{rAD}$  is greater than the specified  $t_{rAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
11.  $t_{wCS}$  is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If  $t_{wCS} \geq t_{wCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
12. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles.
13.  $t_{RASP}$  is defines  $\overline{\text{RAS}}$  pulse width in Fast Page Mode cycles.
14. Access time is determined by the longer of  $t_{AA}$  or  $t_{CAC}$  or  $t_{ACP}$ .
15. An initial pause of  $200\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$  clock such as  $\overline{\text{RAS}}$  only refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles are required.

**Timing Waveforms : Please refer to attached Timing Waveform-5**

