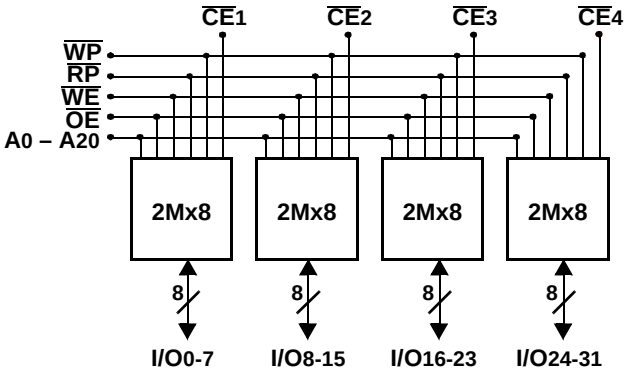
ACT–F2M32 High Speed 64 Megabit FLASH Multichip Module

AEROFLEX CIRCUIT TECHNOLOGY

Features

- 4 Low Power 2M x 8 FLASH Die in One MCM Package
- Organized as 2M x 32
  - User Configurable to 4M x 16 or 8M x 8
- TTL and CMOS Compatible Inputs and Outputs
- Access Times of 80, 100 and 120nS
- +12V Only Programing, +5V ±10% Supply
- 100,000 Erase/Program Cycles
- Low Power Dissipation
  - 8 mA CMOS Standby Current Typical
- Sector Architecture (Each Die)
  - 32 Equal Sectors of 64K bytes per each 2M x 8 Chip
  - Two Step Sequence of Erase Ensures that Memory Contents are not Accidently Erased
- Pipeline Command Execution
- Write During Erase
- Industry Standard Pinouts
- Packaging – Hermetic Ceramic
  - 68 Lead, 1.56" x 1.56" x .140" Low Profile CQFP, Aeroflex code# "F1"
  - 66 Pin, 1.38" x 1.38" x .245" PGA Type, Aeroflex code# "P1"
- Automated Byte Write and Block Erase
  - Command User Interface
  - Compatible Status Register (CSR)
  - Global Status Register (GSR)
  - 32 Block Status Registers (BSRs) per Die
- MIL-H-38534 Compliant MCMs Available
- Decoupling Capacitors and Multiple Grounds for Low Noise
- Industrial and Military Temperature Ranges

Block Diagram – PGA Type Package(P1) & CQFP(F1)



Pin Description

I/O0-31	Data I/O	$\overline{WP}$	Write Protect
A0–20	Address Inputs	VCC	Power Supply
$\overline{WE}$	Write Enable	VPP	Program/Erase Supply
$\overline{CE}$1-4	Chip Enables	GND	Ground
$\overline{OE}$	Output Enable	NC	Not Connected Reserved for further expansion
$\overline{RP}$	Reset/Pwrdown		

General Description

The ACT–F2M32 is a high speed, 64 megabit CMOS Flash multichip module (MCM) designed for full temperature range military, space, or high reliability applications.

The ACT-F2M32 consists of four high performance 16 Mbit (16,777,216 bit) memory die. Each die is organized as 2 Mbyte (2,097,152 bytes) by 8 bits with thirty-two, 64K byte (65,536 byte) blocks.

The products are designed for operation over the temperature range of -55°C to +125°C and under the full military environment. A DESC Standard Military Drawing (SMD) number is pending.

The ACT-S512K32 is manufactured in Aeroflex's 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.

Absolute Maximum Ratings

Parameter	Range	Units
Storage Temperature Range	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (except V_{CC} and V_{PP}) (2)	-2.0 to +7.0	V
V_{PP} Program Voltage with Respect to Ground during Block Erase/Byte Write (2,3)	-0.2 to +14.0	V
Vcc Supply Voltage with Respect to Ground (2)	-0.2 to +7.0	V

Notes:
1. Minimum DC input voltage is -0.5V. During Transitions, inputs may undershoot to -2.0V for periods less than 20nS. Maximum DC voltage on output pins is Vcc + 0.5V, which may overshoot to Vcc + 2.0V for periods less than 20nS.
2. Maximum DC voltage on Vpp may overshoot to +14.0V for periods less than 20nS.
3. Output shorted for no more than 1 second. No more than one output shorted at one time.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V
T_A	Operating Temperature (Military)	-55	+125	°C

Capacitance

(V_{IN} = 0V, f = 1MHz, T_A = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A0 – A20 Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{CE}	Chip Enable Capacitance		
	CQFP(F1) Package	20	pF
	PGA(P1) Package	20	pF
C_{WE}	Write Enable Capacitance	50	pF
$C_{I/O}$	I/O0 – I/O31 Capacitance	20	pF

Capacitance Guaranteed by design, but not tested.

DC Characteristics – CMOS Compatible

(Vcc = 5.0V, Vss = 0V)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{IN} = V_{CC} to GND		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V, V_{OUT} = V_{CC} to GND		10	µA
Vcc Standby Current	I_{CCS}	V_{CC} = 5.5V, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IN}, f = 5Mhz		16	mA
Vcc Read Current	I_{CCR}	V_{CC} = 5.5V, $\overline{CE}$ = V_{IL}, f = 5MHz, I_{OUT} = 0 mA		175	mA
Vcc Write Current	I_{CCW}	Write in Progress		175	mA
Vcc Block Erase Current	I_{CCE}	Block Erase in Progress		60	mA
Vcc Powerdown Current	I_{CCD}	$\overline{RP}$ = GND		8	µA
V_{PP} Standby Current	I_{PPS}	V_{PP} < V_{CC}		80	µA
V_{PP} Powerdown Current	I_{PPD}	$\overline{RP}$ = GND		80	µA
V_{PP} Byte Write Current	I_{PPW}	V_{PP} = VPPH, Byte Write in Progress		60	mA
V_{PP} Block Erase Current	I_{PPE}	V_{PP} = VPPH, Block Erase in Progress		60	mA
Output Low Voltage	V_{OL}	V_{CC} = 4.5V, I_{OL} = 5.8 mA		0.45	V
Output High Voltage	V_{OH}	V_{CC} = 4.5V, I_{OH} = -2.5 mA	2.4 or 0.85V_{CC}		V
V_{PPL} DuringNormal Operations	V_{PPL}		0.0	6.5	
V_{PP} During Erase/Write Operations	V_{PPH}		11.4	12.6	V
Vcc Erase/Write Lock Voltage	V_{LKO}		2.0		V

NOTES: 1) Block Erases/Byte Writes are inhibited when $V_{PP} \leq V_{PPLK}$. 2) DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC Characteristics – Write/Erase/Program Operations – $\overline{WE}$ Controlled

(Vcc = 5.0V, Vss = 0V)

Parameter	Symbol		–080		–100		–120		Units
	JEDEC	Standard	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	80		100		120		nS
Chip Enable Setup Time	t_{ELWL}	t_{CE}	0		0		0		nS
Write Enable Pulse Width	t_{WLWH}	t_{WP}	50		50		50		nS
Vpp Setup Time (1)	t_{VPWH}	t_{VPS}	100		100		100		nS
Address Setup Time	t_{AVWH}	t_{AS}	50		50		50		nS
Data Setup Time	t_{DVWH}	t_{DS}	60		60		60		nS
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		nS
Address Hold Time	t_{WHAX}	t_{AH}	10		10		10		nS
Chip Enable Hold Time	t_{WHEH}	t_{CH}	10		10		10		nS
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		50		50		nS
Duration of Byte Write Operation (1,2,3)	t_{WHQV1}		4.5		4.5		4.5		µS
Duration of Block Erase Operation (1,2,3)	t_{WHQV2}		0.3		0.3		0.3		Sec
Write Recovery before Read	t_{WHGL}		65		80		80		nS
$\overline{RP}$ High Recovery Time (1)	t_{PHWL}	t_{PS}	1		1		1		µS

Notes:
1. Guaranteed by design, not tested.
2. The on-chip Write State Machine incorporates all byte write and block erase functions and overhead of the flash memory, this includes byte program and verity, block precondition and verify, erase and verity.
3. Byte write and block erase durations are measured to completion (CSR.7 = 1). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (CSR.3/4/5 = 0).

AC Characteristics – Write Operations, $\overline{CE}$ Controlled (1)

(Vcc = 5.0V, Vss = 0V)

Parameter	Symbol		–080		–100		–120		Units
	JEDEC	Standard	Min	Max	Min	Max	Min	Max	
Write Enable Cycle Time	t_{AVAV}	t_{WC}	80		100		120		nS
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		nS
Chip Enable Pulse Width	t_{ELEH}	t_{CP}	50		50		50		nS
V_{PP} Setup Time (2)	t_{VPEH}	t_{VPS}	100		100		100		nS
Address Setup to $\overline{CE}$ Going High	t_{AVEH}	t_{AS}	50		50		50		nS
Data Setup Time	t_{DVEH}	t_{DS}	60		60		60		nS
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		nS
Address Hold Time	t_{EHAX}	t_{AH}	10		10		10		nS
Write Enable Hold Time	t_{EHWH}	t_{WH}	10		10		10		nS
Chip Enable Pulse Width High	t_{EHEL}	t_{EPH}	30		50		50		nS
Duration of Byte Write Programming (2,3)	t_{EHQV1}		4.5		4.5		4.5		µS
Duration of Block Erase Programming (2,3)	t_{EHQV2}		0.3		0.3		0.3		Sec
Write Recovery Before Read	t_{EHGL}		65		80		80		nS
$\overline{RP}$ High Recovery to $\overline{CE}$ Low (2)	t_{PHEL}	t_{PS}	1.0		1.0		1.0		µS

NOTES:
1. Chip-Select Controlled Writes: Write operations are drive by the valid combination of $\overline{CE}$ and $\overline{WE}$. In systems where $\overline{CE}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.
2. Guaranteed by design, not tested.
3. Byte write and block erase durations are measured to completion (CSR.7 = 1, RY/$\overline{BY}$ = 1, V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (CSR.3/4/5 = 0).

AC Characteristics – Read Only Operations

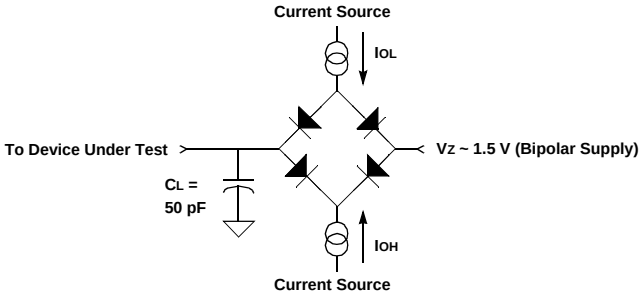
(Vcc = 5.0V, Vss = 0V)

Parameter	Symbol		–080		–100		–120		Units
	JEDEC	Standard	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	80		100		120		nS
Address Access Time	t_{AVQV}	t_{ACC}		80		100		120	nS
Chip Enable to Output Valid (1)	t_{ELQV}	t_{CE}		80		100		120	nS
Output Enable to Output Valid (1)	t_{GLQV}	t_{OE}		35		40		45	nS
Chip Enable to Output Low Z (2)	t_{ELQX}	t_{LZ}	0		0		0		nS
Chip Enable High to Output High Z (2)	t_{ELQZ}	t_{HZ}		30		35		40	nS
Output Enable to Output Low Z (2)	t_{GHQX}	t_{QLZ}	0		0		0		nS
Reset to Output Valid	t_{PHQV}	t_{PWH}		480		550		620	nS
Output Enable High to Output High Z (2)	t_{GHQZ}	t_{DF}		30		35		40	nS
Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First (2)		t_{OH}	0		0		0		nS

Notes:

1. $\overline{OE}$ may be delayed up to t_{CE}–t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
2. Guaranteed by design, but not tested.

Figure 1
AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	nS
Input and Output Timing Reference	1.5	V
Output Lead Capacitance	50	pF

Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance $Z_O = 75\Omega$. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Figure 2
AC Waveform for Write–Erase–Program Operations, $\overline{WE}$ Controlled

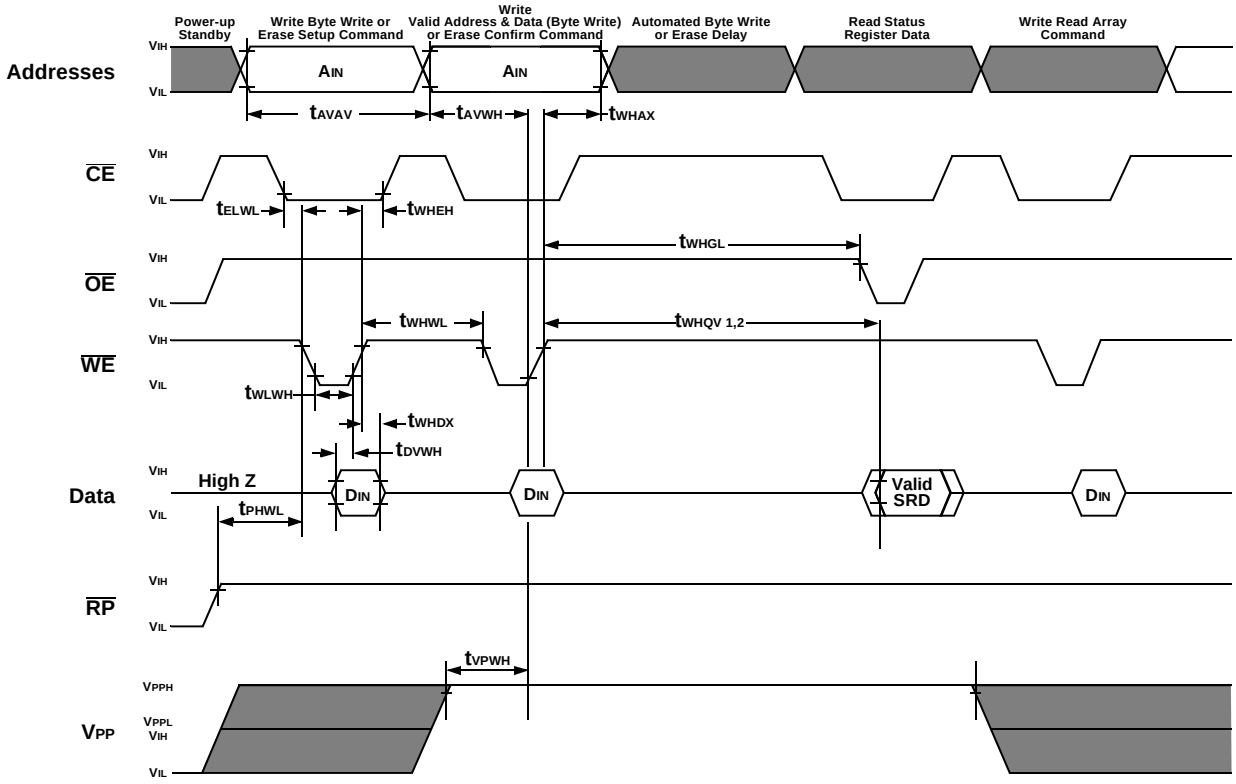


Figure 3
Alternate AC Waveforms For Write Operations – $\overline{CE}$ Controlled

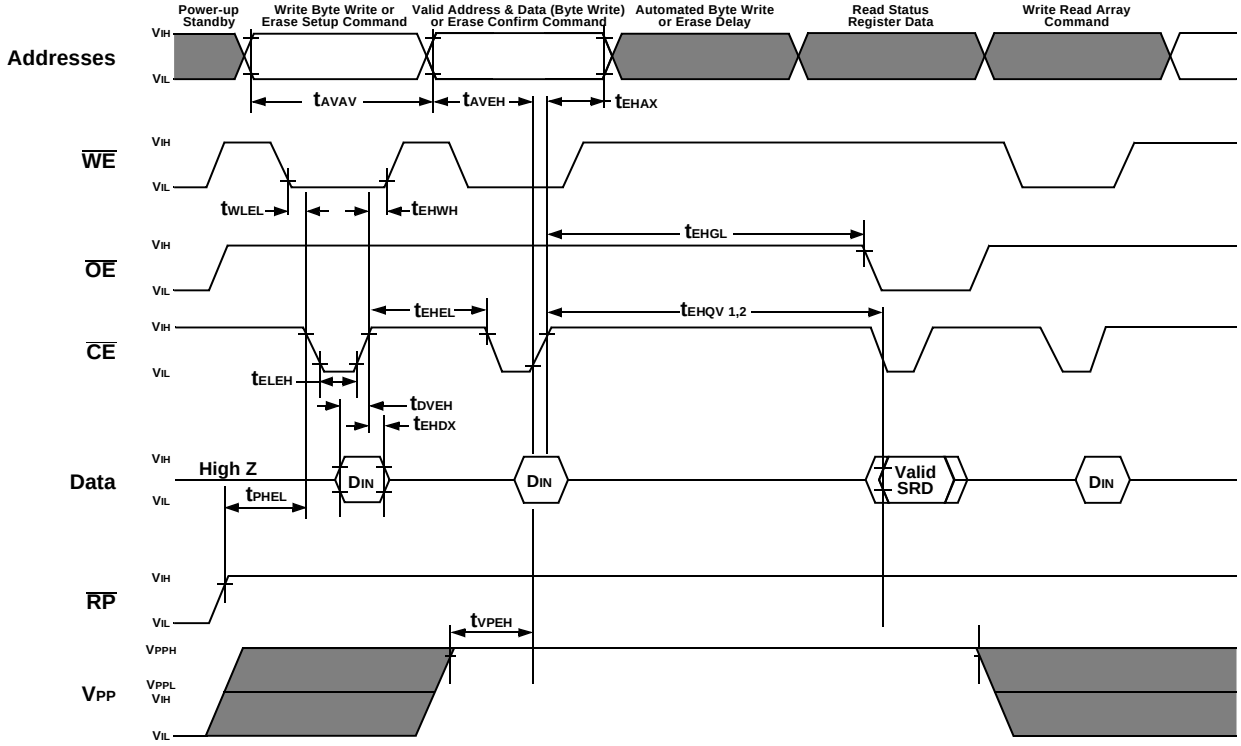
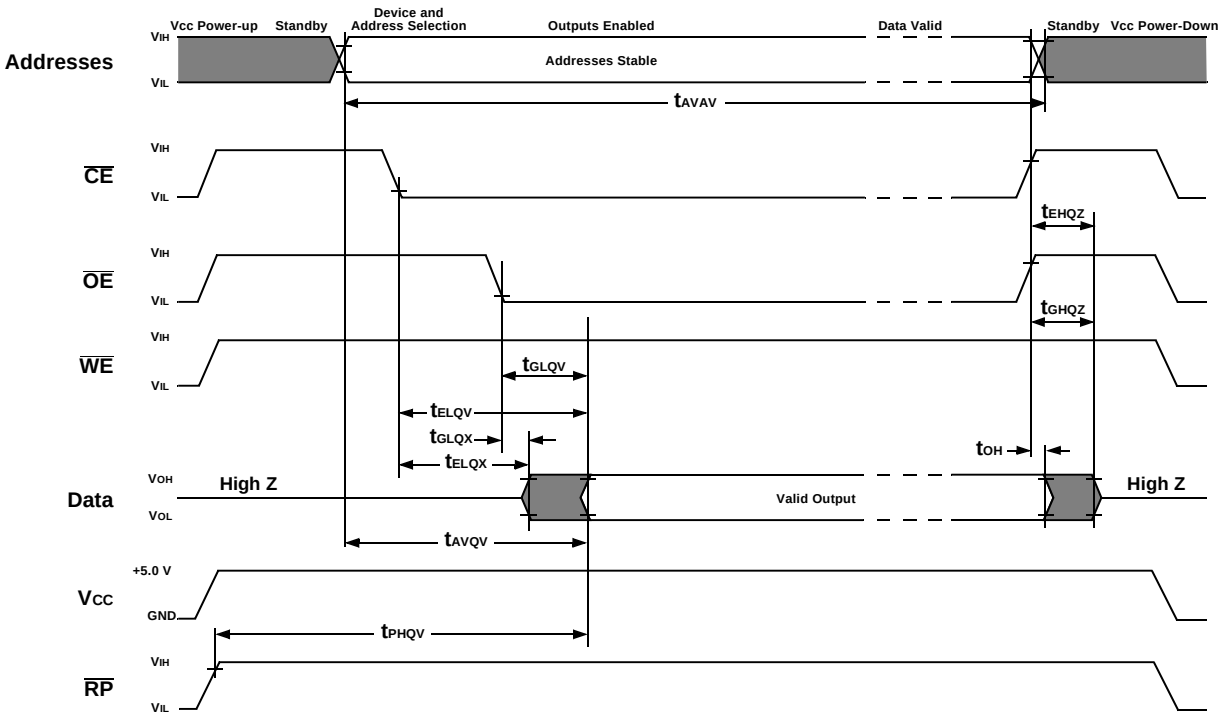


Figure 4
AC Waveform For Read Operations



Principles of Operation

The ACT–2M32 MCM is composed of four (4), sixteen (16) megabit memory chips inside the MCM. Chip 1 is distinguished by $\overline{CE}_1$ and I/O_{1-7}, Chip 2 by $\overline{CE}_2$ and I/O_{8-15}, Chip 3 by $\overline{CE}_3$ and I/O_{16-23}, Chip 4 by $\overline{CE}_4$ and I/O_{24-31}. The ACT-F2M32 includes write automation to manage write and erase functions. The Write State Machine allows for 100% TTL–level control inputs; fixed power supplies during block erasure and byte write and minimal processor overhead with RAM like interface timings.

After initial device powerup the ACT–F2M32 functions as a read-only memory. Manipulation of external memory control pins allow array read, standby and output disable operations. The status register can also be accessed through the command user interface when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables successful block erasure and byte writing of the device. Functions associated with altering memory contents, byte write, block erase, are accessed via the command user interface and verified through the status register.

Commands are written using standard microprocessor write timings. Command user interface contents serve as input to the write status machine, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the device are again possible via the read array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

COMPARISON OF ACT-F1M32 TO ACT-F2M32

A Superset of commands have been added to the basic ACT-F1M32 command set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Command Queuing Capability
- Automatic Data Writes During Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Writes in 8-bit Systems
- Erase all Unlocked Blocks

Writing of memory data is performed in either byte or word increments typically within 6 µsec, a 33% improvement over the ACT-F1M32. A Block Erase operation erases one of the 32 blocks, which is about 65% improvement over the ACT-F1M32.

Each block can be written and erased a minimum of 100,000 cycles. Systems can achieve 1 million block erase cycles by providing wear leveling algorithms and block retirement.

Each chip in ACT-F2M32 incorporates two page buffers of 256 Bytes (128 Words) each to allow page data writes. This feature can improve a system write performance by up to 4.8 times over previous flash memory devices.

All operations are started by a sequence of write commands to the device. Three Status Registers (described in detail later) and a RY/$\overline{BY}$ output pin provide information on the progress of the requested operation.

While the ACT-F1M32 requires an operation to complete before the next operation can be requested, the ACT-F2M32 allows queueing of the next operation while memory executes the current operation. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The ACT-F2M32 can also perform write operations to one block of memory while performing erase of another block.

The ACT-F2M32 provides user selectable block locking to protect code or data. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the ACT-F2M32 has a master Write Protect pin ($\overline{WP}$) which prevents any modifications to memory blocks whose lock-bits are set.

The ACT-F2M32 contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the ACT-F1M32 flash memory's Status Register. This register, when used alone. provides a straightforward upgrade capability to the ACT-F2M32 from a ACT-F1M32 based design.
- A Global Status Register (GSR) which informs the system of command queue status, page buffer status and overall Write State Machine (WSM) status.
- 32 Block Status Registers (BSRS) which provide block specific status information such as the block lock-bit status.

COMMAND USER INTERFACE AND WRITE AUTOMATION

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block preconditioning and erase, returning progress via the Status Register on each of the four memory chips in the MCM. QFP options with RY/$\overline{BY}$ also return progress via the Status Register for each of the four memory chips. Byte write is similarly controlled, after destination address and expected data are supplied.

DATA PROTECTION

Depending on the application, the system designer

may choose to make the V_{PP} power supply switchable (available only when memory byte writes/block erases are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. Additionally, all functions are disabled whenever Vcc is below the write lockout voltage V_{LKO} or when RP is at V_{IL}. The two step byte write/block erase command user interface write sequence provides additional software write protection.

Bus Operation

Flash memory reads, erase and writes in system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

READ

The ACT–2M32 can be read from any of its blocks, and information can be read from the status register of each chip selected. V_{PP} can be at either V_{PPL} or V_{PPH}.

The first task is to write the appropriate read mode command to the command user interface. The device automatically resets to read array mode upon initial device powerup or after exit from deep powerdown. Chip Enable $\overline{CE}$ is the device selection control, and when active enables the selected memory device. Output Enable ($\overline{OE}$) is the data input/output (I/O0-I/O31) direction control, and when active drives data from the select memory onto the I/O bus. $\overline{RP}$ and $\overline{WE}$ must also be at V_{IH}. Figure 4 illustrates read bus cycle waveforms.

OUTPUT DISABLE

With $\overline{OE}$ at a logic high level (V_{IH}), the device outputs are disabled.Output pins (I/O_{0-31}) are placed in a high impedance state.

STANDBY

$\overline{CE}$ at a logic high level (V_{IH}) places the device in a standby mode. Standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (I/O_{0-31}) are placed in a high impedance state independent of the status of M. If the device is deselected during block erase or byte write, it will continue functioning and consuming normal active power until the operation is completed.

WRITES

Writes to the command user interface enable reading of device data. They also control inspection and cleaning of the status register. Additionally, when $V_{PP} = V_{PPH}$, the command user interface controls block erasure and byte write. The contents of the interface register serve as input to the internal state machine.

The command user interface itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase setup and erase confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written, while the Byte Write command consists of the data to be written and the address of the location to be written.

The command user interface is written by bringing $\overline{WE}$ to a logic low level (V_{IL}) while $\overline{CE}$ is low. Address and data are latched on the rising edge of $\overline{WE}$. Standard microprocessor write timings are used. Refer to AC Write Characteristics and the AC waveforms for Write Operation, Figures 2 and 3, for specific timing parameters.

Command Definitions

When V_{PPL} is applied to the V_{PP} pin of the chip selected, read operations from the status register, or array blocks are enabled. Placing V_{PPH} on V_{PP} enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands into the command user interface of the chip selected. Table 2 defines the ACT–2M32 commands.

READ ARRAY COMMAND

Upon initial device powerup the device defaults to Read Array mode. This operation is also initiated by writing FFH into the command user interface. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command user interface contents are altered. Once the internal Write State Machine has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

READ STATUS REGISTER COMMAND

Each chip of the ACT–2M32 contains a status register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the read status register command (70H) to the command user interface. After writing this command, all subsequent read operations output data from the status register, until another valid command is written to the command user interface. The contents of the status register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last in the read cycle. $\overline{OE}$ or $\overline{CE}$ must be toggled to V_{IH} before further reads to update the status register latch. The read status register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

CLEAR STATUS REGISTER COMMAND

The erase status and byte write status bits are set to "1"s by the Write State Machine on each chip and can only be reset by the clear status register command.

These bits indicate various failure conditions (See Table 3). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The status register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} Status bit (CSR.3) of the chip selected MUST be reset by system software before further byte writes or block erases are attempted. To clear the status register, the clear status register command (50H) is written to the command user interface. The clear status register command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

ERASE SETUP/ERASE CONFIRM COMMANDS

Erase is executed one block at a time, initiated by a two cycle command sequence. An erase setup command (20H) is first written to the command user interface, followed by the Erase Confirm command (D0H). These commands require both appropriate sequencing and address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After the two command erase sequence is written to it, the ACT–2M32 automatically outputs status register data when read (See Figure 6; Block Erase Algorithm). The CPU can detect the completion of the erase event by analyzing the output of the WSM Status bit of the status register.

When erase is completed, the Erase Status bit should be checked. If erase error is detected, the status register should be cleared. The command user interface remains in read status register mode until further commands are issued to it.

This two step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, reliable block ensure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

BYTE WRITE SETUP/WRITE COMMANDS

Byte write is executed by a two command sequence. The byte write setup command (40H) is written to the command user interface of the chip selected, followed by a second write specifying the address and data (latched on the rising edge of $\overline{WE}$) to be written. The WSM then takes over, controlling the byte write and write verify algorithms internally. After the two command byte write sequence is written to it, the device automatically outputs status register data when read (See Figure 5; Byte Write Algorithm). The CPU can detect the completion of the byte write event by analyzing the output of the WSM Status bit of the status register. Only the read status register command is valid while byte write is active.

When byte write is complete, the byte write status bit should be checked. If byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The command user interface remains in read status register mode until further commands are issued to it. If byte write is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Byte write attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce sourious results and should not be attempted.

ERASE SUSPEND/ERASE RESUME COMMANDS

The erase suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the erase suspend command (B0H) to the command user interface requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The ACT-F2M32 continues to output status register data when read, after the erase suspend command is written to it. Polling the WSM status and erase suspend status bits will determine when the erase operation has been suspended (both will be set to "1").

At this point, a read array command can be written to the command user interface to read data from blocks other than that which is suspended. The only other valid commands at this time are read status register (70H) and erase resume (D0H), at which time the WSM will continue with the erase process. The erase suspend status and WSM status bits of the status register will be automatically cleared. After the erase resume command is written to it, the device automatically outputs status register data when read (See Figure 7). V_{PP} must remain at V_{PPH} while in erase suspend.

Vcc, VPP, $\overline{RP}$ TRANSITIONS AND THE COMMAND/STATUS REGISTERS

Byte write and block erase completion are not guaranteed if V_{PP} drops below V_{PPH}. If the V_{PP} Status bit of the Status Register (CSR.3) is set to "1", a Clear Status Register command must be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the Byte Write (CSR.4) or Erase (CSR.5) Status bits of the Status Register will be set to “1"s if error is detected. $\overline{RP}$ transitions to V_{IL} during byte write and block erase also abort the operations. Data is partially altered in either case and the command sequence must be repeated after normal operation is restored. Device poweroff, or $\overline{RP}$ transitions to V_{IL}, clear the Status Register to initial value 10000 for the upper 5 bits.

The Command User Interface latches commands as issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its state upon powerup, after exit from deep powerdown or after Vcc transitions below V_{LKO}, is Read Array Mode.

After byte write or block erase is complete, even after

V_{PP} transitions down to V_{PPL}, the Command User interface must be reset to Read Array mode via the Read Array command if access to the memory array is desired.

POWER UP/DOWN PROTECTION

The ACT-F2M32 is designed to offer protection against accidental block erasure or byte writing during power transitions. Upon power-up, the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the device ensures that the Command User interface is reset to the Read Array mode on power up.

POWERDOWN AND RESET

The ACT-F2M32 offers a deep Powerdown feature, entered when $\overline{RP}$ is a V_{IL}. Current draw through Vcc is 0.8 µA typical in deep Powerdown mode, with current draw through V_{PP} typically 0.4µA. During read modes. $\overline{RP}$-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. The device requires time t_{PWH} (See AC Characteristics-Read-Only Operations) after return from powerdown until initial memory access outputs are valid. After this wake up interval, normal operation is restored. The Command User Interface is reset to Read Array, and the upper 5 bits of the Status Register are cleared to value 10000, upon return to normal operation.

During block erase or byte write modes. $\overline{RP}$ low will abort either operation. Memory contents of the block being altered are no longer valid as the data will be partially written or erased. Time t_{PS} after $\overline{RP}$ goes to logic high (V_{IH}) is required before another command can be written.

This use of $\overline{RP}$ during system reset is important with automated write/erase devices. When the system comes out of reset it expects to read from the flash memory. Automated flash memories provide status information when accessed during write/erase modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization would not occur because the flash memory would be providing the status information instead of array data. These flash memories allow proper CPU initialization following a system reset through the use of the $\overline{RP}$ input. In this application $\overline{RP}$ is controlled by the same RESET signal that resets the system CPU.

Table 1 – Bus Operations

Command	Notes	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O0-7
Read		V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	High Z
Standby	1	V_{IH}	V_{IL}	X	X	High Z
			V_{IH}			
			V_{IH}			
Deep Powerdown	1,2	V_{IL}	X	X	X	High Z
Write		V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}

Notes:
1. X can be V_{IL} or V_{IH} for control and address pins.
2. $\overline{RP}$ at GND ±0.2V ensures the lowest deep power-down current.
3. Commands for different Erase operations. Data write operations or Lock-Block operations can only be successfully completed when $V_{PP} = V_{PPH}$.

Table 2 – Commands Definitions – Compatible Mode

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Array		Write	X	FFH	Read	AA	AD
Read Compatible Status Register	1	Write	X	70H	Read	X	CSRD
Clear Status Register	2	Write	X	50H			
Word/Byte Write		Write	X	40H	Write	WA	WD
Alternate Word/Byte Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm		Write	X	20H	Write	BA	DOH
Erase Suspend/Resume		Write	X	80H	Write	X	DOH

Address
AA = Array Address BA = Block Address
IA = Identifier Address WA = Write Address X = Don't care

Data
AD= Array Data CSRD = CSR Data
ID = Identifier Data WD = Write Data

NOTES:
1. The CSR is Automatically available after device enters Data Write, Erase or Suspend operations.
2. Clears CSR 3. CSR 4. CSR 5. Also Clears GSR 5 and BSR 5 and BSR 2 bits. See status register definitions

Table 3 – Commands Definitions – Enhanced Mode

Command	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
		Operation	Address	Data	Operation	Address	Data	Operation	Address	Data
Read Extend Status Register	1	Write	X	71H	Read	RA	GSRD BSRD			
Page Buffer Swap	5	Write	X	72H	Read					
Read Page Buffer		Write	X	75H	Write	PA	PD			
Single load to Page Buffer		Write	X	74H	Write	PA	PD			
Sequential Single load to Page Buffer	3,4,6	Write	X	E0H	Write	X	BCL	Write	X	BCH
Page Buffer Write to Flash	3,6	Write	X	0CH	Write	A0	BC(L,H)	Write	WA	BC(H,L)
	3,6	Write	X	0CH	Write	X	WCL	Write	WA	WCH
Two Byte Write		Write	X	FBH	Write	A0	WD(L,H)	Write	WA	WD(H,L)
Lock Block/Confirm		Write	X	77H	Write	BA	D0H			
Upload Status Bits/Confirm	2	Write	X	97H	Write	X	D0H			
Upload Device Information		Write	X	99H	Write	X	D0H			
Erase all Unlocked Blocks/Confirm		Write	X	A7H	Write	X	D0H			
Sleep		Write	X	F0H						
Abort		Write	X	80H						

Address
BA = Block Address
PA = Page Buffer Address
RA = Extended Register Address
WA = Write Address
X = Don't Care

Data
AD= Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data
WC(L,H) = Word Count (Low, High)
BC(L,H) = Byte Count (Low, High)
WD(L,H) = Write Data (Low, High)

NOTES:
1. RA can be the GSR address or any BSR address.
2. Upon device power-up, all BSR lock-bits come up locked The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. BCH/WCH must be at 00H for this produce because of the 256-Byle (128 Word) Page Buffer size and to avoid writing the Page Buffer contents into more than one 256Byte segment within an array block. They are simply shown for future Page Buffer expandability.
4. PA and PD (whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle which is not shown.
5. This command allows the user to swap between available Page Butters (0 or 1).
6. BCL = 00H corresponds to a Byte count of 1. Similarly, WCL = 00H corresponds to a Word count of 1.

Table 4 — Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS
- 1 = Ready
- 0 = Busy

CSR.6 = ERASE SUSPENDED STATUS
- 1 = Erase Suspended
- 0 = Erase in Progress/Completed

CSR.5 = ERASE STATUS
- 1 = Error in Block Erasure
- 0 = Successful Block Erase

CSR.4 = DATA WRITE STATUS
- 1 = Error in Byte Write
- 0 = Successful Byte Write

CSR.3 = VPP STATUS
- 1 = VPP Low Detect; Operation Abort
- 0 = VPP OK

CSR.2–CSR.0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use and should be masked out when polling the status register.

NOTES:
1. The WSMS bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bit are checked for success.
2. If the DWS and Erase Status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Clear the CSR and attempt the sequence again.
3. The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the byte write or block erase command sequences have been entered and informs the system it V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

Table 5 — Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS
- 1 = Ready
- 0 = Busy

GSR.6 = OPERATION SUSPEND STATUS
- 1 = Operation Suspended
- 0 = Operation in Progress/Completed

GGR.5 = DEVICE OPERATION STATUS
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

GSR.4 = DEVICE SLEEP STATUS (2,3)
- 1 = Device in Sleep
- 0 = Device not in Sleep

MATRIX 5/4
- 00 = Operation Successful or Currently Running
- 01 = Device in Sleep Mode or Pending Sleep
- 10 = Operation Unsuccessful
- 11 = Operation Aborted

GSR.3 = QUEUE STATUS
- 1 = Queue Full
- 0 = Queue Available

GSR.2 = PAGE BUFFER AVAILABLE STATUS
- 1 = One or Two Pages Available
- 0 = No Page Buffer Available

GSR.1 = PAGE BUFFER STATUS
- 1 = Selected Page Buffer Ready
- 0 = Selected Page Buffer Available

GSR.0 = PAGE BUFFER SELECT STATUS
- 1 = Page Buffer 1 Selected
- 0 = Page Buffer 0 Selected

NOTES:
1. The WSMS bit must first be checked to determine completion of a operation (Block Lock, Suspend, Upload Status Bit, Erase or Data Write), before the appropriate Status bit (OSS or DOS) is checked for success.
2. If the operation currently running, then GSR.7 = 0
3. If device pending sleep, then GSR.7 = 0
4. Operation aborted. Unsuccessful due to Abort Command
5. The Device contains two Page Buffers.
6. Selected Page Buffer is currently busy with WSM operation.

Note:
1. When multiple operations are queued, checking BSR 7 only provides indication of completion for that particular block. GSR 7 provides indication when all queued operations are completed.

Table 6 — Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS
- 1 = Ready
- 0 = Busy

BSR.6 = BLOCK-LOCP STATUS
- 1 = Block Unlocked for Write/Erase
- 0 = Block locked for Write/Erase

BGR.5 = BLOCK OPERATION STATUS
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS
- 1 = Operation Aborted
- 0 = Operation not Aborted

MATRIX 5/4
- 00 = Operation Successful or Currently Running
- 01 = Not a Valid Combination
- 10 = Operation Unsuccessful
- 11 = Operation Aborted (3)

BSR.3 = QUEUE STATUS
- 1 = Queue Full
- 0 = Queue Available

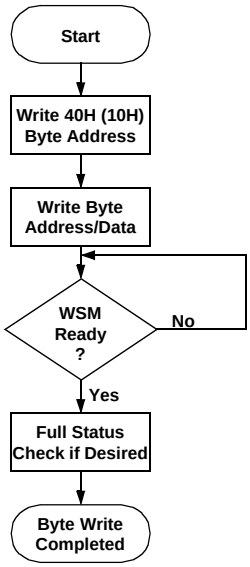
BSR.2 = VPP STATUS
- 1 = VPP Low Detect, Operation Aborted
- 0 = Vpp OK

BSR.1–BSR.0 = RESERVED FOR FUTURE ENHANCEMENTS (4)

NOTES:
1. BS must be checked to determine completion of a n operation (Block Lock, Suspend, Erase or Data Write) before the appropriate Status bit (BOS,BLS) is checked for success.
2. The BOAS bit will not be set until BSR.7 = 1
3. Operation halted via Abort Command.
4. These bits are reserved for future use, mask them out when polling the BSRs.

Note:
1. When multiple operations are queued, checking BSR 7 only provides indication of completion for that particular block. GSR 7 provides indication when all queued operations are completed.

Figure 5 Automated Byte Write Algorithm



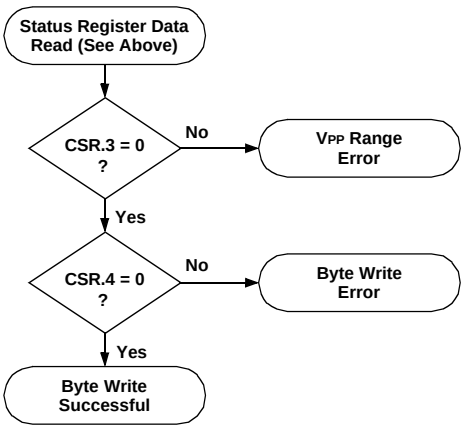
Bus Operations	Command Sequence	Comments
Write	Byte Write Setup	Data = 40H (10H) Address = Byte to be Written
Write	Byte Write	Data to be written Address = Byte to be written
Standby/Reset		Check WSMS bit V_{OH} = Ready, V_{OL} = Busy or Ready Status Register Check CSR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register

Repeat for subsequent bytes

Full status check can be done after each byte or after a sequence of bytes

Write FFH after the last byte write operation to reset the device to Ready Array Mode

Full Status Check Procedure



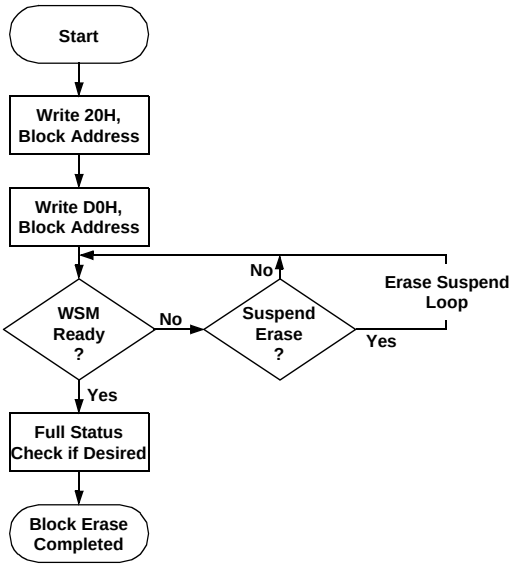
Bus Operations	Command Sequence	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check CSR.3 1 = V_{PP} Low Detect
Standby		Check CSR.4 1 = Byte Write Error

CSR.3 Must be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine.

CSR.4 is only cleared by the clear status register command, in cases where multiple bytes are written before full status is checked.

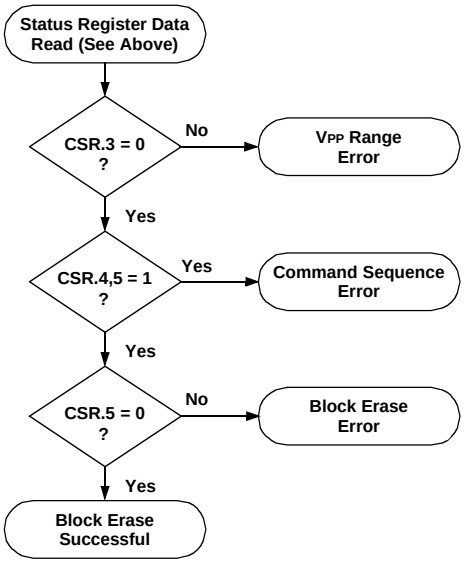
If error is detected, clear the status register before attempting retry on other error recovery.

Figure 6 Automated Block Erase Algorithm



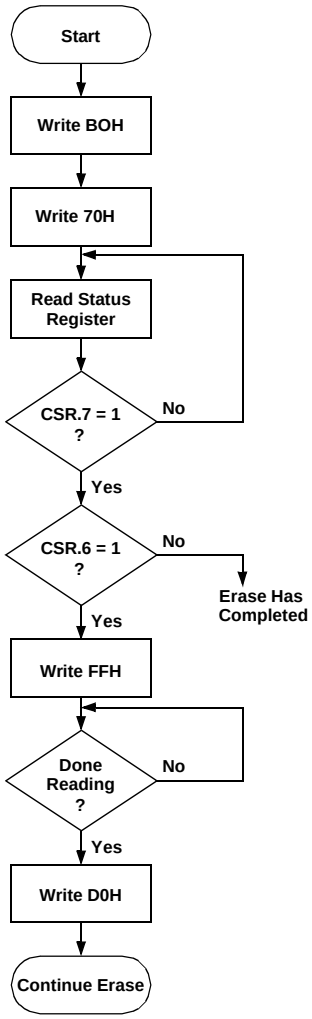
Bus Operations	Command Sequence	Comments
Write	Erase Setup	Data = 20H Address = Within block to be erased
Write	Erase	Data = D0H Address = Within block to be erased
Standby/Reset		Check WSMS bit V_{OH} = Ready, V_{OL} = Busy or Ready Compatible Status Register Check CSR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to update Compatible Status Register
Repeat for subsequent bytes Full status check can be done after each byte or after a sequence of bytes Write FFH after the last byte write operation to reset the device to Ready Array Mode		

Full Status Check Procedure



Bus Operations	Command Sequence	Comments
Optional Read		CPU may already have read Compatible Status Register data in WSM Ready polling above
Standby		Check CSR.3 1 = V_{PP} Low Detect
Standby		Check CSR.4, 5 Both 1 = Command Sequence Error
Standby		Check CSR.5 1 = Block Erase Error

Figure 7 Erase Suspend/Resume Algorithm

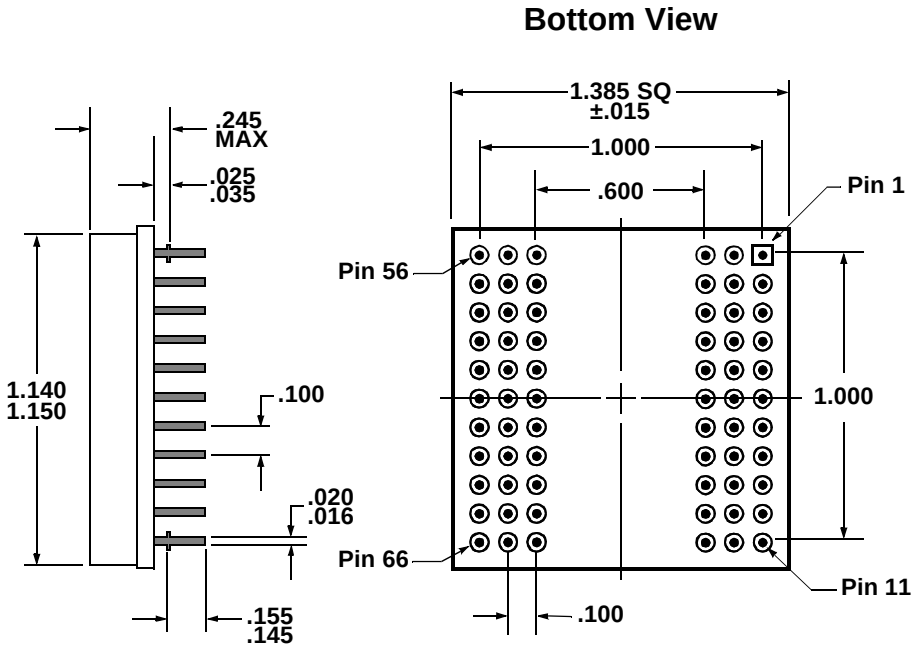


Bus Operations	Command Sequence	Comments
Write	Erase Suspend	Data = 80H
Write	Read Status Register	Data = 70H
Standby/Reset		Read Campatible Status Register
		Check CSR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check CSR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased
Write		Data = D0H

Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O_8	18	A_{15}	35	I/O_{25}	52	A_{20}
2	I/O_9	19	Vcc	36	I/O_{26}	53	$\overline{CE}_3$
3	I/O_{10}	20	$\overline{CE}_1$	37	A_7	54	GND
4	A_{14}	21	A_{19}	38	A_{12}	55	I/O_{19}
5	A_{16}	22	I/O_3	39	V_{PP}	56	I/O_{31}
6	A_{11}	23	I/O_{15}	40	A_{13}	57	I/O_{30}
7	A_0	24	I/O_{14}	41	A_8	58	I/O_{29}
8	A_{18}	25	I/O_{13}	42	I/O_{16}	59	I/O_{28}
9	I/O_0	26	I/O_{12}	43	I/O_{17}	60	A_1
10	I/O_1	27	$\overline{OE}$	44	I/O_{18}	61	A_2
11	I/O_2	28	A_{17}	45	V_{CC}	62	A_3
12	$\overline{RP}$	29	$\overline{WE}$	46	$\overline{CE}_4$	63	I/O_{23}
13	$\overline{CE}_2$	30	I/O_7	47	$\overline{WP}$	64	I/O_{22}
14	GND	31	I/O_6	48	I/O_{27}	65	I/O_{21}
15	I/O_{11}	32	I/O_5	49	A_4	66	I/O_{20}
16	A_{10}	33	I/O_4	50	A_5		
17	A_9	34	I/O_{24}	51	A_6		

"P1"— 1.38" SQ PGA Type Package

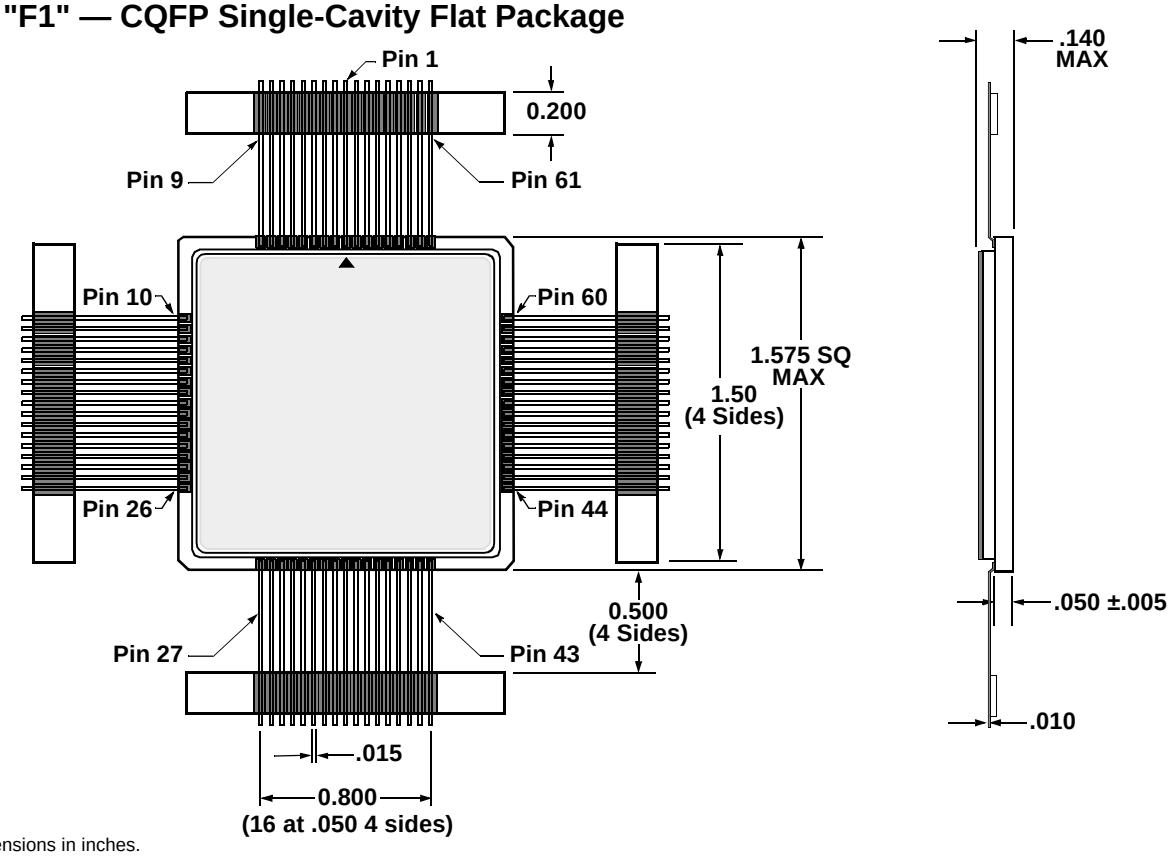


Dimensions in inches.

Pin Numbers & Functions

68 Pins — CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_1$	19	I/O_8	36	$\overline{CE}_4$	53	I/O_{23}
3	A_5	20	I/O_9	37	A_{17}	54	I/O_{22}
4	A_4	21	I/O_{10}	38	A_{18}	55	I/O_{21}
5	A_3	22	I/O_{11}	39	A_{19}	56	I/O_{20}
6	A_2	23	I/O_{12}	40	A_{20}	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	$\overline{RP}$	59	I/O_{17}
9	$\overline{WP}$	26	I/O_{15}	43	V_{PP}	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}$
17	I/O_7	34	$\overline{CE}_2$	51	I/O_{24}	68	$\overline{CE}_3$

"F1" — CQFP Single-Cavity Flat Package



Dimensions in inches.

AEROFLEX
CIRCUIT TECHNOLOGY

Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT–F2M32N–080P1M	5962–TBD	80nS	Plug-in
ACT–F2M32N–100P1M	5962–TBD	100nS	Plug-in
ACT–F2M32N–120P1M	5962–TBD	120nS	Plug-in
ACT–F2M32N–080F1M	5962–TBD	80nS	CQFP
ACT–F2M32N–100F1M	5962–TBD	100nS	CQFP
ACT–F2M32N–120F1M	5962–TBD	120nS	CQFP

Part Number Breakdown

ACT– F 2M 32 N– 020 F1 M

Aeroflex Circuit Technology

Memory Type
- S = SRAM
- F = FLASH EEPROM
- E = EEPROM
- D = Dynamic RAM

Memory Depth, Bits

Memory Width, Bits

Pinout Options
- N = X

Memory Speed, ns

Screening
- C = Commercial Temp, 0°C to +70°C, No 883 Screening
- I = Industrial Temp, -40°C to +85°C, No 883 Screening
- T = Military Temp, -55°C to +125°C, No 883 Screening
- M = Military Temp, -55°C to +125°C, 883 Screening
- Q = MIL-STD-883 Compliant

Package Type & Size

Surface Mount Packages	*Thru-Hole Packages*
F1 = 1.56"SQ 68 Lead CQFP	P1 = 1.385"SQ PGA 66 Pins
F2 = .88"SQ 68 Lead Dual-Cavity CQFP	P2 = 1.185"SQ PGA 66 Pins
F3 = 36 Lead FP	P3 = 1.075"SQ PGA 66 Pins
F4 = 36 Lead CSOJ	P4 = 32 Pin DIP

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