



64K x 4 Static RAM with Separate I/O

Features

- High speed
 - 12 ns
- CMOS for optimum speed/power
- Low active power
 - 880 mW
- Low standby power
 - 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

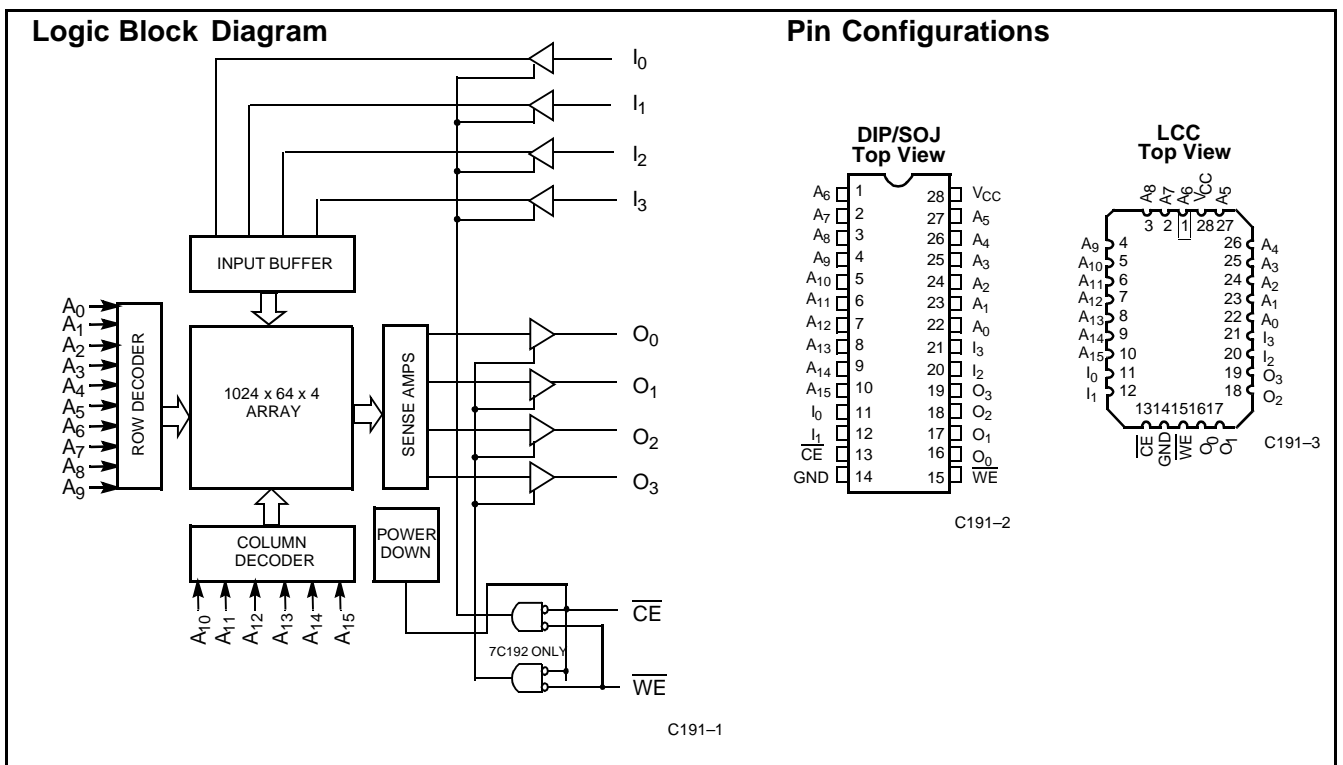
Functional Description

The CY7C192 is a high-performance CMOS static RAM organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW Chip Enable (\overline{CE}) and three-state drivers.

It has an automatic power-down feature, reducing the power consumption by 75% when deselected. Writing to the device is accomplished when the Chip Enable (\overline{CE}) and write enable (\overline{WE}) inputs are both LOW.

Reading the device is accomplished by taking the Chip Enable (\overline{CE}) LOW while the Write Enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when Write Enable (\overline{WE}) is LOW, or Chip Enable (\overline{CE}) is HIGH. A die coat is used to insure alpha immunity.



Selection Guide

| | 7C192-12 | 7C192-15 | 7C192-20 | 7C192-25 |
|--------------------------------|----------|----------|----------|----------|
| Maximum Access Time (ns) | 12 | 15 | 20 | 25 |
| Maximum Operating Current (mA) | 155 | 145 | 135 | 115 |
| Maximum Standby Current (mA) | 30 | 30 | 30 | 30 |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1]..... -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature ^[2] | V_{CC} |
|------------|------------------------------------|----------|
| Commercial | 0°C to +70°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C192-12 | | 7C192-15 | | Unit |
|-----------|--|--|----------|-----------------|----------|-----------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3V$ | 2.2 | $V_{CC} + 0.3V$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -5 | +5 | -5 | +5 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -5 | +5 | -5 | +5 | μA |
| I_{OS} | Output Short Circuit Current ^[3] | $V_{CC} = \text{Max.}, V_{OUT} = GND$ | | -300 | | -300 | mA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$ | | 155 | | 145 | mA |
| I_{SB1} | Automatic \overline{CE} Power-Down Current—TTL Inputs | Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | | 30 | | 30 | mA |
| I_{SB2} | Automatic \overline{CE} Power-Down Current—CMOS Inputs | Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$ | | 10 | | 10 | mA |

Notes:

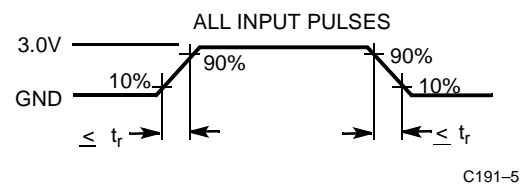
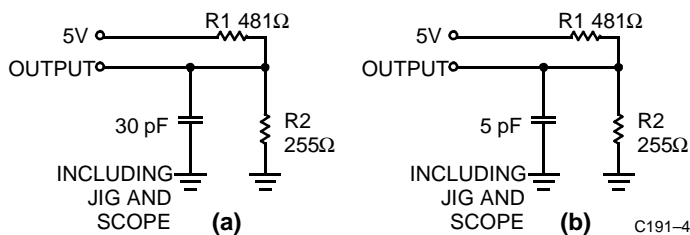
1. Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
2. T_A is the case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range

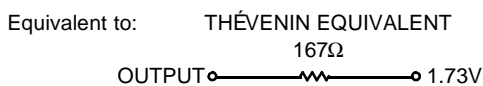
| Parameter | Description | Test Conditions | 7C192-20 | | 7C192-25 | | Unit |
|-----------|--|---|----------|-----------------|----------|-----------------|---------------|
| | | | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3V$ | 2.2 | $V_{CC} + 0.3V$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -3.0 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -5 | +5 | -5 | +5 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -5 | +5 | -5 | +5 | μA |
| I_{OS} | Output Short Circuit Current ^[3] | $V_{CC} = \text{Max.}, V_{OUT} = GND$ | | -300 | | -300 | mA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$ | | 135 | | 115 | mA |
| I_{SB1} | Automatic \overline{CE} Power-Down Current—TTL Inputs | Max. $V_{CC}, \overline{CE} \geq V_{IH}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$ | | 30 | | 30 | mA |
| I_{SB2} | Automatic \overline{CE} Power-Down Current—CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.3V, V_{IN} \leq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$ | | 15 | | 15 | mA |

Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|--------------------|--|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 5.0V$ | 8 | pF |
| C_{OUT} | Output Capacitance | | 10 | pF |

AC Test Loads and Waveforms^[5]


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Notes:

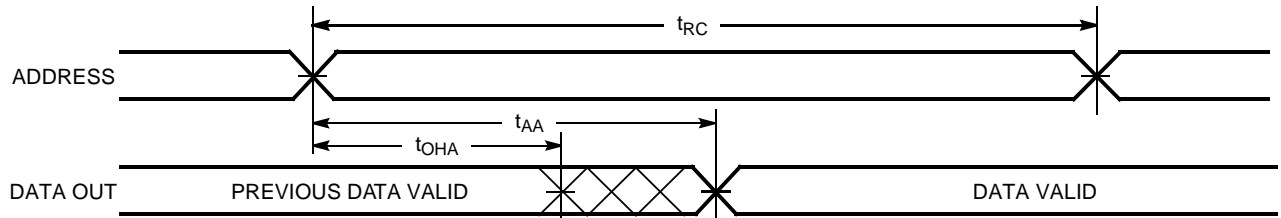
- Tested initially and after any design or process changes that may affect these parameters.
- $t_r = \leq 3 \text{ ns}$ for the -12 and -15 speeds. $t_r = \leq 5 \text{ ns}$ for the -20 and slower speeds.

Switching Characteristics Over the Operating Range^[6]

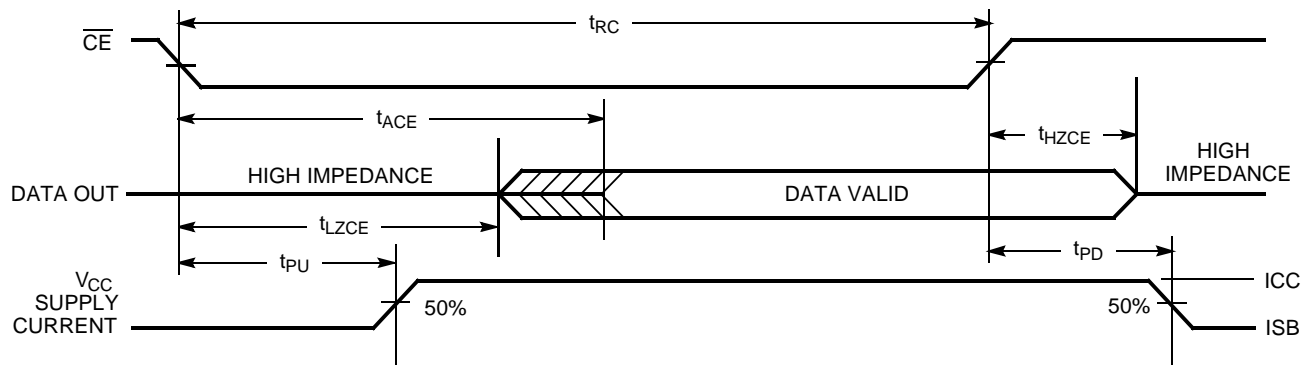
| Parameter | Description | 7C192-12 | | 7C192-15 | | 7C192-20 | | 7C192-25 | | Unit |
|----------------------------------|---|----------|------|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 12 | | 15 | | 20 | | 25 | | ns |
| t _{AA} | Address to Data Valid | | 12 | | 15 | | 20 | | 25 | ns |
| t _{OHA} | Output Hold from Address Change | 3 | | 3 | | 3 | | 3 | | ns |
| t _{ACE} | $\overline{\text{CE}}$ LOW to Data Valid | | 12 | | 15 | | 20 | | 25 | ns |
| t _{LZCE} | $\overline{\text{CE}}$ LOW to Low Z ^[7] | 3 | | 3 | | 3 | | 3 | | ns |
| t _{HZCE} | $\overline{\text{CE}}$ HIGH to High Z ^[7,8] | | 5 | | 7 | | 9 | | 11 | ns |
| t _{PU} | $\overline{\text{CE}}$ LOW to Power-Up | 0 | | 0 | | 0 | | 0 | | ns |
| t _{PD} | $\overline{\text{CE}}$ HIGH to Power-Down | | 12 | | 15 | | 20 | | 25 | ns |
| WRITE CYCLE^[9] | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 12 | | 15 | | 20 | | 25 | | ns |
| t _{SCE} | $\overline{\text{CE}}$ LOW to Write End | 9 | | 10 | | 15 | | 18 | | ns |
| t _{AW} | Address Set-Up to Write End | 9 | | 10 | | 15 | | 20 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | 0 | | ns |
| t _{PWE} | $\overline{\text{WE}}$ Pulse Width | 8 | | 9 | | 15 | | 18 | | ns |
| t _{SD} | Data Set-Up to Write End | 8 | | 9 | | 10 | | 10 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | $\overline{\text{WE}}$ HIGH to Low Z (7C192) ^[7] | 3 | | 3 | | 3 | | 3 | | ns |
| t _{HZWE} | $\overline{\text{WE}}$ LOW to High Z (7C192) ^[7,8] | | 7 | | 7 | | 10 | | 11 | ns |
| t _{DWE} | $\overline{\text{WE}}$ LOW to Data Valid (7C191) | | 12 | | 15 | | 20 | | 25 | ns |
| t _{ADV} | Data Valid to Output Valid (7C191) | | 12 | | 15 | | 20 | | 20 | ns |
| t _{DCE} | $\overline{\text{CE}}$ LOW to Data Valid (7C191) | | 12 | | 15 | | 20 | | 25 | ns |

Notes:

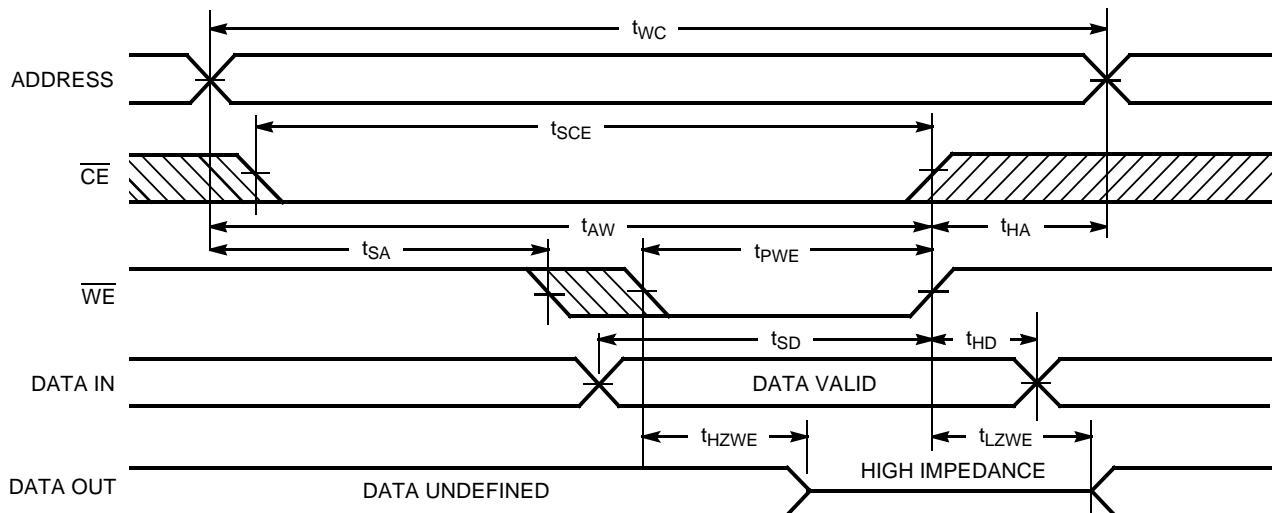
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 through -25 speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZWE} is less than t_{LZWE} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No. 1^[10, 11]


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Read Cycle No. 2^[10, 12]


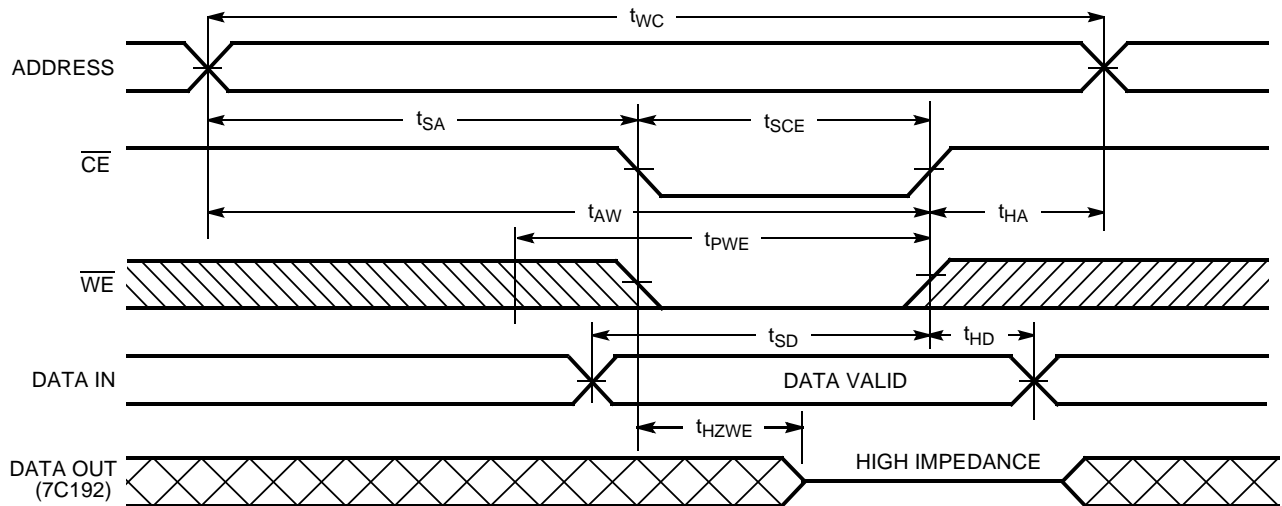
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Write Cycle No. 1 (WE Controlled)^[9]


C191-8

Notes:

10. WE is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. Address valid prior to or coincident with CE transition LOW.

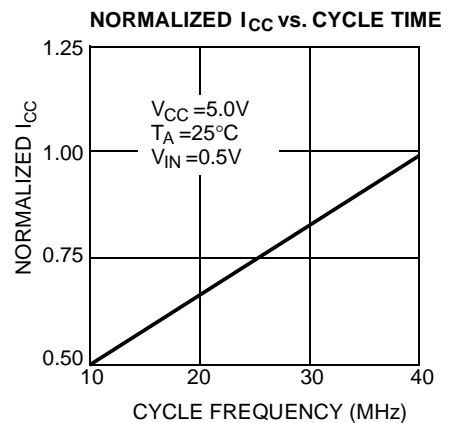
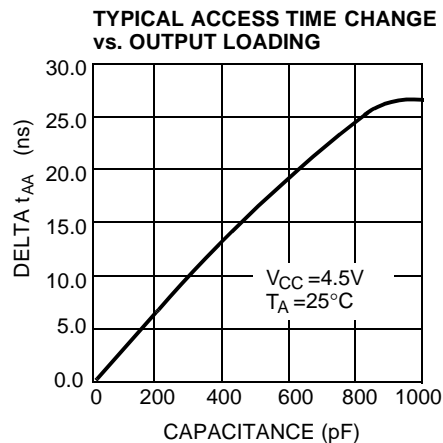
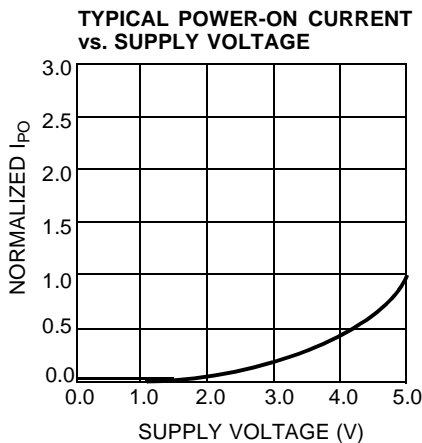
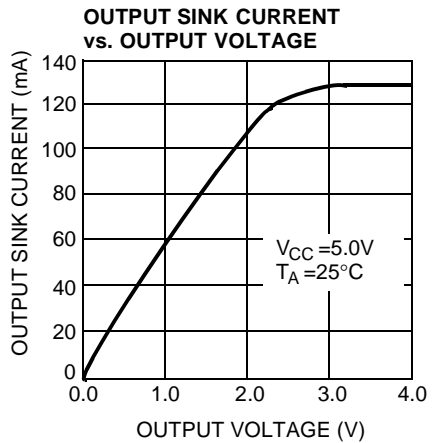
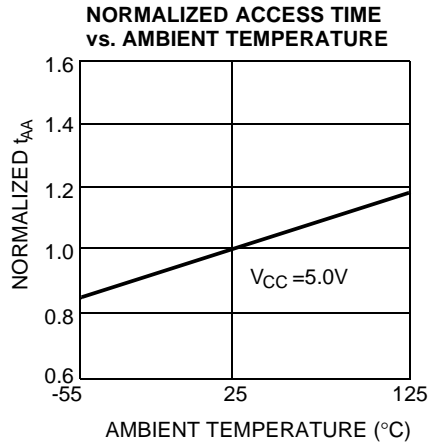
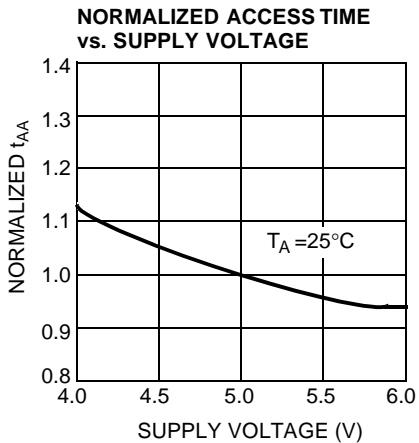
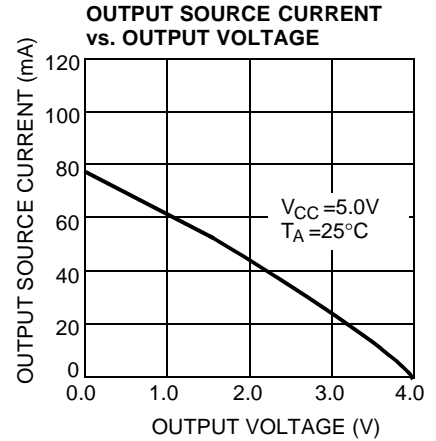
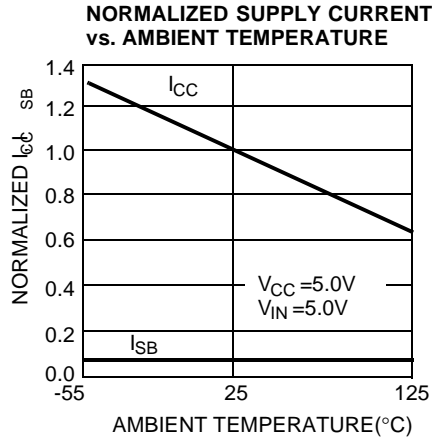
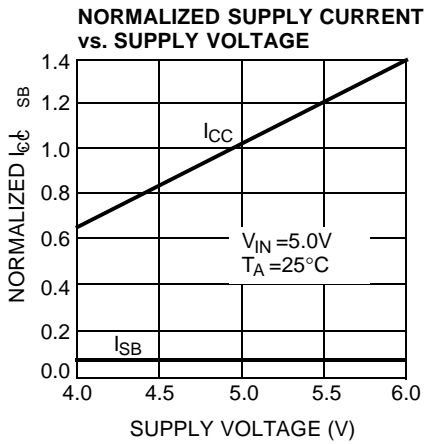
Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CE} Controlled)^[9, 13]


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Notes:

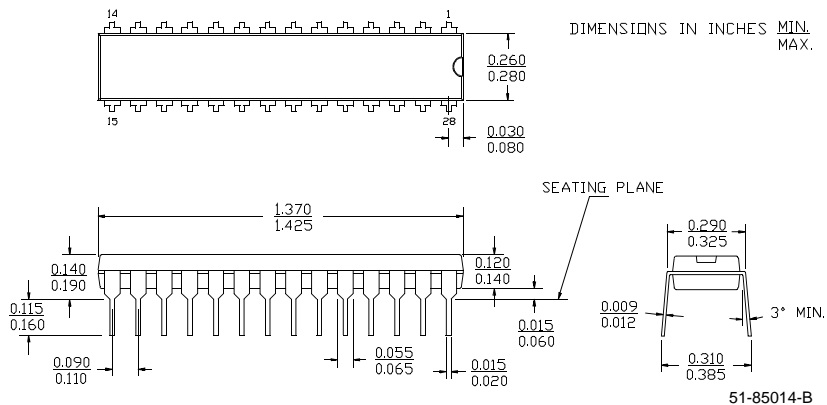
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

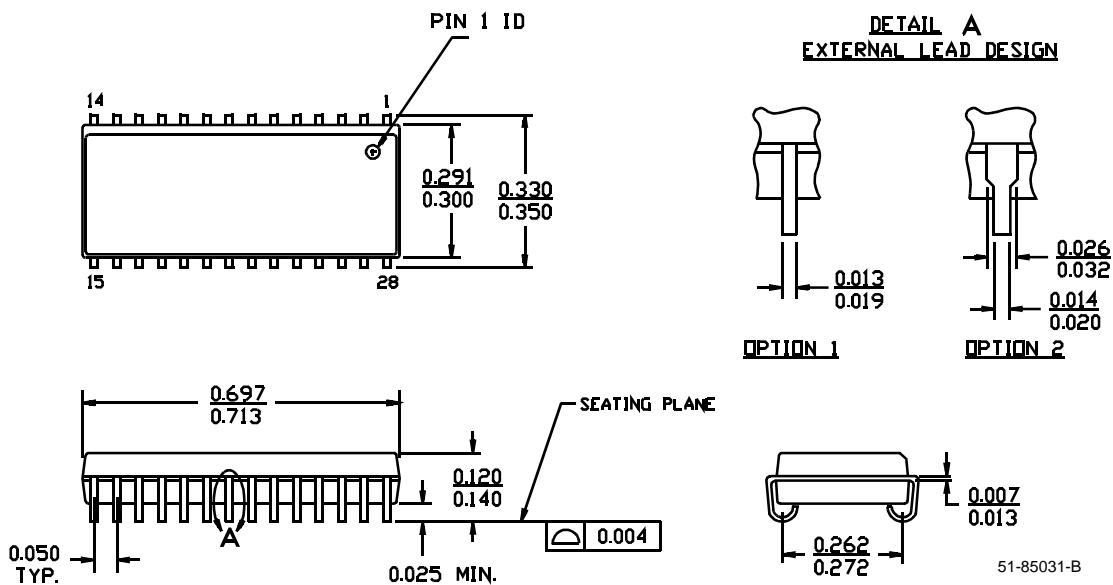


Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|------------------------------|-----------------|
| 12 | CY7C192-12PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C192-12VC | V21 | 28-Lead Molded SOJ | |
| 15 | CY7C192-15PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C192-15VC | V21 | 28-Lead Molded SOJ | |
| 20 | CY7C192-20PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C192-20VC | V21 | 28-Lead Molded SOJ | |
| 25 | CY7C192-25PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C192-25VC | V21 | 28-Lead Molded SOJ | |

Package Diagrams
28-Lead (300-Mil) Molded DIP P21

28-Lead (300-Mil) Molded SOJ V21

DIMENSIONS IN INCHES MIN.
MAX.





Document Title: CY7C192 64K x 4 Static RAM with Separate I/O
Document Number: 38-05047

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|-------------|----------------|-------------------|------------------------|---|
| ** | 107149 | 09/10/01 | SZV | Change Spec number from: 38-00076 to 38-05047 |