REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change case outline X to case outline Q. Add case outline Y. Delete group C programmability test and add margin test. Convert to military drawing format.	86 SEP 23	M.A. Frye
B	Add vendor CAGE 34335. Add device type 02. Change drawing CAGE number. Editorial changes throughout.	88 MAY 26	M.A. Frye

CURRENT CAGE CODE 67268

REV STATUS OF SHEETS																						
REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Fitz

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 24 JUNE 1985

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, N-CHANNEL, MOS 8-BIT MICROCOMPUTER WITH 32 K-BIT UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	84190

SHEET 1 OF 20

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E917

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

84190	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	8751H-8	8-bit microcomputer with 32 K-bit UVEPROM	8.0 MHz max
02	8751H	8-bit microcomputer with 32 K-bit UVEPROM	12.0 MHz max

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline 1/
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
Y	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Voltage on any pin (except V_{PP}) 2/	-0.5 V dc to +7.0 V dc
Voltage (V_{PP})	21.5 V dc
Power dissipation (P_D)	2.0 W
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+165°C
Lead temperature (soldering, 5 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Q and Y	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Program voltage (V_{PP})	21.0 V dc ±0.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to V_{SS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Programmed EPROM device. The requirements for supplying programmed EPROM devices are not part of this drawing.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		All	1, 2, 3		0.7	V
Input high voltage (except XTAL2, RST)	V_{IH}		All	1, 2, 3	2.2		V
Input high voltage to XTAL2, RST	V_{IH1}	XTAL1 = V_{SS}	All	1, 2, 3	2.5		V
Output low voltage ports 1, 2, 3	V_{OL}	I_{OL} = 1.2 mA	All	1, 2, 3		0.45	V
Output low voltage port 0 ALE, $\overline{PSEN}$	V_{OL1}	I_{OL} = 2.8 mA I_{OL} = 2.4 mA	All	1, 2, 3		0.60 0.45	V
Output high voltage ports 1, 2, 3	V_{OH}	I_{OH} = -60 µA	All	1, 2, 3	2.4		V
Output high voltage port 0 (in external bus mode), ALE, $\overline{PSEN}$	V_{OH1}	I_{OH} = -300 µA	All	1, 2, 3	2.4		V
Logical 0 input current P1, P2, P3	I_{IL}	V_{IN} = 0.45 V	All	1, 2, 3		-500	µA
Logical 0 input current to $\overline{EA}/V_{PP}$	I_{IL1}	V_{IN} = 0.45 V	All	1, 2, 3		-15	mA
Logical 0 input current to XTAL2	I_{IL2}	XTAL1 = V_{SS} V_{IN} = 0.45 V	All	1, 2, 3		-4.5	mA
Input leakage current to port 0	I_{LI}	$0.45 < V_{IN} < V_{CC}$	All	1, 2, 3		±125	µA
Logical input current to $\overline{EA}/V_{PP}$	I_{IH}	V_{IN} = 2.4 V	All	1, 2, 3		500	µA
Input current to RST/V_{PD} to activate reset	I_{IH1}	$V_{IN} < (V_{CC} - 1.5\ V)$	All	1, 2, 3		500	µA
Power supply current	I_{CC}	All outputs disconnected, $\overline{EA}$ = V_{CC}	All	1, 2, 3		275	mA
Capacitance of I/O buffers	$C_{I/O}$	fc = 1 MHz, T_C = +25°C See 4.3.1c	All	4		10	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Limits 2/ Min	Limits 2/ Max	Unit
Oscillator period	t_{CLCL}	C_L (Port 0, ALE, $\overline{PSEN}$) = 100 pF	01	9,10,11	125	286	t_{CLCL}	t_{CLCL}	ns
			02		83	286			
High time 1/ 3/	t_{CHCX}	C_L (all others) = 80 pF	All		20		20		
Low time 1/ 3/	t_{CLCX}	f_{MAX} = 8 MHz device 01			20		20		
Rise time 1/ 3/	t_{CLCH}	f_{MAX} = 12 MHz device 02				20		20	
Fall time 1/ 3/	t_{CHCL}	See figures 3 and 4 4/				20		20	
ALE pulse width	t_{LHLL}		01		195		$2t_{CLCL}$ -55		
			02		112				
Address valid to ALE	t_{AVLL}		01		70		t_{CLCL} -55		
			02		28				
Address hold after ALE	t_{LLAX}		01		75		t_{CLCL} -50		
			02		33				
ALE to valid instr in	t_{LLIV}		01			335		$4t_{CLCL}$ -165	
			02			168			
ALE to $\overline{PSEN}$	t_{LLPL}		01		85		t_{CLCL} -40		
			02		43				
$\overline{PSEN}$ pulse width	t_{PLPH}		01		300		$3t_{CLCL}$ -75		
			02		175				
$\overline{PSEN}$ to valid instr in	t_{PLIV}		01			210		$3t_{CLCL}$ -165	
			02			85			
Input instr hold after $\overline{PSEN}$	t_{PXIX}		All		0		0		
Input instr float 1/ after $\overline{PSEN}$	t_{PXIZ}		01			90		t_{CLCL} -35	
			02			48			
$\overline{PSEN}$ to address valid	t_{PXAV}		01		100		t_{CLCL} -25		
			02		58				
Address to valid instr in	t_{AVIV}		01			460		$5t_{CLCL}$ -165	
			02			252			
Address float 1/ to $\overline{PSEN}$	t_{AZPL}		All		0		0		
$\overline{RD}$ pulse width	t_{RLRH}		01		650		$6t_{CLCL}$ -100		
			02		400				
$\overline{WR}$ pulse width	t_{WLWH}		01		650		$6t_{CLCL}$ -100		
			02		400				
Address hold after ALE	t_{LLAX}		01		75		t_{CLCL} -50		
			02		33				
$\overline{RD}$ to valid data in	t_{RLDV}		01			440		$5t_{CLCL}$ -185	
			02			232			
Data hold after $\overline{RD}$	t_{RHDX}		All		0		0		
Data float 1/ after $\overline{RD}$	t_{RHDZ}		01			165		$2t_{CLCL}$ -85	
			02			82			
ALE to valid data in	t_{LLDV}		01			830		$8t_{CLCL}$ -170	
			02			496			
Address to valid data in	t_{AVDV}		01			940		$9t_{CLCL}$ -185	
			02			565			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Limits 2/ Min	Limits 2/ Max	Unit
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	C_L (Port 0, ALE, $\overline{PSEN}$) = 100 pF C_L (all others) = 80 pF See figures 3 and 4 4/ f_{MAX} = 8 MHz device 01 f_{MAX} = 12 MHz device 02	01	9,10,11	310	440	$3t_{CLCL}$ -65	$3t_{CLCL}$ +65	ns
			02		185	315			
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}		01		355		$4t_{CLCL}$ -145		
			02		188				
Data valid to $\overline{WR}$ transition	t_{QVWX}		01		40		t_{CLCL} -85		
			02		0				
Data setup to $\overline{WR}$ high	t_{QVWH}		01		800		$7t_{CLCL}$ -75		
			02		508				
Data held after $\overline{WR}$	t_{WHQX}		01		60		t_{CLCL} -65		
			02		18				
$\overline{RD}$ low to address float 1/	t_{RLAZ}		All		0		0		
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		01		60	190	t_{CLCL} -65	t_{CLCL} +65	
			02		18	148			

1/ Tested only initially and after any design changes.

2/ Variable oscillator equations provided for design purposes.

3/ Required external clock drive characteristics (XTAL2).

4/ AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.9.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.9.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.9.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.9.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using Vm = +5.9 V at +25°C using loose timing (i.e., T_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at Vm = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.9.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.9.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified and the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved source of supply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/ 2/ 3/ 4/
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10 or 1, 2, 3
Additional electrical subgroups for group C periodic inspections	---

1/ (*) Indicates PDA applies to subgroup 1.
2/ Any or all subgroup may be combined when using a high speed tester.
3/ Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified and the instruction set.
4/ For all electrical tests, the device shall be programmed to the pattern specified (see 4.3.1d).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasures, all bits are in the high state.

4.5 Programming procedures for method A. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration (see figure 5) for programming the waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

TABLE III. Programming characteristics.

Parameter	Symbol	Conditions	Min	Max	Units
Programming supply voltage	V_{PP}	V_{CC} = 5.0 V ±10%	20.5	21.5	V
Programming current	I_{PP}	T_C = +25°C		30	mA
Oscillator frequency	$1/t_{CLCL}$		4	6	MHz
Address setup to $\overline{PROG}$	t_{AVGL}		$48t_{CLCL}$		ns
Address hold after $\overline{PROG}$	t_{GHAX}		$48t_{CLCL}$		ns
Data setup to $\overline{PROG}$	t_{DVGL}		$48t_{CLCL}$		ns
Data hold after $\overline{PROG}$	t_{GHDX}		$48t_{CLCL}$		ns
$\overline{ENABLE}$ high to V_{PP}	t_{EHSH}		$48t_{CLCL}$		ns
V_{PP} setup to $\overline{PROG}$	t_{SHGL}		10		µs
V_{PP} hold after $\overline{PROG}$	t_{GHSL}		10		µs
$\overline{PROG}$ width	t_{GLGH}		45	55	ms
Address to data valid	t_{AVQV}			$48t_{CLCL}$	ns
$\overline{ENABLE}$ to data valid	t_{ELQV}			$48t_{CLCL}$	ns
Data float after $\overline{ENABLE}$	t_{EHQZ}		0	$48t_{CLCL}$	ns

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

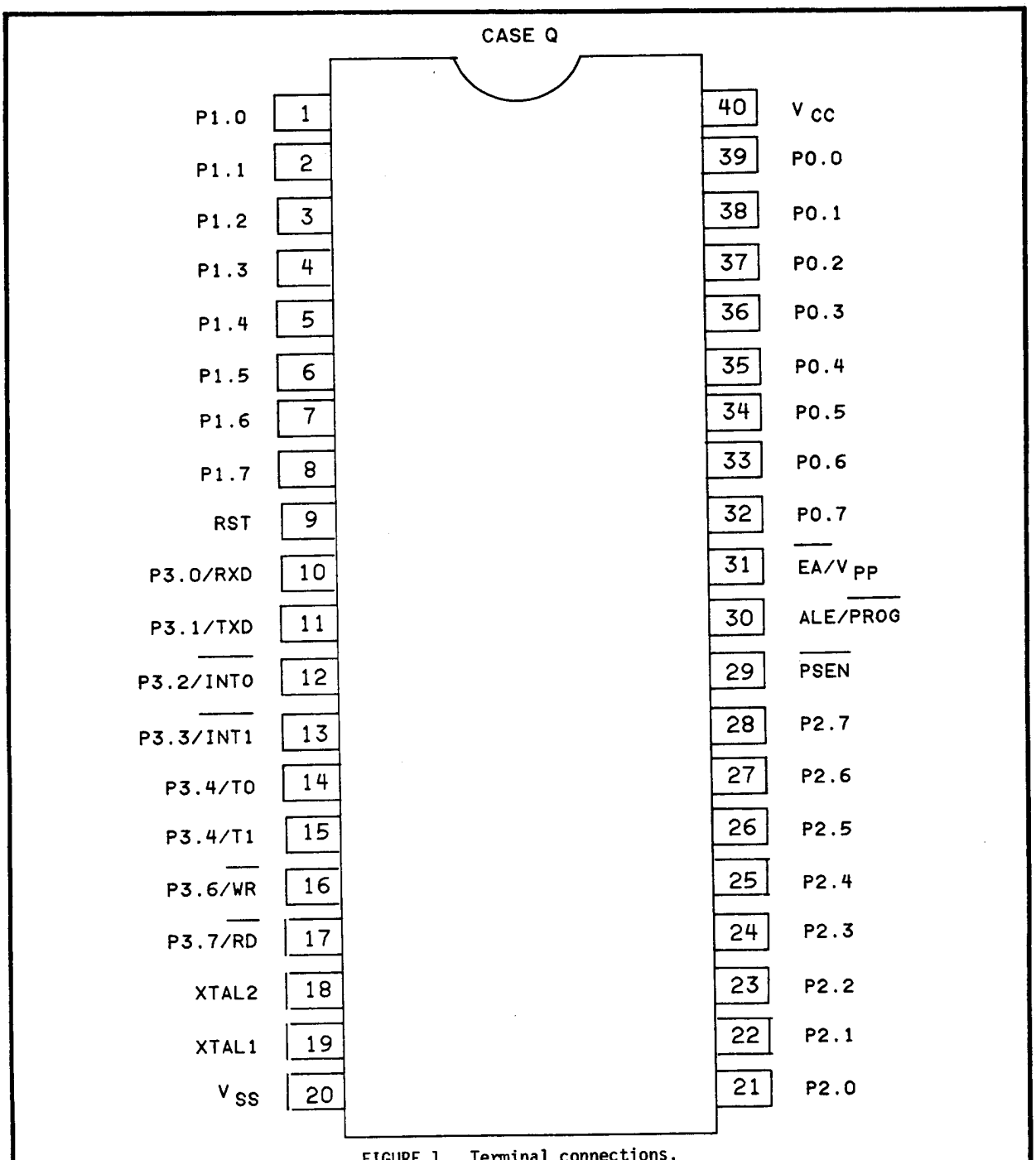

FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84190
		REVISION LEVEL B	SHEET 10

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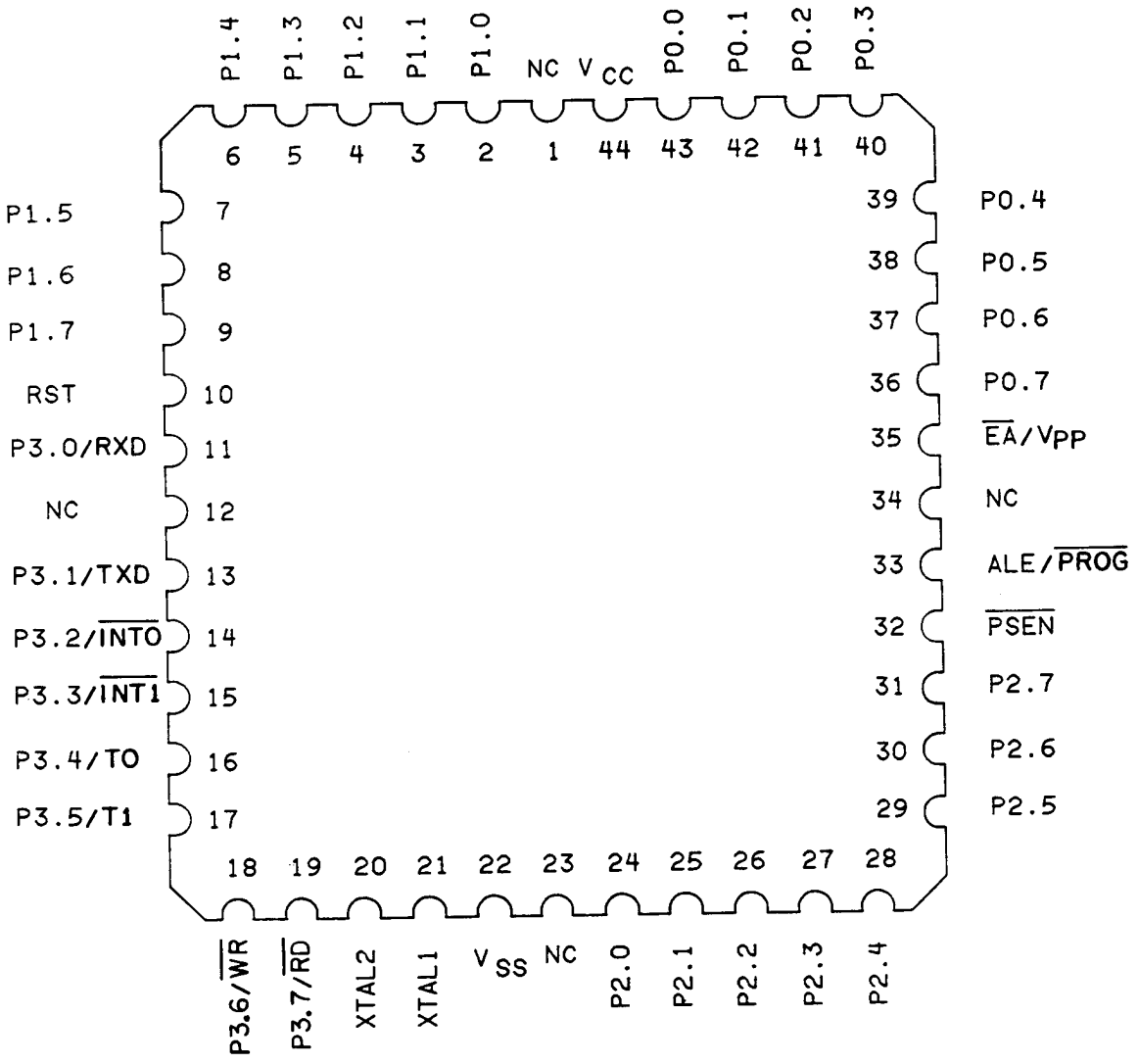
CASE Y



TOP VIEW

FIGURE 1. Terminal connections - Continued.

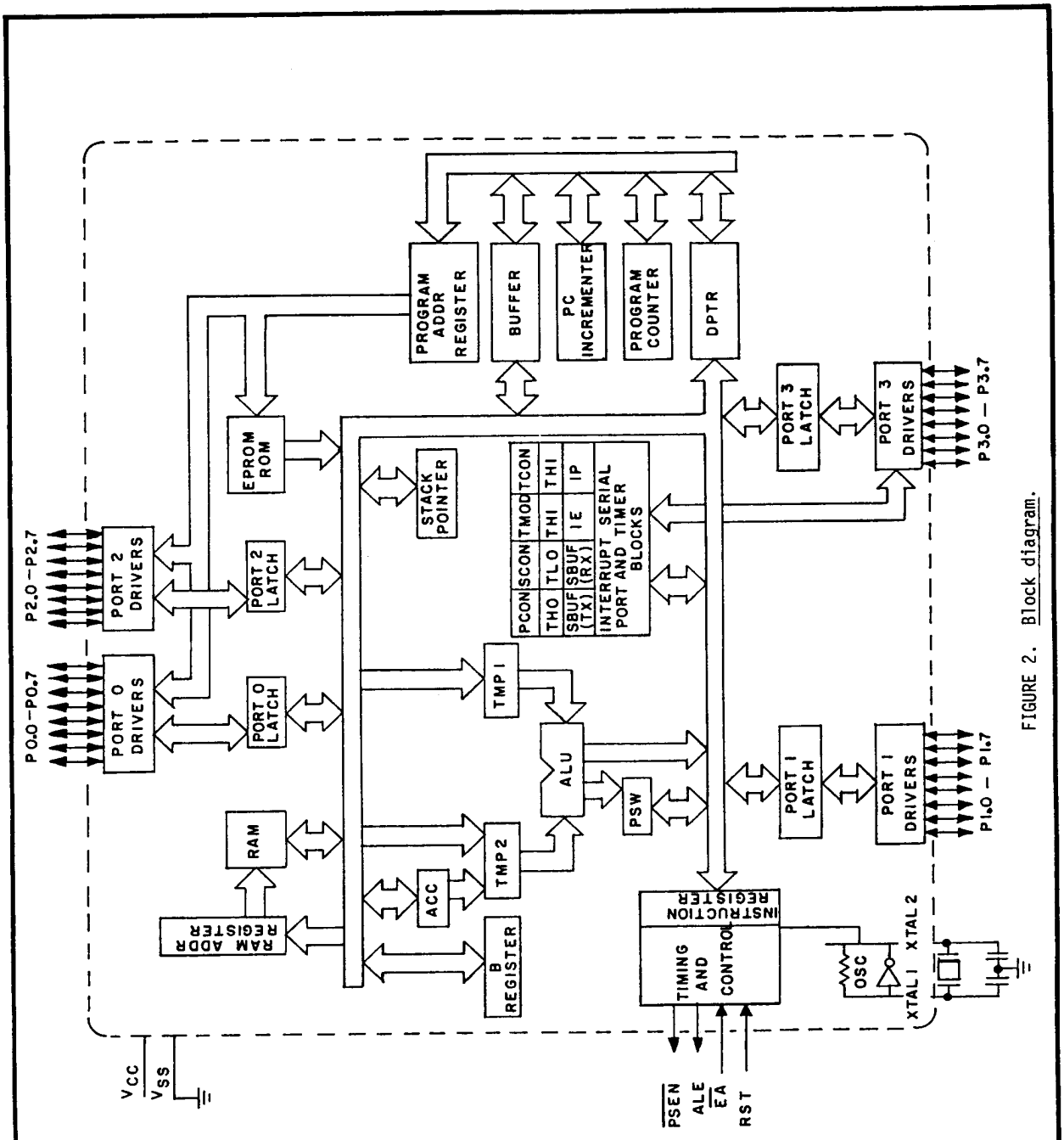


FIGURE 2. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84190
		REVISION LEVEL B	SHEET 12

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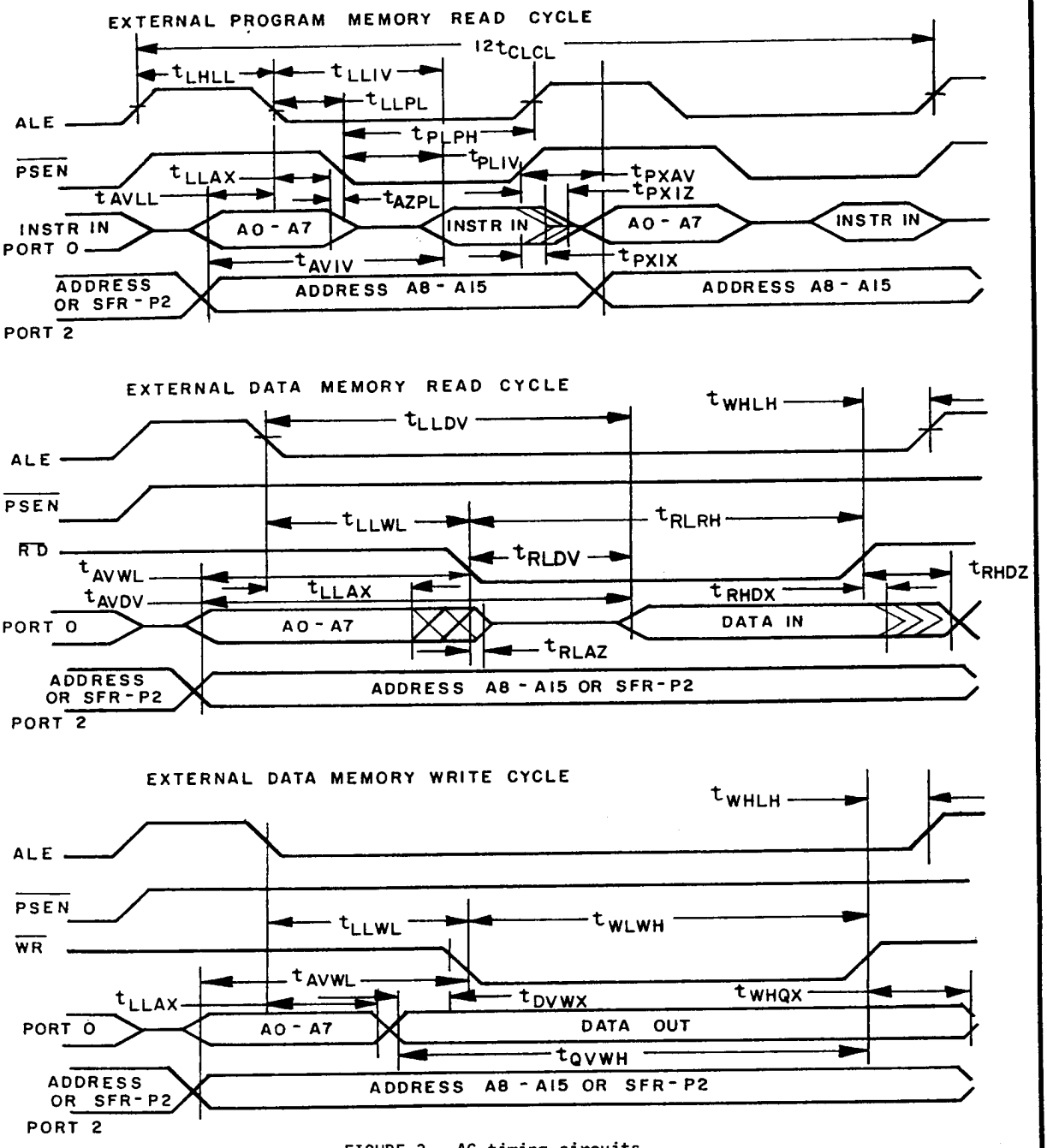

FIGURE 3. AC timing circuits.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84190
		REVISION LEVEL B	SHEET 13

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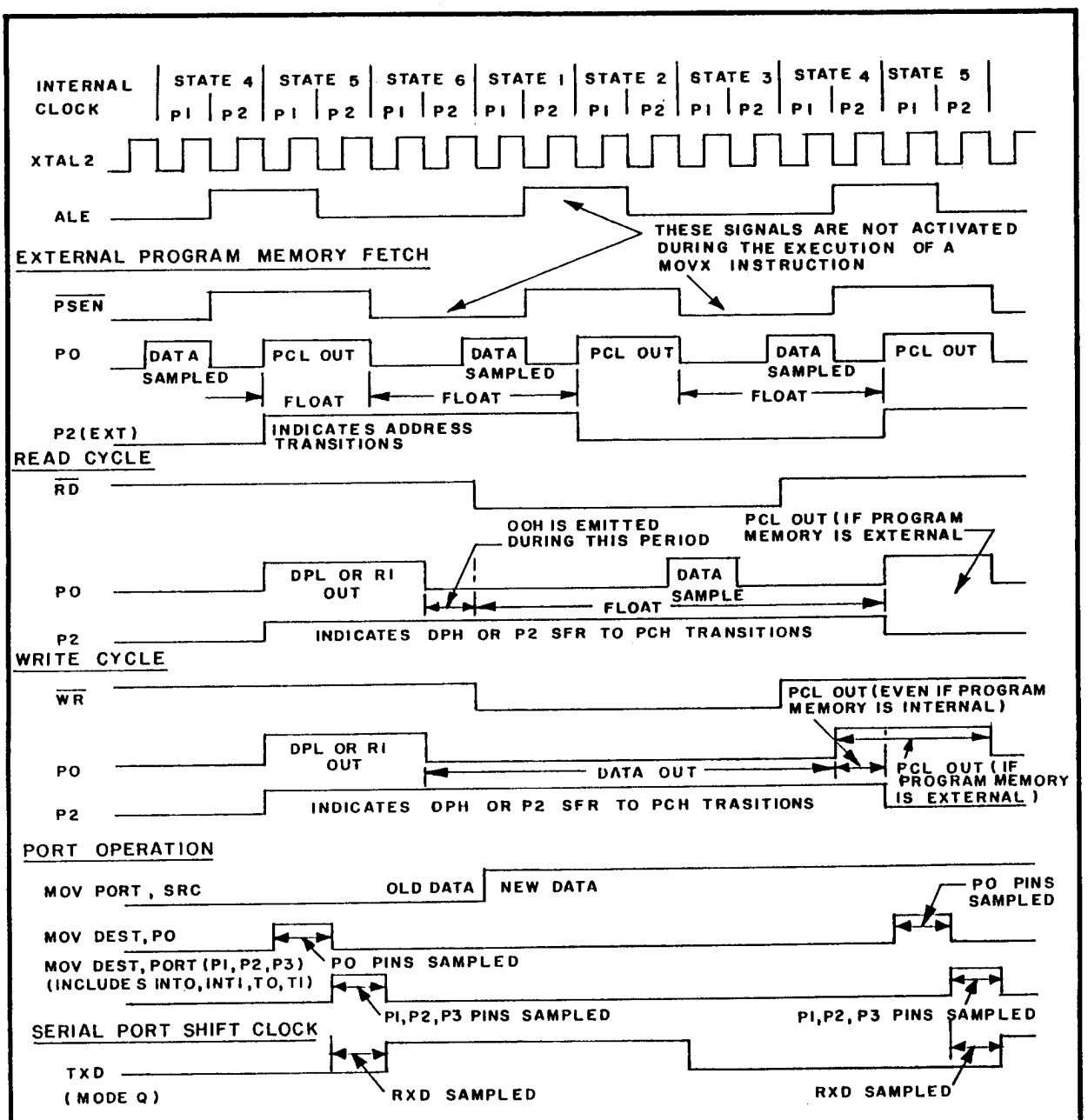

FIGURE 4. Clock waveforms.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84190
		REVISION LEVEL B	SHEET 14

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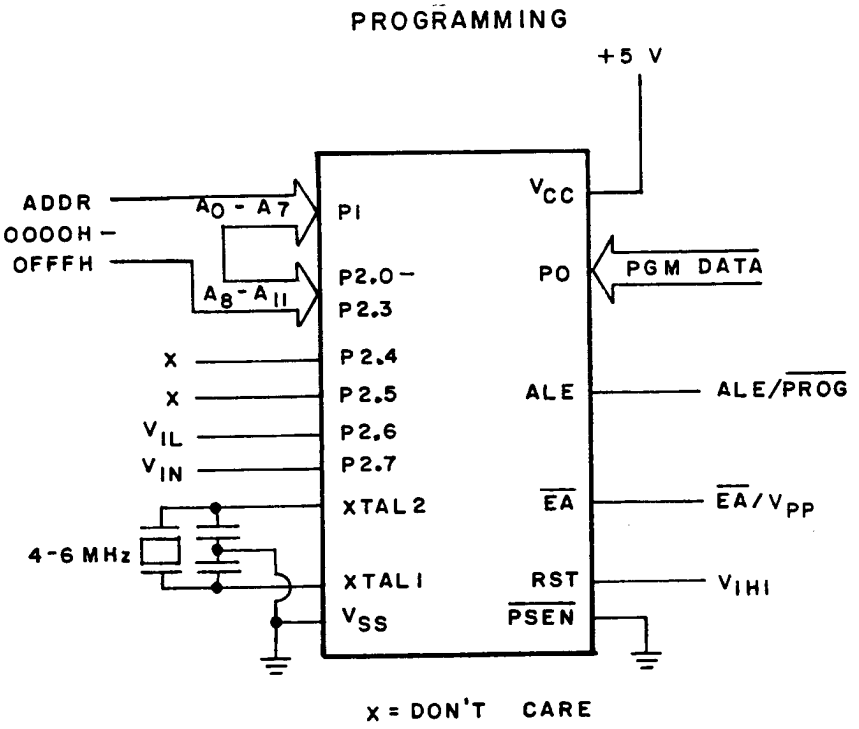

FIGURE 5. Programming logic.

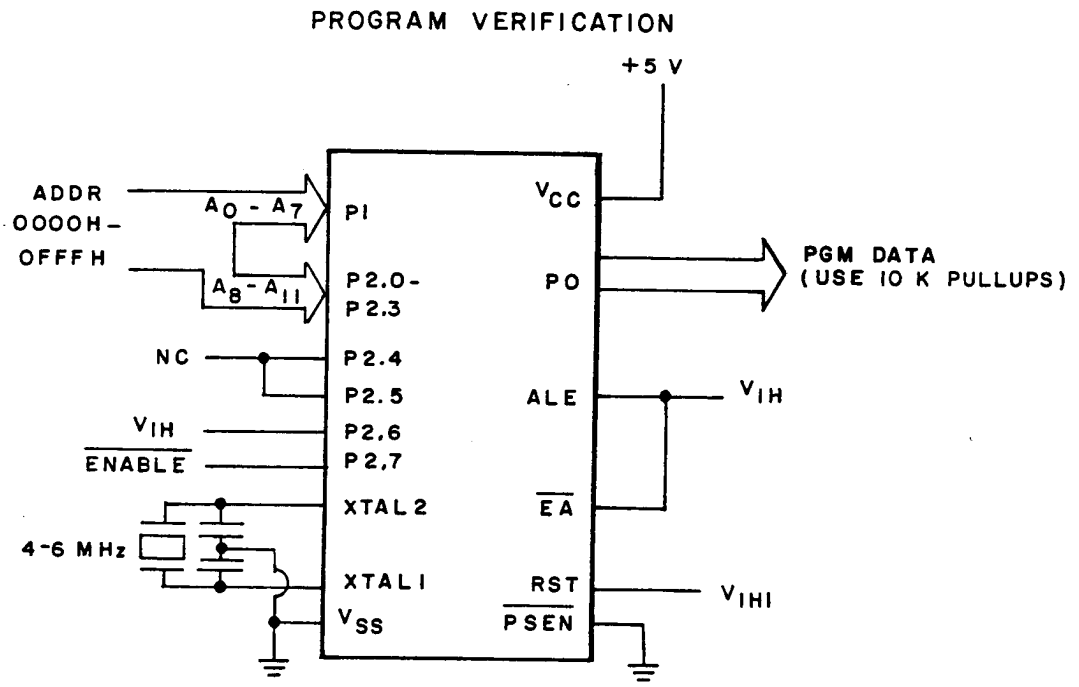

FIGURE 5. Programming logic - Continued.

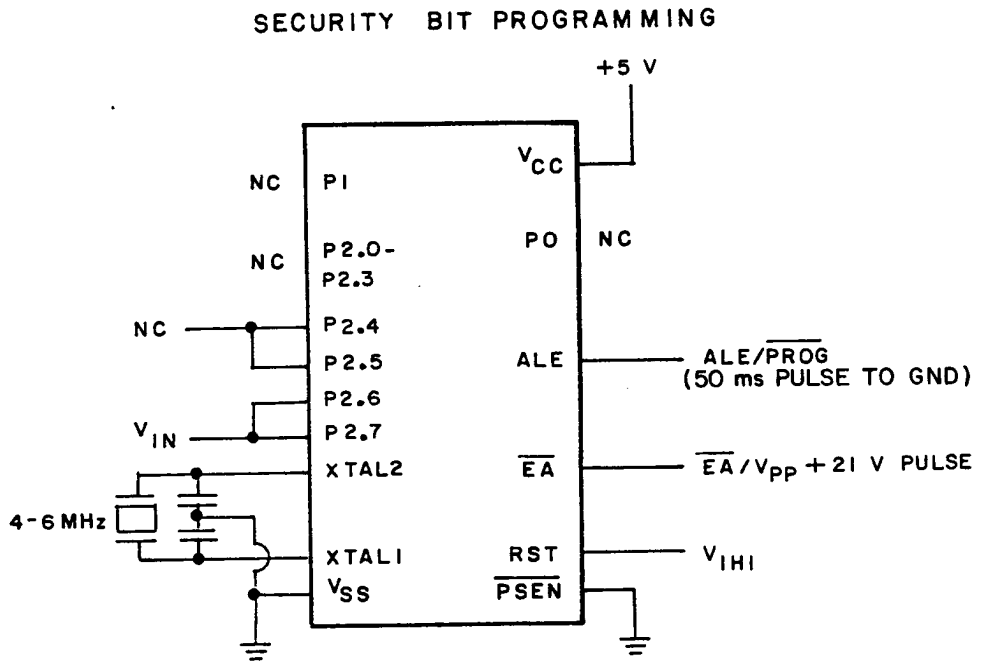

FIGURE 5. Programming logic - Continued.

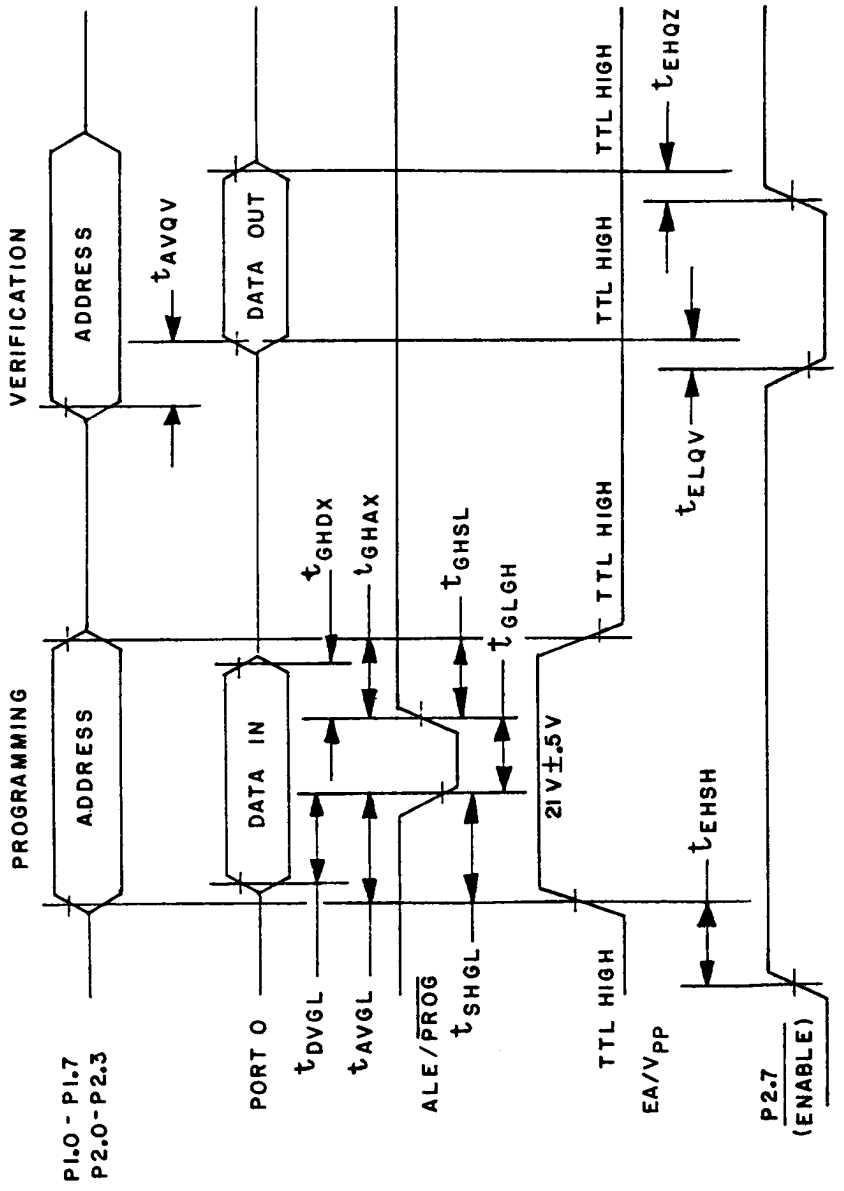

FIGURE 6. Programming waveforms.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional description for this device shall be as follows:

Port 0 — Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory. It also receives the instruction bytes during EPROM programming, and outputs instruction bytes during program verification. (External pullups are required during program verification.) Port 0 can sink (and in bus operations can source) eight LS TTL inputs.

Port 1 — Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during EPROM programming and program verification. Port 1 can sink/source four LS TTL inputs.

Port 2 — Port 2 is an 8-bit bidirectional I/O port with internal pullups. It emits the high-order address byte during accesses to external memory. It also receives the high-order address bits during EPROM programming and program verification. Port 2 can sink/source four LS TTL inputs.

Port 3 — Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features as listed below:

Port pin	Alternate function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt)
P3.3	$\overline{\text{INT1}}$ (external interrupt)
P3.4	T0 (timer/counter 0 external input)
P3.5	T1 (timer/counter 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Port 3 can sink/source four LS TTL inputs

RST — A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor (8.2 kΩ) from RST to V_{SS} permits power-on reset when a capacitor (10 μF) is also connected from this pin to V_{CC}.

ALE/$\overline{\text{PROG}}$ — Address latch enable output for latching the low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming.

$\overline{\text{PSEN}}$ — Program store enable output is the read strobe to external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external program memory. (However, even when executing out of external program memory two activations of $\overline{\text{PSEN}}$ are skipped during each access to external data memory). $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. $\overline{\text{PSEN}}$ can sink/source 8 LS TTL inputs.

$\overline{EA}$/Vpp — When $\overline{EA}$ is held high, the device executes out of internal program memory (unless the program counter exceeds OFFFH). When $\overline{EA}$ is held low, the device executes only out of external program memory. This pin also receives the 21 V programming supply voltage (Vpp) during EPROM programming. This pin should not be floated during normal operation.

XTAL1 — Input to the inverting amplifier that forms the oscillator, XTAL1 should be grounded when an external oscillator is used.

XTAL2 — Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator signal when an external oscillator is used.

6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Program method
8419001QX	34649	MD8751H-8/B	A
8419001QX	34335	8751H-8/BQA	A
8419001YX	34649	MR8751H-8/B	A
8419002QX	34335	8751H/BQA	A

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Williams Field Road Chandler, AZ 85224
34335	Advanced Micro Devices 901 Thompson Place P. O. Box 3453 Sunnyvale, CA 94088