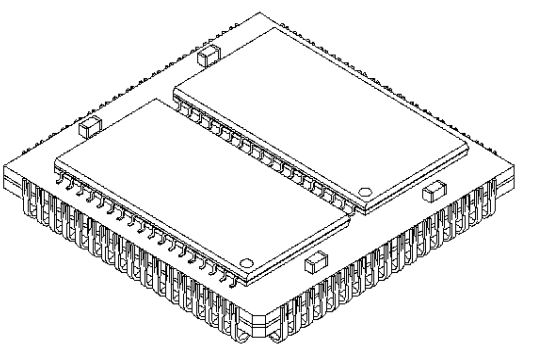
DENSE-PAC
MICROSYSTEMS

16 Megabit CMOS SRAM
DPS512X32MXP

PRELIMINARY

DESCRIPTION:

The DPS512X32MXP is a 68-pin surface mount module consisting of four 512K x 8 SRAM devices in plastic TSOP packages surface mounted on a FR-4 substrate. The module is available with "J"-Leads.

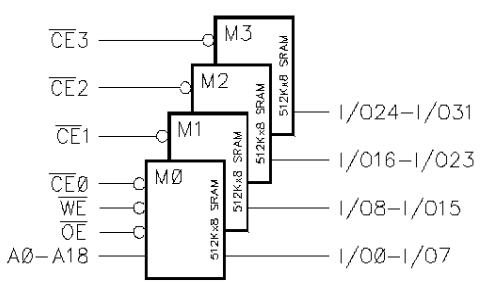


FEATURES:

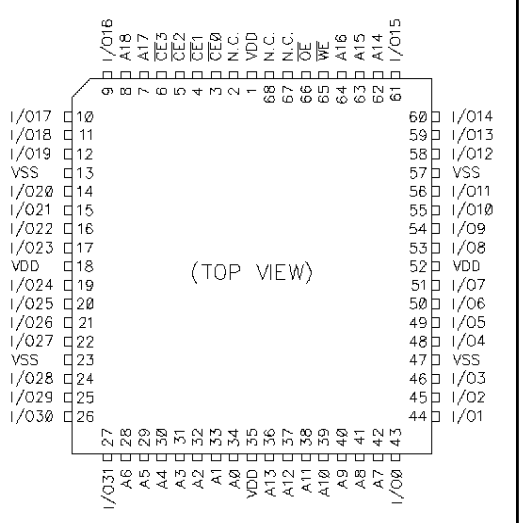
- Organizations Available:
  2M x 8, 1M x 16 or 512K x 32
- Access Times:
  15, 17, 20, 25ns
- Fully Static Operation - No clock or refresh required
- TTL-compatible Inputs and Outputs
- I/O Compatible with 3.3 Volt Devices
- 68-Pin Surface Mount Module

PIN NAMES	
A0 - A18	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CE0}$ - $\overline{CE3}$	Low Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



PRELIMINARY

RECOMMENDED OPERATING RANGE [4]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+0.5[3]	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		CI	-40	+25	+85	

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -4.0mA	2.4		V
V_{OL}	LOW Voltage	I_{OL}=8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS [4]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to +7.0	V

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	30pF	except t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5pF	t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

TRUTH TABLE					
Mode	$\overline{CE}$n	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	X	X	X	High-Z	Standby
Not Selected	H	X	X	High-Z	Standby
D_{OUT} Disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

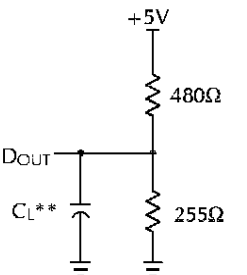
H = HIGH L = LOW X = Don't Care

* If $\overline{OE}$ is LOW during Write, t_{WHZ} must be observed before data is presented to the device.

CAPACITANCE [5]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	30	pF	V_{IN}[2] = 0V
C_{CE}	Chip Enable	8		
C_{WE}	Write Enable	30		
C_{OE}	Output Enable	30		
$C_{I/O}$	Data Input/Output	9		

Figure 1. Output Load

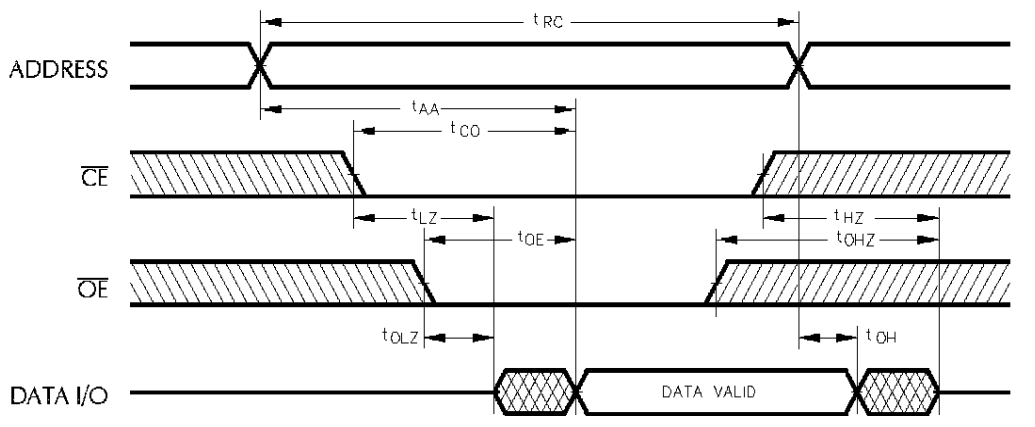
** Including Probe and Jig Capacitance.



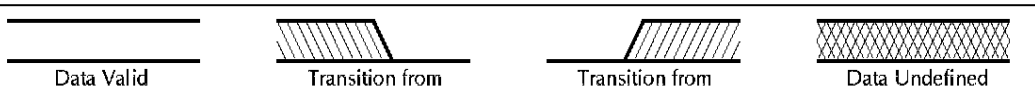
DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	x8		x16		x32		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}, V_{DD} = max.	-8	+8	-8	+8	-8	+8	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, V_{DD} = max., $\overline{CE}$ = V_{IH}	-8	+8	-4	+4	-2	+2	µA
I_{CC}	Dynamic Operating Current	$\overline{CE}$ = V_{IL}, V_{DD} = max. I_{OUT} = 0mA, f = f max.		320		480		800	mA
I_{SB1}	Full Standby Supply Current (CMOS)	f = 0, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, $\overline{CE} \geq V_{DD}$ -0.2V		40		40		40	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, f = f max.		160		160		160	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA	2.4		2.4		2.4		V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	15ns		17ns		20ns		25ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	15		17		20		25		ns
2	t_{AA}	Address Access Time		15		17		20		25	ns
3	t_{CO}	$\overline{CE}$ to Output Valid		15		17		20		25	ns
4	t_{OE}	Output Enable to Output Valid		7		9		9		10	ns
5	t_{LZ}	$\overline{CE}$ to Output in LOW-Z [5, 6]	3		3		3		3		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [5, 6]	0		0		0		0		ns
7	t_{HZ}	$\overline{CE}$ to Output in HIGH-Z [5, 6]		7		8		8		10	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z [5, 6]		7		8		8		10	ns
9	t_{OH}	Output Hold from Address Change	3		3		3		3		ns

READ CYCLE



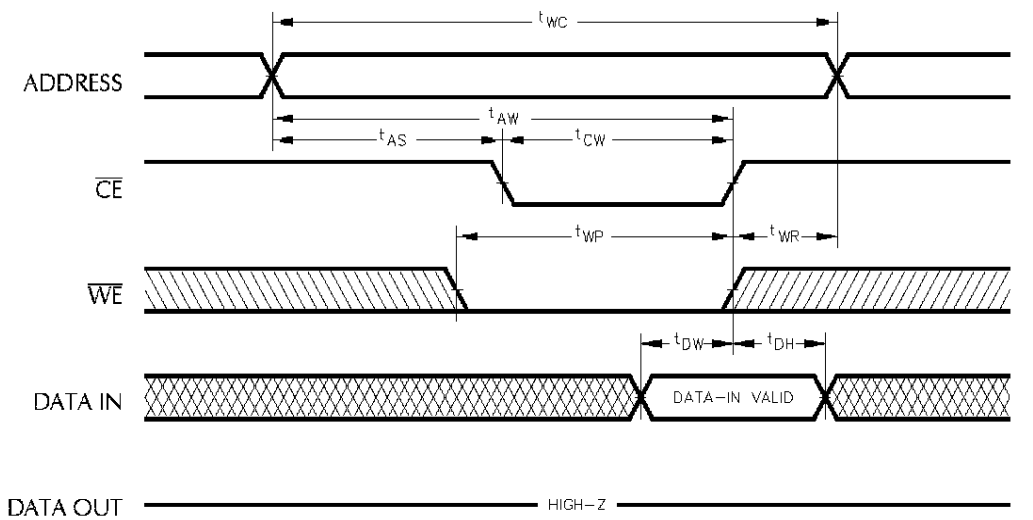
WAVEFORM KEY



AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [7, 8]: Over operating ranges											
No.	Symbol	Parameter	15ns		17ns		20ns		25ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	15		17		20		25		ns
11	t_{AW}	Address Valid to End of Write	10		11		15		20		ns
12	t_{CW}	Chip Enable to End of Write	10		11		15		20		ns
13	t_{AS}	Address Set-Up Time *	0		0		0		0		ns
14	t_{WP}	Write Pulse Width	10		11		12		15		ns
15	t_{WR}	Write Recovery Time, $\overline{CE}$, $\overline{WE}$	0		0		0		0		ns
16	t_{WHZ}	Write Enable to Output in HIGH-Z [5, 6]		7		8		10		12	ns
17	t_{DW}	Data to Write Time Overlap	7		8		10		12		ns
18	t_{DH}	Data Hold from Write Time	0		0		0		0		ns
19	t_{OW}	Output Active from End of Write	3		3		3		3		ns

* Valid for both Read and Write Cycles.

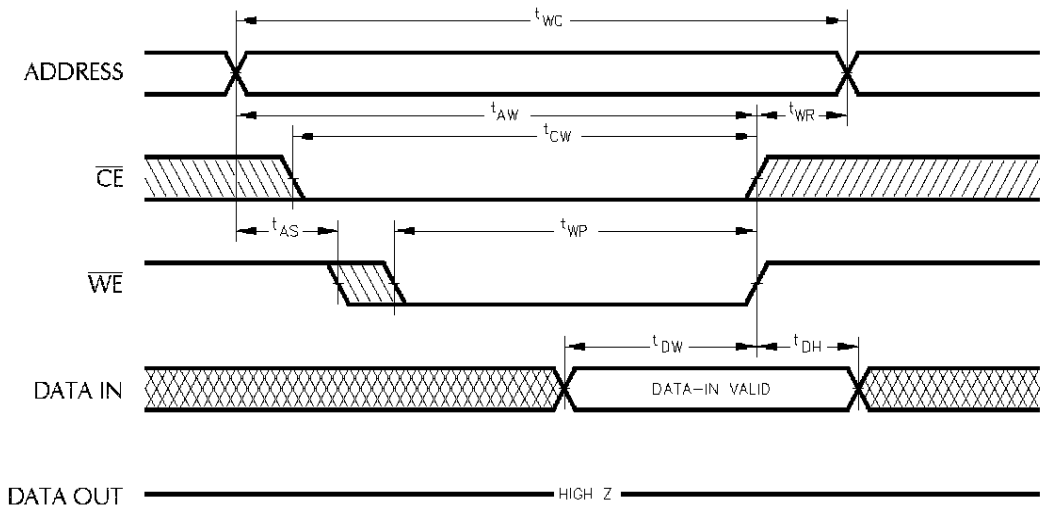
WRITE CYCLE 1: $\overline{CE}$ Controlled.



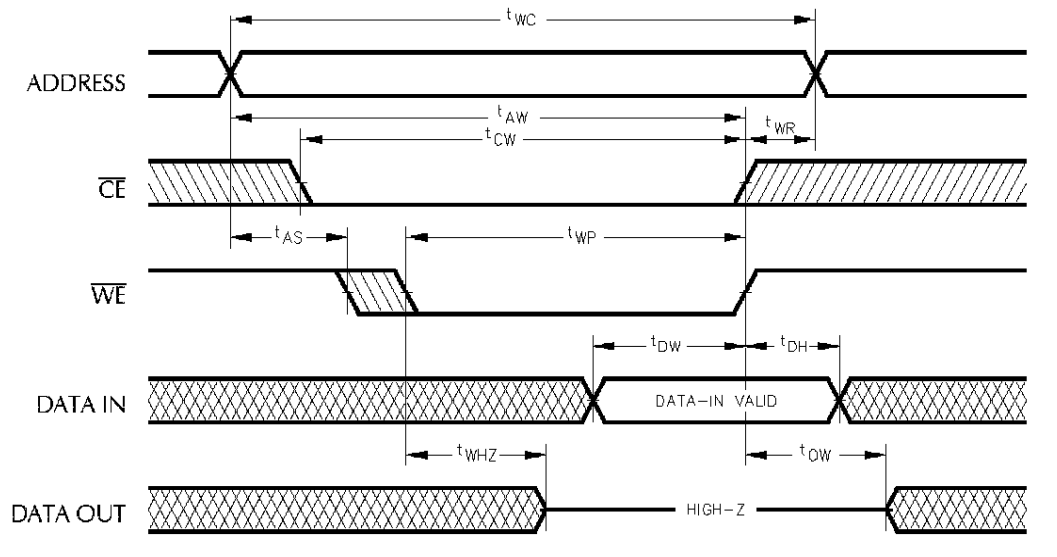
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. V_{IH} (max.)=V_{DD}+2.0Vdc (Pulse Width ≤ 8ns) for I ≤ 20mA.
4. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. This parameter is guaranteed and not 100% tested.
6. Transition is measured at the point of ±500mV from steady state voltage.
7. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
9. Chip Enable and Write Enable can initiate and terminate WRITE Cycle.

WRITE CYCLE 2: $\overline{WE}$ Controlled. $\overline{OE}$ is HIGH. [9]



WRITE CYCLE 3: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW. [9]

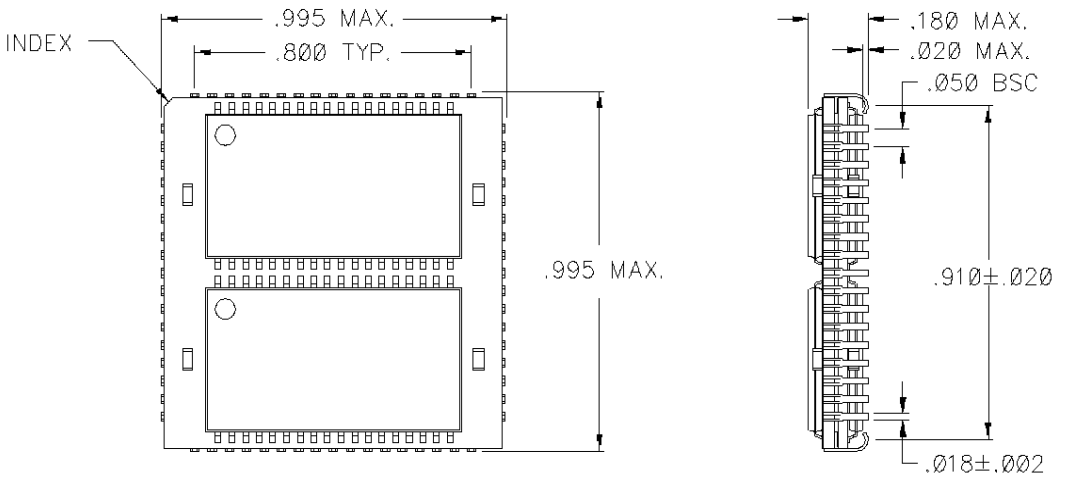


ORDERING INFORMATION

DP	S	512	X	32	M	XP	– nn	C
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE	SPEED	GRADE

- C COMMERCIAL 0°C to +70°C
- CI COMMERCIAL PROCESSED– INDUSTRIAL TEMPERATURE –40°C to +85°C
- 15 15ns
- 17 17ns
- 20 20ns
- 25 25ns
- 68–PIN J–LEADED PLASTIC SURFACE MOUNT MODULE
- 4 MEG BASED DEVICES
- MEMORY MODULE WITHOUT SUPPORT LOGIC
- CMOS SRAM

MECHANICAL DRAWING



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