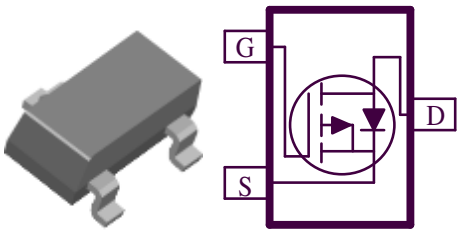
P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-20	0.130 @ V_{GS} = -4.5V	-2.6
	0.190 @ V_{GS} = -2.5V	-2.1

ESD Protected



Pb-free
RoHS COMPLIANT
HALOGEN FREE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current[a]	T_A=25°C	I_D	-2.6	A
	T_A=70°C		-1.5	
Pulsed Drain Current[b]		I_{DM}	-10	
Continuous Source Current (Diode Conduction)[a]		I_S	±1.6	A
Power Dissipation[a]	T_A=25°C	P_D	1.25	W
	T_A=70°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	t <= 5 sec	R_{THJA}	100	°C/W
	Steady-State		166	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

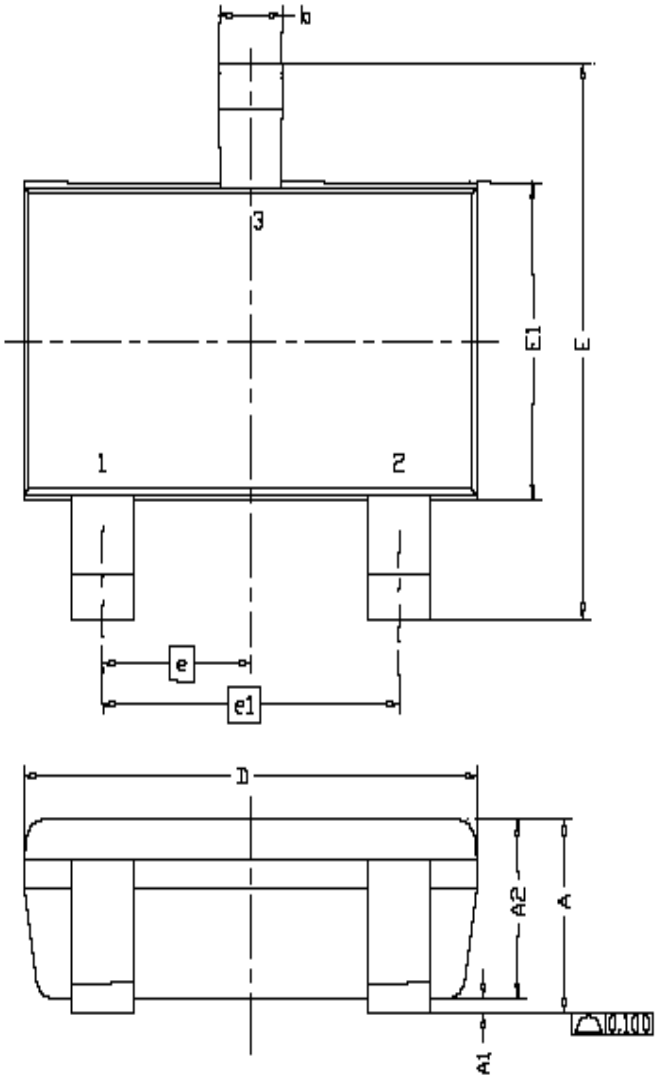
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 uA	-0.4		-1	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +/-8 V			±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
		V_{DS} = -16 V, V_{GS} = 0 V, T_J = 55°C			-10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -4.5 V	-3			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = -4.5 V, I_D = -1 A			0.130	Ω
		V_{GS} = -2.5 V, I_D = -1 A			0.190	
Forward Tranconductance[A]	g_{fs}	V_{DS} = -5 V, I_D = -1 A		3		S
Diode Forward Voltage	V_{SD}	I_S = -1 A, V_{GS} = 0 V		-0.70		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -5 V, V_{GS} = -4.5 V, I_D = -1 A		3		nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			0.9		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -5 V, R_L = 5 OHM, V_{GEN} = -4.5 V, R_G = 6 OHM		9		ns
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			30		
Fall-Time	t_f			10		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM