



## GENERAL DESCRIPTION



The ICS83948I-147 is a low skew, 1-to-12 Differential-to-LVCMOS/LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83948I-147 has two selectable clock inputs.

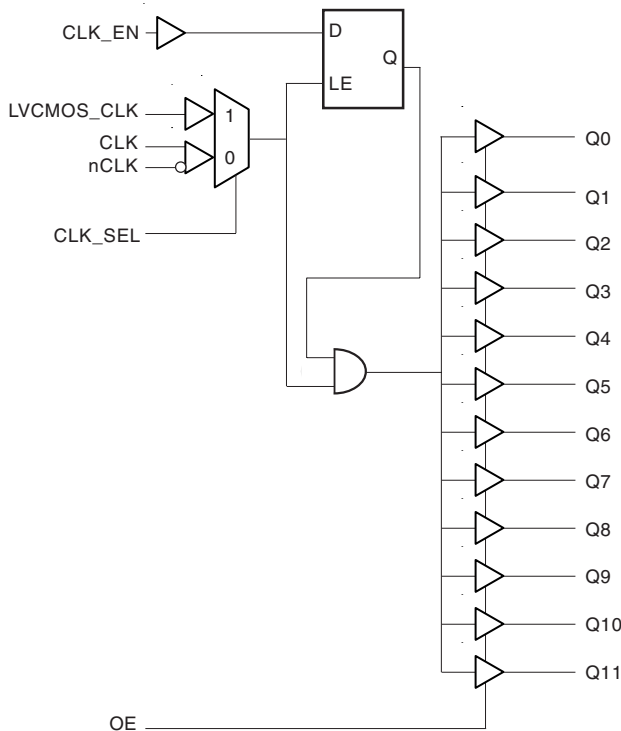
The CLK, nCLK pair can accept most standard differential input levels. The LVCMOS\_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83948I-147 is characterized at full 3.3V or full 2.5V operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83948I-147 ideal for those clock distribution applications demanding well defined performance and repeatability.

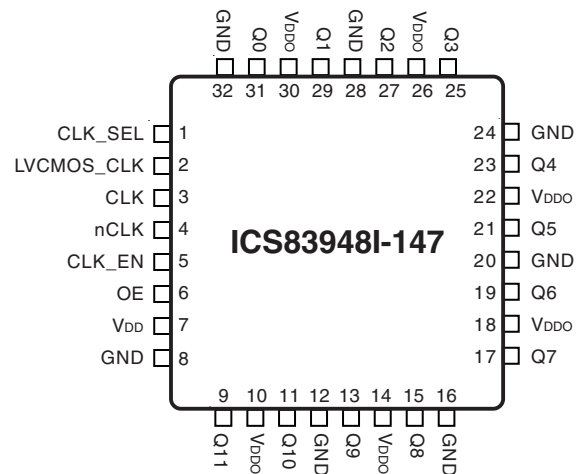
## FEATURES

- Twelve LVCMOS/LVTTL outputs
- Selectable LVCMOS/LVTTL clock or differential CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- LVCMOS\_CLK accepts the following input levels: LVCMOS or LVTTL
- Output frequency: 350MHz (maximum)
- Output skew (at 3.3V ± 5%): 100ps (maximum)
- Part-to-part skew (at 3.3V ± 5%): 1ns (maximum)
- Full 3.3V or full 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**32-Lead LQFP**  
7mm x 7mm x 1.4mm package body  
**Y Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	CLK_SEL	Input	Pullup	Clock select input. Selects LVCMOS_CLK input when HIGH. Selects CLK, nCLK inputs when LOW. LVCMOS/LVTTL interface levels
2	LVCMOS_CLK	Input	Pullup	Clock input. LVCMOS/LVTTL interface levels.
3	CLK	Input	Pullup	Non-inverting differential clock input.
4	nCLK	Input	Pulldown	Inverting differential clock input.
5	CLK_EN	Input	Pullup	Clock enable. LVCMOS/ LVTTL interface levels.
6	OE	Input	Pullup	Output enable. LVCMOS/LVTTL interface levels.
7	V <sub>DD</sub>	Power		Power supply pin.
8, 12, 16, 20, 24, 28, 32	GND	Power		Power supply ground.
9, 11, 13, 15, 17, 19, 21, 23 25, 27, 29, 31	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. LVCMOS/LVTTL interface levels.
10, 14, 18, 22, 26, 30	V <sub>DDO</sub>	Power		Output supply pins.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance (per output)			12		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance		5	7	12	Ω

**TABLE 3A. CLOCK SELECT FUNCTION TABLE**

Control Input	Clock
0	CLK, nCLK inputs selected
1	LVCMOS_CLK input selected

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	CLK	nCLK	Q0:Q11		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".



#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_i$	-0.5V to $V_{DD} + 0.5$ V
Outputs, $V_o$	-0.5V to $V_{DDO} + 0.5$ V
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				55	mA

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				52	mA

**TABLE 4C. DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	LVCMOS	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	LVCMOS	-0.3		0.8	V
$I_{IN}$	Input Current	$V_{IN} = V_{DD}$ or $V_{IN} = GND$			300	$\mu$ A
$V_{OH}$	Output High Voltage; NOTE 1	$I_{OH} = -24$ mA	2.4			V
$V_{OL}$	Output Low Voltage; NOTE 1	$I_{OL} = 24$ mA			0.55	V
		$I_{OL} = 12$ mA			0.30	V
$V_{PP}$	Peak-to-Peak Input Voltage	CLK, nCLK	0.15		1.3	V
$V_{CMR}$	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK	GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Outputs capable of driving 50 $\Omega$  transmission lines terminated with 50 $\Omega$  to  $V_{DDO}/2$ .

See Parameter Measurement section, "3.3V Output Load AC Test Circuit".

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{DD} + 0.3$ V.

NOTE 3: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 4D. DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	LVCMOS	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	LVCMOS	-0.3		0.7	V
$I_{IN}$	Input Current	$V_{IN} = V_{DD}$ or $V_{IN} = GND$			300	$\mu A$
$V_{OH}$	Output High Voltage; NOTE 1	$I_{OH} = -15mA$	1.8			V
$V_{OL}$	Output Low Voltage; NOTE 1	$I_{OL} = 15mA$			0.6	V
$V_{PP}$	Peak-to-Peak Input Voltage	CLK, nCLK	0.15		1.3	V
$V_{CMR}$	Input Common Mode Voltage; NOTE 2, 3	CLK, nCLK	GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Outputs capable of driving 50 $\Omega$  transmission lines terminated with 50 $\Omega$  to  $V_{DDO}/2$ .

See Parameter Measurement section, "2.5V Output Load AC Test Circuit".

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{DD} + 0.3V$ .

NOTE 3: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				350	MHz
$t_{PD}$	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq 350MHz$	2	4	ns
		LVCMOS_CLK; NOTE 2	$f \leq 350MHz$	2	4	ns
$t_{sk(o)}$	Output Skew; NOTE 3, 7	Measured on rising edge @ $V_{DDO}/2$			100	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 7	Measured on rising edge @ $V_{DDO}/2$			1	ns
$t_R / t_F$	Output Rise/Fall Time	0.8V to 2V	0.2		1.0	ns
odc	Output Duty Cycle	$f \leq 150MHz$ , Ref = CLK, nCLK	45	50	55	%
$t_{PZL}, t_{PZH}$	Output Enable Time; NOTE 5				5	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time; NOTE 5				5	ns
$t_S$	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK	1			ns
		CLK_EN to LVCMOS_CLK	0			ns
$t_H$	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN	0			ns
		LVCMOS_CLK to CLK_EN	1			ns

NOTE 1: Measured from the differential input crossing point to  $V_{DDO}/2$  of the output.

NOTE 2: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.



**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ$  TO  $85^\circ$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				350	MHz
$t_{PD}$	Propagation Delay;	CLK, nCLK; NOTE 1	$f \leq 350\text{MHz}$	1.5	4.2	ns
		LVCMOS_CLK; NOTE 2	$f \leq 350\text{MHz}$	1.7	4.4	ns
$t_{sk(o)}$	Output Skew; NOTE 3, 7	Measured on rising edge @ $V_{DDO}/2$			160	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 7	Measured on rising edge @ $V_{DDO}/2$			2	ns
$t_R / t_F$	Output Rise/Fall Time	0.6V to 1.8V	0.1		1.0	ns
odc	Output Duty Cycle	$f \leq 150\text{MHz}$ , Ref = CLK, nCLK	40		60	%
$t_{PZL}, t_{PZH}$	Output Enable Time; NOTE 5				5	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time; NOTE 5				5	ns
$t_S$	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK, nCLK	1			ns
		CLK_EN to LVCMOS_CLK	0			ns
$t_H$	Clock Enable Hold Time; NOTE 6	CLK, nCLK to CLK_EN	0			ns
		LVCMOS_CLK to CLK_EN	1			ns

NOTE 1: Measured from the differential input crossing point to  $V_{DDO}/2$  of the output.

NOTE 2: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

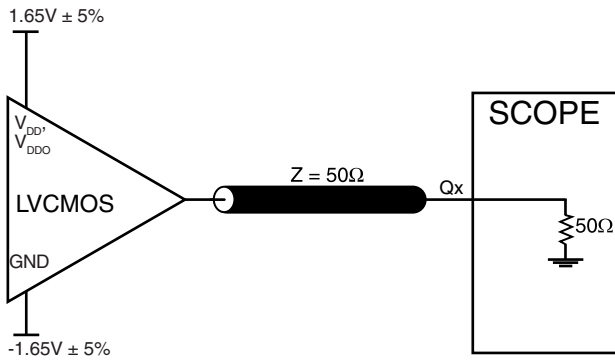
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.

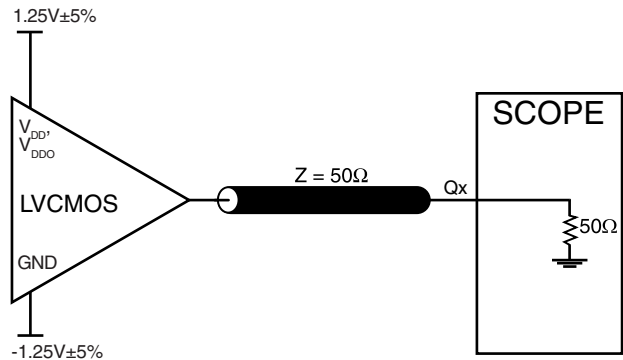
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.



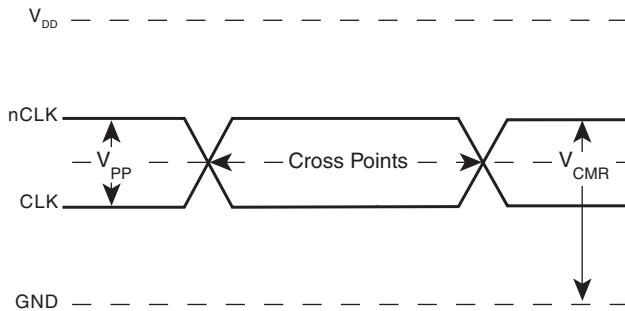
**PARAMETER MEASUREMENT INFORMATION**



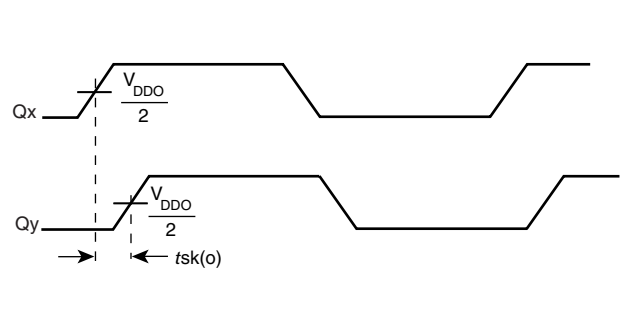
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



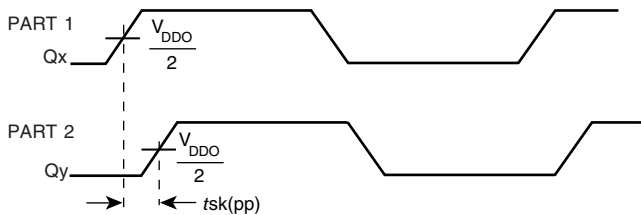
**2.5V OUTPUT LOAD AC TEST CIRCUIT**



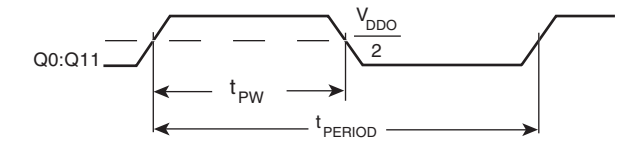
**DIFFERENTIAL INPUT LEVEL**



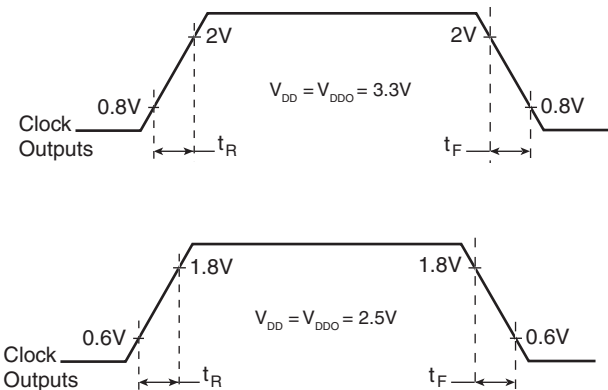
**OUTPUT SKEW**



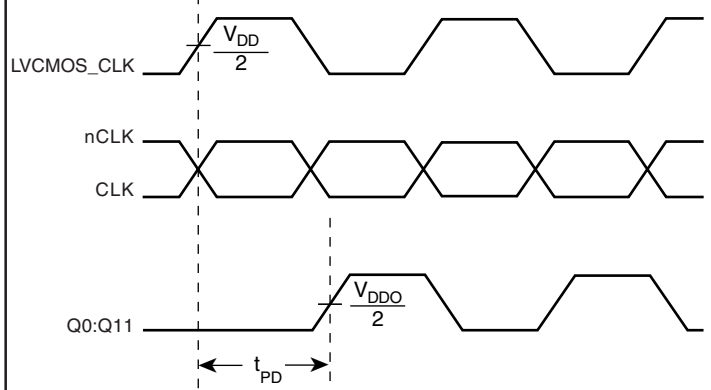
**PART-TO-PART SKEW**



**odc &  $t_{PERIOD}$**



**OUTPUT RISE/FALL TIME**



**PROPAGATION DELAY**



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

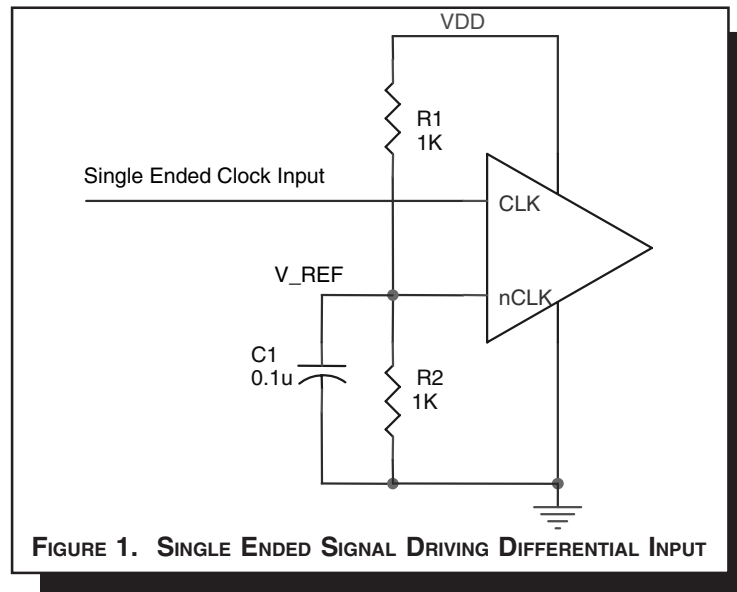


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

##### CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

##### LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### OUTPUTS:

##### LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.



**RELIABILITY INFORMATION**

**TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 32 LEAD LQFP**

<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TRANSISTOR COUNT**

The transistor count for ICS83948I-147 is: 1040

Pin compatible with the MPC9448





PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

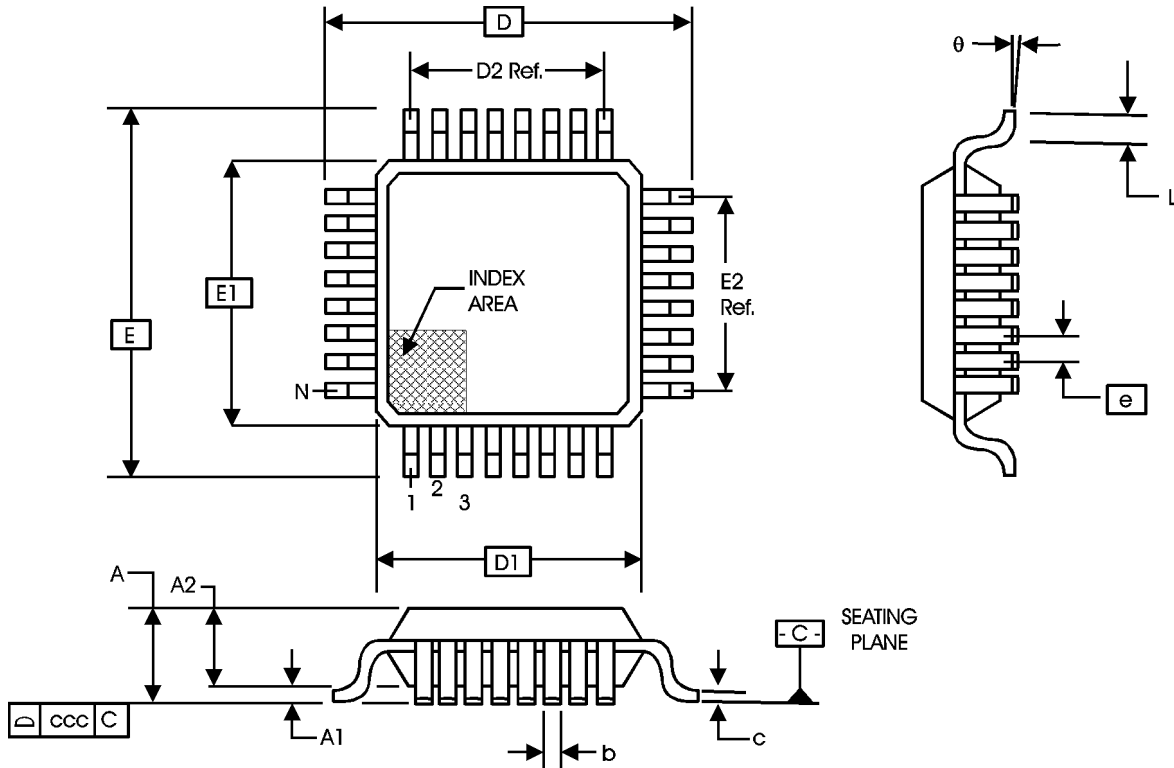


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
theta	0°	--	7°
ccc	--	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MS-026



Integrated  
Circuit  
Systems, Inc.

**ICS83948I-147**

LOW SKEW, 1-TO-12

DIFFERENTIAL-TO-LVCMOS/LVTTL FANOUT BUFFER

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83948AYI-147	ICS83948AI147	32 Lead LQFP	tray	-40°C to 85°C
ICS83948AYI-147T	ICS83948AI147	32 Lead LQFP	1000 tape & reel	-40°C to 85°C
ICS83948AYI-147LF	ICS948AI147L	32 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS83948AYI-147LFT	ICS948AI147L	32 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Integrated  
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**ICS83948I-147**

LOW SKEW, 1-TO-12

DIFFERENTIAL-TO-LVCMOS/LVTTL FANOUT BUFFER

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T2	1	Features Sectiton - added Lead-Free bullet.	11/21/05
		2	Pin Characteristics Table - changed $C_{IN}$ from 4pF max. to 4pF typical; and added 5Ω min. and 12Ω max to $R_{OUT}$ .	
	7	Updated Single Ended Signal Driving Differential Input diagram		
	10	Added <i>Recommendations for Unused Input and Output Pins.</i> Ordering Information Table - added lead-free part number, marking, and note.		