Marvell® PXA3xx (88AP3xx) Processor Family

Electrical, Mechanical, and Thermal Functional Specification

PXA30x Processor (88AP300, 88AP301, 88AP302, 88AP303)
PXA31x Processor (88AP310, 88AP311, 88AP312)
PXA32x Processor (88AP320, 88AP322)

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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

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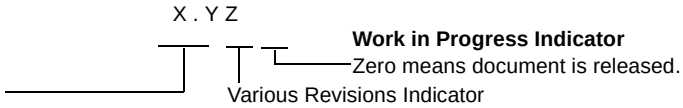

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1 Introduction

The Marvell PXA3xx Processor Family is a system-on-chip based on XScale® microarchitecture[1] that incorporates the latest Marvell advances in mobile technology over its predecessor, the Marvell PXA27x Processor Family. The PXA32x processor, PXA31x processor, and PXA30x processor provide high-performance multimedia, low-power capabilities, and rich peripheral integration. The PXA3xx Processor Family (referred throughout this document as “the processor” for simplicity) provide enhanced features compared to the PXA27x Processor Family, and are the first Marvell applications processors to integrate a hardware video accelerator unit. The PXA3xx Processor Family redefines scalability by operating up to 806 MHz, providing high performance at low power for many demanding mobile applications and markets such as multimedia-enabled cellular phones, personal digital assistants (PDA), and embedded devices.

The PXA3xx Processor Family includes Intel® Wireless MMX™ 2 technology, enabling high-performance, low-power multimedia acceleration with a general-purpose instruction set. Marvell® Quick Capture Interface technology provides a flexible and powerful camera interface for capturing digital still and video images. While performance is a key feature in the PXA3xx Processor Family, power consumption is also a critical component. Marvell® Scalable Power Manager technology helps enable low-power consumption with sophisticated power management capabilities.

1.1 Product Summary

The following table describes the basic features of the processor:

High-performance processor:
- XScale® microarchitecture with Intel® Wireless MMX™ 2 media enhancement technology
- 7-8 stage pipeline
- 32 Kbytes instruction cache
- 32 Kbytes data cache
- 2 Kbytes “mini” data cache
- Extensive data buffering

Up to 768 Kbytes of internal SRAM for high speed code or data storage preserved during low-power states

Rich serial peripheral set:
- AC ’97 audio port
- USB v. 2.0 client controller
- USB v. 1.1 client controller
- Up to 3 USB v. 1.1 host controller
- USB on-the-go controller
- Three high-speed UARTs with hardware flow control
- SIR and Consumer IR infrared communications ports

Hardware debug features — IEEE JTAG interface with boundary scan

Hardware performance-monitoring features with on-chip trace buffer

Real-time clock

Operating-system timers

LCD controller

Quick Capture Interface Controller

Low power:
- Dynamic voltage management support
- Less than 500 mW typical internal power dissipation
- Core supply voltage may be reduced to 0.95 V
- Five low-power modes

High-performance memory controller:
- Mobile DDR SDRAM interface
- EMPI and Data Flash interface
- Up to four static chip selects
- Companion-chip interface

Mini-LCD controller

Two Universal Subscriber Identity Module (USIM) interface

Flexible clocking:
- CPU clock from 104 to 806 MHz
- Flexible memory clock ratios
- Frequency change capability
- Functional clock gating

Additional peripherals for system connectivity:
- SD/SDIO/MMC Controller (with SPI mode support)
- Four SSP controllers
- Two I^2C controllers (one targeted for PMIC control)
- Four pulse-width modulators (PWMs)
- Keypad interface with both direct and matrix keys, rotary encoder support
- Most peripheral pins double as GPIOs

1. XScale is a trademark or registered trademark of Intel Corporation and its subsidiaries in the United States and other countries.

1.2 Document Purpose

This document constitutes the electrical, mechanical, and thermal specifications for the PXA3xx Processor Family. It contains a functional overview, mechanical data, package signal locations, targeted electrical specifications, and functional bus waveforms. For detailed functional descriptions other than parametric performance, refer to the *PXA3xx Processor Family Developers Manual (four volumes)*.

Note This document may contain shortened references to the “PXA32x/PXA31x/PXA30x processor” or “the processor” in some chapters. Where differences exist among or between PXA3xx processors, they are called out individually.

Note The PXA3xx Processor Family consists of the following product SKUs:

PXA30x: 88AP300, 88AP301, 88AP302, 88AP303
PXA31x: 88AP311, 88AP312
PXA32x: 88AP320, 88AP322

These product SKUs are not referenced in this version of the EMTS.

1.3 Number Representation

All numbers in this document are decimal (base 10) unless designated otherwise. Hexadecimal numbers have a prefix of 0x, and binary numbers have a prefix of 0b. For example, 107 is represented as 0x6B in hexadecimal and 0b110_1011 in binary.

1.4 Naming Conventions

All signal and register-bit names appear in uppercase. Active low items are prefixed with a lowercase “n”.

Pins within a signal name are enclosed in angle brackets:

```
EXTERNAL_ADDRESS<31:0>
nCS<1>
```

Bits within a register bit field are enclosed in square brackets:

```
REGISTER_BITFIELD[3:0]
REGISTER_BIT[0]
```

Single-bit items have either of two states:

- **Clear** — the item contains the value 0b0.
- **Set** — the item contains the value 0b1.

1.5 Applicable Documents

Table 1 lists supplemental information sources for the PXA30x and PXA31x processor. Contact a Marvell representative for the latest document revisions and ordering instructions.

Table 1: Supplemental Documentation

Document Title
PXA3xx Processor Family Vol. I: System and Timer Configuration Developers Manual
PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual
PXA3xx Processor Family Vol. III: Graphics and Input Controller Configuration Developers Manual
PXA3xx Processor Family Vol. IV: Serial Controller Configuration Developers Manual
Intel® Wireless MMX™ 2 Technology Developer's Guide
Using the Intel® Wireless MMX™ 2 Coprocessor with Marvell® PXA3xx Processors Programmers Reference Manual
PXA3xx Processor Family Design Guide
ARM Architecture Version* V5TE *Specification* (Document number ARM* DDI 0100D-10), and *ARM* Architecture Reference Manual* (Document number ARM* DDI 0100B)

2 Functional Overview

The PXA3xx processors are integrated system-on-a-chip microprocessors for high-performance, low-power portable handheld and handset devices. They incorporate the XScale® microarchitecture with on-the-fly voltage and frequency scaling and sophisticated power management to provide industry leading MIPS/mW performance across its wide range of operating frequencies. The processors comply with the ARM* Architecture V5TE instruction set (excluding floating point instructions) and follow the ARM* programmers model. The multimedia coprocessor provides enhanced Intel® Wireless MMX™ 2 instructions to accelerate audio and video processing. The processors are available in a discrete package configuration. They provide a high degree of backward compatibility with the Marvell PXA27x Processor Family, but they offer significant performance and feature set enhancements.

The processor memory architecture offers greater flexibility and higher performance than previous core products. This architecture supports two dedicated memory interfaces for high-speed DDR SDRAM, VLIO devices, and NAND flash devices. This flexibility enables high-performance “store-and-download” as well as “execute-in-place” system architectures. The processor memory architecture features a memory switch that allows multiple simultaneous memory transactions among different sources and targets. For example, the processor architecture allows memory traffic between the core and DDR SDRAM to move in parallel with DMA-generated traffic between the LCD controller and internal SRAM. In an architecture with a single shared system bus, these transactions block each other. The PXA32x processor also provides a 256-Kbyte, unified L2 cache to maintain high memory system performance, lower power with a full feature OS, and several complex multimedia applications running simultaneously.

The processor incorporates an internal boot ROM and a Marvell® Wireless Trusted Transaction Technology module to provide flexible boot-loading options while maintaining platform security. They have up to six 128 Kbyte banks of internal SRAM for a combination of display frame buffer, program code, or multimedia data. Each bank can be configured to retain its contents when the processor enters a low-power mode.

The processor provides OS timer channels and synchronous serial ports (SSPs) that accept an external network clock input so that they can be synchronized to the cellular network.

An integrated LCD panel controller supports active and passive displays. It permits color depths of up to 18-bits per pixels (24-bits per pixel for smart panels). The LCD controller also supports hardware cursor and two display overlays.

The processor incorporates a comprehensive set of system and peripheral functions that make it useful in a variety of low-power applications. Figure 1 illustrates the system-on-a-chip PXA30x processor, Figure 2 illustrates PXA31x processor and Figure 3 illustrates the PXA32x processor. The diagram shows a multi-port memory switch and system bus architecture with the core attached, along with an LCD controller and USB 1.1 controllers, and internal memory. The key features of all of the sub-blocks are described in the PXA3xx Processor Family Developers Manual (four volumes).

Figure 1: PXA32x Processor Block Diagram

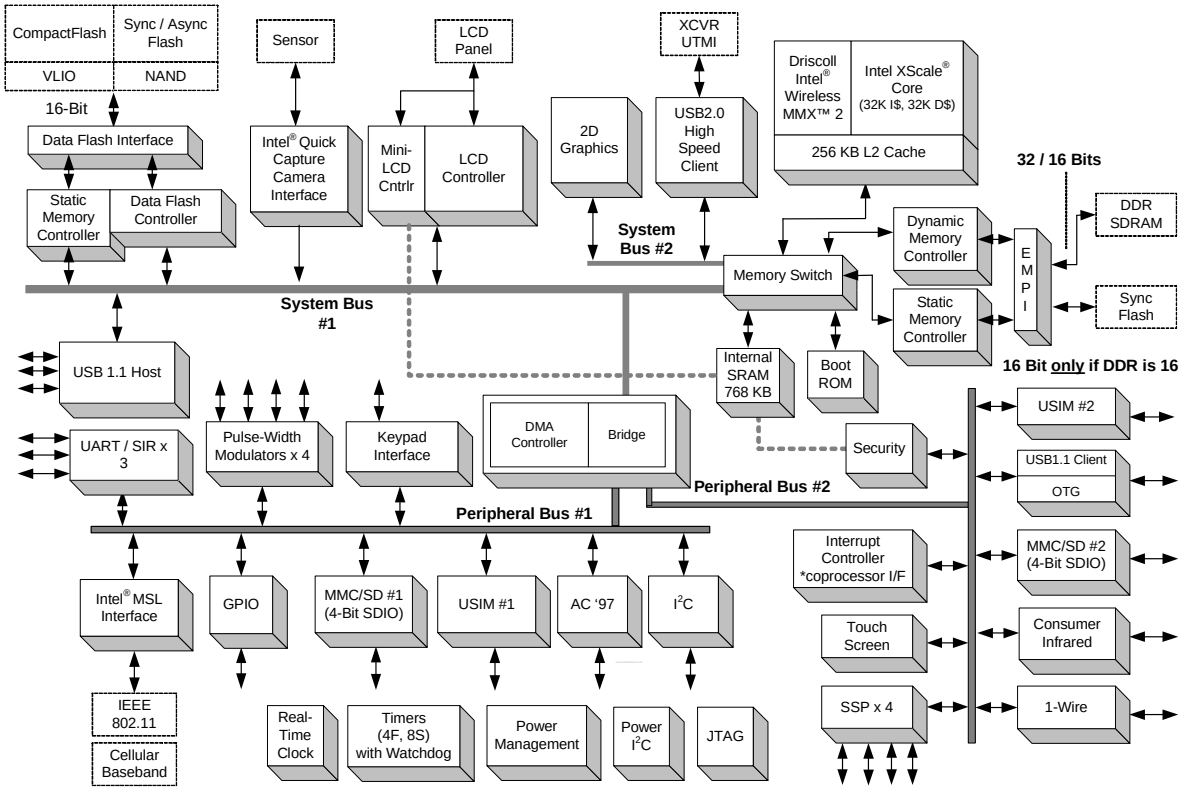


Figure 2: PXA31x Processor Block Diagram

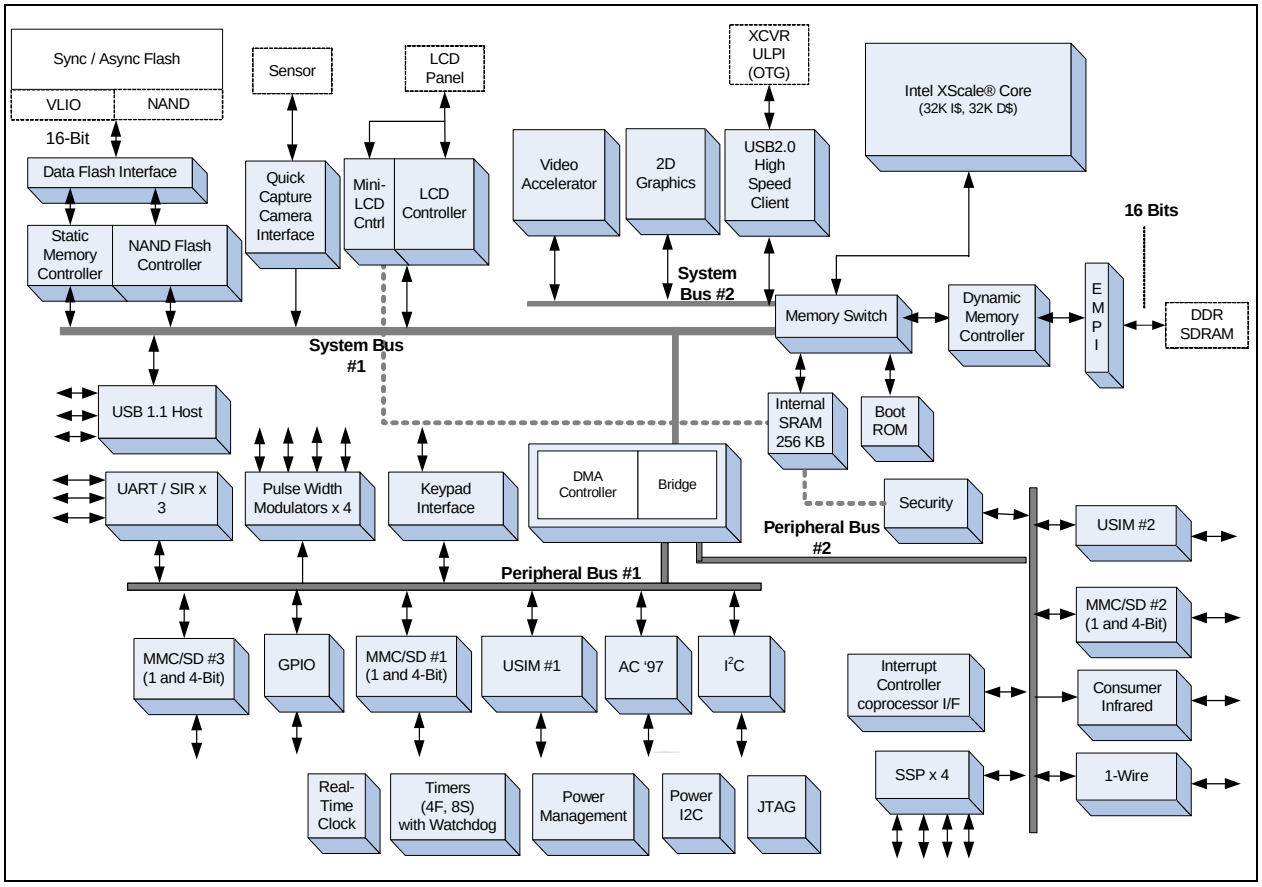
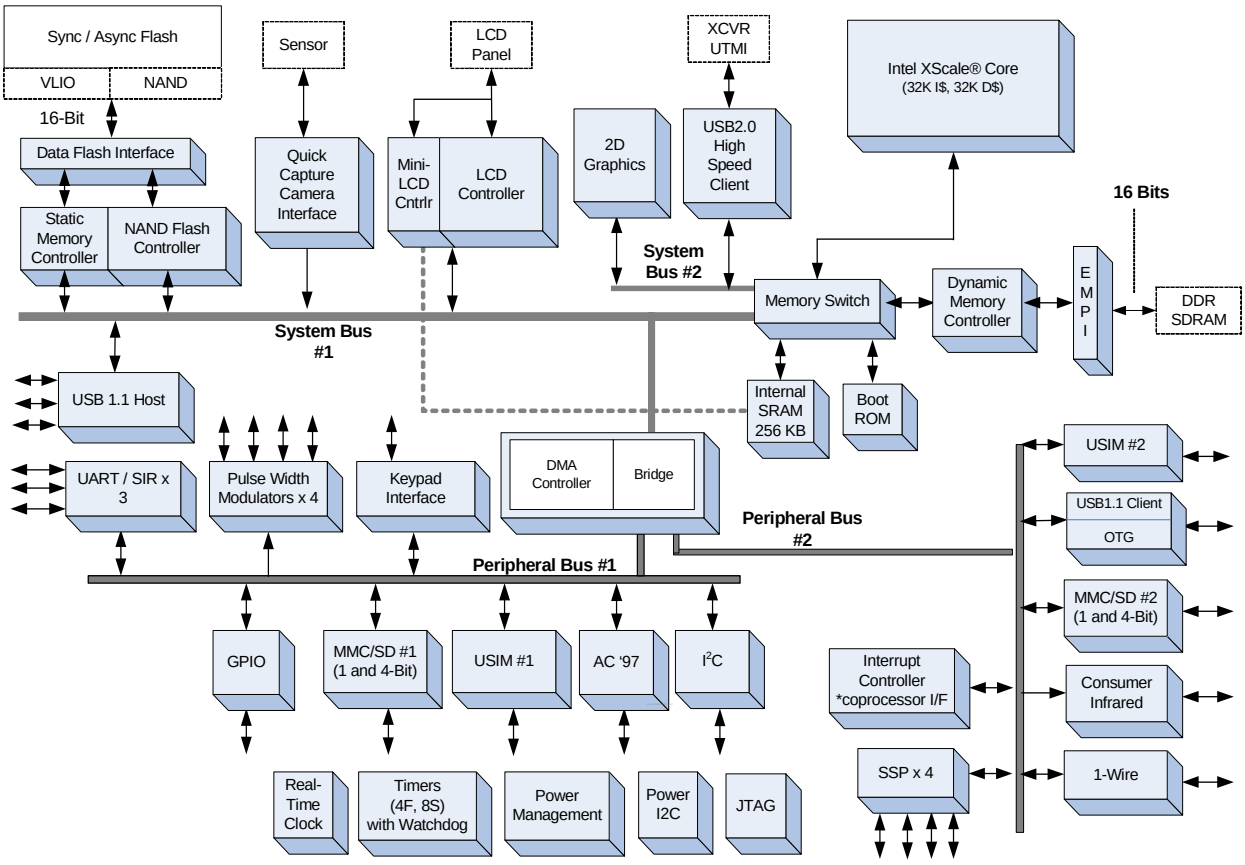


Figure 3: PXA30x Processor Block Diagram



3 Package Information

3.1 Introduction

This chapter provides the mechanical specifications for the PXA3xx Processor Family.

3.2 Packaging Materials

Table 2 shows the mold compound and solder ball material list.

Table 2: Package Materials

Component Material	Solder Balls
Mold compound Sumitomo EME-7730L	98.5 Sn/1.0 Ag/0.5 Cu
NOTE: Pb-free parts, lead has not been added intentionally, but lead may persist as an impurity below 1000 ppm	

3.3 PXA32x Processor Packaging Views

3.3.1 PXA32x Processor 456-Ball VF-BGA Package

The PXA32x Processor package is a 14x14 mm, 456-pin, 0.5-mm VF-BGA, as shown in Figure 5, Figure 6 shows the daisy chain version of the package.

Figure 4: PXA320 Processor 14x14 mm VF-BGA Package, Top View

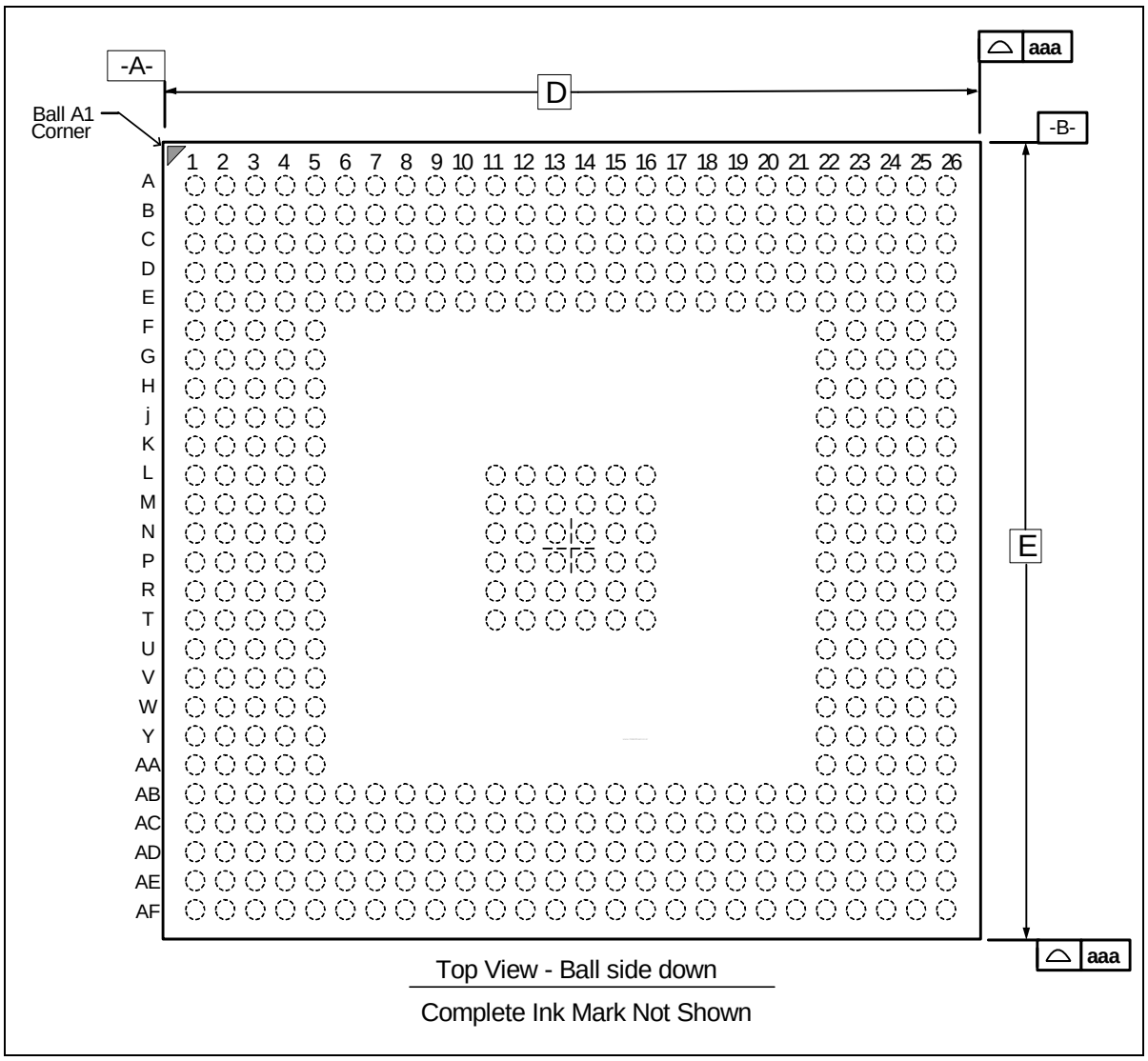


Figure 5: PXA320 Processor 14x14 mm VF-BGA Package, Bottom View

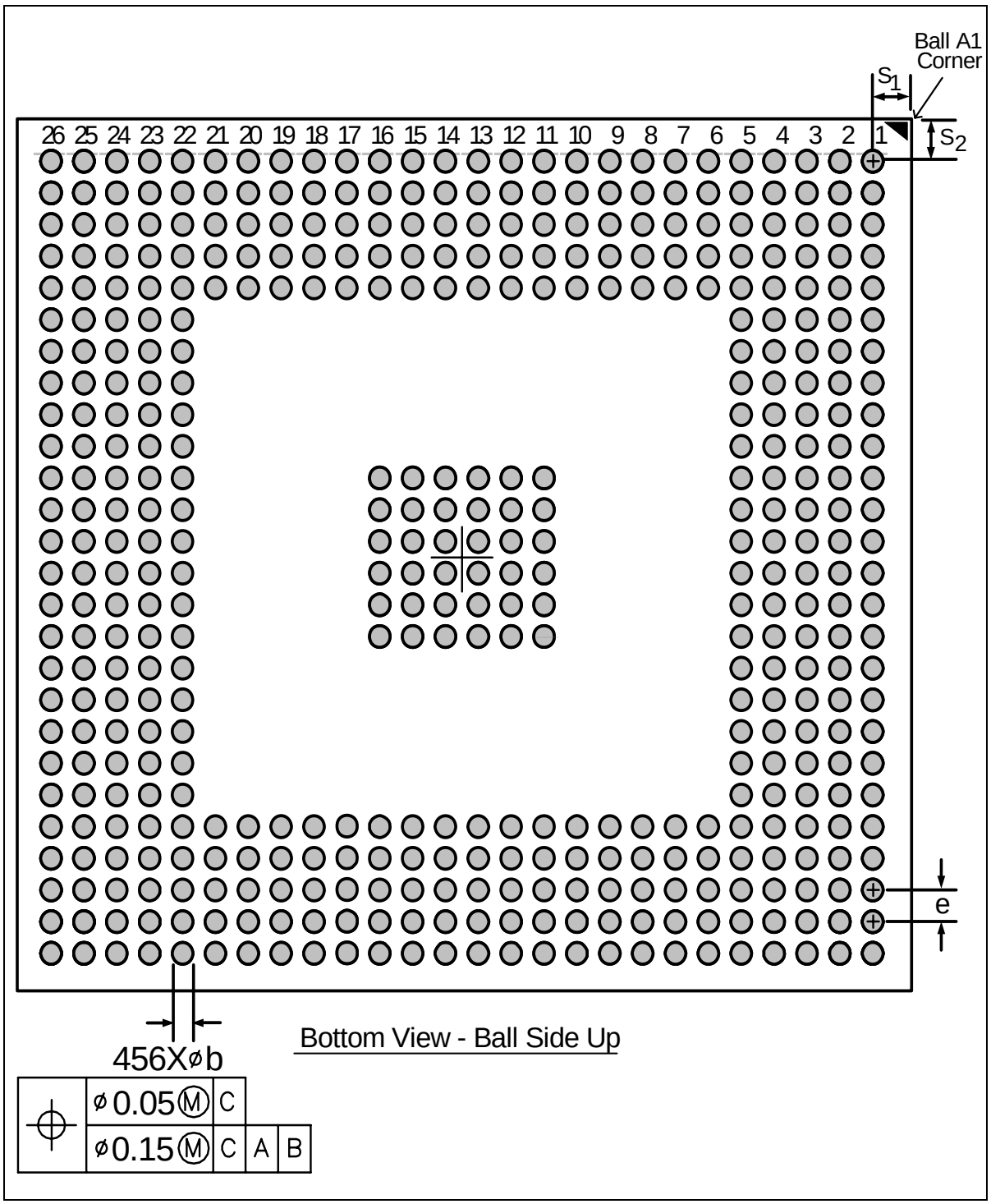


Figure 6: PXA320 Processor 14x14 mm VF-BGA Package, Side View

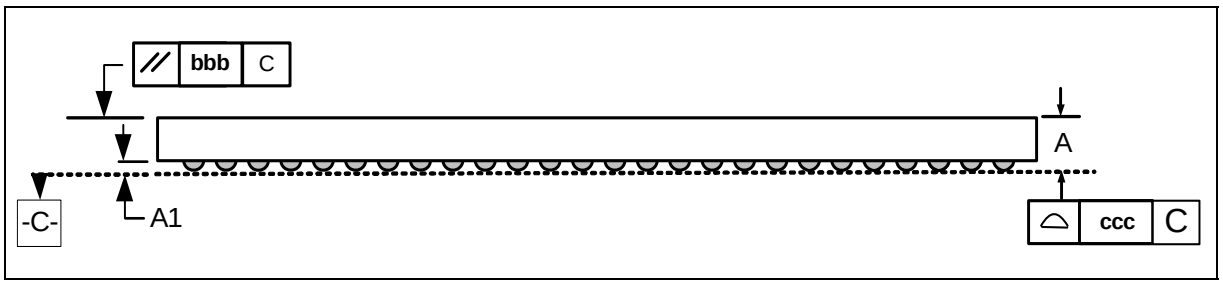
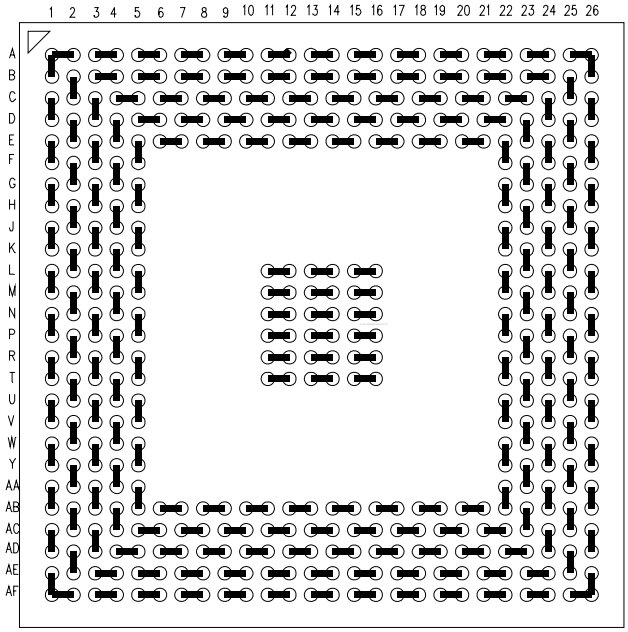


Figure 7: 14x14mm VF-BGA Daisy-Chain Substrate Diagram



3.3.2 PXA320 Processor Detailed Package Dimensions

Table 3 contains both Imperial (inches) and Metric (millimeters) systems for the package dimensions. The Imperial data has been rounded down. The Metric measurements are exact and do not contain any rounding. Marvell recommends using the Metric (millimeters) data.

Table 3: PXA320 Processor 14x14 mm VF-BGA Package Dimensions

Description	Symbol	Millimeters		
		Min	Nom	Max
Package Height	A			1.000
Ball Height	A1	0.200	0.250	0.300
Ball (Lead) Width	b	0.250	0.300	0.350
Package Body Width	D	13.950	14.000	14.050
Package Body Length	E	13.950	14.000	14.050
Pitch	[e]		0.500	
Ball (Lead) Count	N		456	
Corner to Ball A1 Distance Along D	S1		0.750	
Corner to Ball A1 Distance Along E	S2		0.750	
Package Edge Tolerance	aaa			0.15
Mold Flatness	bbb			0.20
Seating Plane Coplanarity	ccc			0.10

3.3.3 PXA322 Processor Package-on-Package (PoP)

The PXA322 Processor Package-on-Package (PoP) is in a 15-by-15 mm (15 mm^2), 416-pin, 0.65-mm ball pitch, as shown in Figure 16, Figure 17, and Figure 18.

Figure 8: PXA322 Processor 15-mm^2 PoP Package, Top View

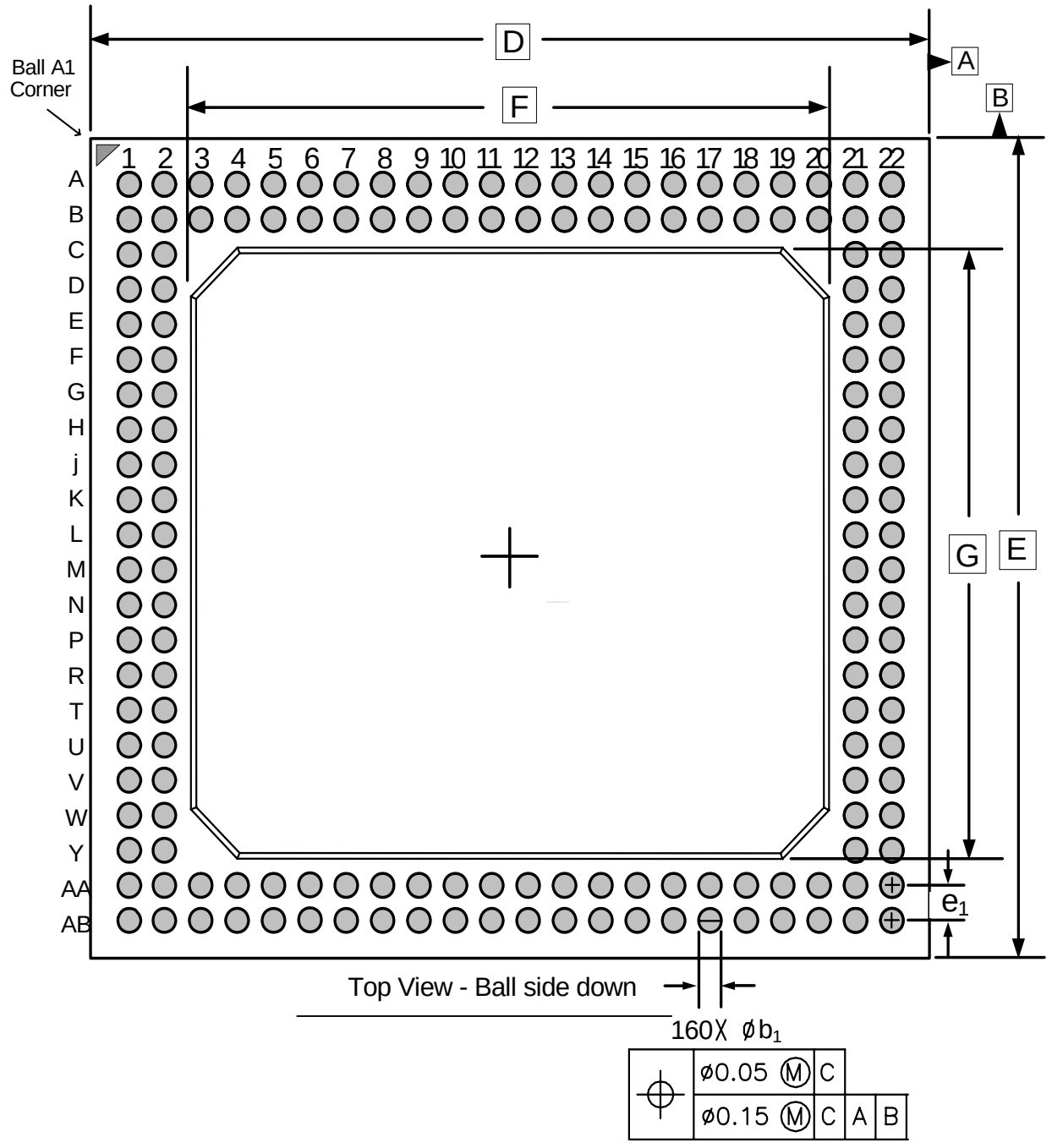


Figure 9: PXA322 Processor 15-mm^2 PoP Package, Bottom View

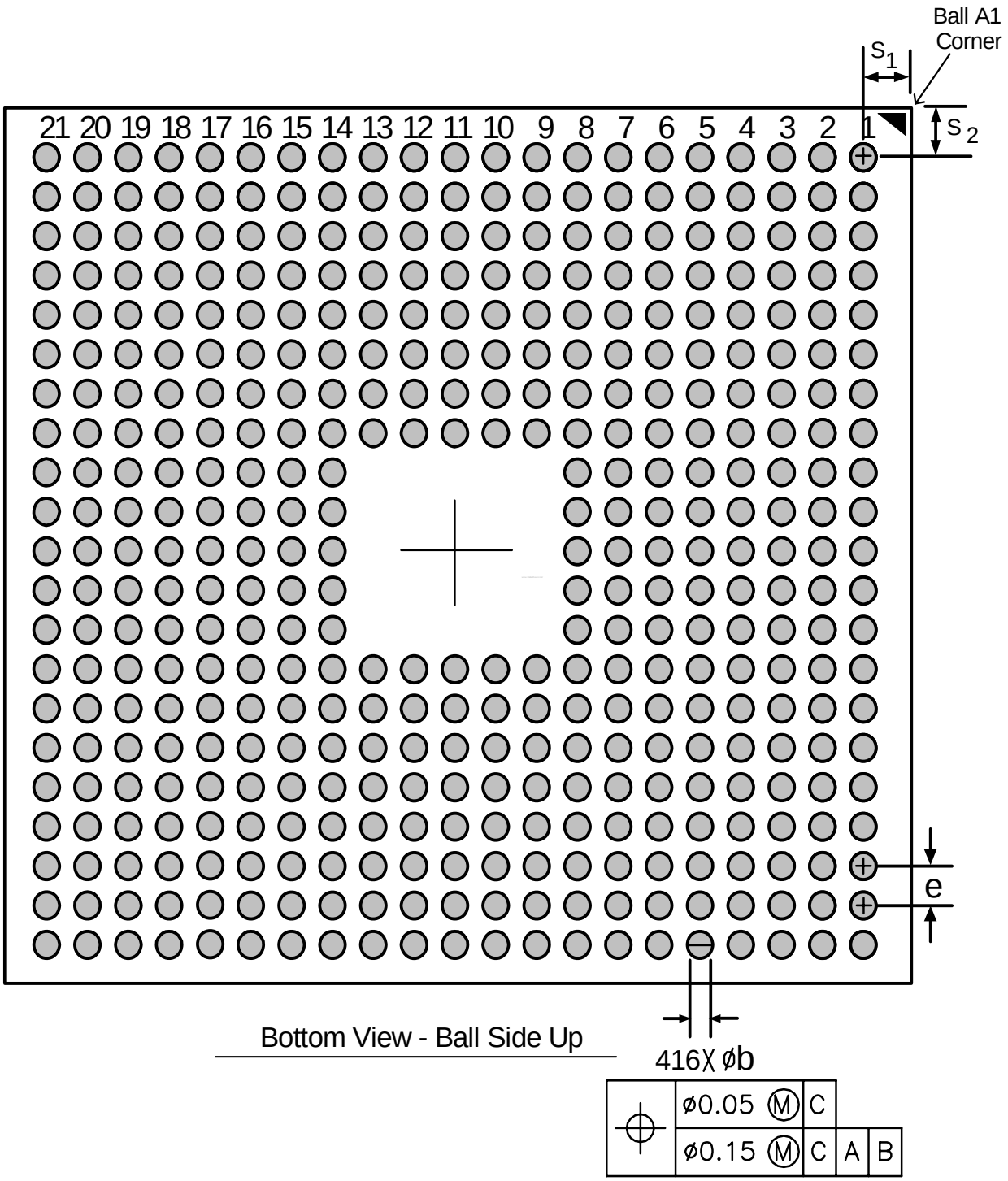


Figure 10: PXA322 Processor 15-mm^2 PoP Package, Side View

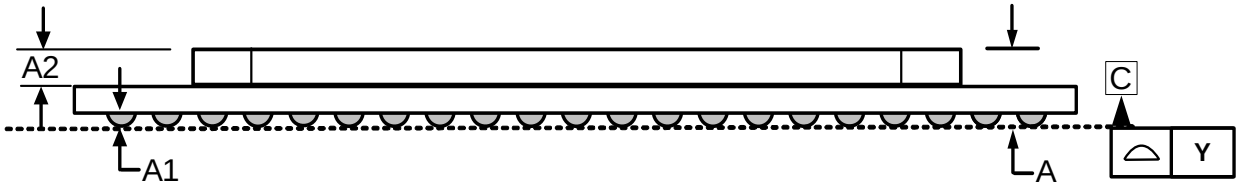
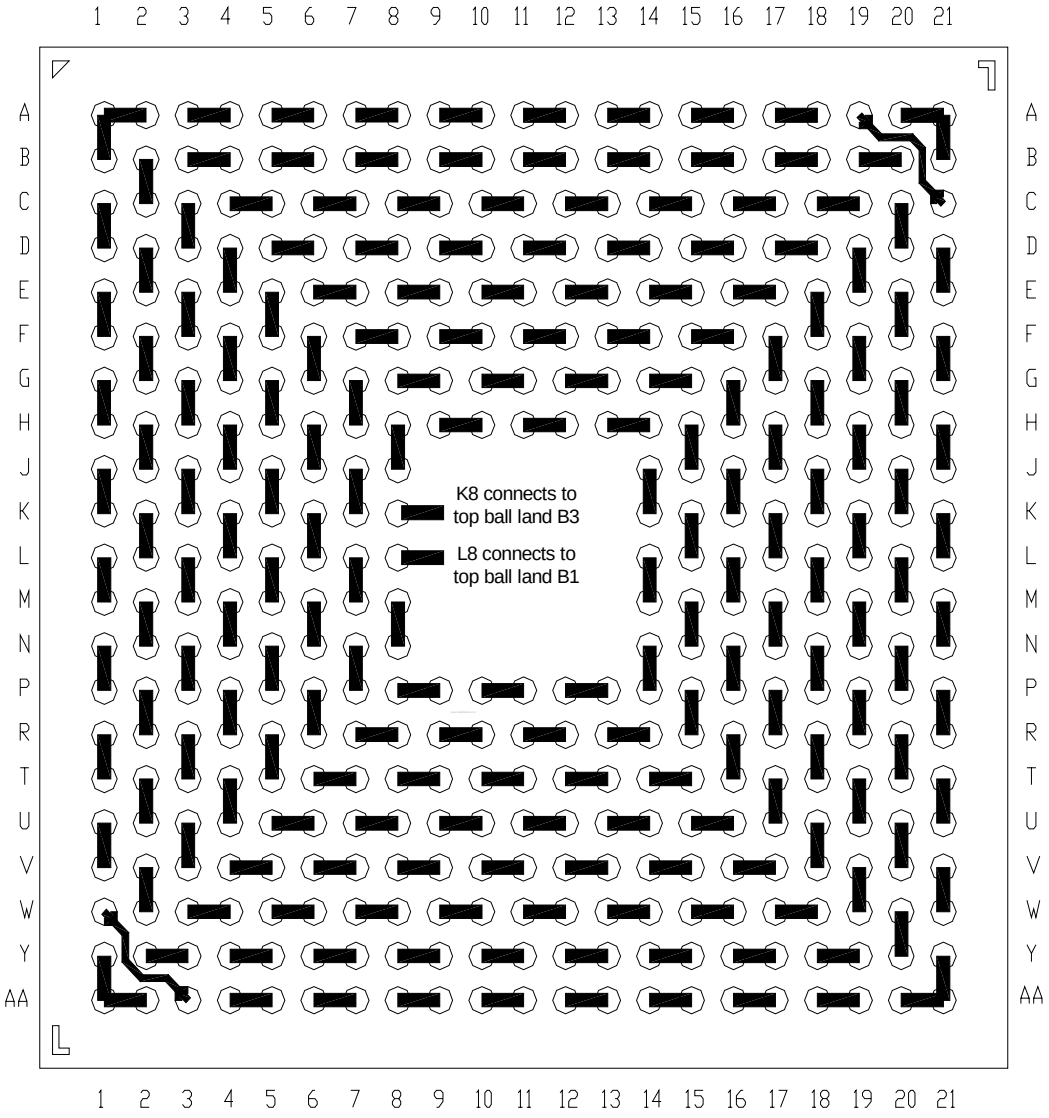


Figure 11: PXA322 15-mm^2 PoP Daisy-Chain Substrate Diagram



3.3.4 PXA322 Processor Detailed 15mm^2 POP Dimensions

Table 4 contains both Imperial (inches) and Metric (millimeters) systems for the package dimensions. The Imperial data has been rounded down. The Metric measurements are exact and do not contain any rounding. Marvell recommends using the Metric (millimeters) data.

Table 4: PXA322 Processor 15-mm^2 POP Dimensions

Description	Symbol	Millimeters		
		Min	Nom	Max
Package Height	A			0.930
Ball Height	A1	0.180		0.280
Mold Compound Thickness	A2	0.27	0.30	0.33
SMD Pad for Package Stack	b1	0.29	0.32	0.35
Ball (Lead) Width	b	0.25	0.30	0.35
Package Body Width	D	14.950	15.000	15.050
Package Body Length	E	14.950	15.000	15.050
Mold Cap Width	F	11.430	11.450	11.470
Mold Cap Width	G	11.430	11.450	11.470
Pitch	[e]		0.650	
Top Package Pitch	[e1]		0.650	
Ball (Lead) Count	N		416	
Seating Plane Coplanarity	Y			0.100
Corner to Ball A1 Distance Along D	S1		1.000	
Corner to Ball A1 Distance Along E	S2		1.000	

3.4 PXA31x and PXA30x Processor Package Views

3.4.1 PXA301 Processor and PXA311 Processor Multi-Chip Package (MCP)

The PXA301 Processor and PXA311 Processor Multi-Chip Package (MCP) is available in a 15-by-15 mm (15 mm^2), 416-pin, 0.65-mm ball pitch, as shown in Figure 12, Figure 13, Figure 14 and Figure 15.

Figure 12: PXA301 Processor and PXA311 Processor 15-mm^2 MCP Package, Top View

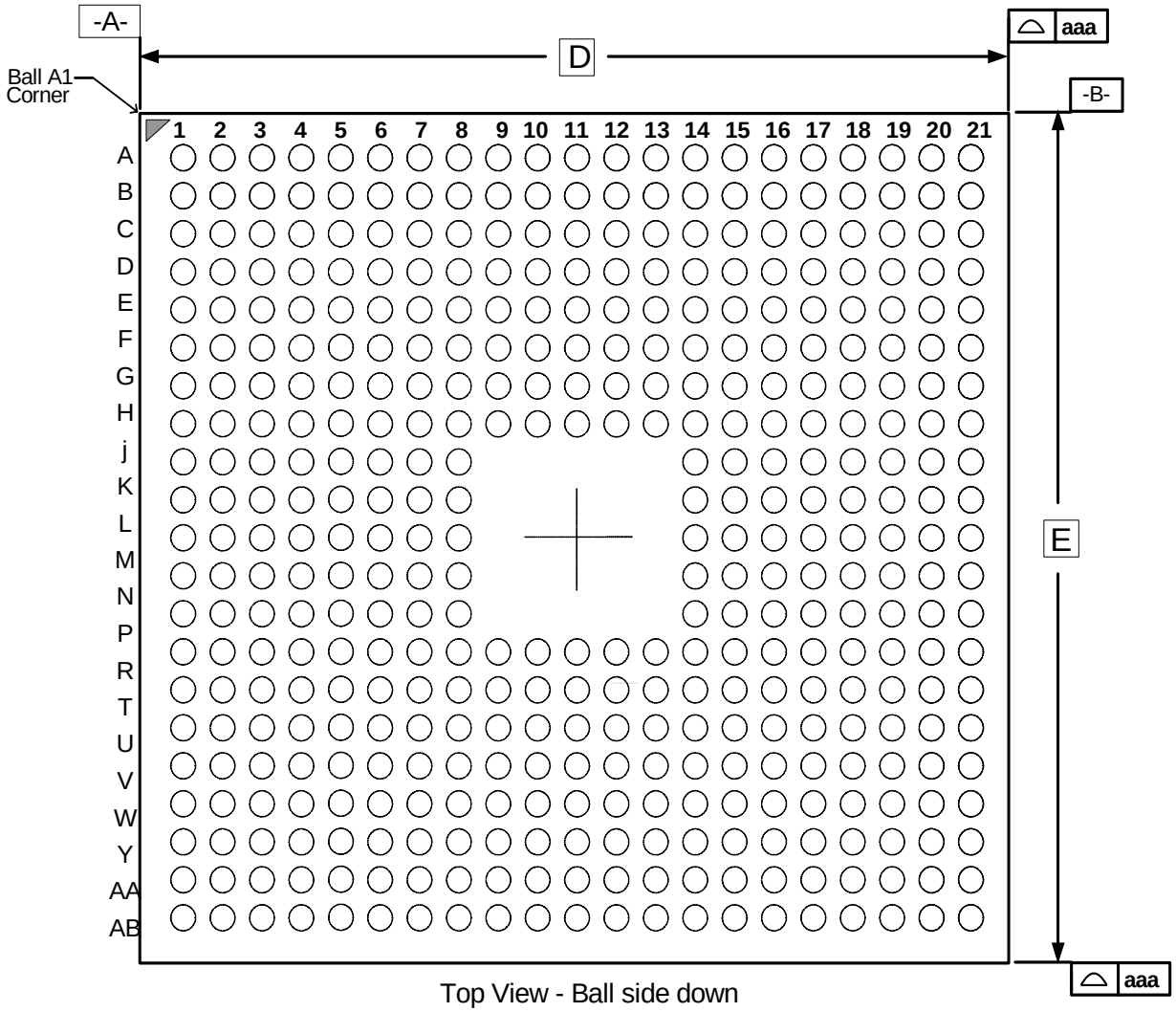


Figure 13: PXA301 Processor and PXA311 Processor 15-mm^2 MCP Package, Bottom View

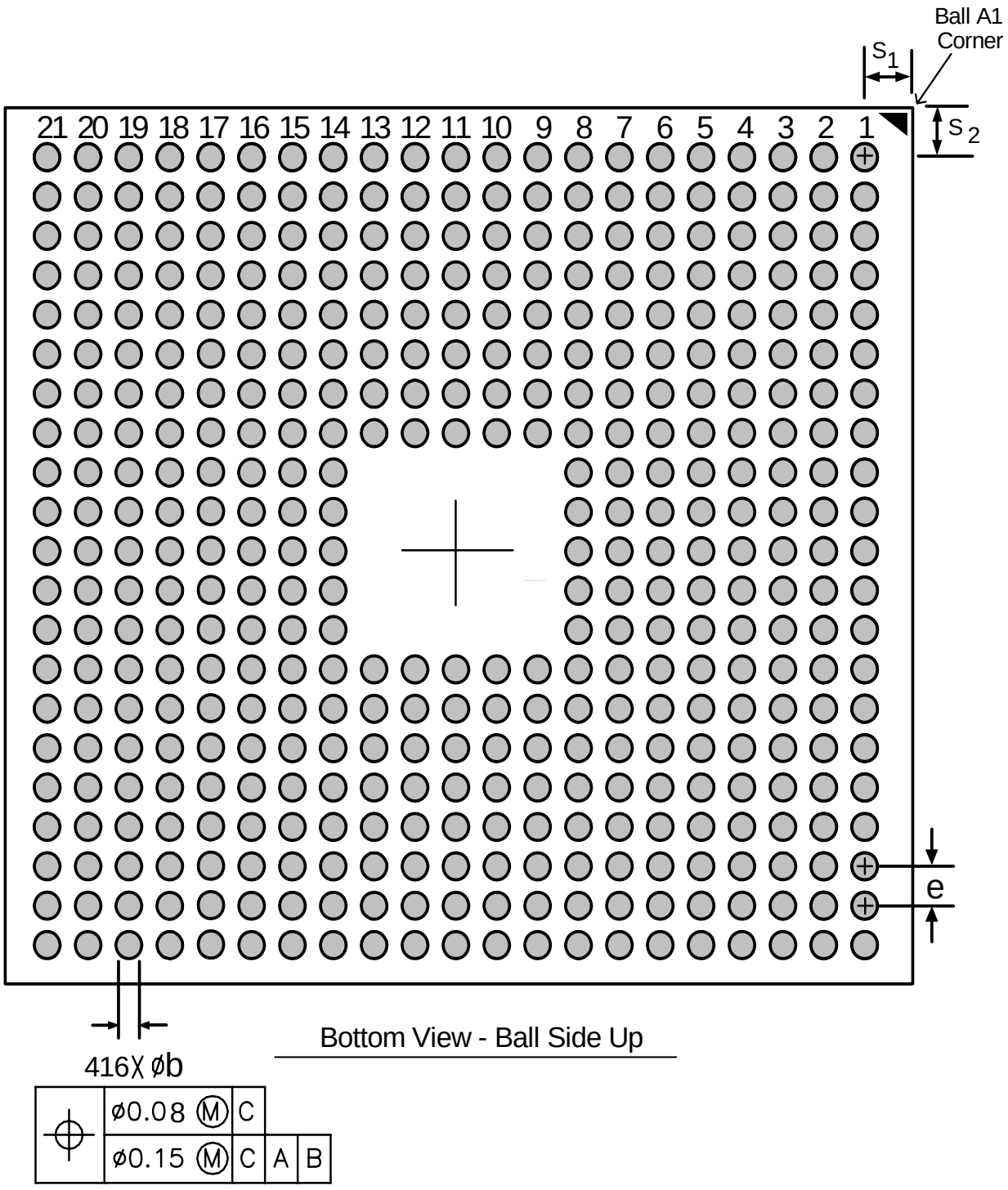


Figure 14: PXA301 Processor and PXA311 Processor 15-mm^2 MCP Package, Side View

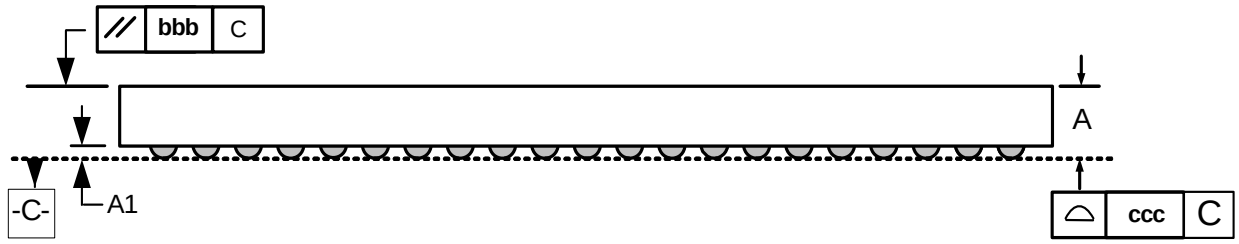
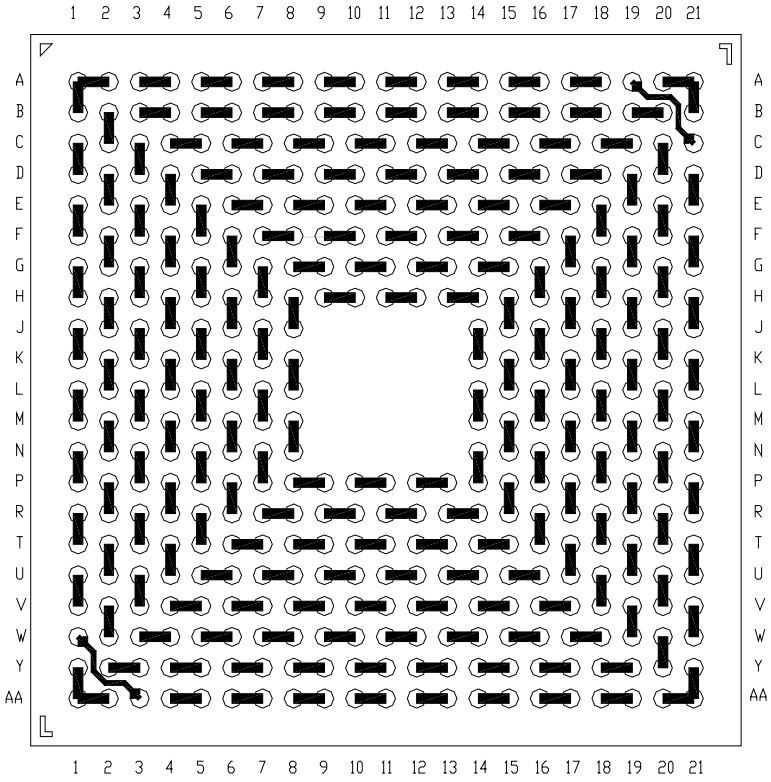


Figure 15: PXA301 Processor and PXA311 Processor 15-mm^2 MCP Daisy-Chain Substrate Diagram



3.4.2 PXA301 Processor and PXA311 Processor Detailed MCP Package Dimensions

Table 5 contains both Imperial (inches) and Metric (millimeters) systems for the package dimensions. The Imperial data has been rounded down. The Metric measurements are exact and do not contain any rounding. Marvell recommends using the Metric (millimeters) data.

Table 5: PXA301 Processor and PXA311 Processor 15-mm^2 MCP Package Dimensions

Description	Symbol	Millimeters		
		Min	Nom	Max
PXA301 Processor Package Height	A			1.400
PXA311 Processor Package Height	A			1.500
PXA301 Processor Ball Height	A1	0.270		0.370
PXA311 Processor Ball Height	A1	0.220		0.320
PXA301 Processor MCP Ball (Lead) Width	b	0.330	0.400	0.470
PXA311 Processor Ball (Lead) Width	b	0.280	0.350	0.420
Package Body Width	D	14.900	15.000	15.100
Package Body Length	E	14.900	15.000	15.100
Pitch	[e]		0.650	
Ball (Lead) Count	N		416	
Corner to Ball A1 Distance Along D	S1		0.750	
Corner to Ball A1 Distance Along E	S2		0.750	
Package Edge Tolerance	aaa			0.15
Mold Flatness	bbb			0.20
Seating Plane Coplanarity	ccc			0.10

3.4.3 PXA302 and PXA312 Processor Package-on-Package (PoP)

The PXA302 Processor and PXA312 Processor Package-on-Package (PoP) is in a 15-by-15 mm (15 mm^2), 416-pin, 0.65-mm ball pitch, as shown in Figure 16, Figure 17, and Figure 18.

Figure 16: PXA302 Processor and PXA312 Processor 15-mm^2 PoP Package, Top View

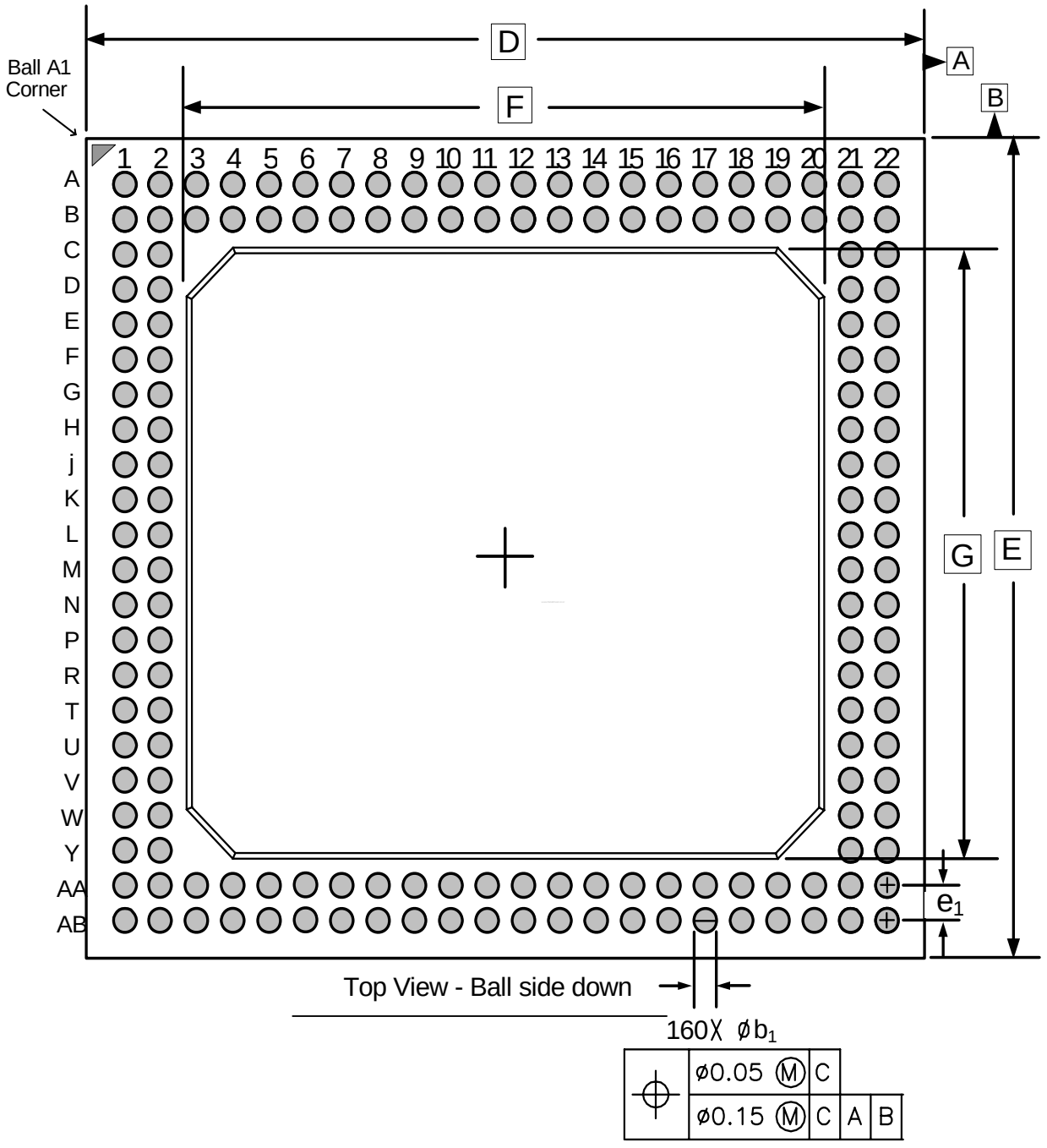


Figure 17: PXA302 Processor and PXA312 Processor 15-mm^2 PoP Package, Bottom View

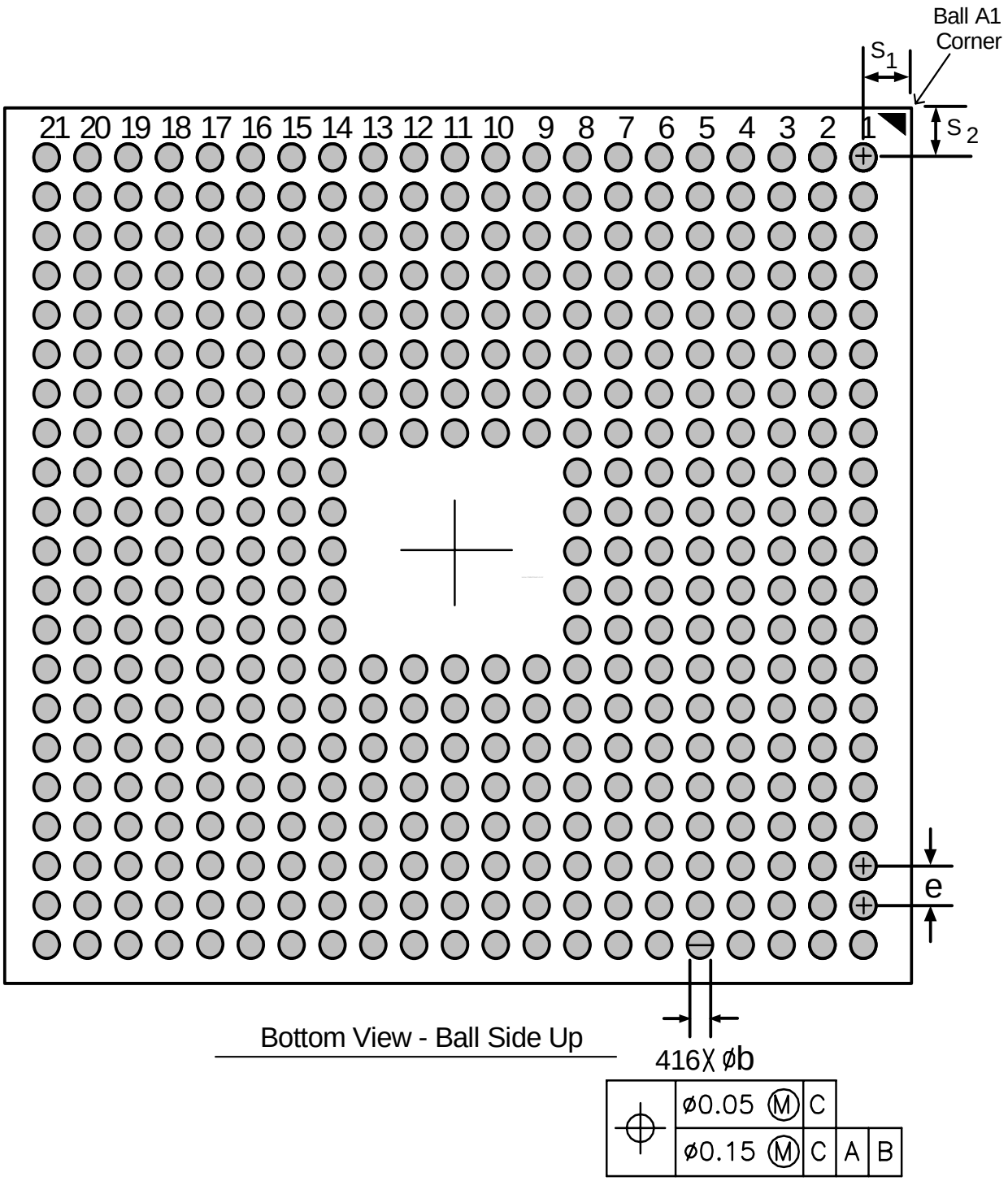


Figure 18: PXA302 Processor and PXA312 Processor 15-mm^2 PoP Package, Side View

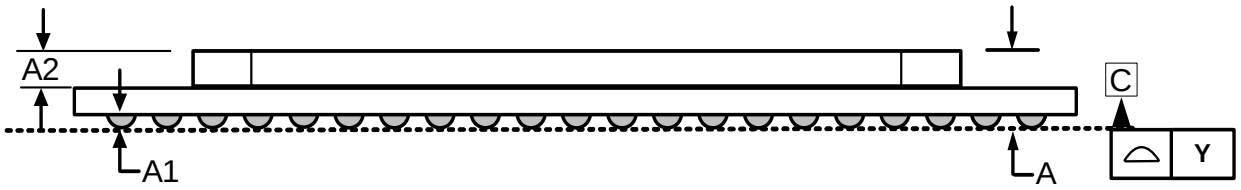
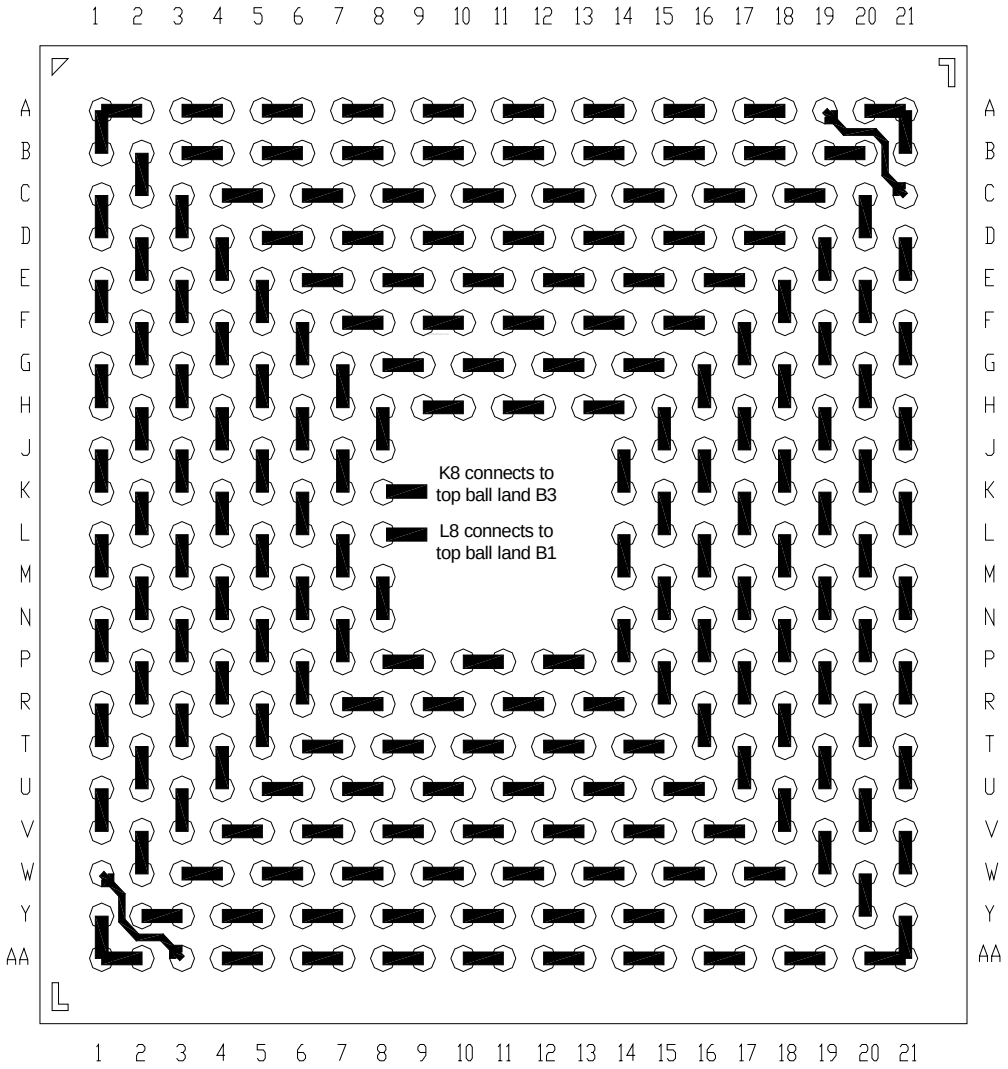


Figure 19: PXA302 Processor and PXA312 Processor 15-mm^2 PoP Daisy-Chain Substrate Diagram



3.4.4 PXA302 Processor and PXA312 Processor Detailed 15mm^2 POP Dimensions

Table 6 contains both Imperial (inches) and Metric (millimeters) systems for the package dimensions. The Imperial data has been rounded down. The Metric measurements are exact and do not contain any rounding. Marvell recommends using the Metric (millimeters) data.

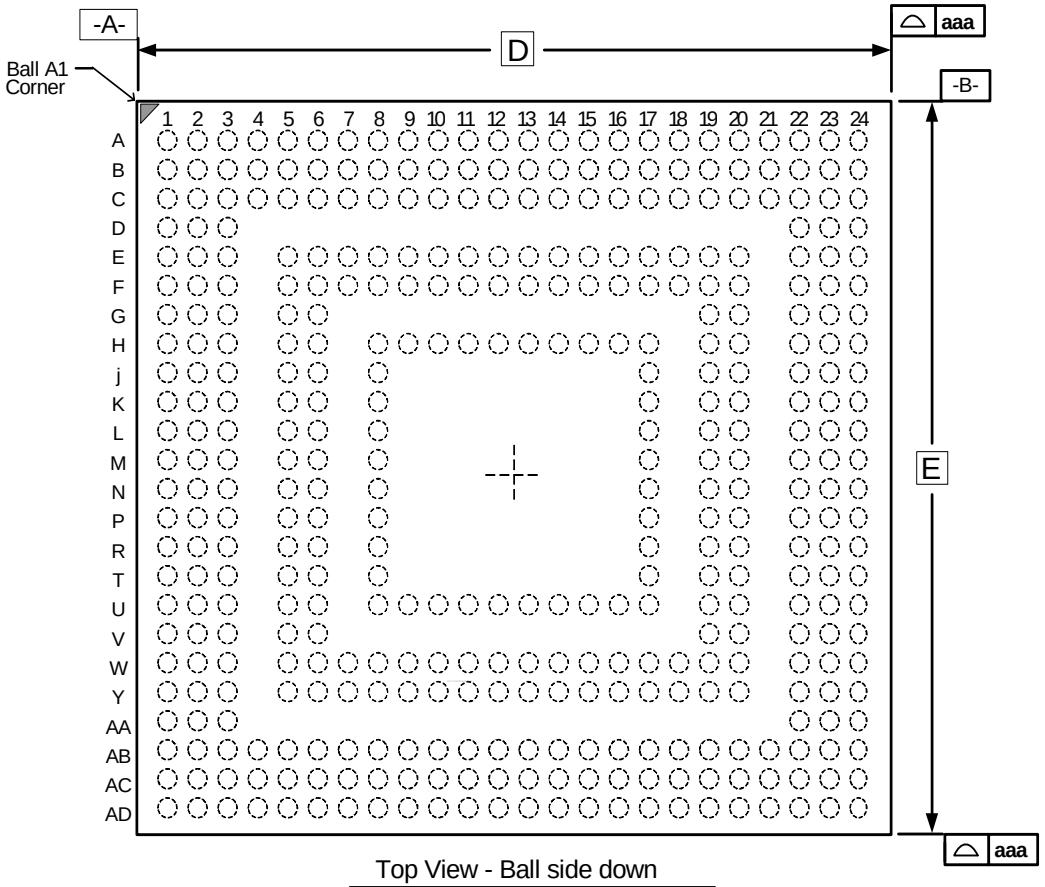
Table 6: PXA302 Processor and PXA312 Processor 15-mm^2 POP Dimensions

Description	Symbol	Millimeters		
		Min	Nom	Max
Package Height	A			0.930
Ball Height	A1	0.180		0.280
Mold Compound Thickness	A2	0.27	0.30	0.33
SMD Pad for Package Stack	b1	0.29	0.32	0.35
Ball (Lead) Width	b	0.25	0.30	0.35
Package Body Width	D	14.950	15.000	15.050
Package Body Length	E	14.950	15.000	15.050
Mold Cap Width	F	11.430	11.450	11.470
Mold Cap Width	G	11.430	11.450	11.470
Pitch	[e]		0.650	
Top Package Pitch	[e1]		0.650	
Ball (Lead) Count	N		416	
Seating Plane Coplanarity	Y			0.100
Corner to Ball A1 Distance Along D	S1		1.000	
Corner to Ball A1 Distance Along E	S2		1.000	

3.4.5 PXA300 Processor and PXA310 Processor Discrete Package (VF-BGA)

The PXA300 Processor and PXA310 Processor packages are available in a 13-by-13 mm (13 mm^2) VF-BGA, 400-pin, 0.5-mm ball pitch configuration, as shown in Figure 20, Figure 21, and Figure 22.

Figure 20: PXA300 Processor and PXA310 Processor 13-mm^2 VF-BGA Package, Top View



Top View - Ball side down

Complete Ink Mark Not Shown

Figure 21: PXA300 Processor and PXA310 Processor 13-mm^2 VF-BGA Package, Bottom View

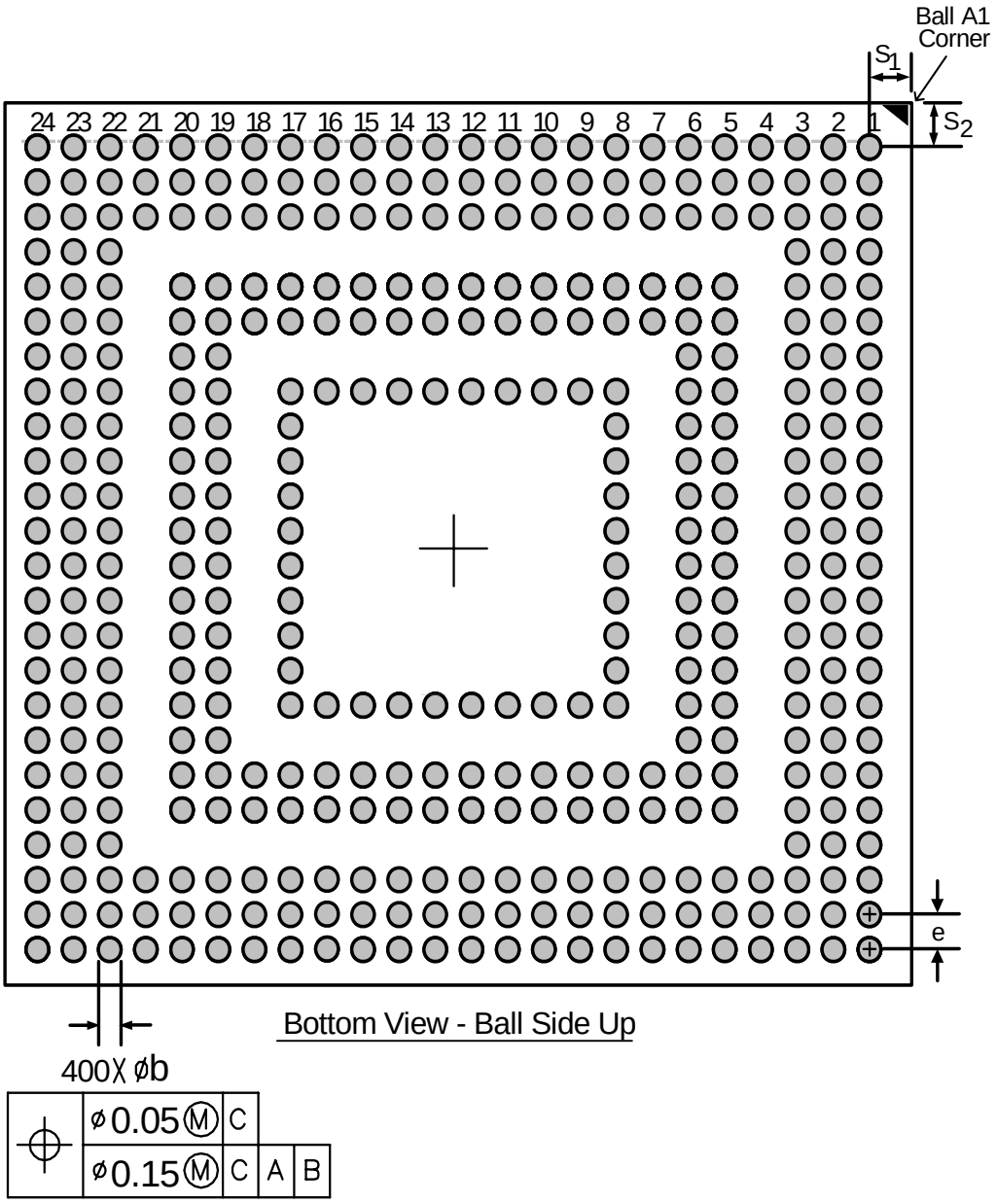


Figure 22: PXA300 Processor and PXA310 Processor 13-mm^2 VF-BGA Package, Side View

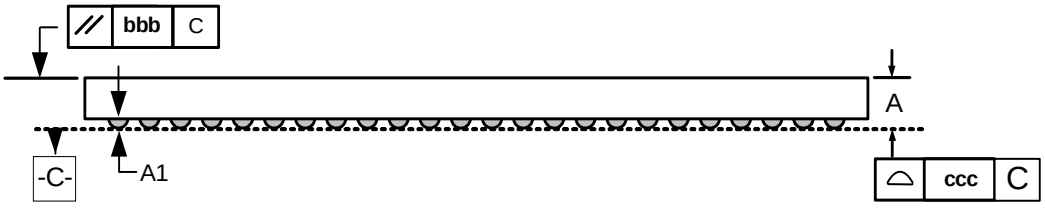


Figure 23: PXA300 Processor and PXA310 Processor 13-mm^2 VF-BGA Daisy-Chain Substrate Diagram

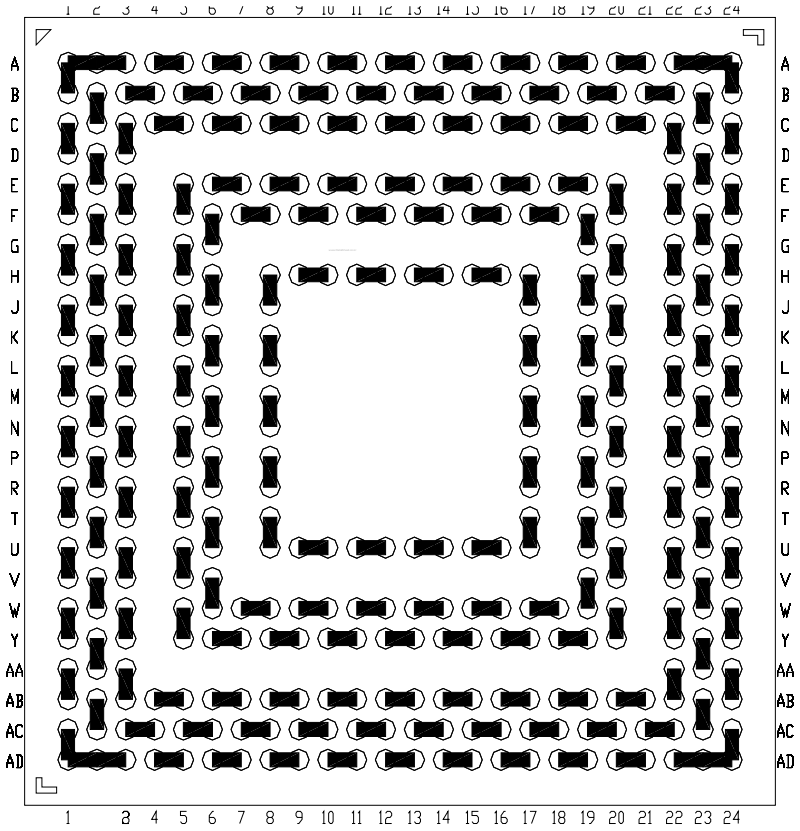


Table 7: PXA300 Processor and PXA310 Processor 13-mm^2 VF-BGA Package Dimensions

Description	Symbol	Millimeters		
		Min	Nom	Max
Package Height	A			1.000
Ball Height	A1	0.18	0.250	0.300
Ball (Lead) Width	b	0.260	0.300	0.340
Package Body Width	D	12.900	13.000	13.100
Package Body Length	E	12.900	13000	13.100
Pitch	[e]		0.500	
Ball (Lead) Count	N		400	
Corner to Ball A1 Distance Along D	S1		0.750	
Corner to Ball A1 Distance Along E	S2		0.750	
Package Edge Tolerance	aaa			0.10
Mold Flatness	bbb			0.10
Seating Plane Coplanarity	ccc			0.08

3.5 PXA30x Processor Package Views

3.5.1 PXA303 Processor 19mm^2 Discrete Package (VF-BGA)

The PXA303 processor package is provided in a 19-by-19 mm (19 mm^2) VF-BGA, 409-pin, 0.8-mm ball pitch configuration, as shown in Figure 24, Figure 25, Figure 26, and Figure 27. Table 7 contain both Imperial (inches) and Metric (millimeters) for the package dimensions. The Imperial data has been rounded down. The Metric measurements are exact and do not contain any rounding. Marvell recommends using the Metric (millimeters) data.

Figure 24: PXA303 Processor 19-mm^2 VF-BGA Package, Top View

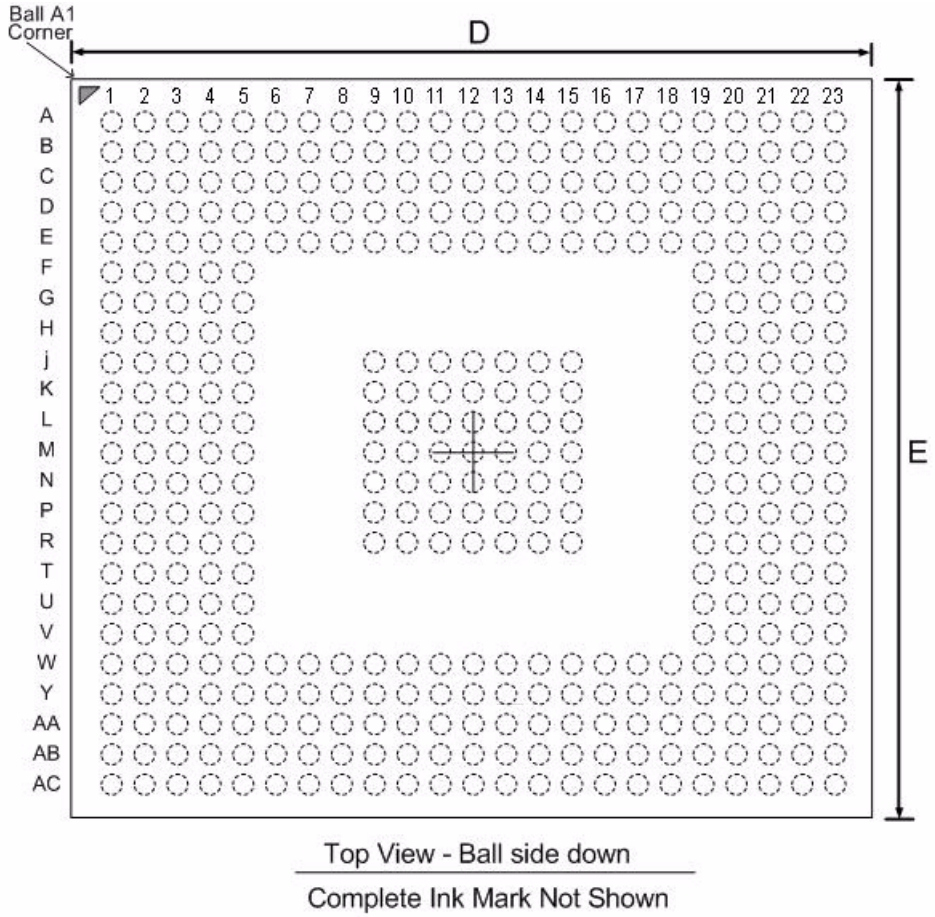


Figure 25: PXA303 Processor 19-mm^2 VF-BGA Package, Bottom View

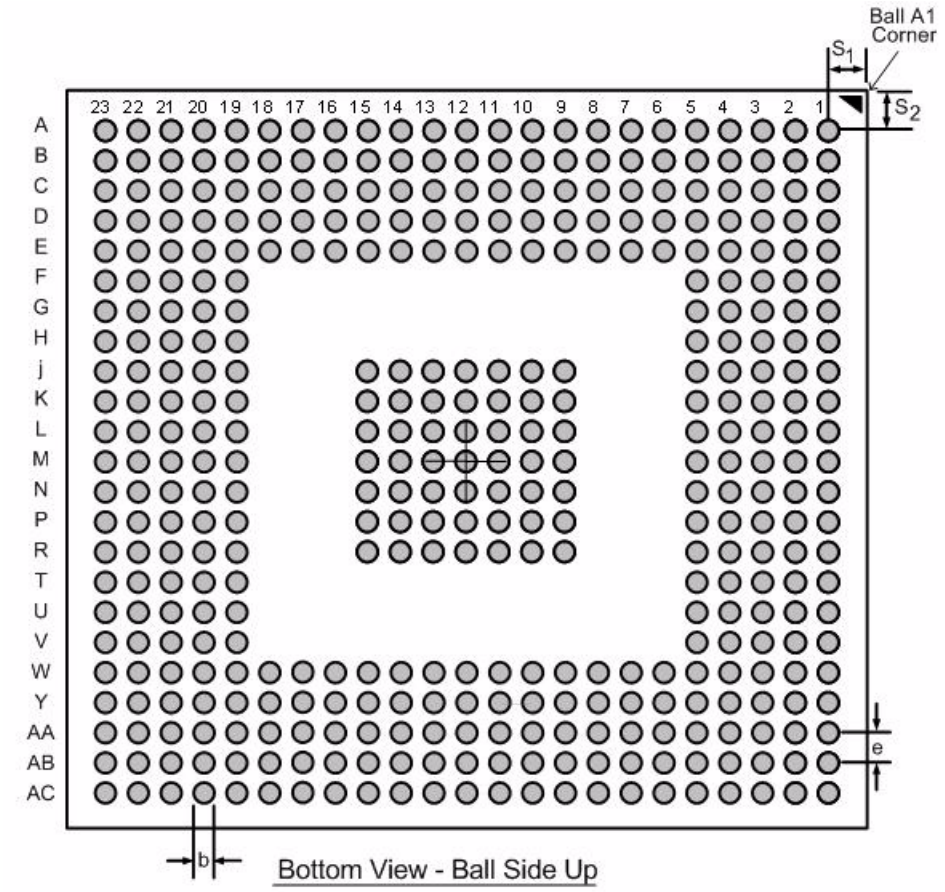
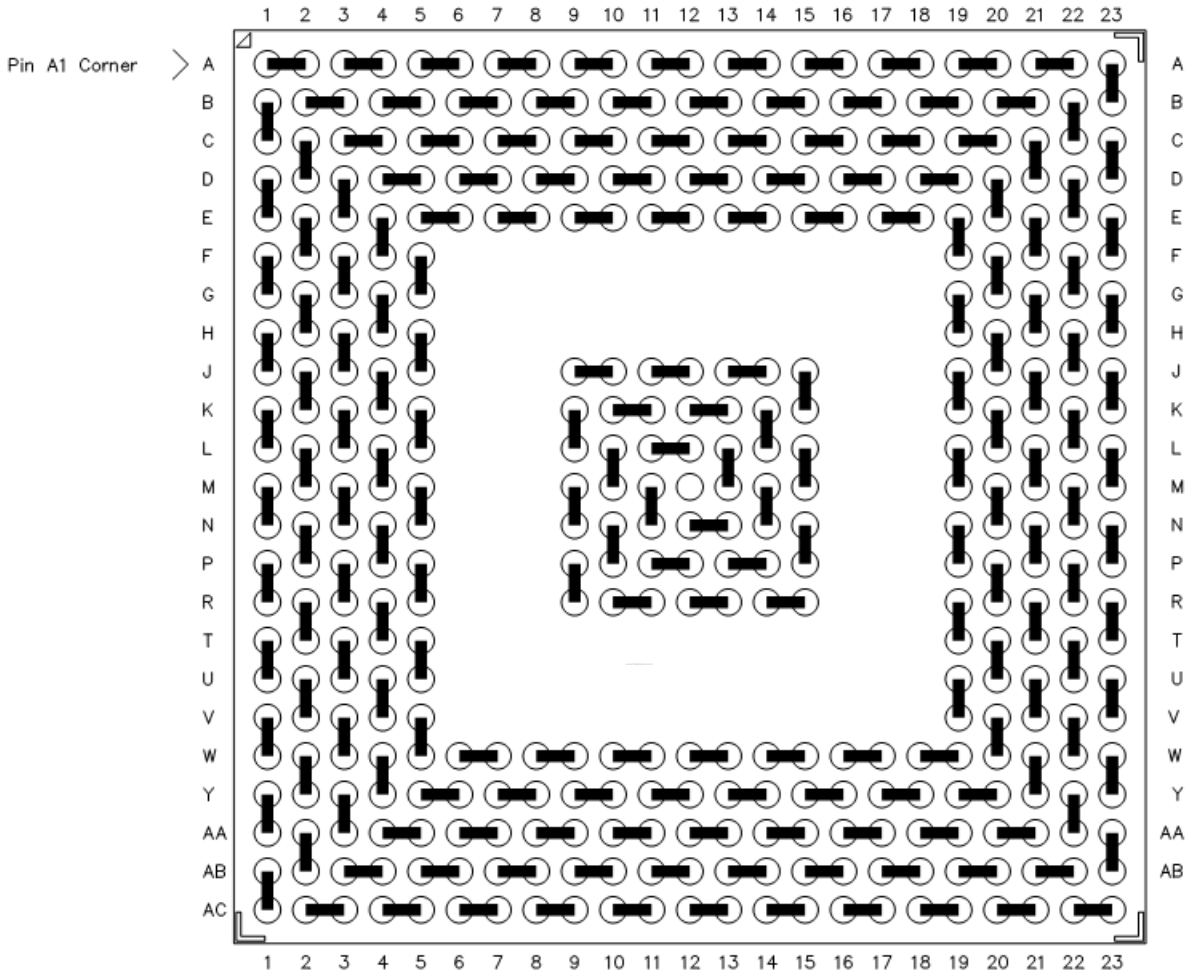


Figure 26: PXA303 Processor 19-mm^2 VF-BGA Package, Side View

Figure 27: PXA303 Processor 19-mm^2 VF-BGA Daisy-Chain Substrate Diagram



3.5.2 PXA303 Processor Detailed VF-BGA Package Dimensions

Table 8 contains both Imperial (inches) and Metric (millimeters) systems for the package dimensions. The Imperial data has been rounded down. The Metric measurements are exact and do not contain any rounding. Marvell recommends using the Metric (millimeters) data.

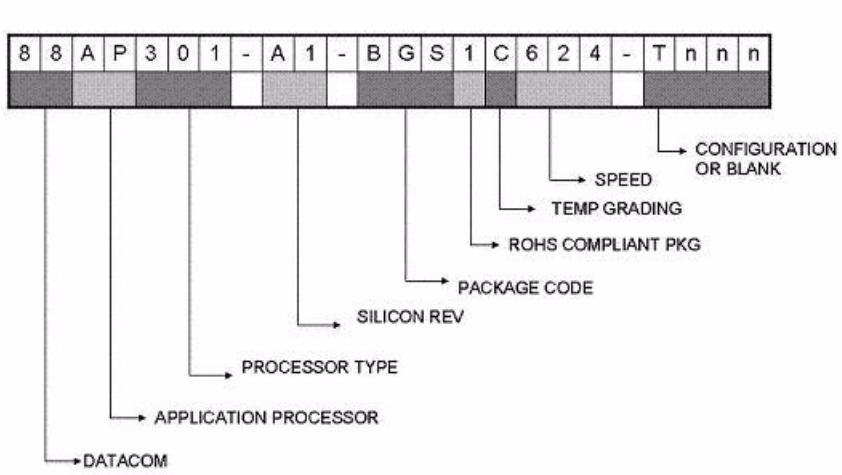
Table 8: PXA303 Processor 19-mm^2 VF-BGA Package Dimensions

Description	Symbol	Millimeters		
		Min	Nom	Max
Package Height	A			1.560
Ball Height	A1	0.350		0.450
Package Body Thickness	A2		1.060	
Ball (Lead) Width	b	0.450	0.500	0.550
Package Body Width	D	18.900	19.000	19.100
Package Body Length	E	18.900	19.000	19.100
Pitch	[e]		0.800	
Ball (Lead) Count	N		409	
Seating Plane Coplanarity	Y			0.140
Corner to Ball A1 Distance Along D	S1		0.700	
Corner to Ball A1 Distance Along E	S2		0.700	

3.6 PXA3xx Processor Family Markings

Each PXA30x and PXA31x processor includes markings on top of the package. Figure 28 contains the processor product marking information that explains each part of the marking. There are two different decoders, one for samples, and one for production material.

Figure 28: PX3xx (88AP3xx) Processor Family Product Marking Information



3.6.1 PXA32x Processor Markings

Each PXA300 processor or PXA310 processor includes markings on top of the package. Figure 29 contains a “Product Information Decoder” that explains what each part of the marking means. Note that there are two different decoders, one for samples and one for production material. Figure 30 contains the “Configuration Line Decoder” that explains the configuration line for production material.

Figure 29: PXA32x Processor VF-BGA Product Information Decoder

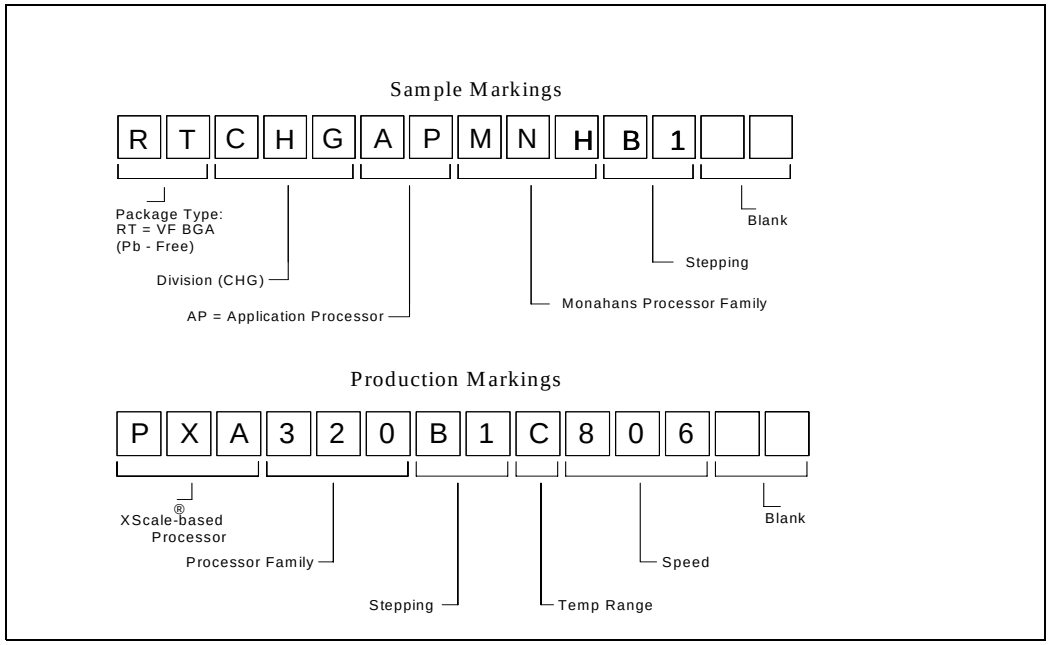


Figure 30: PXA32x Processor Configuration Line Decoding

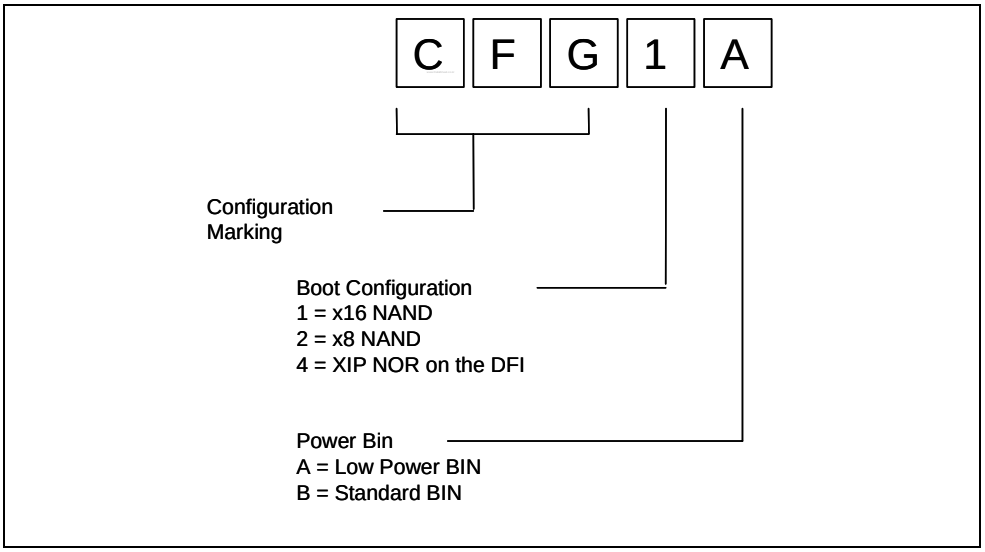


Figure 31: PXA32x Processor Engineering Sample Markings

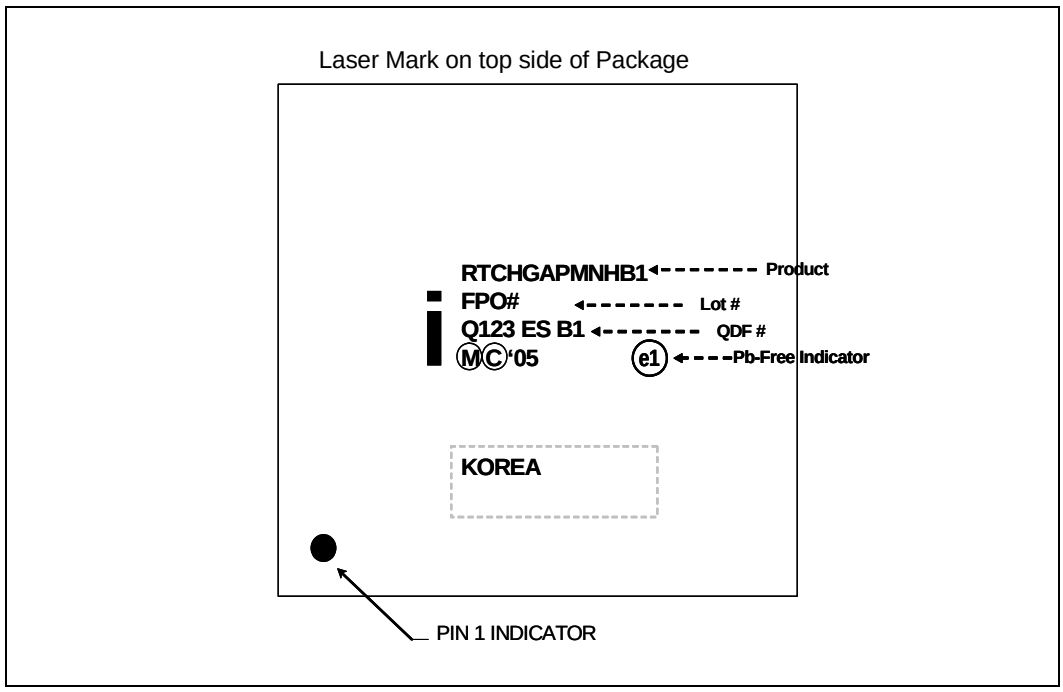


Figure 32: PXA32x Processor Daisy Chain Samples Markings

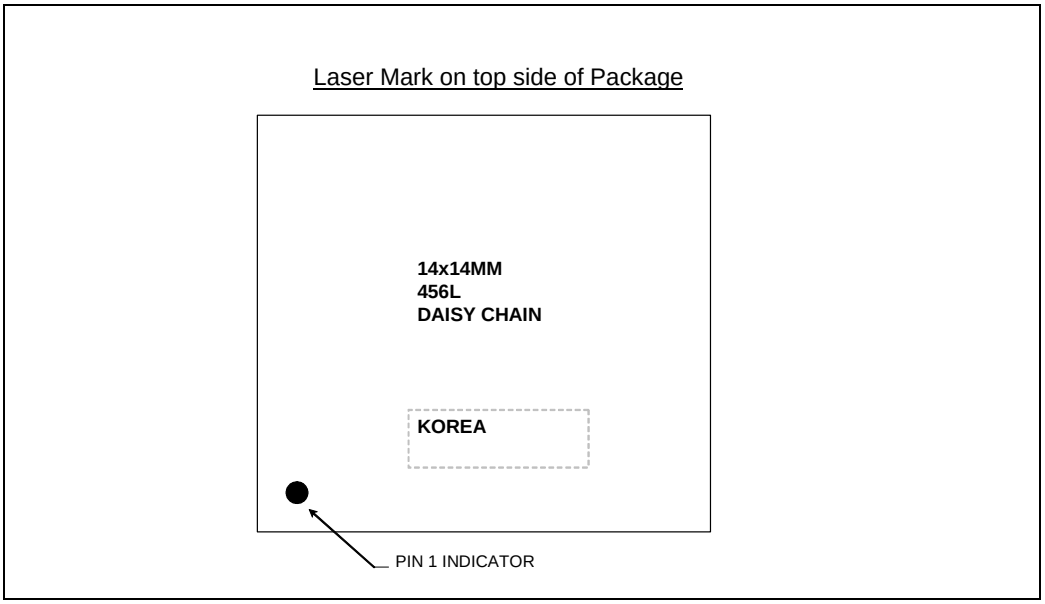
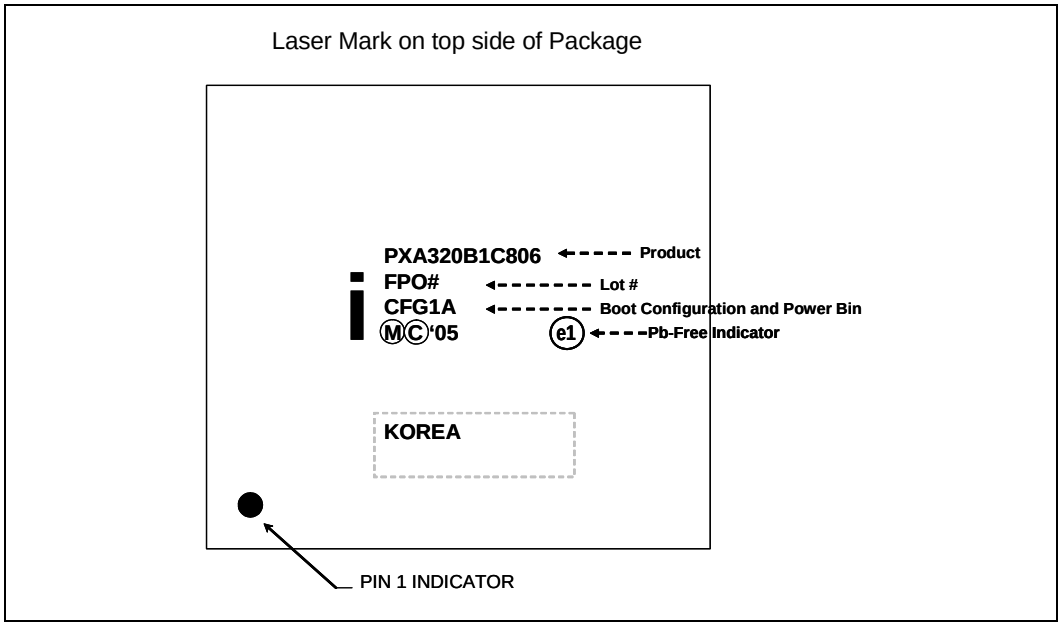


Figure 33: PXA32x Processor Production Markings



4 Pin Listing and Signal Definitions

This chapter describes the signals and pins for the PXA3xx Processor Family.

Many of the package pins are multiplexed so that they can be configured for use as a general-purpose I/O signal or any one of the alternate functions using the GPIO alternate-function select registers. Some signals can be configured to appear on one of several different pins using alternate function controls.

4.1 Ball Map View

In the following ball map figures, the lowercase letter “n”, which normally indicates negation, appears as uppercase “N”. “RFU” means “Reserved For Future Use”. NC means “No Connect”. Do not connect these pins. The balls highlighted in yellow show the difference between the PXA30x and PXA31x processor.

4.1.1 PXA32x Processor Ball Maps

4.1.1.1 PXA320 Processor 456-Ball VF-BGA Ball Map

Figure 34 and Figure 35 show the ball map for the 456-ball VF-BGA PXA320 processor discrete package.

Figure 34: PXA320 Processor 14mm^2 VF-BGA Ball Map, Left Half

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	NC	NC	USBOTG_N	USBOTG_P	USBH1_N	USBH1_P	PWR_EN	TMS	VSS	VCC_BBATT	NGPIO_RESET	PWR_SDA	TEST	A
B	NC	MD1	MD0	TCK	VSS_USB	TDI	NBATT_FAULT	PWR_OUT	VSS_BBATT	PXTAL_IN	VSS_OSC13M	VCTCXO_EN	GPIO4_2	B
C	MD4	MD2	DQM0	MD3	VCC_USB	CLK_TOUT	PWR_CAP1	TXTAL_OUT	NRESET_OUT	PXTAL_OUT	PWR_SCL	TESTCLK	GPIO2_2	C
D	MD7	DQS0	MD5	VCC_MEM	TDO	NTRST	PWR_CAP0	TXTAL_IN	VCC_BG	VSS_BG	CLK_POUT	GPIO5_2	GPIO127	D
E	DQS1	MD6	MD8	VSS_MEM	SYS_EN	NRESET	VCC_MVT	VCC_OSC13M	VCC_SRAM	VCC_IO1	VSS_IO1	GPIO0_2	GPIO125	E
F	DQM1	MD10	MD9	VCC_MEM	EXT_WAKEUP1									F
G	MD14	MD13	MD11	VSS_MEM	EXT_WAKEUP0									G
H	MA3	MD15	MD12	VCC_MEM	VCC_MVT									H
J	MA1	MA2	VCC_SRAM	VSS_MEM	VCC_MEM									J
K	MA14	SDMA10	RFU_K3	MA0	VCC_MEM									K
L	NSDCS0	MA13	MA12	MA15	VSS_MEM						VSS	VSS	VCC_APPS	L
M	SDCLK0	SDCKE	NSDWE	VCC_MVT	VCC_MEM						VSS	VSS	VCC_APPS	M
N	SDCLK1	NSDRAS	MA8	NSDCS1	VSS_MEM						VCC_APPS	VCC_APPS	VSS	N
P	MA5	MA9	MA7	MA11	VCC_MEM						VCC_APPS	VCC_APPS	VSS	P
R	RCOMP_DDR	RFU_R2	MA6	NSDCAS	VSS_MEM						VSS	VSS	VCC_APPS	R
T	RFU_T1	RFU_T2	RFU_T3	MA4	VCC_MEM						VSS	VSS	VCC_APPS	T
U	RFU_U1	RFU_U2	RFU_U3	RFU_U4	VSS_MEM									U
V	MD18	DQM2	MD17	MD16	VSS_MEM									V
W	MD19	DQS2	MD23	VCC_MVT	VCC_MEM									W
Y	MD20	MD24	MD22	VSS	VCC_MEM									Y
AA	MD21	DQS3	DQM3	MD25	VSS_MEM									AA
AB	MD26	MD31	MD30	MD27	VCC_MEM	DF_ALE_NWE2	VCC_DF	VCC_MVT	VSS	DF_IO8	VCC_SRAM	VSS	DF_IO12	AB
AC	MD28	GPIO2	GPIO1	GPIO0	VSS_MEM	VSS_DF	VSS_DF	DF_ADDR0	VCC_DF	VSS_DF	DF_IO1	DF_IO4	DF_IO15	AC
AD	MD29	GPIO3	GPIO4	RFU_AD4	DF_CLE_NOE	VCC_DF	DF_NRE	DF_ADDR1	DF_IO0	DF_IO2	DF_IO11	DF_IO13	VSS_DF	AD
AE	NC	NC	NXCVREN	NBE0	DF_INT_RNB	DF_NCS0	NLUA	NLLA	DF_ADDR3	DF_IO10	VCC_DF	DF_IO6	VCC_DF	AE
AF	NC	NC	DF_ALE_NWE1	DF_SCLK_E	NBE1	DF_NCS1	DF_NWE	DF_ADDR2	DF_IO9	DF_IO3	VSS_DF	DF_IO5	DF_IO7	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 35: PXA320 Processor 14mm^2 VF-BGA Ball Map, Right Half

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GPIO3_2	GPIO126	GPIO123	GPIO114	VCC_TSI	GPIO109	GPIO106	GPIO102	GPIO101	GPIO100	GPIO99	NC	NC	A
B	GPIO1_2	VCC_PLL	GPIO121	GPIO119	GPIO113	GPIO110	GPIO107	GPIO103	VCC_IO6	GPIO94	GPIO98	GPIO97	NC	B
C	VSS_PLL	GPIO122	GPIO118	GPIO115	VSS_TSI	GPIO112	VCC_IO6	GPIO105	VSS_IO6	GPIO95	GPIO96	GPIO88	GPIO90	C
D	GPIO124	VCC_IO1	VCC_SRAM	GPIO116	TSI_YM	TSI_XM	VSS_IO6	GPIO93	GPIO87	GPIO92	GPIO91	GPIO89	GPIO84	D
E	GPIO120	VSS_IO1	GPIO117	TSI_YP	TSI_XP	GPIO111	VCC_MVT	GPIO108	GPIO104	GPIO85	GPIO86	GPIO81	GPIO82	E
F									GPIO83	GPIO80	VCC_MSL	GPIO79	VSS_MSL	F
G									GPIO78	VCC_MVT	GPIO77	VSS	VSS	G
H									GPIO15_2	GPIO75	GPIO76	GPIO17_2	VCC_SRAM	H
J									GPIO73	GPIO74	GPIO16_2	VSS_LCD	VCC_LCD	J
K									GPIO66	GPIO71	GPIO72	GPIO14_2	GPIO70	K
L	VCC_APPS	VSS	VSS						GPIO11_2	GPIO69	GPIO67	GPIO64	GPIO68	L
M	VCC_APPS	VSS	VSS						GPIO9_2	VSS_LCD	GPIO63	GPIO13_2	GPIO65	M
N	VSS	VCC_APPS	VCC_APPS						VSS	GPIO8_2	VCC_LCD	GPIO10_2	GPIO12_2	N
P	VSS	VCC_APPS	VCC_APPS						VCC_MVT	GPIO7_2	GPIO61	GPIO6_2	GPIO62	P
R	VCC_APPS	VSS	VSS						GPIO57	GPIO60	GPIO59	VSS_CI	VCC_CI	R
T	VCC_APPS	VSS	VSS						GPIO53	GPIO58	GPIO56	VCC_APPS	VSS	T
U									GPIO51	GPIO52	VSS_CI	GPIO54	GPIO55	U
V									GPIO48	GPIO50	VCC_CI	VCC_APPS	VSS	V
W									GPIO43	VCC_IO4	GPIO45	GPIO10	GPIO49	W
Y									GPIO39	GPIO41	VSS_IO4	GPIO47	GPIO46	Y
AA									GPIO32	GPIO40	GPIO42	GPIO44	VSS	AA
AB	DF_IO14	GPIO7	GPIO11	GPIO12	VCC_IO3	GPIO16	GPIO19	VCC_CARD1	GPIO28	VSS_IO4	VCC_IO4	GPIO37	VCC_MVT	AB
AC	VCC_APPS	GPIO8	VCC_APPS	GPIO14	VSS_PLL	GPIO17	VCC_APPS	GPIO20	GPIO22	GPIO30	GPIO34	GPIO36	GPIO38	AC
AD	VSS	VCC_MVT	VSS	VSS	VSS	VCC_APPS	VSS_CARD1	VSS	GPIO25	GPIO27	GPIO31	GPIO33	GPIO35	AD
AE	GPIO6	VSS	VCC_APPS	VSS_IO3	VCC_PLL	VSS	GPIO18	VSS	GPIO24	VCC_CARD2	VSS_CARD2	GPIO29	NC	AE
AF	GPIO5	VCC_APPS	GPIO9	GPIO13	VCC_APPS	GPIO15	VCC_APPS	VCC_APPS	GPIO21	GPIO23	GPIO26	NC	NC	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

4.1.1.2 PXA322 Processor 15mm^2 Package on Package (POP) Bottom Ball Map

Figure 36 and Figure 37 show the bottom ball map for the bottom PXA322 processor POP package.

Figure 36: PXA322 Processor 15mm^2 POP Bottom Ball Map, Left Half

	1	2	3	4	5	6	7	8	9	10	11	
A	NC_A1	NC_A2	VSS_DF	RFU_A4	TDI	PWR_EN	TXTAL_IN	TXTAL_OUT	VSS_OSC13M	PWR_SDA	GPIO4_2	A
B	NC_B1	VCC_MEM	RFU_B3	VCC_DFCORE	DF_NCS1	VCC_USB	NRESET_IN	PWR_CAP0	VCC_DF	RFU_B10	RFU_B11	B
C	VSS_MEM	MD1	RFU_C3	VSS	USBOTG_P	CLK_TOUT	PWR_OUT	VSS_BBATT	VSS_BG	DF_CLE_NOE	GPIO2_2	C
D	VSS	MD0	VCC_MEM	RFU_D4	USBOTG_N	RFU_D6	NGPIO_RESET	DF_ALE_NWE1	CLK_POUT	TEST	VSS_IO1	D
E	MD3	MD2	VSS_USB	TCK	USBH1_N	USBH1_P	TMS	VCC_APPS	NBATT_FAULT	PXTAL_OUT	GPIO5_2	E
F	MD5	MD4	VCC_MVT	VCC_MVT	MA2	TDO	NTRST	VSS	PXTAL_IN	VCC_OSC13M	VCTCXO_EN	F
G	VCC_SRAM	VCC_SRAM	MD7	MA3	MD9	MD11	SYS_EN	PWR_CAP1	NRESET_OUT	VCC_BG	GPIO1_2	G
H	VSS_MEM	DQM1	NSDWE	MD15	MD13	EXT_WAKEUP1	RFU_H7	EXT_WAKEUP0	VCC_BBATT	GPIO127	PWR_SCL	H
J	MD6	DQS0	MA1	MA14	VSS	MA12	NSDCS1	MA0				J
K	DQM0	VSS_MEM	SDMA10	NSDCS0	VCC_MEM	MA6	MA4	GPIO119				K
L	RCOMP_DDR	MA11	VCC_MEM	NSDRAS	VCC_APPS	VCC_APPS	RFU_L7	VCC_MVT				L
M	VSS_MEM	DQS1	VCC_MEM	VSS	VCC_APPS	SDCLK1	VCC_MEM	GPIO4				M
N	MD10	VCC_MEM	VSS	VCC_MEM	MD17	VCC_APPS	VCC_APPS	MA13				N
P	VSS_MEM	VCC_MEM	VCC_MVT	VCC_MVT	VCC_APPS	DF_IO1	VSS_MEM	DF_NCS0	VCC_SRAM	DF_IO15	GPIO5	P
R	VSS_MEM	MD8	MD24	VSS_MEM	VSS_MEM	GPIO3	GPIO111	DF_IO14	GPIO109	GPIO7	VSS_LCD	R
T	VSS_MEM	MD12	DQM2	MD29	VCC_DF	NBE0	DF_ALE_NWE2	DF_NWE	DF_IO4	DF_IO3	DF_IO12	T
U	VSS	SDCKE	GPIO0	MD28	MD31	DF_NRE	DF_IO2	NLUA	DF_IO0	DF_IO5	VSS	U
V	VSS	VSS	GPIO2	GPIO1	NXCVREN	VCC_DF	VSS	DF_ADDR2	DF_IO8	DF_IO6	DF_IO9	V
W	DF_INT_RNB	MD14	MD22	DQM3	DF_SCLK_E	VSS_DF	DF_ADDR0	DF_ADDR1	MD27	DF_IO7	VSS	W
Y	NC_Y1	SDCLK0	MD16	MD26	MD18	NBE1	NC_Y7	DF_ADDR3	DF_IO11	VSS_DF	MD25	Y
AA	NC_AA1	NC_AA2	VCC_MEMCORE	MD19	MD30	MD20	MD21	NLLA	MD23	DQS2	DQS3	AA
	1	2	3	4	5	6	7	8	9	10	11	

Figure 37: PXA322 Processor 15mm^2 POP Bottom Ball Map, Right Half

	12	13	14	15	16	17	18	19	20	21	
A	GPIO0_2	GPIO126	GPIO120	GPIO116	TSI_XP_HV	GPIO108	GPIO104	VCC_SRAM	NC_A20	NC_A21	A
B	GPIO122	GPIO118	GPIO114	VCC_IO1	GPIO110	TSI_YP_HV	GPIO102	GPIO106	VSS_DF	NC_B21	B
C	VSS_PLL	GPIO124	TSI_YM_HV	GPIO112	GPIO105	GPIO100	GPIO99	GPIO103	DF_NWP	GPIO95	C
D	GPIO121	LOCK_PRE	VSS_TSI	GPIO107	GPIO88	GPIO90	GPIO101	GPIO97	GPIO87	GPIO96	D
E	VCC_TSI	GPIO125	VSS	VCC_IO6	GPIO94	VCC_MVT	GPIO91	VSS_IO6	GPIO93	GPIO92	E
F	VCC_PLL	GPIO3_2	VCC_SRAM	TSI_XM_HV	GPIO84	GPIO86	GPIO85	GPIO89	GPIO75	GPIO79	F
G	TESTCLK	GPIO123	GPIO117	GPIO76	GPIO78	VSS_MSL	GPIO83	VCC_MSL	GPIO81	GPIO77	G
H	GPIO113	GPIO115	GPIO80	GPIO16_2	GPIO14_2	GPIO74	GPIO73	GPIO17_2	GPIO71	GPIO15_2	H
J			GPIO70	GPIO68	GPIO72	GPIO66	GPIO65	GPIO67	GPIO69	VSS_LCD	J
K			GPIO98	GPIO9_2	GPIO82	GPIO64	VCC_LCD	GPIO63	VCC_LCD	GPIO61	K
L			GPIO7_2	GPIO60	GPIO62	GPIO13_2	GPIO11_2	GPIO10_2	GPIO8_2	GPIO12_2	L
M			GPIO52	VCC_CI	GPIO56	GPIO54	GPIO53	GPIO57	GPIO59	MA5	M
N			VCC_APPS	VCC_MVT	VSS_CI	GPIO58	MA15	GPIO55	GPIO6_2	MA7	N
P	GPIO9	GPIO14	GPIO10	GPIO50	GPIO45	VSS	GPIO47	GPIO49	GPIO48	VSS	P
R	VCC_PLL	DF_IO10	VSS_CARD1	GPIO43	GPIO41	VSS_IO4	GPIO46	GPIO44	GPIO42	GPIO51	R
T	VSS_IO3	GPIO16	DF_IO13	GPIO39	GPIO37	GPIO36	GPIO34	GPIO40	GPIO38	NSDCAS	T
U	GPIO31	GPIO12	GPIO17	GPIO20	GPIO29	GPIO35	VCC_IO4	GPIO28	GPIO30	MA9	U
V	VCC_APPS	GPIO11	VSS	VCC_APPS	GPIO27	GPIO22	GPIO33	VSS_CARD2	GPIO32	MA8	V
W	GPIO6	VCC_APPS	VSS_PLL	GPIO18	GPIO19	VCC_CARD2	GPIO25	GPIO24	ND_RST	VSS_MEM	W
Y	VSS_DF	GPIO13	GPIO15	VCC_APPS	VCC_APPS	GPIO23	VSS	RFU_Y19	RFU_Y20	NC_Y21	Y
AA	GPIO8	VCC_IO3	VCC_APPS	VCC_APPS	GPIO21	VCC_CARD1	VSS	GPIO26	NC_AA20	NC_AA21	AA
	12	13	14	15	16	17	18	19	20	21	

Figure 37: PXA322 Processor 15mm^2 POP Bottom Ball Map, Right Half

NOTES:
1. The LOCK_PRE ball (D13) connects directly to the A14 on the top package. Consult the datasheet for the top package memory device for appropriate requirements for this pin.
2. The DF_NWP ball (C20) connects directly to C21 and F22 on the top package. Consult the datasheet for the top package memory device for appropriate requirements for these pins.
3. The ND_RST ball (W20) connects directly to Y21 on the top package. Consult the datasheet for the top package memory device for appropriate requirements for these pins
4. The VCC_DF balls (V6, T5 and B9) connect to the VCC_DFQ balls (B9, B15, B21 and AB21) on the top package and are powered from the VCC_DF power domain. These balls are used for the IO voltage domain for the device connected to the Data Flash Interface (DFI).
5. The VCC_DFCORE ball (B4) is directly connected to the VCC_DF balls (B4, B20, AA3 and AA12) on the top package. A seperate power supply can be used for this ball in order to keep the core voltage on while the processor is in S3/D4/C4 power mode. If this is not needed for the device connected to the DFI bus connect this pin to the VCC_DF power domain.
6. The VCC_MEM balls (B2, D3, K5, L3, N2, N4, M3, M7 and P2) are connected to the VCC_MEMQ balls (E2, H2, M2, U2, AA5, AA8, AA15 and AA18) on the top package and are powered from the VCC_MEM power domain. These balls are used for the IO voltage domain for the DDR SDRAM.
7. The VCC_MEMCORE ball (AA3) is connected to the VCC_MEM balls (B2, J21, P2, AA21 and AB2) on the top package. A separate power supply can be used for this ball in order to keep the DDR SDRAM core voltage on while the processor is in S3/D4/C4 power mode. If power does not need to be supplied to the core voltage for the DDR SDRAM while the processor is in S3/D4/C4 connect this pin to the VCC_MEM power domain.

4.1.1.3 PXA322 15mm^2 Package-on-Package (PoP) Top Ball Map

Figure 38 and Figure 39 show the top ball map for the 416-ball bottom PXA322 processor POP package.

Figure 38: PXA322 Processor 15mm^2 PoP Top Ball Map, Left Side

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	VSS_MEM	DF_IO1	VSS_DF	DF_IO3	DF_IO5	DF_IO7	DF_IO9	VSS_DF	DF_CLE_NOE	DF_IO11	A
B	VSS_MEM	VCC_MEM	DF_IO0	VCC_DF	DF_IO2	DF_IO4	DF_IO6	DF_IO8	VCC_DFQ	DF_ALE_NWE1	DF_IO10	B
C	DF_NWE	DF_INT_RNB										C
D	MD1	MD0										D
E	VSS_MEM	VCC_MEMQ										E
F	MD3	MD2										F
G	MD5	MD4										G
H	VSS_MEM	VCC_MEMQ										H
J	MD7	MD6										J
K	DQM0	DQS0										K
L	DQM1	DQS1										L
M	VSS_MEM	VCC_MEMQ										M
N	MD9	MD8										N
P	VSS_MEM	VCC_MEM										P
R	MD11	MD10										R
T	MD13	MD12										T
U	VSS_MEM	VCC_MEMQ										U
V	MD15	MD14										V
W	SDCKE	SDCLK0										W
Y	NC	SDCLK1										Y
AA	NC	VSS_DF	VCC_DF	MD16	VCC_MEMQ	MD18	MD20	VCC_MEMQ	MD22	DQS2	DF_SCLK_S	AA
AB	NC	VCC_MEM	VSS_DF	MD17	VSS_MEM	MD19	MD21	VSS_MEM	MD23	DQM2	NC	AB
	1	2	3	4	5	6	7	8	9	10	11	

Figure 39: PXA322 Processor 15mm^2 PoP Top Ball Map, Right Side

	12	13	14	15	16	17	18	19	20	21	22	
A	DF_IO13	DF_IO15	LOCK_PRE	VSS_DF	NC	NC	NC	NC	NC	VSS_DF	NC	A
B	DF_IO12	DF_IO14	NC	VCC_DFQ	NC	NC	NC	NC	VCC_DF	VCC_DFQ	VSS_DF	B
C										DF_NWP	NC	C
D										GPIO3	GPIO4	D
E										DF_NCS0	DF_NCS1	E
F										DF_NRE	DF_NWP	F
G										DF_ALE_NWE1	NC	G
H										NSDWE	DF_CLE_NOE	H
J										VCC_MEM	VSS_MEM	J
K										MA0	MA1	K
L										MA2	MA3	L
M										MA4	MA5	M
N										MA6	MA7	N
P										MA14	MA15	P
R										NSDCS0	NSDCS1	R
T										NSDRAS	NSDCAS	T
U										MA8	MA9	U
V										SDMA10	MA11	V
W										MA12	MA13	W
Y										ND_RST	VSS_MEM	Y
AA	VCC_DF	DQS3	MD24	VCC_MEMQ	MD26	MD28	VCC_MEMQ	MD30	NLLA	VCC_MEM	NC	AA
AB	VSS_DF	DQM3	MD25	VSS_MEM	MD27	MD29	VSS_MEM	MD31	NC	VCC_DFQ	NC	AB
	12	13	14	15	16	17	18	19	20	21	22	

4.1.2 PXA31x Processor Ball Maps

4.1.2.1 PXA310 Processor 13mm^2 VF-BGA Ball Map

Figure 40 and Figure 41 show the bottom ball map for the PXA310 processor 13mm^2 discrete package. The balls highlighted in yellow have different functionality on the PXA30x processor.

Figure 40: PXA310 Processor 13mm^2 VF-BGA Ball Map, Left side

	1	2	3	4	5	6	7	8	9	10	11	12	
A	NC	NC	RFU_A3	VCC_BIAS	TCK	CLK_TOUT	PWR_CAP 0	NRESET_O UT	PXTAL_IN	PWR_SCL	VCC_IO1	GPIO1_2	A
B	NC	RFU_B2	RFU_B3	RFU_B4	TDI	NRESET	PWR_OUT	VCC_OSC1 3M	PXTAL_OU T	VCTCXO_E N	VSS_IO1	CLK_POUT	B
C	VSS_MEM	VSS_MEM	RFU_C3	TDO	PWR_EN	NBATT_FA ULT	TXTAL_IN	TXTAL_OU T	VCC_BG	VSS_OSC1 3M	VCC_PLL	GPIO127	C
D	MD0	VCC_MEM	TMS										D
E	MD1	MD2	VCC_MEM		NTRST	EXT_WAKE UP0	VSS	VCC_BBAT T	NGPIO_RE SET	TESTCLK	VCC_APPS	VSS	E
F	MD3	DQM0	VCC_MEM		VSS_MEM	SYS_EN	PWR_CAP 1	VSS_BBAT T	VCC_MVT	VSS_BG	PWR_SDA	GPIO125	F
G	MD4	MD5	DQS0		VCC_MEM	VSS_MEM							G
H	MD7	MA2	MD6		VSS_MEM	VCC_MVT		VSS	VSS	VCC_APPS	VSS	TEST	H
J	MA6	MA15	MA14		VCC_MEM	VSS_MEM		VSS					J
K	SDMA10	MA8	MA4		VCC_MEM	VSS_MEM		VCC_APPS					K
L	SDCLK0	SDCLK1	MA12		VCC_APPS	VSS_MEM		VSS					L
M	MA0	NSDCS1	NSDCS0		MA13	VSS		VSS					M
N	MA9	MA11	MA7		VCC_MEM	VSS_MEM		VSS					N
P	RCOMP_D DR	NSDRAS	MA5		MA3	VCC_MVT		VSS					P
R	RFU_R1	SDCKE	NSDWE		MA1	VSS_MEM		VCC_APPS					R
T	MD9	MD8	NSDCAS		VCC_MEM	VSS_MEM		VSS					T
U	DQM1	MD11	MD10		VSS	VCC_MVT		VSS	VSS	VCC_APPS	VSS	VSS	U
V	MD13	MD12	DQS1		VCC_MEM	VSS_MEM							V
W	GPIO0	MD14	MD15		NC	DF_CLE_N OE	NC	NC	NC	DF_NCS0	VCC_SRA M	NC	W
Y	GPIO2	VCC_MEM	VSS_MEM		VSS_DF	VCC_DF	DF_IO0	VSS_DF	NC	VSS_DF	VSS_DF	DF_IO7	Y
AA	NCS1	GPIO1	DF_INT_R NB										AA
AB	NCS0	DF_NWE	DF_NRE	VCC_DF	DF_ADDR1	NC	VCC_DF	DF_IO9	DF_IO3	VCC_DF	NLLA	DF_IO13	AB
AC	NC	DF_ALE_N WE	NBE1	DF_ADDR0	DF_ADDR3	NC	DF_IO1	VCC_MVT	VCC_APPS	VSS	DF_SCLK_ E	VCC_DF	AC
AD	NC	NC	NBE0	DF_ADDR2	DF_IO8	DF_IO2	DF_IO10	VSS	DF_IO11	NLUA	RFU_AD11	DF_IO4	AD
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 41: PXA310 Processor 13mm^2 VF-BGA Ball Map, Right side

	13	14	15	16	17	18	19	20	21	22	23	24	
A	GPIO0_2	GPIO126	GPIO115	GPIO116	GPIO107	VSS_IO1	GPIO110	GPIO102	GPIO100	GPIO97	NC	NC	A
B	GPIO123	GPIO119	GPIO113	GPIO99	VCC_APPS	VCC_MVT	GPIO101	GPIO106	VCC_SRAM	VSS_IO1	GPIO96	NC	B
C	VSS_PLL	VCC_APPS	GPIO118	VCC_IO1	VSS	GPIO108	GPIO104	GPIO103	VCC_MVT	GPIO92	GPIO94	GPIO98	C
D										GPIO91	GPIO90	GPIO95	D
E	GPIO121	GPIO117	GPIO111	GPIO114	NC	GPIO9_2	NC	GPIO7_2		GPIO88	GPIO87	GPIO93	E
F	GPIO124	GPIO122	GPIO120	GPIO109	GPIO105	GPIO10_2	GPIO8_2	GPIO84		GPIO85	GPIO83	VCC_IO1	F
G							GPIO75	VSS_MSL		GPIO82	GPIO81	GPIO89	G
H	VSS	VSS	VCC_APPS	GPIO112	VSS		GPIO71	VCC_MSL		GPIO77	GPIO80	GPIO86	H
J					VSS		GPIO63	GPIO79		GPIO74	GPIO76	GPIO78	J
K					VCC_APPS		VCC_LCD	GPIO69		GPIO66	GPIO72	GPIO73	K
L					VSS		GPIO60	GPIO68		GPIO65	GPIO67	GPIO70	L
M					VSS		GPIO59	VSS_LCD		GPIO61	GPIO62	GPIO64	M
N					ULPI_DIR		VCC_MVT	GPIO52		GPIO55	GPIO57	GPIO51	N
P					ULPI_NXT		GPIO58	GPIO49		GPIO47	GPIO54	GPIO56	P
R					VCC_APPS		GPIO48	GPIO45		VCC_CI	GPIO53	GPIO50	R
T					GPIO46		VSS_CI	GPIO44		GPIO42	VSS	VCC_APPS	T
U	VSS	VSS	VCC_APPS	VSS	ULPI_STP		GPIO39	VSS_ULPI		GPIO38	GPIO41	GPIO43	U
V							GPIO37	GPIO35		VCC_ULPI	GPIO36	GPIO40	V
W	DF_IO12	VSS_DF	GPIO2_2	VCC_MVT	GPIO18	GPIO33	GPIO27	GPIO3_2		GPIO31	GPIO32	GPIO34	W
Y	VSS_DF	DF_IO14	VSS_CARD1	GPIO8	GPIO15	GPIO4_2	GPIO6_2	GPIO5_2		GPIO21	GPIO28	GPIO29	Y
AA										GPIO30	GPIO25	GPIO26	AA
AB	VCC_DF	GPIO3	GPIO5	VCC_APPS	GPIO7	GPIO10	GPIO11	VCC_IO3	GPIO19	GPIO23	GPIO20	VSS_IO3	AB
AC	DF_NCS1	GPIO4	VCC_CARD1	VSS	VSS	VSS_CARD2	GPIO13	GPIO12	GPIO17	VCC_PLL	GPIO22	NC	AC
AD	DF_IO5	DF_IO6	DF_IO15	GPIO9	GPIO6	VCC_CARD2	GPIO16	GPIO14	VSS_PLL	GPIO24	NC	NC	AD
	13	14	15	16	17	18	19	20	21	22	23	24	

4.1.2.2 PXA311 and PXA312 15mm^2 Multi-Chip Package (MCP) and Package on Package (POP) Bottom Ball Map.

Figure 42 and Figure 43 show the bottom ball map for the PXA31x processor 15mm^2 MCP and POP packages. The balls highlighted in yellow have different functionality on the PXA30x processor.

Figure 42: PXA31x Processor 15mm^2 MCP and Package-on-Package (PoP, Bottom) Ball Map, Left side

	1	2	3	4	5	6	7	8	9	10	11	
A	VSS	VSS	RFU_A3	RFU_A4	RFU_A5	NTRST	PWR_CAP0	TXTAL_IN	VSS	VCC_APPS	GPIO0_2	A
B	VSS	VSS	VCC_BIAS	NC	RFU_B5	CLK_TOUT	EXT_WAKEUP0	TXTAL_OUT	PXTAL_IN	PWR_SDA	TEST	B
C	NC	VSS	TMS	TCK	NC	NBATT_FAULT	PWR_OUT	VCC_BBATT	PXTAL_OUT	VSS_BG	CLK_POUT	C
D	MD0	TDO	PWR_EN	SYS_EN	VCC_MEM	NRESET	VSS	VSS_BBATT	VCC_OSC13M	VCC_BG	GPIO1_2	D
E	MD1	MD2	TDI	VCC_MVT	GPIO3_2	GPIO2_2	GPIO6_2	NGPIO_RESET	VSS_OSC13M	VCTCXO_EN	VSS_PLL	E
F	MD3	MD4	DQS0	VSS	GPIO5_2	VSS_MEM	VSS_MEM	PWR_CAP1	NRESET_OUT	PWR_SCL	TESTCLK	F
G	MD5	MD6	DQM0	NC	VCC_MEM	VCC_MEM	VSS_MEM	GPIO4_2	VCC_MVT	VCC_IO1	VCC_DF	G
H	MD7	MA14	MA2	MA4	MA13	VCC_MEM	VSS_MEM	VSS	VSS	VCC_APPS	VCC_APPS	H
J	MA8	NSDCS1	SDMA10	MA15	VCC_MVT	VCC_MEM	VSS_MEM	GPIO10_2				J
K	SDCLK0	SDCLK1	MA12	MA6	VSS	VCC_MEM	VSS_MEM	GPIO9_2				K
L	NSDCS0	MA9	MA0	NC	VCC_APPS	VCC_MEM	VSS_MEM	NC				L
M	MA3	MA7	MA5	MA11	VSS	VCC_MEM	VSS_MEM	NC				M
N	RCOMP_DDR	RFU_N2	NSDCAS	MA1	VCC_APPS	VCC_MEM	VSS_MEM	GPIO8_2				N
P	NSDWE	NSDRAS	MD8	NC	NC	VCC_MEM	VSS_MEM	GPIO7_2	VSS	VCC_APPS	VCC_APPS	P
R	MD10	SDCKE	MD9	DQS1	VSS	VCC_MEM	VSS_MEM	VSS	VSS_DF	VSS_DF	VSS_DF	R
T	MD12	MD11	MD14	DQM1	VCC_MVT	VCC_MEM	VSS_MEM	VSS	VCC_DF	VCC_DF	VCC_DF	T
U	MD15	MD13	NC	GPIO1	DF_NWP	VCC_MEM	VSS_MEM	DF_IO8	VCC_MVT	DF_NCS1	GPIO3	U
V	GPIO2	NC	GPIO0	NCS1	VCC_MEM	DF_ADDR1	DF_ALE_NWE	DF_CLE_NOE	DF_NCS0	DF_IO4	DF_IO7	V
W	NCS0	NC	DF_INT_RNB	DF_NWE	DF_NRE	DF_ADDR2	DF_IO2	DF_IO11	RFU_W9	DF_IO13	DF_IO14	W
Y	VSS_DF	VSS_DF	NBE0	DF_ADDR3	DF_IO9	DF_IO10	VSS	DF_IO3	NLUA	NLLA	VCC_CARD1	Y
AA	VSS_DF	VSS_DF	NBE1	DF_ADDR0	DF_IO0	DF_IO1	VCC_APPS	VCC_SRAM	VCC_APPS	DF_SCLK_E	GPIO4	AA
	1	2	3	4	5	6	7	8	9	10	11	

Figure 43: PXA31x Processor 15mm^2 MCP and Package-on-Package (PoP, Bottom) Ball Map, Right side

	12	13	14	15	16	17	18	19	20	21	
A	GPIO126	VCC_APPS	GPIO116	VCC_APPS	GPIO110	GPIO102	GPIO99	GPIO96	VSS	VSS	A
B	GPIO124	VSS	GPIO120	GPIO112	VSS	GPIO106	GPIO100	VCC_SRAM	VSS	VSS	B
C	GPIO127	GPIO115	GPIO122	GPIO113	GPIO107	GPIO108	VCC_SRAM	GPIO101	GPIO95	GPIO98	C
D	VCC_PLL	GPIO123	GPIO118	GPIO114	GPIO109	GPIO105	GPIO103	NC	GPIO97	GPIO94	D
E	VSS_PLL	GPIO119	GPIO117	VCC_IO1	GPIO86	GPIO89	GPIO91	GPIO104	GPIO93	GPIO92	E
F	GPIO125	GPIO121	GPIO111	VSS_IO1	GPIO79	VSS_MSL	GPIO87	GPIO85	GPIO88	GPIO90	F
G	VSS_DF	VSS_IO1	VCC_MVT	VCC_IO1	GPIO78	VCC_MSL	GPIO81	GPIO83	GPIO82	GPIO84	G
H	VCC_APPS	VSS	VSS	VCC_MVT	GPIO73	GPIO74	GPIO75	GPIO77	GPIO76	GPIO80	H
J			VSS	VCC_MVT	GPIO71	GPIO65	GPIO67	GPIO69	GPIO70	GPIO72	J
K			VCC_APPS	VSS_LCD	VCC_LCD	GPIO64	GPIO68	GPIO61	GPIO63	GPIO66	K
L			VCC_APPS	VSS_LCD	VCC_LCD	GPIO59	GPIO56	GPIO62	GPIO58	GPIO60	L
M			VCC_APPS	VSS_LCD	VCC_LCD	GPIO53	GPIO55	GPIO57	GPIO52	GPIO54	M
N			VSS	VCC_MVT	GPIO47	GPIO49	GPIO50	GPIO51	VSS	VCC_APPS	N
P	VCC_APPS	VSS	VSS	VCC_CI	GPIO43	GPIO45	GPIO46	VSS_CI	VCC_CI	GPIO48	P
R	VSS_DF	VSS_DF	VCC_MVT	VSS_ULPI	VCC_ULPI	GPIO37	GPIO39	GPIO42	GPIO41	GPIO44	R
T	VCC_DF	VCC_DF	VSS	VSS_IO3	VCC_IO3	GPIO38	GPIO35	GPIO40	GPIO34	GPIO36	T
U	GPIO9	DF_LOCKPRE	GPIO8	DF_IO12	GPIO12	GPIO19	GPIO31	GPIO33	GPIO32	GPIO28	U
V	GPIO5	GPIO6	GPIO11	GPIO13	GPIO16	ULPI_DIR	GPIO20	GPIO29	GPIO30	GPIO27	V
W	DF_IO6	DF_IO5	GPIO7	DF_IO15	VSS_PLL	GPIO17	GPIO18	GPIO21	ULPI_NXT	ULPI_STP	W
Y	VSS_CARD1	VCC_APPS	GPIO10	GPIO14	GPIO15	GPIO23	GPIO25	GPIO26	VSS_IO3	VSS_IO3	Y
AA	VCC_APPS	VSS	VCC_CARD2	VSS_CARD2	VCC_PLL	GPIO22	GPIO24	NC	VSS_IO3	VSS_IO3	AA
	12	13	14	15	16	17	18	19	20	21	

4.1.3 PXA30x Processor Ball Maps

4.1.3.1 PXA300 Processor 13mm^2 VF-BGA Ball

Figure 44 and Figure 45 show the bottom ball map for the PXA300 processor 13mm^2 discrete package. The balls highlighted in yellow have different functionality on the PXA31x processor.

Figure 44: PXA300 Processor 13mm^2 VF-BGA Ball Map, Left side

	1	2	3	4	5	6	7	8	9	10	11	12	
A	NC	NC	USBOTG_P	VCC_USB	TCK	CLK_TOUT	PWR_CAP0	NRESET_OUT	PXTAL_IN	PWR_SCL	VCC_IO1	GPIO1_2	A
B	NC	VSS_USB	USBOTG_N	USBH1_P	TDI	NRESET	PWR_OUT	VCC_OSC13M	PXTAL_OUT	VCTCXO_EN	VSS_IO1	CLK_POUT	B
C	VSS_MEM	VSS_MEM	USBH1_N	TDO	PWR_EN	NBATT_FAULT	TXTAL_IN	TXTAL_OUT	VCC_BG	VSS_OSC13M	VCC_PLL	GPIO127	C
D	MD0	VCC_MEM	TMS										D
E	MD1	MD2	VCC_MEM		NTRST	EXT_WAKEUP0	VSS	VCC_BBATT	NGPIO_RESET	TESTCLK	VCC_APPS	VSS	E
F	MD3	DQM0	VCC_MEM		VSS_MEM	SYS_EN	PWR_CAP1	VSS_BBATT	VCC_MVT	VSS_BG	PWR_SDA	GPIO125	F
G	MD4	MD5	DQS0		VCC_MEM	VSS_MEM							G
H	MD7	MA2	MD6		VSS_MEM	VCC_MVT		VSS	VSS	VCC_APPS	VSS	TEST	H
J	MA6	MA15	MA14		VCC_MEM	VSS_MEM		VSS					J
K	SDMA10	MA8	MA4		VCC_MEM	VSS_MEM		VCC_APPS					K
L	SDCLK0	SDCLK1	MA12		VCC_APPS	VSS_MEM		VSS					L
M	MA0	NSDCS1	NSDCS0		MA13	VSS		VSS					M
N	MA9	MA11	MA7		VCC_MEM	VSS_MEM		VSS					N
P	RCOMP_DDR	NSDRAS	MA5		MA3	VCC_MVT		VSS					P
R	RFU_R1	SDCKE	NSDWE		MA1	VSS_MEM		VCC_APPS					R
T	MD9	MD8	NSDCAS		VCC_MEM	VSS_MEM		VSS					T
U	DQM1	MD11	MD10		VSS	VCC_MVT		VSS	VSS	VCC_APPS	VSS	VSS	U
V	MD13	MD12	DQS1		VCC_MEM	VSS_MEM							V
W	GPIO0	MD14	MD15		NC	DF_CLE_NOE	NC	NC	NC	DF_NCS0	VCC_SRAM	NC	W
Y	GPIO2	VCC_MEM	VSS_MEM		VSS_DF	VCC_DF	DF_IO0	VSS_DF	NC	VSS_DF	VSS_DF	DF_IO7	Y
AA	NCS1	GPIO1	DF_INT_RNB										AA
AB	NCS0	DF_NWE	DF_NRE	VCC_DF	DF_ADDR1	NC	VCC_DF	DF_IO9	DF_IO3	VCC_DF	NLLA	DF_IO13	AB
AC	NC	DF_ALE_NWE	NBE1	DF_ADDR0	DF_ADDR3	NC	DF_IO1	VCC_MVT	VCC_APPS	VSS	DF_SCLK_E	VCC_DF	AC
AD	NC	NC	NBE0	DF_ADDR2	DF_IO8	DF_IO2	DF_IO10	VSS	DF_IO11	NLUA	RFU_AD11	DF_IO4	AD
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 45: PXA300 Processor 13mm^2 VF-BGA Ball Map, Right side

	13	14	15	16	17	18	19	20	21	22	23	24	
A	GPIO0_2	GPIO126	GPIO115	GPIO116	GPIO107	VSS_IO1	GPIO110	GPIO102	GPIO100	GPIO97	NC	NC	A
B	GPIO123	GPIO119	GPIO113	GPIO99	VCC_APPS	VCC_MVT	GPIO101	GPIO106	VCC_SRAM	VSS_IO1	GPIO96	NC	B
C	VSS_PLL	VCC_APPS	GPIO118	VCC_IO1	VSS	GPIO108	GPIO104	GPIO103	VCC_MVT	GPIO92	GPIO94	GPIO98	C
D										GPIO91	GPIO90	GPIO95	D
E	GPIO121	GPIO117	GPIO111	GPIO114	NC	RFU_E18	NC	RFU_E20		GPIO88	GPIO87	GPIO93	E
F	GPIO124	GPIO122	GPIO120	GPIO109	GPIO105	RFU_F18	RFU_F19	GPIO84		GPIO85	GPIO83	VCC_IO1	F
G							GPIO75	VSS_MSL		GPIO82	GPIO81	GPIO89	G
H	VSS	VSS	VCC_APPS	GPIO112	VSS		GPIO71	VCC_MSL		GPIO77	GPIO80	GPIO86	H
J					VSS		GPIO63	GPIO79		GPIO74	GPIO76	GPIO78	J
K					VCC_APPS		VCC_LCD	GPIO69		GPIO66	GPIO72	GPIO73	K
L					VSS		GPIO60	GPIO68		GPIO65	GPIO67	GPIO70	L
M					VSS		GPIO59	VSS_LCD		GPIO61	GPIO62	GPIO64	M
N					RFU_N17		VCC_MVT	GPIO52		GPIO55	GPIO57	GPIO51	N
P					RFU_P17		GPIO58	GPIO49		GPIO47	GPIO54	GPIO56	P
R					VCC_APPS		GPIO48	GPIO45		VCC_CI	GPIO53	GPIO50	R
T					GPIO46		VSS_CI	GPIO44		GPIO42	VSS	VCC_APPS	T
U	VSS	VSS	VCC_APPS	VSS	RFU_U17		GPIO39	VSS_IO3		GPIO38	GPIO41	GPIO43	U
V							GPIO37	GPIO35		VCC_IO3	GPIO36	GPIO40	V
W	DF_IO12	VSS_DF	GPIO2_2	VCC_MVT	GPIO18	GPIO33	GPIO27	GPIO3_2		GPIO31	GPIO32	GPIO34	W
Y	VSS_DF	DF_IO14	VSS_CARD1	GPIO8	GPIO15	GPIO4_2	GPIO6_2	GPIO5_2		GPIO21	GPIO28	GPIO29	Y
AA										GPIO30	GPIO25	GPIO26	AA
AB	VCC_DF	GPIO3	GPIO5	VCC_APPS	GPIO7	GPIO10	GPIO11	VCC_IO3	GPIO19	GPIO23	GPIO20	VSS_IO3	AB
AC	DF_NCS1	GPIO4	VCC_CARD1	VSS	VSS	VSS_CARD2	GPIO13	GPIO12	GPIO17	VCC_PLL	GPIO22	NC	AC
AD	DF_IO5	DF_IO6	DF_IO15	GPIO9	GPIO6	VCC_CARD2	GPIO16	GPIO14	VSS_PLL	GPIO24	NC	NC	AD
	13	14	15	16	17	18	19	20	21	22	23	24	

4.1.4 PXA30x Processor and PXA302 Processor 15mm^2 Multi-Chip Package (MCP) and Package on Package (POP) Bottom Ball Map

Figure 46 and Figure 47 show the bottom ball map for the PXA30x processor 15mm^2 MCP and POP packages.The balls highlighted in yellow have different functionality on the PXA31x processor.

Figure 46: PXA30x 15mm^2 MCP and Package-on-Package (PoP) Bottom Ball Map, Left side

	1	2	3	4	5	6	7	8	9	10	11	
A	VSS_USB	VSS_USB	USBOTG_N	USBOTG_P	USBH1_N	NTRST	PWR_CAP0	TXTAL_IN	VSS	VCC_APPS	GPIO0_2	A
B	VSS_USB	VSS_USB	VCC_USB	NC	USBH1_P	CLK_TOUT	EXT_WAKEUP0	TXTAL_OUT	PXTAL_IN	PWR_SDA	TEST	B
C	NC	VSS	TMS	TCK	NC	NBATT_FAULT	PWR_OUT	VCC_BBATT	PXTAL_OUT	VSS_BG	CLK_POUT	C
D	MD0	TDO	PWR_EN	SYS_EN	VCC_MEM	NRESET	VSS	VSS_BBATT	VCC_OSC13M	VCC_BG	GPIO1_2	D
E	MD1	MD2	TDI	VCC_MVT	GPIO3_2	GPIO2_2	GPIO6_2	NGPIO_RESET	VSS_OSC13M	VCTCXO_EN	VSS_PLL	E
F	MD3	MD4	DQS0	VSS	GPIO5_2	VSS_MEM	VSS_MEM	PWR_CAP1	NRESET_OUT	PWR_SCL	TESTCLK	F
G	MD5	MD6	DQM0	NC	VCC_MEM	VCC_MEM	VSS_MEM	GPIO4_2	VCC_MVT	VCC_IO1	VCC_DF	G
H	MD7	MA14	MA2	MA4	MA13	VCC_MEM	VSS_MEM	VSS	VSS	VCC_APPS	VCC_APPS	H
J	MA8	NSDCS1	SDMA10	MA15	VCC_MVT	VCC_MEM	VSS_MEM	RFU_J8				J
K	SDCLK0	SDCLK1	MA12	MA6	VSS	VCC_MEM	VSS_MEM	RFU_K8				K
L	NSDCS0	MA9	MA0	NC	VCC_APPS	VCC_MEM	VSS_MEM	NC				L
M	MA3	MA7	MA5	MA11	VSS	VCC_MEM	VSS_MEM	NC				M
N	RCOMP_DDR	RFU_N2	NSDCAS	MA1	VCC_APPS	VCC_MEM	VSS_MEM	RFU_N8				N
P	NSDWE	NSDRAS	MD8	NC	NC	VCC_MEM	VSS_MEM	RFU_P8	VSS	VCC_APPS	VCC_APPS	P
R	MD10	SDCKE	MD9	DQS1	VSS	VCC_MEM	VSS_MEM	VSS	VSS_DF	VSS_DF	VSS_DF	R
T	MD12	MD11	MD14	DQM1	VCC_MVT	VCC_MEM	VSS_MEM	VSS	VCC_DF	VCC_DF	VCC_DF	T
U	MD15	MD13	NC	GPIO1	DF_NWP	VCC_MEM	VSS_MEM	DF_IO8	VCC_MVT	DF_NCS1	GPIO3	U
V	GPIO2	NC	GPIO0	NCS1	VCC_MEM	DF_ADDR1	DF_ALE_NWE	DF_CLE_NOE	DF_NCS0	DF_IO4	DF_IO7	V
W	NCS0	NC	DF_INT_RNB	DF_NWE	DF_NRE	DF_ADDR2	DF_IO2	DF_IO11	RFU_W9	DF_IO13	DF_IO14	W
Y	VSS_DF	VSS_DF	NBE0	DF_ADDR3	DF_IO9	DF_IO10	VSS	DF_IO3	NLUA	NLLA	VCC_CARD1	Y
AA	VSS_DF	VSS_DF	NBE1	DF_ADDR0	DF_IO0	DF_IO1	VCC_APPS	VCC_SRAM	VCC_APPS	DF_SCLK_E	GPIO4	AA
	1	2	3	4	5	6	7	8	9	10	11	

Figure 47: PXA30x Processor 15mm^2 MCP and Package-on-Package (PoP, Bottom) Ball Map, Right side

	12	13	14	15	16	17	18	19	20	21	
A	GPIO126	VCC_APPS	GPIO116	VCC_APPS	GPIO110	GPIO102	GPIO99	GPIO96	VSS	VSS	A
B	GPIO124	VSS	GPIO120	GPIO112	VSS	GPIO106	GPIO100	VCC_SRAM	VSS	VSS	B
C	GPIO127	GPIO115	GPIO122	GPIO113	GPIO107	GPIO108	VCC_SRAM	GPIO101	GPIO95	GPIO98	C
D	VCC_PLL	GPIO123	GPIO118	GPIO114	GPIO109	GPIO105	GPIO103	NC	GPIO97	GPIO94	D
E	VSS_PLL	GPIO119	GPIO117	VCC_IO1	GPIO86	GPIO89	GPIO91	GPIO104	GPIO93	GPIO92	E
F	GPIO125	GPIO121	GPIO111	VSS_IO1	GPIO79	VSS_MSL	GPIO87	GPIO85	GPIO88	GPIO90	F
G	VSS_DF	VSS_IO1	VCC_MVT	VCC_IO1	GPIO78	VCC_MSL	GPIO81	GPIO83	GPIO82	GPIO84	G
H	VCC_APPS	VSS	VSS	VCC_MVT	GPIO73	GPIO74	GPIO75	GPIO77	GPIO76	GPIO80	H
J			VSS	VCC_MVT	GPIO71	GPIO65	GPIO67	GPIO69	GPIO70	GPIO72	J
K			VCC_APPS	VSS_LCD	VCC_LCD	GPIO64	GPIO68	GPIO61	GPIO63	GPIO66	K
L			VCC_APPS	VSS_LCD	VCC_LCD	GPIO59	GPIO56	GPIO62	GPIO58	GPIO60	L
M			VCC_APPS	VSS_LCD	VCC_LCD	GPIO53	GPIO55	GPIO57	GPIO52	GPIO54	M
N			VSS	VCC_MVT	GPIO47	GPIO49	GPIO50	GPIO51	VSS	VCC_APPS	N
P	VCC_APPS	VSS	VSS	VCC_CI	GPIO43	GPIO45	GPIO46	VSS_CI	VCC_CI	GPIO48	P
R	VSS_DF	VSS_DF	VCC_MVT	RFU_R15	RFU_R16	GPIO37	GPIO39	GPIO42	GPIO41	GPIO44	R
T	VCC_DF	VCC_DF	VSS	VSS_IO3	VCC_IO3	GPIO38	GPIO35	GPIO40	GPIO34	GPIO36	T
U	GPIO9	NC	GPIO8	DF_IO12	GPIO12	GPIO19	GPIO31	GPIO33	GPIO32	GPIO28	U
V	GPIO5	GPIO6	GPIO11	GPIO13	GPIO16	RFU_V17	GPIO20	GPIO29	GPIO30	GPIO27	V
W	DF_IO6	DF_IO5	GPIO7	DF_IO15	VSS_PLL	GPIO17	GPIO18	GPIO21	RFU_W20	RFU_W21	W
Y	VSS_CARD1	VCC_APPS	GPIO10	GPIO14	GPIO15	GPIO23	GPIO25	GPIO26	VSS_IO3	VSS_IO3	Y
AA	VCC_APPS	VSS	VCC_CARD2	VSS_CARD2	VCC_PLL	GPIO22	GPIO24	NC	VSS_IO3	VSS_IO3	AA
	12	13	14	15	16	17	18	19	20	21	

4.1.5 PXA303 Processor 19mm^2 VF-BGA Ball

Figure 48 and Figure 49 show the bottom ball map for the PXA303 processor 19mm^2 discrete package.

Figure 48: PXA303 Processor 19mm^2 VF-BGA Ball Map, Left side

	1	2	3	4	5	6	7	8	9	10	11	12	
A	NC	NC	USBH1_N	USBH1_P	NBATT_FAULT	PWR_CAP0	NGPIO_RESET	VCC_OSC13M	PWR_SCL	TEST	GPIO1_2	GPIO127	A
B	NC	NC	USBOTG_P	VCC_USB	SYS_EN	PWR_OUT	VSS_BBATT	PXTAL_IN	VCC_BG	TESTCLK	VCC_IO1	GPIO0_2	B
C	MD2	MD1	USBOTG_N	VSS_USB	NTRST	VSS	TXTAL_OUT	PXTAL_OUT	VSS_OSC13M	PWR_SDA	CLK_POUT	GPIO126	C
D	VCC_MEM	DQS0	MD0	TMS	TDO	CLK_TOUT	VCC_BBATT	TXTAL_IN	NRESET_OUT	VCC_MVT	VSS_BG	VSS_IO1	D
E	MD5	VSS_MEM	DQM0	PWR_EN	TDI	TCK	EXT_WAKEUP0	NRESET	PWR_CAP1	VSS	VCC_APPS	VCTCXO_EN	E
F	MD7	MD6	MD4	VSS_MEM	VSS_MEM								F
G	MA14	MA15	VCC_MEM	MD3	VCC_MEM								G
H	MA8	MA6	MA4	VSS_MEM	VCC_MVT								H
J	VCC_MEM	VSS_MEM	MA12	MA2	VSS				VSS	VSS	VSS	VSS	J
K	NSDCS0	NSDCS1	SDCLK0	SDCLK1	SDMA10				VSS	VSS	VSS	VSS	K
L	MA13	MA11	MA0	VCC_APPS	VSS				VSS	VSS	VSS	VSS	L
M	MA5	MA7	MA9	VSS_MEM	VCC_MEM				VSS	VSS	VSS	VSS	M
N	MA1	NSDRAS	NSDCAS	MA3	RCOMP_DDR				VSS	VSS	VSS	VSS	N
P	NSDWE	SDCKE	VCC_MVT	RFU	VSS_MEM				VSS	VSS	VSS	VSS	P
R	MD8	MD9	MD10	MD11	VCC_MEM				VSS	VSS	VSS	VSS	R
T	DQM1	DQS1	MD12	VSS_MEM	VCC_MEM								T
U	MD13	MD14	MD15	VSS_MEM	NCS1								U
V	GPIO0	GPIO1	GPIO2	VCC_DF	VSS_DF								V
W	NCS0	DF_INT_RNB	DF_NWE	DF_NRE	NBE0	VCC_DF	VSS_DF	VCC_DF	VCC_APPS	NC	VSS_DF	VSS	W
Y	DF_ADDR2	DF_ADDR1	DF_ALE_NWE	NBE1	DF_ADDR0	DF_ADDR3	DF_IO9	DF_IO10	VCC_SRAM	VSS	VCC_DF	VCC_APPS	Y
AA	DF_IO0	DF_IO8	DF_IO1	DF_IO2	NC	VSS	VCC_MVT	NLUA	DF_SCLK_E	DF_IO6	GPIO3	VCC_CARD1	AA
AB	NC	NC	DF_CLE_NOE	DF_IO11	DF_IO3	DF_NCS0	NLLA	DF_IO12	DF_IO7	DF_NCS1	GPIO5	VSS_CARD1	AB
AC	NC	NC	DF_IO4	DF_IO5	DF_IO13	DF_IO14	DF_IO15	GPIO4	GPIO6	GPIO7	GPIO9	GPIO10	AC
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 49: PXA303 Processor 19mm^2 VF-BGA Ball Map, Right side

	13	14	15	16	17	18	19	20	21	22	23	
A	GPIO125	GPIO122	GPIO120	GPIO115	GPIO112	GPIO109	GPIO106	GPIO102	GPIO101	NC	NC	A
B	GPIO124	GPIO121	GPIO117	GPIO114	GPIO110	GPIO108	GPIO103	GPIO100	RFU_B21	NC	NC	B
C	VCC_PLL	GPIO118	GPIO116	GPIO111	GPIO107	GPIO105	RFU_C19	RFU_C20	GPIO97	GPIO96	GPIO93	C
D	VSS_PLL	GPIO123	GPIO119	VSS_IO1	GPIO104	RFU_D18	VCC_SRAM	GPIO98	GPIO95	GPIO92	GPIO90	D
E	VSS	VCC_APPS	GPIO113	VCC_IO1	VCC_MVT	GPIO99	VSS_IO1	GPIO94	GPIO91	GPIO87	GPIO86	E
F							VCC_IO1	GPIO89	GPIO88	GPIO85	GPIO83	F
G							VSS	VCC_MVT	GPIO84	GPIO81	GPIO80	G
H							VSS_MSL	VCC_MSL	GPIO82	GPIO78	GPIO77	H
J	VSS	VSS	VSS				GPIO75	GPIO79	GPIO76	GPIO74	GPIO73	J
K	VSS	VSS	VSS				VCC_LCD	VSS_LCD	GPIO71	GPIO72	GPIO70	K
L	VSS	VSS	VSS				GPIO69	GPIO67	GPIO65	GPIO68	GPIO66	L
M	VSS	VSS	VSS				VCC_LCD	VSS_LCD	GPIO63	GPIO64	GPIO62	M
N	VSS	VSS	VSS				GPIO57	GPIO54	GPIO59	GPIO60	GPIO61	N
P	VSS	VSS	VSS				VCC_MVT	GPIO52	GPIO55	GPIO56	GPIO58	P
R	VSS	VSS	VSS				VCC_CI	VCC_APPS	GPIO50	GPIO51	GPIO53	R
T							VSS_CI	GPIO41	GPIO47	GPIO48	GPIO49	T
U							GPIO27	VSS_IO3	GPIO44	GPIO45	GPIO46	U
V							NC	NC	GPIO36	GPIO42	GPIO43	V
W	VCC_APPS	VCC_MVT	VSS_PLL	VCC_PLL	GPIO25	GPIO6_2	NC	GPIO30	VCC_IO3	GPIO39	GPIO40	W
Y	VSS	VCC_CARD2	GPIO15	GPIO19	GPIO24	GPIO4_2	NC	NC	GPIO31	GPIO37	GPIO38	Y
AA	GPIO8	VSS_CARD1	GPIO16	VCC_IO3	GPIO23	GPIO3_2	NC	NC	GPIO33	GPIO34	GPIO35	AA
AB	GPIO11	GPIO13	GPIO18	VSS_IO3	GPIO22	GPIO2_2	NC	NC	GPIO32	NC	NC	AB
AC	GPIO12	GPIO14	GPIO17	GPIO20	GPIO21	GPIO26	GPIO5_2	GPIO28	GPIO29	NC	NC	AC
	13	14	15	16	17	18	19	20	21	22	23	

4.1.6 PXA312 and PXA302 Package on Package (POP) Top Ball Maps

4.1.6.1 PXA312 and PXA302 Processor 15mm^2 Package-on-Package (PoP) Top Ball Map

Figure 50: PXA302 Processor and PXA312 Processor PoP Top Ball Map, Left Side

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	VSS_MEM	NC	VSS_DF	NC	NC	NC	NC	VSS_DF	DF_CLE_NOE	NC	A
B	VSS_MEM	VCC_MEM	NC	VCC_DF	NC	NC	NC	NC	VCC_DF	DF_ALE_NWE	NC	B
C	DF_NWE	DF_INT_RNB										C
D	MD1	MD0										D
E	VSS_MEM	VCC_MEM										E
F	MD3	MD2										F
G	MD5	MD4										G
H	VSS_MEM	VCC_MEM										H
J	MD7	MD6										J
K	DQM0	DQS0										K
L	DQM1	DQS1										L
M	VSS_MEM	VCC_MEM										M
N	MD9	MD8										N
P	VSS_MEM	VCC_MEM										P
R	MD11	MD10										R
T	MD13	MD12										T
U	VSS_MEM	VCC_MEM										U
V	MD15	MD14										V
W	SDCKE	SDCLK0										W
Y	NC	SDCLK1										Y
AA	NC	VSS_DF	VCC_DF	DF_IO0	VCC_DF	DF_IO2	DF_IO4	VCC_DF	DF_IO6	NC	DF_SCLK_E	AA
AB	NC	VCC_MEM	VSS_DF	DF_IO1	VSS_DF	DF_IO3	DF_IO5	VSS_DF	DF_IO7	NC	NC	AB
	1	2	3	4	5	6	7	8	9	10	11	

Figure 51: PXA302 Processor and PXA312 Processor PoP Top Ball Map, Right Side

	12	13	14	15	16	17	18	19	20	21	22	
A	NC	NC	NC	VSS_DF	NC	NC	NC	NC	NC	VSS_DF	NC	A
B	NC	NC	NC	VCC_DF	NC	NC	NC	NC	VCC_DF	VCC_DF	VSS_DF	B
C										DF_NWP	NC	C
D										GPIO1	GPIO2	D
E										DF_NCS0	DF_NCS1	E
F										DF_NRE	DF_NWP	F
G										DF_ALE_NWE	NC	G
H										NSDWE	DF_CLE_NOE	H
J										VCC_MEM	VSS_MEM	J
K										MA0	MA1	K
L										MA2	MA3	L
M										MA4	MA5	M
N										MA6	MA7	N
P										MA14	MA15	P
R										NSDCS0	NSDCS1	R
T										NSDRAS	NSDCAS	T
U										MA8	MA9	U
V										SDMA10	MA11	V
W										MA12	MA13	W
Y										NC	VSS_MEM	Y
AA	VCC_DF	NC	DF_IO8	VCC_DF	DF_IO10	DF_IO12	VCC_DF	DF_IO14	NLLA	VCC_MEM	NC	AA
AB	VSS_DF	NC	DF_IO9	VSS_DF	DF_IO11	DF_IO13	VSS_DF	DF_IO15	NC	VCC_DF	NC	AB
	12	13	14	15	16	17	18	19	20	21	22	

NOTE: The DF_nWP signal is used as a write-protect pin for packages that use NAND devices (F22) and as a reset signal for packages that use a Static Memory Controller (SMC) device on GPIO1 (nCS2) (C21). The DF_nWP signal on the bottom package must be connected to either an external reset circuit or tied accordingly for write protection of the NAND device. When making connections to the DF_nWP pin, hardware must ensure the proper voltage levels are used for the voltage requirements on the top package. For example, when connecting nRESET_OUT (3V) to DF_nWP as a reset for a OneNAND device (1.8V), a level shifter must be used to reduce the voltage.

4.2 Pin Use Tables

These tables include the ball number, ball name, and type for each of pins. See Table 12 to decode the pin “Type”. Also included is the state of each pin with respect to reset and power modes. Additionally, at the beginning of each group of pins is the power domain that powers all the pins in that group. For example, the VCC_BATT group of pins in Table 11 starts with ball C6 and ends with C8. The next group of pins are on the VCC_IO1 domain.

Each multi-function pin (MFP) signal alternate function inputs and outputs are shown in the *PXA3xx Processor Family Vol. I: System and Timer Configuration Developers Manual*, “Pin Description and Control” chapter.

4.2.1 PXA32x Processor Pin Use

Table 9 lists the mapping of signals to specific PXA32x processor package pins.

Table 9: PXA32x Processor Pin Usage Summary

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
VCC_BBATT							
C6	C6	CLK_TOUT	CLK_TOUT	OC	Clk-Out	4	4
H8	G5	EXT_WAKEUP0	EXT_WAKEUP0	ICOCZ	Pd-0[11]	Pd-0[11]	Pd-0[11]
H6	F5	EXT_WAKEUP1	EXT_WAKEUP1	ICOCZ	Pu-1[11]	Pu-1[11]	Pu-1[11]
E9	B7	NBATT_FAULT	nBATT_FAULT	IC	Input	Input	Input
D7	A11	NGPIO_RESET	nGPIO_RESET	IC	Pu-1[11]	Pu-1[11]	Pu-1[11]
B7	E6	NRESET	nRESET	IC	Input[7]	Input	Input
G9	C9	NRESET_OUT	nRESET_OUT	OC	Low	12	12
F7	D6	NTRST	nTRST	IC	Input[7]	Input[7]	Input[7]
B8	D7	PWR_CAP0	PWR_CAP0	OA	-	-	-
G8	C7	PWR_CAP1	PWR_CAP1	OA	-	-	-
A6	A7	PWR_EN	PWR_EN	OC	Low	Low	Low
C7	B8	PWR_OUT	PWR_OUT	OA	-	-	-
G7	E5	SYS_EN	SYS_EN	OC	Low	Low	High
E4	B4	TCK	TCK	IC	Input	Input	Input
A5	B6	TDI	TDI	IC	Input[7]	Input[7]	Input[7]
F6	D5	TDO	TDO	OCZ	Hi-Z	Hi-Z	Hi-Z
E7	A8	TMS	TMS	IC	Input[7]	Input[7]	Input[7]
A7	D8	TXTAL_IN	TXTAL_IN	IA	2	2	2
A8	C8	TXTAL_OUT	TXTAL_OUT	OA	2	2	2
VCC_MVT							
F9	B10	PXTAL_IN	PXTAL_IN	IA	2	2	2

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
E10	C10	PXTAL_OUT	PXTAL_OUT	OA	2	2	2
VCC_IO1							
D9	D11	CLK_POUT	CLK_POUT	OC	Low	Float	Low
H12	B18	GPIO113	GPIO113	ICOCZ	Pd-0[1]	Float[1]	3
B14	A17	GPIO114	GPIO114	ICOCZ	Pd-0[1]	Float[1]	3
H13	C17	GPIO115	GPIO115	ICOCZ	Pd-0[1]	Float[1]	3
A15	D17	GPIO116	GPIO116	ICOCZ	Pd-0[1]	Float[1]	3
G14	E16	GPIO117	GPIO117	ICOCZ	Pd-0[1]	Float[1]	3
B13	C16	GPIO118	GPIO118	ICOCZ	Pd-0[1]	Float[1]	3
K8	B17	GPIO119	GPIO119	ICOCZ	Pd-0[1]	Float[1]	3
A14	E14	GPIO120	GPIO120	ICOCZ	Pd-0[1]	Float[1]	3
D12	B16	GPIO121	GPIO121	ICOCZ	Pd-0[1]	Float[1]	3
B12	C15	GPIO122	GPIO122	ICOCZ	Pd-0[1]	Float[1]	3
G13	A16	GPIO123	GPIO123	ICOCZ	Pd-0[1]	Float[1]	3
C13	D14	GPIO124	GPIO124	ICOCZ	Pd-0[1]	Float[1]	3
E13	E13	GPIO125	GPIO125	ICOCZ	Pd-0[1]	Float[1]	3
A13	A15	GPIO126	GPIO126	ICOCZ	Pd-0[1]]	Float[1]	3
H10	D13	GPIO127	GPIO127	ICOCZ	Pd-0[1]	Float[1]	3
A12	E12	GPIO0_2	GPIO0_2	ICOCZ	Pu-1[1]	Float[1]	3
G11	B14	GPIO1_2	GPIO1_2	ICOCZ	Pu-1[1]	Float[1]	3
C11	C13	GPIO2_2	GPIO2_2	ICOCZ	Pd-0[1]	Float[1]	3
F13	A14	GPIO3_2	GPIO3_2	ICOCZ	Pd-0[1]	Float[1]	3
A11	B13	GPIO4_2	GPIO4_2	ICOCZ	Pd-0[1]	Float[1]	3
E11	D12	GPIO5_2	GPIO5_2	ICOCZ	Pd-0[1]	Float[1]	3
H11	C11	PWR_SCL	PWR_SCL	ICOCZ	Pu-1[11]	Pu-1[11]	Float[1]
A10	A12	PWR_SDA	PWR_SDA	ICOCZ	Pu-1[11]	Pu-1[11]	Float[1]
D10	A13	TEST	TEST	IC	Input [5]	Input[5]	Input[5]
G12	C12	TESTCLK	TESTCLK	IC	Input[5]	Input [5]	Input[5]

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
F11	B12	VCTCXO_EN	VCTCXO_EN	OC	Low	Float	Low
VCC_DF							
W7	AC8	DF_ADDR0	DF_ADDR0	OCZ	Pd-0[1]	Float[1]	3
W8	AD8	DF_ADDR1	DF_ADDR1	OCZ	Pd-0[1]	Float[1]	3
V8	AF8	DF_ADDR2	DF_ADDR2	OCZ	Pd-0[1]	Float[1]	3
Y8	AE9	DF_ADDR3	DF_ADDR3	OCZ	Pd-0[1]	Float[1]	3
W1	AE5	DF_INT_RNB	DF_RnB	ICZ	Pu-1[1]	Float[1]	3
U9	AD9	DF_IO0	DF_IO0	ICOCZ	Pd-0[1]	Float[1]	3
P6	AC11	DF_IO1	DF_IO1	ICOCZ	Pd-0[1]	Float[1]	3
U7	AD10	DF_IO2	DF_IO2	ICOCZ	Pd-0[1]	Float[1]	3
T10	AF10	DF_IO3	DF_IO3	ICOCZ	Pd-0[1]	Float[1]	3
T9	AC12	DF_IO4	DF_IO4	ICOCZ	Pd-0[1]	Float[1]	3
U10	AF12	DF_IO5	DF_IO5	ICOCZ	Pd-0[1]	Float[1]	3
V10	AE12	DF_IO6	DF_IO6	ICOCZ	Pd-0[1]	Float[1]	3
W10	AF13	DF_IO7	DF_IO7	ICOCZ	Pd-0[1]	Float[1]	3
V9	AB10	DF_IO8	DF_IO8	ICOCZ	Pd-0[1]	Float[1]	3
V11	AF9	DF_IO9	DF_IO9	ICOCZ	Pd-0[1]	Float[1]	3
R13	AE10	DF_IO10	DF_IO10	ICOCZ	Pd-0[1]	Float[1]	3
Y9	AD11	DF_IO11	DF_IO11	ICOCZ	Pd-0[1]	Float[1]	3
T11	AB13	DF_IO12	DF_IO12	ICOCZ	Pd-0[1]	Float[1]	3
T14	AD12	DF_IO13	DF_IO13	ICOCZ	Pd-0[1]	Float[1]	3
R8	AB14	DF_IO14	DF_IO14	ICOCZ	Pd-0[1]	Float[1]	3
P10	AC13	DF_IO15	DF_IO15	ICOCZ	Pd-0[1]	Float[1]	3
D8	AF3	DF_ALE_NWE1	DF_ALE	OCZ	Pu-1[1]	Float[1]	3
T7	AB6	DF_ALE_NWE2	DF_ALE	OCZ	Pu-1[1]	Float[1]	3
P8	AE6	DF_NCS0	DF_nCS0	OCZ	Pu-1[1]	Float[1]	3
B5	AF6	DF_NCS1	DF_nCS1	OCZ	Pu-1[1]	Float[1]	3
U6	AD7	DF_NRE	DF_nOE	OCZ	Pu-1[1]	Float[1]	3

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
T8	AF7	DF_NWE	DF_nWE	OCZ	Pu-1[1]	Float[1]	3
W5	AF4	DF_SCLK_E	DF_SCLK_E	OCZ	Pd-0[1]	Float[1]	3
V3	AC2	GPIO2	GPIO2	ICOCZ	Pd-0[1]	Float[1]	3
R6	AD2	GPIO3	GPIO3	ICOCZ	Pu-1[1]	Float[1]	3
M8	AD3	GPIO4	GPIO4	ICOCZ	Pu-1[1]	Float[1]	3
P11	AF14	GPIO5	GPIO5	ICOCZ	Pu-1[1]	Float[1]	3
W12	AE14	GPIO6	GPIO6	ICOCZ	Pu-1[1]	Float[1]	3
R10	AB15	GPIO7	GPIO7	ICOCZ	Pu-1[1]	Float[1]	3
AA12	AC15	GPIO8	GPIO8	ICOCZ	Pu-1[1]	Float[1]	3
T6	AE4	NBE0	nBE0	OCZ	Pu-1[1]	Float[1]	3
Y6	AF5	NBE1	nBE1	OCZ	Pu-1[1]	Float[1]	3
C10	AD5	DF_CLE_NOE	ND_CLE	OCZ	Pu-1[1]	Float[1]	3
AA8	AE8	NLLA	nLLA	OCZ	Pu-1[1]	Float[1]	3
U8	AE7	NLUA	nLUA	OCZ	Pu-1[1]	Float[1]	3
V5	AE3	NXCVREN	NXCVREN	OCZ	Pu-1[1]	Float[1]	3
VCC_IO3							
P12	AF16	GPIO9	GPIO9	ICOCZ	Pu-1[1]	Float[1]	3
V13	AB16	GPIO11	GPIO11	ICOCZ	Pd-0[1]	Float[1]	3
U13	AB17	GPIO12	GPIO12	ICOCZ	Pd-0[1]	Float[1]	3
Y13	AF17	GPIO13	GPIO13	ICOCZ	Pd-0[1]	Float[1]	3
P13	AC17	GPIO14	GPIO14	ICOCZ	Pu-1[1]	Float[1]	3
Y14	AF19	GPIO15	GPIO15	ICOCZ	Pu-1[1]	Float[1]	3
T13	AB19	GPIO16	GPIO16	ICOCZ	Pu-1[1]	Float[1]	3
U14	AC19	GPIO17	GPIO17	ICOCZ	Pu-1[1]	Float[1]	3
VCC_IO4							
P14	W25	GPIO10	GPIO10	ICOCZ	Pd-0[1]	Float[1]	3
U20	AC23	GPIO30	GPIO30	ICOCZ	Pd-0[1]	Float[1]	3
U12	AD24	GPIO31	GPIO31	ICOCZ	Pd-0[1]	Float[1]	3

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
V20	AA22	GPIO32	GPIO32	ICOCZ	Pu-1[1]	Float[1]	3
V18	AD25	GPIO33	GPIO33	ICOCZ	Pu-1[1]	Float[1]	3
T18	AC24	GPIO34	GPIO34	ICOCZ	Pd-0[1]	Float[1]	3
U17	AD26	GPIO35	GPIO35	ICOCZ	Pd-0[1]	Float[1]	3
T17	AC25	GPIO36	GPIO36	ICOCZ	Pd-0[1]	Float[1]	3
T16	AB25	GPIO37	GPIO37	ICOCZ	Pd-0[1]	Float[1]	3
T20	AC26	GPIO38	GPIO38	ICOCZ	Pd-0[1]	Float[1]	3
T15	Y22	GPIO39	GPIO39	ICOCZ	Pd-0[1]	Float[1]	3
T19	AA23	GPIO40	GPIO40	ICOCZ	Pu-1[1]	Float[1]	3
R16	Y23	GPIO41	GPIO41	ICOCZ	Pd-0[1]	Float[1]	3
R20	AA24	GPIO42	GPIO42	ICOCZ	Pd-0[1]	Float[1]	3
R15	W22	GPIO43	GPIO43	ICOCZ	Pu-1[1]	Float[1]	3
R19	AA25	GPIO44	GPIO44	ICOCZ	Pu-1[1]	Float[1]	3
P16	W24	GPIO45	GPIO45	ICOCZ	Pu-1[1]	Float[1]	3
R18	Y26	GPIO46	GPIO46	ICOCZ	Pu-1[1]	Float[1]	3
P18	Y25	GPIO47	GPIO47	ICOCZ	Pu-1[1]	Float[1]	3
P20	V22	GPIO48	GPIO48	ICOCZ	Pu-1[1]	Float[1]	3
	VCC_CI						
P19	W26	GPIO49	GPIO49	ICOCZ	Pd-0[1]	Float[1]	3
P15	V23	GPIO50	GPIO50	ICOCZ	Pd-0[1]	Float[1]	3
R21	U22	GPIO51	GPIO51	ICOCZ	Pd-0[1]	Float[1]	3
M14	U23	GPIO52	GPIO52	ICOCZ	Pd-0[1]	Float[1]	3
M18	T22	GPIO53	GPIO53	ICOCZ	Pd-0[1]	Float[1]	3
M17	U25	GPIO54	GPIO54	ICOCZ	Pd-0[1]	Float[1]	3
N19	U26	GPIO55	GPIO55	ICOCZ	Pd-0[1]	Float[1]	3
M16	T24	GPIO56	CIF_DD7	ICOCZ	Pd-0[1]	Float[1]	3
M19	R22	GPIO57	GPIO57	ICOCZ	Pd-0[1]	Float[1]	3
N17	T23	GPIO58	GPIO58	ICOCZ	Pd-0[1]	Float[1]	3

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
M20	R24	GPIO59	CIF_MCLK	ICOCZ	Pd-0[1]	Float[1]	3
L15	R23	GPIO60	CIF_PCLK	ICZ	Pd-0[1]	Float[1]	3
K21	P24	GPIO61	CIF_HSYNC	ICOCZ	Pd-0[1]	Float[1]	3
L16	P26	GPIO62	CIF_VSYNC	ICOCZ	Pd-0[1]	Float[1]	3
	VCC_IO6						
G18	F22	GPIO83	GPIO83	ICOCZ	Pd-0[1]	Float[1]	3
F16	D26	GPIO84	GPIO84	ICOCZ	Pd-0[1]	Float[1]	3
F18	E23	GPIO85	GPIO85	ICOCZ	Pd-0[1]	Float[1]	3
F17	E24	GPIO86	GPIO86	ICOCZ	Pd-0[1]	Float[1]	3
D20	D22	GPIO87	GPIO87	ICOCZ	Pu-1[1]	Float[1]	3
D16	C25	GPIO88	GPIO88	ICOCZ	Pu-1[1]	Float[1]	3
F19	D25	GPIO89	GPIO89	ICOCZ	Pu-1[1]	Float[1]	3
D17	C26	GPIO90	GPIO90	ICOCZ	Pu-1[1]	Float[1]	3
E18	D24	GPIO91	GPIO91	ICOCZ	Pd-0[1]	Float[1]	3
E21	D23	GPIO92	GPIO92	ICOCZ	Pd-0[1]	Float[1]	3
E20	D21	GPIO93	GPIO93	ICOCZ	Pd-0[1]	Float[1]	3
E16	B23	GPIO94	GPIO94	ICOCZ	Pd-0[1]	Float[1]	3
C21	C23	GPIO95	GPIO95	ICOCZ	Pd-0[1]	Float[1]	3
D21	C24	GPIO96	GPIO96	ICOCZ	Pd-0[1]	Float[1]	3
D19	B25	GPIO97	GPIO97	ICOCZ	Pd-0[1]	Float[1]	3
K14	B24	GPIO98	GPIO98	ICOCZ	Pd-0[1]	Float[1]	3
C18	A24	GPIO99	GPIO99	ICOCZ	Pu-1[1]	Float[1]	3
C17	A23	GPIO100	GPIO100	ICOCZ	Pu-1[1]	Float[1]	3
D18	A22	GPIO101	GPIO101	ICOCZ	Pu-1[1]	Float[1]	3
B18	A21	GPIO102	GPIO102	ICOCZ	Pu-1[1]	Float[1]	3
C19	B21	GPIO103	GPIO103	ICOCZ	Pu-1[1]	Float[1]	3
A18	E22	GPIO104	GPIO104	ICOCZ	Pu-1[1]	Float[1]	3
C16	C21	GPIO105	GPIO105	ICOCZ	Pu-1[1]	Float[1]	3

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
B19	A20	GPIO106	GPIO106	ICOCZ	Pu-1[1]	Float[1]	3
D15	B20	GPIO107	GPIO107	ICOCZ	Pd-0[1]	Float[1]	3
A17	E21	GPIO108	GPIO108	ICOCZ	Pd-0[1]	Float[1]	3
R9	A19	GPIO109	GPIO109	ICOCZ	Pu-1[1]	Float[1]	3
B16	B19	GPIO110	GPIO110	ICOCZ	Pd-0[1]	Float[1]	3
R7	E19	GPIO111	GPIO111	ICOCZ	Pd-0[1]	Float[1]	3
C15	C19	GPIO112	GPIO112	ICOCZ	Pu-1[1]	Float[1]	3
	VCC_LCD						
K19	M24	GPIO63	GPIO63	ICOCZ	Pu-1[1]	Float[1]	3
K17	L25	GPIO64	GPIO64	ICOCZ	Pd-0[1]	Float[1]	3
J18	M26	GPIO65	GPIO65	ICOCZ	Pd-0[1]	Float[1]	3
J17	K22	GPIO66	GPIO66	ICOCZ	Pd-0[1]	Float[1]	3
J19	L24	GPIO67	GPIO67	ICOCZ	Pd-0[1]	Float[1]	3
J15	L26	GPIO68	GPIO68	ICOCZ	Pd-0[1]	Float[1]	3
J20	L23	GPIO69	GPIO69	ICOCZ	Pd-0[1]	Float[1]	3
J14	K26	GPIO70	GPIO70	ICOCZ	Pd-0[1]	Float[1]	3
H20	K23	GPIO71	GPIO71	ICOCZ	Pd-0[1]	Float[1]	3
J16	K24	GPIO72	GPIO72	ICOCZ	Pd-0[1]	Float[1]	3
H18	J22	GPIO73	GPIO73	ICOCZ	Pu-1[1]	Float[1]	3
H17	J23	GPIO74	GPIO74	ICOCZ	Pd-0[1]	Float[1]	3
N20	P25	GPIO6_2	GPIO6_2	ICOCZ	Pd-0[1]	Float[1]	3
L14	P23	GPIO7_2	GPIO7_2	ICOCZ	Pd-0[1]	Float[1]	3
L20	N23	GPIO8_2	GPIO8_2	ICOCZ	Pd-0[1]	Float[1]	3
K15	M22	GPIO9_2	GPIO9_2	ICOCZ	Pd-0[1]	Float[1]	3
L19	N25	GPIO10_2	GPIO10_2	ICOCZ	Pd-0[1]	Float[1]	3
L18	L22	GPIO11_2	GPIO11_2	ICOCZ	Pd-0[1]	Float[1]	3
L21	N26	GPIO12_2	GPIO12_2	ICOCZ	Pd-0[1]	Float[1]	3
L17	M25	GPIO13_2	GPIO13_2	ICOCZ	Pd-0[1]	Float[1]	3

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
H16	K25	GPIO14_2	GPIO14_2	ICOCZ	Pd-0[1]	Float[1]	3
H21	H22	GPIO15_2	GPIO15_2	ICOCZ	Pd-0[1]	Float[1]	3
H15	J24	GPIO16_2	GPIO16_2	ICOCZ	Pd-0[1]	Float[1]	3
H19	H25	GPIO17_2	GPIO17_2	ICOCZ	Pd-0[1]	Float[1]	3
	VCC_MEM						
K1	C3	DQM0	DQM0	OC	High	High	High
H2	F1	DQM1	DQM1	OC	High	High	High
T3	V2	DQM2	DQM2	OC	High	High	High
W4	AA3	DQM3	DQM3	OC	High	High	High
J2	D2	DQS0	DQS0	ISOCZ	Pd-0	Pd-0	Pd-0
M2	E1	DQS1	DQS1	ISOCZ	Pd-0	Pd-0	Pd-0
AA10	W2	DQS2	DQS2	ISOCZ	Pd-0	Pd-0	Pd-0
AA11	AA2	DQS3	DQS3	ISOCZ	Pd-0	Pd-0	Pd-0
U3	AC4	GPIO0	GPIO0	ICOCZ	Pd-0[1]	Pd-0[1]	3
V4	AC3	GPIO1	GPIO1	ICOCZ	Pd-0[1]	Pd-0[1]	3
J8	K4	MA0	MA0	OC	high	high	high
J3	J1	MA1	MA1	OC	high	high	high
F5	J2	MA2	MA2	OC	high	high	high
G4	H1	MA3	MA3	OC	high	high	high
K7	T4	MA4	MA4	OC	high	high	high
M21	P1	MA5	MA5	OC	high	high	high
K6	R3	MA6	MA6	OC	high	high	high
N21	P3	MA7	MA7	OC	high	high	high
V21	N3	MA8	MA8	OC	high	high	high
U21	P2	MA9	MA9	OC	high	high	high
L2	P4	MA11	MA11	OC	high	high	high
J6	L3	MA12	MA12	OC	high	high	high
N8	L2	MA13	MA13	OC	high	high	high

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
J4	K1	MA14	MA14	OC	high	high	high
N18	L4	MA15	MA15	OC	high	high	high
D2	B3	MD0	MD0	ICSOCZ	Pd-0	Pd-0	Pd-0
C2	B2	MD1	MD1	ICSOCZ	Pd-0	Pd-0	Pd-0
E2	C2	MD2	MD2	ICSOCZ	Pd-0	Pd-0	Pd-0
E1	C4	MD3	MD3	ICSOCZ	Pd-0	Pd-0	Pd-0
F2	C1	MD4	MD4	ICSOCZ	Pd-0	Pd-0	Pd-0
F1	D3	MD5	MD5	ICSOCZ	Pd-0	Pd-0	Pd-0
J1	E2	MD6	MD6	ICSOCZ	Pd-0	Pd-0	Pd-0
G3	D1	MD7	MD7	ICSOCZ	Pd-0	Pd-0	Pd-0
R2	E3	MD8	MD8	ICSOCZ	Pd-0	Pd-0	Pd-0
G5	F3	MD9	MD9	ICSOCZ	Pd-0	Pd-0	Pd-0
N1	F2	MD10	MD10	ICSOCZ	Pd-0	Pd-0	Pd-0
G6	G3	MD11	MD11	ICSOCZ	Pd-0	Pd-0	Pd-0
T2	H3	MD12	MD12	ICSOCZ	Pd-0	Pd-0	Pd-0
H5	G2	MD13	MD13	ICSOCZ	Pd-0	Pd-0	Pd-0
W2	G1	MD14	MD14	ICSOCZ	Pd-0	Pd-0	Pd-0
H4	H2	MD15	MD15	ICSOCZ	Pd-0	Pd-0	Pd-0
Y3	V4	MD16	MD16	ICSOCZ	Pd-0	Pd-0	Pd-0
N5	V3	MD17	MD17	ICSOCZ	Pd-0	Pd-0	Pd-0
Y5	V1	MD18	MD18	ICSOCZ	Pd-0	Pd-0	Pd-0
AA4	W1	MD19	MD19	ICSOCZ	Pd-0	Pd-0	Pd-0
AA6	Y1	MD20	MD20	ICSOCZ	Pd-0	Pd-0	Pd-0
AA7	AA1	MD21	MD21	ICSOCZ	Pd-0	Pd-0	Pd-0
W3	Y3	MD22	MD22	ICSOCZ	Pd-0	Pd-0	Pd-0
AA9	W3	MD23	MD23	ICSOCZ	Pd-0	Pd-0	Pd-0
R3	Y2	MD24	MD24	ICSOCZ	Pd-0	Pd-0	Pd-0
Y11	AA4	MD25	MD25	ICSOCZ	Pd-0	Pd-0	Pd-0

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
Y4	AB1	MD26	MD26	ICSOCZ	Pd-0	Pd-0	Pd-0
W9	AB4	MD27	MD27	ICSOCZ	Pd-0	Pd-0	Pd-0
U4	AC1	MD28	MD28	ICSOCZ	Pd-0	Pd-0	Pd-0
T4	AD1	MD29	MD29	ICSOCZ	Pd-0	Pd-0	Pd-0
AA5	AB3	MD30	MD30	ICSOCZ	Pd-0	Pd-0	Pd-0
U5	AB2	MD31	MD31	ICSOCZ	Pd-0	Pd-0	Pd-0
T21	R4	NSDCAS	nSDCAS	OC	High	High	High
K4	L1	NSDCS0	nSDCS0	OC	High	High	High
J7	N4	NSDCS1	nSDCS1	OC	High	High	High
L4	N2	NSDRAS	nSDRAS	OC	High	High	High
H3	M3	NSDWE	nSDWE	OC	High	High	High
L1	R1	RCOMP_DDR	RCOMP_DDR	OA	-	-	-
U2	M2	SDCKE	SDCKE	OC	Low	Low	Low
Y2	M1	SDCLK0	SDCLK0	OC	Low	Low	Low
M6	N1	SDCLK1	SDCLK1	OC	High	High	High
K3	K2	SDMA10	SDMA10	OC	High	High	High
VCC_MSL							
F20	H23	GPIO75	GPIO75	ICOCZ	Pd-0[1]	Float[1]	3
G15	H24	GPIO76	GPIO76	ICOCZ	Pd-0[1]	Float[1]	3
G21	G24	GPIO77	GPIO77	ICOCZ	Pd-0[1]	Float[1]	3
G16	G22	GPIO78	GPIO78	ICOCZ	Pd-0[1]	Float[1]	3
F21	F25	GPIO79	GPIO79	ICOCZ	Pd-0[1]	Float[1]	3
H14	F23	GPIO80	GPIO80	ICOCZ	Pd-0[1]	Float[1]	3
G20	E25	GPIO81	GPIO81	ICOCZ	Pd-0[1]	Float[1]	3
K16	E26	GPIO82	GPIO82	ICOCZ	Pu-1[1]	Float[1]	3
VCC_TSI							
F15	D19	TSI_XM	TSI_XM	IAOA	Hi-Z	Hi-Z	Hi-Z
A16	E18	TSI_XP	TSI_XP	IAOA	Hi-Z	Hi-Z	Hi-Z

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
C14	D18	TSI_YM	TSI_YM	IAOA	Hi-Z	Hi-Z	Hi-Z / 0[8]
B17	E17	TSI_YP	TSI_YP	IAOA	Hi-Z	Hi-Z	Hi-Z
VCC_USB							
E5	A5	USBH1_N	USBH1_N	IAOA	Pd-0 Note[8]	Pd-0[8]	Pd-0[8]
E6	A6	USBH1_P	USBH1_P	IAOA	Pd-0 Note[8]	Pd-0[8]	Pd-0[8]
D5	A3	USBOTG_N	USBOTG_N	IAOA	Hi-Z	Hi-Z or Pd-0[9]	Hi-Z or Pd-0[9]
C5	A4	USBOTG_P	USBOTG_P	IAOA	Hi-Z	Hi-Z or Pd-0 or Pu-1[8,10]	Hi-Z or Pd-0 or Pu-1[8,10]
VCC_CARD1							
W15	AE20	GPIO18	GPIO18	ICOCZ	Pd-0[1]	Float[1]	3
W16	AB20	GPIO19	GPIO19	ICOCZ	Pd-0[1]	Float[1]	3
U15	AC21	GPIO20	GPIO20	ICOCZ	Pd-0[1]	Float[1]	3
AA16	AF22	GPIO21	GPIO21	ICOCZ	Pu-1[1]	Float[1]	3
V17	AC22	GPIO22	GPIO22	ICOCZ	Pd-0[1]	Float[1]	3
Y17	AF23	GPIO23	GPIO23	ICOCZ	Pd-0[1]	Float[1]	3
VCC_CARD2							
W19	AE22	GPIO24	GPIO24	ICOCZ	Pd-0[1]	Float[1]	3
W18	AD22	GPIO25	GPIO25	ICOCZ	Pd-0[1]	Float[1]	3
AA19	AF24	GPIO26	GPIO26	ICOCZ	Pd-0[1]	Float[1]	3
V16	AD23	GPIO27	GPIO27	ICOCZ	Pu-1[1]	Float[1]	3
U19	AB22	GPIO28	GPIO28	ICOCZ	Pd-0[1]	Float[1]	3
U16	AE25	GPIO29	GPIO29	ICOCZ	Pd-0[1]	Float[1]	3
No Connect Balls							
A1	A1	NC					
A2	A2	NC					
A20	A25	NC					
A21	A26	NC					

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AA1	B1	NC					
AA2	B26	NC					
AA20	AE1	NC					
AA21	AE2	NC					
B1	AE26	NC					
B21	AF1	NC					
Y1	AF2	NC					
Y21	AF25	NC					
Y7	AF26	NC					
Reserved For Future Use (RFU) Balls							
A4	K3	RFU_A4/ RFU_K3					
B10	R2	RFU_B10/ RFU_R2					
B11	T1	RFU_B11/ RFU_T1					
B3	T2	RFU_B3/ RFU_T2					
C3	T3	RFU_C3/ RFU_T3					
D4	U1	RFU_D4/ RFU_U1					
D6	U2	RFU_D6/ RFU_U2					
H7	U3	RFU_H7/ RFU_U3					
L7	U4	RFU_L7/ RFU_U4					
Y19	AD4	RFU_Y19/ RFU_AD4					
Y20		RFU_Y20					
Package on Package (POP) Signals							

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
D13		LOCK_PRE			Input	Input	Input
W20		ND_RST			Input	Input	Input
C20		DF_NWP			Input	Input	Input
Power Supplies							
L5	AC14	VCC_APPS	VCC_APPS	PS	Input	Input	Input
M5	AC16	VCC_APPS	VCC_APPS	PS	Input	Input	Input
P5	AC20	VCC_APPS	VCC_APPS	PS	Input	Input	Input
L6	AD19	VCC_APPS	VCC_APPS	PS	Input	Input	Input
N6	AE16	VCC_APPS	VCC_APPS	PS	Input	Input	Input
N7	AF15	VCC_APPS	VCC_APPS	PS	Input	Input	Input
E8	AF18	VCC_APPS	VCC_APPS	PS	Input	Input	Input
V12	AF20	VCC_APPS	VCC_APPS	PS	Input	Input	Input
W13	AF21	VCC_APPS	VCC_APPS	PS	Input	Input	Input
N14	L13	VCC_APPS	VCC_APPS	PS	Input	Input	Input
AA14	L14	VCC_APPS	VCC_APPS	PS	Input	Input	Input
V15	M13	VCC_APPS	VCC_APPS	PS	Input	Input	Input
Y15	M14	VCC_APPS	VCC_APPS	PS	Input	Input	Input
AA15	N11	VCC_APPS	VCC_APPS	PS	Input	Input	Input
Y16	N12	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	N15	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	N16	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	P11	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	P12	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	P15	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	P16	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	R13	VCC_APPS	VCC_APPS	PS	Input	Input	Input

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
	R14	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	T13	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	T14	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	T25	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	V25	VCC_APPS	VCC_APPS	PS	Input	Input	Input
H9	A10	VCC_BBATT	VCC_BBATT	PS	Input	Input	Input
G10	D9	VCC_BG	VCC_BG	PS	Input	Input	Input
AA17	AB21	VCC_CARD1	VCC_CARD1	PS	Input	Input	Input
W17	AE23	VCC_CARD2	VCC_CARD2	PS	Input	Input	Input
M15	R26	VCC_CI	VCC_CI	PS	Input	Input	Input
	V24	VCC_CI	VCC_CI	PS	Input	Input	Input
B4	AB7	VCC_DF	VCC_DF	PS	Input	Input	Input
T5	AC9	VCC_DF	VCC_DF	PS	Input	Input	Input
V6	AD6	VCC_DF	VCC_DF	PS	Input	Input	Input
B9	AE11	VCC_DF	VCC_DF	PS	Input	Input	Input
	AE13	VCC_DF	VCC_DF	PS	Input	Input	Input
B15	D15	VCC_IO1	VCC_IO1	PS	Input	Input	Input
	E10	VCC_IO1	VCC_IO1	PS	Input	Input	Input
AA13	AB18	VCC_IO3	VCC_IO3	PS	Input	Input	Input
U18	AB24	VCC_IO4	VCC_IO4	PS	Input	Input	Input
	W23	VCC_IO4	VCC_IO4	PS	Input	Input	Input
E15	B22	VCC_IO6	VCC_IO6	PS	Input	Input	Input
	C20	VCC_IO6	VCC_IO6	PS	Input	Input	Input
K18	J26	VCC_LCD	VCC_LCD	PS	Input	Input	Input
K20	N24	VCC_LCD	VCC_LCD	PS	Input	Input	Input
B2	AB5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
N2	D4	VCC_MEM	VCC_MEM	PS	Input	Input	Input
P2	F4	VCC_MEM	VCC_MEM	PS	Input	Input	Input

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
D3	H4	VCC_MEM	VCC_MEM	PS	Input	Input	Input
L3	J5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
M3	K5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
AA3	M5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
N4	P5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
K5	T5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
M7	W5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
	Y5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
G19	F24	VCC_MSL	VCC_MSL	PS	Input	Input	Input
F3	AB26	VCC_MVT	VCC_MVT	PS	Input	Input	Input
P3	AB8	VCC_MVT	VCC_MVT	PS	Input	Input	Input
F4	AD15	VCC_MVT	VCC_MVT	PS	Input	Input	Input
P4	E20	VCC_MVT	VCC_MVT	PS	Input	Input	Input
L8	E7	VCC_MVT	VCC_MVT	PS	Input	Input	Input
N15	G23	VCC_MVT	VCC_MVT	PS	Input	Input	Input
E17	H5	VCC_MVT	VCC_MVT	PS	Input	Input	Input
	M4	VCC_MVT	VCC_MVT	PS	Input	Input	Input
	P22	VCC_MVT	VCC_MVT	PS	Input	Input	Input
	W4	VCC_MVT	VCC_MVT	PS	Input	Input	Input
F10	E8	VCC_OSC13M	VCC_OSC13M	PS	Input	Input	Input
F12	AE18	VCC_PLL	VCC_PLL	PS	Input	Input	Input
R12	B15	VCC_PLL	VCC_PLL	PS	Input	Input	Input
G1	AB11	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
G2	D16	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
P9	E9	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
F14	H26	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
A19	J3	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
E12	A18	VCC_TSI	VCC_TSI	PS	Input	Input	Input

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
B6	C5	VCC_USB	VCC_USB	PS	Input	Input	Input
D1	AA26	VSS	VSS	PS	Input	Input	Input
U1	AB12	VSS	VSS	PS	Input	Input	Input
V1	AB9	VSS	VSS	PS	Input	Input	Input
V2	AD14	VSS	VSS	PS	Input	Input	Input
N3	AD16	VSS	VSS	PS	Input	Input	Input
C4	AD17	VSS	VSS	PS	Input	Input	Input
M4	AD18	VSS	VSS	PS	Input	Input	Input
J5	AD21	VSS	VSS	PS	Input	Input	Input
V7	AE15	VSS	VSS	PS	Input	Input	Input
F8	AE19	VSS	VSS	PS	Input	Input	Input
U11	AE21	VSS	VSS	PS	Input	Input	Input
W11	G25	VSS	VSS	PS	Input	Input	Input
E14	G26	VSS	VSS	PS	Input	Input	Input
V14	L11	VSS	VSS	PS	Input	Input	Input
P17	L12	VSS	VSS	PS	Input	Input	Input
Y18	L15	VSS	VSS	PS	Input	Input	Input
AA18	L16	VSS	VSS	PS	Input	Input	Input
P21	M11	VSS	VSS	PS	Input	Input	Input
	M12	VSS	VSS	PS	Input	Input	Input
	M15	VSS	VSS	PS	Input	Input	Input
	M16	VSS	VSS	PS	Input	Input	Input
	N13	VSS	VSS	PS	Input	Input	Input
	N14	VSS	VSS	PS	Input	Input	Input
	N22	VSS	VSS	PS	Input	Input	Input
	P13	VSS	VSS	PS	Input	Input	Input
	P14	VSS	VSS	PS	Input	Input	Input
	R11	VSS	VSS	PS	Input	Input	Input

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
	R12	VSS	VSS	PS	Input	Input	Input
	R15	VSS	VSS	PS	Input	Input	Input
	R16	VSS	VSS	PS	Input	Input	Input
	T11	VSS	VSS	PS	Input	Input	Input
	T12	VSS	VSS	PS	Input	Input	Input
	T15	VSS	VSS	PS	Input	Input	Input
	T16	VSS	VSS	PS	Input	Input	Input
	T26	VSS	VSS	PS	Input	Input	Input
	V26	VSS	VSS	PS	Input	Input	Input
	Y4	VSS	VSS	PS	Input	Input	Input
	A9	VSS	VSS	PS	Input	Input	Input
C8	B9	VSS_BBATT	VSS_BBATT	PS	Input	Input	Input
C9	D10	VSS_BG	VSS_BG	PS	Input	Input	Input
R14	AD20	VSS_CARD1	VSS_CARD1	PS	Input	Input	Input
V19	AE24	VSS_CARD2	VSS_CARD2	PS	Input	Input	Input
N16	R25	VSS_CI	VSS_CI	PS	Input	Input	Input
	U24	VSS_CI	VSS_CI	PS	Input	Input	Input
A3	AC10	VSS_DF	VSS_DF	PS	Input	Input	Input
W6	AC6	VSS_DF	VSS_DF	PS	Input	Input	Input
Y10	AC7	VSS_DF	VSS_DF	PS	Input	Input	Input
Y12	AD13	VSS_DF	VSS_DF	PS	Input	Input	Input
B20	AF11	VSS_DF	VSS_DF	PS	Input	Input	Input
D11	E11	VSS_IO1	VSS_IO1	PS	Input	Input	Input
	E15	VSS_IO1	VSS_IO1	PS	Input	Input	Input
T12	AE17	VSS_IO3	VSS_IO3	PS	Input	Input	Input
R17	AB23	VSS_IO4	VSS_IO4	PS	Input	Input	Input
	Y24	VSS_IO4	VSS_IO4	PS	Input	Input	Input
E19	C22	VSS_IO6	VSS_IO6	PS	Input	Input	Input

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
	D20	VSS_IO6	VSS_IO6	PS	Input	Input	Input
R11	J25	VSS_LCD	VSS_LCD	PS	Input	Input	Input
J21	M23	VSS_LCD	VSS_LCD	PS	Input	Input	Input
C1	AA5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
H1	AC5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
M1	E4	VSS_MEM	VSS_MEM	PS	Input	Input	Input
P1	G4	VSS_MEM	VSS_MEM	PS	Input	Input	Input
R1	J4	VSS_MEM	VSS_MEM	PS	Input	Input	Input
T1	L5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
K2	N5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
R4	R5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
R5	U5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
P7	V5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
W21		VSS_MEM	VSS_MEM	PS	Input	Input	Input
G17	F26	VSS_MSL	VSS_MSL	PS	Input	Input	Input
A9	B11	VSS_OSC13M	VSS_OSC13M	PS	Input	Input	Input
C12	AC18	VSS_PLL	VSS_PLL	PS	Input	Input	Input
W14	C14	VSS_PLL	VSS_PLL	PS	Input	Input	Input
D14	C18	VSS_TSI	VSS_TSI	PS	Input	Input	Input
E3	B5	VSS_USB	VSS_USB	PS	Input	Input	Input

Table 9: PXA32x Processor Pin Usage Summary (Continued)

15mm² Ball #	14mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode

NOTE:
1. GPIO reset/S3 operation: After any reset is asserted or if PXA32x processor is in S3/D4/C4 power mode, these pins are configured as the primary function of the MFP (generally as GPIO input) and default pullup or pulldown occurs.
2. Crystal oscillator pins: These pins connect the external crystals to the on-chip oscillators and are not affected by either reset or S2/D3/C4 power mode. For more information, see the “Services Clock Control Unit” chapter in the PXA3xx Processor Family Developers Manual.
3. Each MFP output value is based on MFPRxx[Sleep_sel], MFPRxx[sleep_data], MFPRxx[sleep_oe_n], MFPRxx[pull_sel], MFPRxx[pullup_en] and MFPRxx[pulldown_en] following S2/D3/C4 wake-up. To prevent unnecessary current drain, ensure input signals are not floating during low-power modes. Each GPIO to be driven can be programmed to a 0/1 or be pulled up or pulled down during S2/D3/C4 power mode if the MVT and the IO (HVT) supplies are present.
4. Logic low when OSCC[TENSx] bit is cleared, CLK_TOUT when OSCC[TENSx] is set. Configure TENS2 for S2/D3/C4 mode and TENS3 for S3/D4/C4 power mode.
5. Pulldown always enabled.
6. Output functions during S2/D3/C4 power mode.
7. Pullup always enabled.
8. AD2D0ER[WETSI] bit is set before entry into S2, TSI_YM is driven low (not pulled low). AD2D0ER[WETSI] bit is clear before entry into S2, TSI_YM signal is Hi-Z (no pulldown or pullup).
9. 20 KΩ nominal, 14.5 KΩ min - 24.5 KΩ max
10. Pd-0 if UP2OCR[DMPDE] is set, then Pd-0, Hi-Z if UP2OCR[DMPDE] is cleared.
11. Hi-Z if UP2OCR[DPPDE] is cleared and UP2OCR[DPPUE] is cleared; Pu-1 if UP2OCR[DPPDE] is cleared and UP2OCR[DPPUE] is set; Pd-0 if UP2OCR[DPPDE] is set and UP2OCR[DPPUE] is cleared. Setting UP2OCR[DPPDE] and UP2OCR[DPPUE] at the same time is not allowed.
12. This signal’s pullup/pulldown is enabled during power-on, hardware, global watchdog and GPIO resets. The pullup/pulldown must be disabled by software by setting PCFR[PUDH] after the external devices driving these pins are configured.
13. There is no pullup or pulldown on this pin. Asserts if PCFR[SL_ROD] is clear.
14. See Table 12 for type definitions

4.2.2 PXA31x Processor Pin Use

Table 10 lists the mapping of signals to specific PXA31x processor package pins.

Table 10: PXA31x Processor Pin Usage Summary

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
VCC_BBATT							
B6	A6	CLK_TOUT	CLK_TOUT	OC	Clk-Out	4	4
B7	E6	EXT_WAKEUP0	EXT_WAKEUP0	ICOCZ	Pd-0[10]	Pd-0[10]	Pd-0[10]
C6	C6	NBATT_FAULT	nBATT_FAULT	IC	Input	Input	Input
E8	E9	NGPIO_RESET	nGPIO_RESET	IC	Pu-1[10]	Pu-1[10]	Pu-1[10]

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
D6	B6	NRESET	nRESET	IC	Input[7]	Input	Input
F9	A8	NRESET_OUT	nRESET_OUT	OC	Low	11	11
A6	E5	NTRST	nTRST	IC	Input[7]	Input[7]	Input[7]
A7	A7	PWR_CAP0	PWR_CAP0	OA	-	-	-
F8	F7	PWR_CAP1	PWR_CAP1	OA	-	-	-
D3	C5	PWR_EN	PWR_EN	OC	Low	Low	Low
C7	B7	PWR_OUT	PWR_OUT	OA	-	-	-
D4	F6	SYS_EN	SYS_EN	OC	Low	Low	Low
C4	A5	TCK	TCK	IC	Input	Input	Input
E3	B5	TDI	TDI	IC	Input[7]	Input[7]	Input[7]
D2	C4	TDO	TDO	OCZ	Hi-Z	Hi-Z	Hi-Z
C3	D3	TMS	TMS	IC	Input[7]	Input[7]	Input[7]
A8	C7	TXTAL_IN	TXTAL_IN	IA	2	2	2
B8	C8	TXTAL_OUT	TXTAL_OUT	OA	2	2	2
VCC_MVT							
B9	A9	PXTAL_IN	PXTAL_IN	IA	2	2	2
C9	B9	PXTAL_OUT	PXTAL_OUT	OA	2	2	2
VCC_IO1							
A11	A13	GPIO0_2	GPIO0_2	ICOCZ	Pd-0[1]	Float[1]	3
D11	A12	GPIO1_2	GPIO1_2	ICOCZ	Pd-0[1]	Float[1]	3
E18	D22	GPIO91	GPIO91	ICOCZ	Pu-1[1]	Float[1]	3
E21	C22	GPIO92	GPIO92	ICOCZ	Pu-1[1]	Float[1]	3
E20	E24	GPIO93	GPIO93	ICOCZ	Pd-0[1]	Float[1]	3
D21	C23	GPIO94	GPIO94	ICOCZ	Pd-0[1]	Float[1]	3
C20	D24	GPIO95	GPIO95	ICOCZ	Pd-0[1]	Float[1]	3
A19	B23	GPIO96	GPIO96	ICOCZ	Pd-0[1]	Float[1]	3
D20	A22	GPIO97	GPIO97	ICOCZ	Pd-0[1]	Float[1]	3
C21	C24	GPIO98	GPIO98	ICOCZ	Pd-0[1]	Float[1]	3

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
A18	B16	GPIO99	GPIO99	ICOCZ	Pd-0[1]	Float[1]	3
B18	A21	GPIO100	GPIO100	ICOCZ	Pd-0[1]	Float[1]	3
C19	B19	GPIO101	GPIO101	ICOCZ	Pu-1[1]	Float[1]	3
A17	A20	GPIO102	GPIO102	ICOCZ	Pu-1[1]	Float[1]	3
D18	C20	GPIO103	GPIO103	ICOCZ	Pu-1[1]	Float[1]	3
E19	C19	GPIO104	GPIO104	ICOCZ	Pu-1[1]	Float[1]	3
D17	F17	GPIO105	GPIO105	ICOCZ	Pu-1[1]	Float[1]	3
B17	B20	GPIO106	GPIO106	ICOCZ	Pu-1[1]	Float[1]	3
C16	A17	GPIO107	GPIO107	ICOCZ	Pu-1[1]	Float[1]	3
C17	C18	GPIO108	GPIO108	ICOCZ	Pu-1[1]	Float[1]	3
D16	F16	GPIO109	GPIO109	ICOCZ	Pd-0[1]	Float[1]	3
A16	A19	GPIO110	GPIO110	ICOCZ	Pu-1[1]	Float[1]	3
F14	E15	GPIO111	GPIO111	ICOCZ	Pu-1[1]	Float[1]	3
B15	H16	GPIO112	GPIO112	ICOCZ	Pd-0[1]	Float[1]	3
C15	B15	GPIO113	GPIO113	ICOCZ	Pd-0[1]	Float[1]	3
D15	E16	GPIO114	GPIO114	ICOCZ	Pu-1[1]	Float[1]	3
C13	A15	GPIO115	GPIO115	ICOCZ	Pd-0[1]	Float[1]	3
A14	A16	GPIO116	GPIO116	ICOCZ	Pd-0[1]	Float[1]	3
E14	E14	GPIO117	GPIO117	ICOCZ	Pd-0[1]	Float[1]	3
D14	C15	GPIO118	GPIO118	ICOCZ	Pd-0[1]	Float[1]	3
E13	B14	GPIO119	GPIO119	ICOCZ	Pd-0[1]	Float[1]	3
B14	F15	GPIO120	GPIO120	ICOCZ	Pd-0[1]	Float[1]	3
F13	E13	GPIO121	GPIO121	ICOCZ	Pd-0[1]	Float[1]	3
C14	F14	GPIO122	GPIO122	ICOCZ	Pd-0[1]	Float[1]	3
D13	B13	GPIO123	GPIO123	ICOCZ	Pu-1[1]	Float[1]	3
B12	F13	GPIO124	GPIO124	ICOCZ	Pd-0[1]	Float[1]	3
F12	F12	GPIO125	GPIO125	ICOCZ	Pd-0[1]	Float[1]	3
A12	A14	GPIO126	GPIO126	ICOCZ	Pu-1[1]	Float[1]	3

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
C12	C12	GPIO127	GPIO127	ICOCZ	Pu-1[1]	Float[1]	3
P8	E20	GPIO7_2	GPIO7_2	ICOCZ	Pd-0[1]	Float[1]	3
N8	F19	GPIO8_2	GPIO8_2	ICOCZ	Pd-0[1]	Float[1]	3
K8	E18	GPIO9_2	GPIO9_2	ICOCZ	Pd-0[1]	Float[1]	3
J8	F18	GPIO10_2	GPIO10_2	ICOCZ	Pd-0[1]	Float[1]	3
F10	A10	PWR_SCL	PWR_SCL	ICOCZ	Pu-1[10]	Pu-1[10]	Float - Note[1]
B10	F11	PWR_SDA	PWR_SDA	ICOCZ	Pu-1[10]	Pu-1[10]	Float - Note[1]
B11	H12	TEST	TEST	IC	Input[5]	Input[5]	Input[5]
F11	E10	TESTCLK	TESTCLK	IC	Input[5]	Input[5]	Input[5]
E10	B10	VCTCXO_EN	VCTCXO_EN	OC	Low	Note[6]	Note[6]
C11	B12	CLK_POUT	CLK_POUT	OC	Low	Float	Low
VCC_DF							
AA4	AC4	DF_ADDR0	DF_ADDR0	OCZ	Pd-0[1]	Float[1]	3
V6	AB5	DF_ADDR1	DF_ADDR1	OCZ	Pd-0[1]	Float[1]	3
W6	AD4	DF_ADDR2	DF_ADDR2	OCZ	Pd-0[1]	Float[1]	3
Y4	AC5	DF_ADDR3	DF_ADDR3	OCZ	Pd-0[1]	Float[1]	3
AA5	Y7	DF_IO0	DF_IO0	ICOCZ	Pd-0[1]	Float[1]	3
AA6	AC7	DF_IO1	DF_IO1	ICOCZ	Pd-0[1]	Float[1]	3
W7	AD6	DF_IO2	DF_IO2	ICOCZ	Pd-0[1]	Float[1]	3
Y8	AB9	DF_IO3	DF_IO3	ICOCZ	Pd-0[1]	Float[1]	3
V10	AD12	DF_IO4	DF_IO4	ICOCZ	Pd-0[1]	Float[1]	3
W13	AD13	DF_IO5	DF_IO5	ICOCZ	Pd-0[1]	Float[1]	3
W12	AD14	DF_IO6	DF_IO6	ICOCZ	Pd-0[1]	Float[1]	3
V11	Y12	DF_IO7	DF_IO7	ICOCZ	Pd-0[1]	Float[1]	3
U8	AD5	DF_IO8	DF_IO8	ICOCZ	Pd-0[1]	Float[1]	3
Y5	AB8	DF_IO9	DF_IO9	ICOCZ	Pd-0[1]	Float[1]	3
Y6	AD7	DF_IO10	DF_IO10	ICOCZ	Pd-0[1]	Float[1]	3

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
W8	AD9	DF_IO11	DF_IO11	ICOCZ	Pd-0[1]	Float[1]	3
U15	W13	DF_IO12	DF_IO12	ICOCZ	Pd-0[1]	Float[1]	3
W10	AB12	DF_IO13	DF_IO13	ICOCZ	Pd-0[1]	Float[1]	3
W11	Y14	DF_IO14	DF_IO14	ICOCZ	Pd-0[1]	Float[1]	3
W15	AD15	DF_IO15	DF_IO15	ICOCZ	Pd-0[1]	Float[1]	3
V7	AC2	DF_ALE_NWE	DF_ALE	OCZ	Pu-1[1]	Float[1]	3
V9	W10	DF_NCS0	DF_nCS0	OCZ	Pu-1[1]	Float[1]	3
U10	AC13	DF_NCS1	DF_nCS1	OCZ	Pu-1[1]	Float[1]	3
W5	AB3	DF_NRE	DF_nOE	OCZ	Pu-1[1]	Float[1]	3
W4	AB2	DF_NWE	DF_nWE	OCZ	Pu-1[1]	Float[1]	3
W3	AA3	DF_INT_RNB	DF_RnB	ICZ	Pu-1[1]	Float[1]	3
V8	W6	DF_CLE_NOE	ND_CLE	OCZ	Pu-1[1]	Float[1]	3
AA10	AC11	DF_SCLK_E	DF_SCLK_E	OCZ	Pd-0[1]	Float[1]	3
V3	W1	GPIO0	GPIO0	ICOCZ	Pd-0[1]	Float[1]	3
U4	AA2	GPIO1	GPIO1	ICOCZ	Pu-1[1]	Float[1]	3
V1	Y1	GPIO2	GPIO2	ICOCZ	Pu-1[1]	Float[1]	3
Y3	AD3	NBE0	nBE0	OCZ	Pu-1[1]	Float[1]	3
AA3	AC3	NBE1	nBE1	OCZ	Pu-1[1]	Float[1]	3
Y10	AB11	NLLA	nLLA	OCZ	Pu-1[1]	Float[1]	3
Y9	AD10	NLUA	nLUA	OCZ	Pu-1[1]	Float[1]	3
W1	AB1	NCS0	nCS0	OC	High	High	High
V4	AA1	NCS1	nCS1	OC	High	High	High
VCC_IO3							
W17	AC21	GPIO17	GPIO17	ICOCZ	Pd-0[1]	Float[1]	3
W18	W17	GPIO18	GPIO18	ICOCZ	Pd-0[1]	Float[1]	3
U17	AB21	GPIO19	GPIO19	ICOCZ	Pd-0[1]	Float[1]	3
V18	AB23	GPIO20	GPIO20	ICOCZ	Pu-1[1]	Float[1]	3
W19	Y22	GPIO21	GPIO21	ICOCZ	Pu-1[1]	Float[1]	3

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AA17	AC23	GPIO22	GPIO22	ICOCZ	Pu-1[1]	Float[1]	3
Y17	AB22	GPIO23	GPIO23	ICOCZ	Pu-1[1]	Float[1]	3
AA18	AD22	GPIO24	GPIO24	ICOCZ	Pd-0[1]	Float[1]	3
Y18	AA23	GPIO25	GPIO25	ICOCZ	Pd-0[1]	Float[1]	3
Y19	AA24	GPIO26	GPIO26	ICOCZ	Pd-0[1]	Float[1]	3
V21	W19	GPIO27	GPIO27	ICOCZ	Pd-0[1]	Float[1]	3
U21	Y23	GPIO28	GPIO28	ICOCZ	Pd-0[1]	Float[1]	3
V19	Y24	GPIO29	GPIO29	ICOCZ	Pd-0[1]	Float[1]	3
E6	W15	GPIO2_2	GPIO2_2	ICOCZ	Pu-1[1]	Float[1]	3
E5	W20	GPIO3_2	GPIO3_2	ICOCZ	Pd-0[1]	Float[1]	3
G8	Y18	GPIO4_2	GPIO4_2	ICOCZ	Pd-0[1]	Float[1]	3
F5	Y20	GPIO5_2	GPIO5_2	ICOCZ	Pd-0[1]	Float[1]	3
E7	Y19	GPIO6_2	GPIO6_2	ICOCZ	Pu-1[1]	Float[1]	3
VCC_ULPI							
V20	AA22	GPIO30	GPIO30	ICOCZ	Pd-0[1]	Float[1]	3
U18	W22	GPIO31	GPIO31	ICOCZ	Pd-0[1]	Float[1]	3
U20	W23	GPIO32	GPIO32	ICOCZ	Pu-1[1]	Float[1]	3
U19	W18	GPIO33	GPIO33	ICOCZ	Pu-1[1]	Float[1]	3
T20	W24	GPIO34	GPIO34	ICOCZ	Pu-1[1]	Float[1]	3
T18	V20	GPIO35	GPIO35	ICOCZ	Pu-1[1]	Float[1]	3
T21	V23	GPIO36	GPIO36	ICOCZ	Pu-1[1]	Float[1]	3
R17	V19	GPIO37	GPIO37	ICOCZ	Pu-1[1]	Float[1]	3
T17	U22	GPIO38	GPIO38	ICOCZ	Pd-0[1]	Float[1]	3
V17	N17	ULPI_DIR	ULPI_DIR	IC	Pd-0[1]	Float[1]	3
W20	P17	ULPI_NXT	ULPI_NXT	IC	Pd-0[1]	Float[1]	3
W21	U17	ULPI_STP	ULPI_STP	0C	Pu-1[1]	Float[1]	3
VCC_CI							
R18	U19	GPIO39	GPIO39	ICOCZ	Pd-0[1]	Float[1]	3

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
T19	V24	GPIO40	GPIO40	ICOCZ	Pd-0[1]	Float[1]	3
R20	U23	GPIO41	GPIO41	ICOCZ	Pd-0[1]	Float[1]	3
R19	T22	GPIO42	GPIO42	ICOCZ	Pd-0[1]	Float[1]	3
P16	U24	GPIO43	GPIO43	ICOCZ	Pd-0[1]	Float[1]	3
R21	T20	GPIO44	GPIO44	ICOCZ	Pd-0[1]	Float[1]	3
P17	R20	GPIO45	GPIO45	ICOCZ	Pd-0[1]	Float[1]	3
P18	T17	GPIO46	CIF_DD7	ICOCZ	Pd-0[1]	Float[1]	3
N16	P22	GPIO47	GPIO47	ICOCZ	Pd-0[1]	Float[1]	3
P21	R19	GPIO48	GPIO48	ICOCZ	Pd-0[1]	Float[1]	3
N17	P20	GPIO49	CIF_MCLK	ICOCZ	Pd-0[1]	Float[1]	3
N18	R24	GPIO50	CIF_PCLK	ICOCZ	Pd-0[1]	Float[1]	3
N19	N24	GPIO51	CIF_HSYNC	ICOCZ	Pd-0[1]	Float[1]	3
M20	N20	GPIO52	CIF_VSYNC	ICOCZ	Pd-0[1]	Float[1]	3
VCC_LCD							
M17	R23	GPIO53	GPIO53	ICOCZ	Pu-1[1]	Float[1]	3
M21	P23	GPIO54	GPIO54	ICOCZ	Pd-0[1]	Float[1]	3
M18	N22	GPIO55	GPIO55	ICOCZ	Pd-0[1]	Float[1]	3
L18	P24	GPIO56	GPIO56	ICOCZ	Pd-0[1]	Float[1]	3
M19	N23	GPIO57	GPIO57	ICOCZ	Pd-0[1]	Float[1]	3
L20	P19	GPIO58	GPIO58	ICOCZ	Pd-0[1]	Float[1]	3
L17	M19	GPIO59	GPIO59	ICOCZ	Pd-0[1]	Float[1]	3
L21	L19	GPIO60	GPIO60	ICZ	Pd-0[1]	Float[1]	3
K19	M22	GPIO61	GPIO61	ICOCZ	Pd-0[1]	Float[1]	3
L19	M23	GPIO62	GPIO62	ICOCZ	Pu-1[1]	Float[1]	3
K20	J19	GPIO63	GPIO63	ICOCZ	Pd-0[1]	Float[1]	3
K17	M24	GPIO64	GPIO64	ICOCZ	Pd-0[1]	Float[1]	3
J17	L22	GPIO65	GPIO65	ICOCZ	Pd-0[1]	Float[1]	3
K21	K22	GPIO66	GPIO66	ICOCZ	Pd-0[1]	Float[1]	3

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
J18	L23	GPIO67	GPIO67	ICOCZ	Pd-0[1]	Float[1]	3
K18	L20	GPIO68	GPIO68	ICOCZ	Pd-0[1]	Float[1]	3
J19	K20	GPIO69	GPIO69	ICOCZ	Pd-0[1]	Float[1]	3
J20	L24	GPIO70	GPIO70	ICOCZ	Pd-0[1]	Float[1]	3
J16	H19	GPIO71	GPIO71	ICOCZ	Pd-0[1]	Float[1]	3
J21	K23	GPIO72	GPIO72	ICOCZ	Pd-0[1]	Float[1]	3
H16	K24	GPIO73	GPIO73	ICOCZ	Pd-0[1]	Float[1]	3
H17	J22	GPIO74	GPIO74	ICOCZ	Pd-0[1]	Float[1]	3
H18	G19	GPIO75	GPIO75	ICOCZ	Pd-0[1]	Float[1]	3
H20	J23	GPIO76	GPIO76	ICOCZ	Pd-0[1]	Float[1]	3
VCC_MEM							
G3	F2	DQM0	DQM0	OC	High	High	High
T4	U1	DQM1	DQM1	OC	High	High	High
F3	G3	DQS0	DQS0	ISOCZ	Pd-0	Pd-0	Pd-0
R4	V3	DQS1	DQS1	ISOCZ	Pd-0	Pd-0	Pd-0
L3	M1	MA0	MA0	OC	High	High	High
N4	R5	MA1	MA1	OC	High	High	High
H3	H2	MA2	MA2	OC	High	High	High
M1	P5	MA3	MA3	OC	High	High	High
H4	K3	MA4	MA4	OC	High	High	High
M3	P3	MA5	MA5	OC	High	High	High
K4	J1	MA6	MA6	OC	High	High	High
M2	N3	MA7	MA7	OC	High	High	High
J1	K2	MA8	MA8	OC	High	High	High
L2	N1	MA9	MA9	OC	High	High	High
J3	K1	SDMA10	SDMA10	OC	High	High	High
M4	N2	MA11	MA11	OC	High	High	High
K3	L3	MA12	MA12	OC	High	High	High

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
H5	M5	MA13	MA13	OC	High	High	High
H2	J3	MA14	MA14	OC	High	High	High
J4	J2	MA15	MA15	OC	High	High	High
D1	D1	MD0	MD0	ICSOCZ	Pd-0	Pd-0	Pd-0
E1	E1	MD1	MD1	ICSOCZ	Pd-0	Pd-0	Pd-0
E2	E2	MD2	MD2	ICSOCZ	Pd-0	Pd-0	Pd-0
F1	F1	MD3	MD3	ICSOCZ	Pd-0	Pd-0	Pd-0
F2	G1	MD4	MD4	ICSOCZ	Pd-0	Pd-0	Pd-0
G1	G2	MD5	MD5	ICSOCZ	Pd-0	Pd-0	Pd-0
G2	H3	MD6	MD6	ICSOCZ	Pd-0	Pd-0	Pd-0
H1	H1	MD7	MD7	ICSOCZ	Pd-0	Pd-0	Pd-0
P3	T2	MD8	MD8	ICSOCZ	Pd-0	Pd-0	Pd-0
R3	T1	MD9	MD9	ICSOCZ	Pd-0	Pd-0	Pd-0
R1	U3	MD10	MD10	ICSOCZ	Pd-0	Pd-0	Pd-0
T2	U2	MD11	MD11	ICSOCZ	Pd-0	Pd-0	Pd-0
T1	V2	MD12	MD12	ICSOCZ	Pd-0	Pd-0	Pd-0
U2	V1	MD13	MD13	ICSOCZ	Pd-0	Pd-0	Pd-0
T3	W2	MD14	MD14	ICSOCZ	Pd-0	Pd-0	Pd-0
U1	W3	MD15	MD15	ICSOCZ	Pd-0	Pd-0	Pd-0
N3	T3	NSDCAS	nSDCAS	OC	High	High	High
L1	M3	NSDCS0	nSDCS0	OC	High	High	High
J2	M2	NSDCS1	nSDCS1	OC	High	High	High
P2	P2	NSDRAS	nSDRAS	OC	High	High	High
P1	R3	NSDWE	nSDWE	OC	High	High	High
N1	P1	RCOMP_DDR	RCOMP_DDR	OA	-	-	-
R2	R2	SDCKE	SDCKE	OC	Low	Low	Low
K1	L1	SDCLK0	SDCLK0	OC	Low	Low	Low
K2	L2	SDCLK1	SDCLK1	OC	High	High	High

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
VCC_MSL							
H19	H22	GPIO77	GPIO77	ICOCZ	Pd-0[1]	Float[1]	3
G16	J24	GPIO78	GPIO78	ICOCZ	Pd-0[1]	Float[1]	3
F16	J20	GPIO79	GPIO79	ICOCZ	Pd-0[1]	Float[1]	3
H21	H23	GPIO80	GPIO80	ICOCZ	Pd-0[1]	Float[1]	3
G18	G23	GPIO81	GPIO81	ICOCZ	Pd-0[1]	Float[1]	3
G20	G22	GPIO82	GPIO82	ICOCZ	Pd-0[1]	Float[1]	3
G19	F23	GPIO83	GPIO83	ICOCZ	Pd-0[1]	Float[1]	3
G21	F20	GPIO84	GPIO84	ICOCZ	Pu-1[1]	Float[1]	3
F19	F22	GPIO85	GPIO85	ICOCZ	Pd-0[1]	Float[1]	3
E16	H24	GPIO86	GPIO86	ICOCZ	Pd-0[1]	Float[1]	3
F18	E23	GPIO87	GPIO87	ICOCZ	Pd-0[1]	Float[1]	3
F20	E22	GPIO88	GPIO88	ICOCZ	Pd-0[1]	Float[1]	3
E17	G24	GPIO89	GPIO89	ICOCZ	Pu-1[1]	Float[1]	3
F21	D23	GPIO90	GPIO90	ICOCZ	Pu-1[1]	Float[1]	3
VCC_CARD1							
U11	AB14	GPIO3	GPIO3	ICOCZ	Pd-0[1]	Float[1]	3
AA11	AC14	GPIO4	GPIO4	ICOCZ	Pd-0[1]	Float[1]	3
V12	AB15	GPIO5	GPIO5	ICOCZ	Pd-0[1]	Float[1]	3
V13	AD17	GPIO6	GPIO6	ICOCZ	Pu-1[1]	Float[1]	3
W14	AB17	GPIO7	GPIO7	ICOCZ	Pd-0[1]	Float[1]	3
U14	Y16	GPIO8	GPIO8	ICOCZ	Pd-0[1]	Float[1]	3
VCC_CARD2							
U12	AD16	GPIO9	GPIO9	ICOCZ	Pd-0[1]	Float[1]	3
Y14	AB18	GPIO10	GPIO10	ICOCZ	Pd-0[1]	Float[1]	3
V14	AB19	GPIO11	GPIO11	ICOCZ	Pd-0[1]	Float[1]	3
U16	AC20	GPIO12	GPIO12	ICOCZ	Pu-1[1]	Float[1]	3
V15	AC19	GPIO13	GPIO13	ICOCZ	Pd-0[1]	Float[1]	3

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
Y15	AD20	GPIO14	GPIO14	ICOCZ	Pd-0[1]	Float[1]	3
Y16	Y17	GPIO15	GPIO15	ICOCZ	Pu-1[1]	Float[1]	3
V16	AD19	GPIO16	GPIO16	ICOCZ	Pu-1[1]	Float[1]	3
RFU Balls							
A3	A3	RFU_A3/RFU_A3	—	—	—	—	—
A4	B2	RFU_A4/RFU_B2	—	—	—	—	—
A5	B3	RFU_A5/RFU_B3	—	—	—	—	—
B5	B4	RFU_B5/RFU_B4	—	—	—	—	—
N2	C3	RFU_N2/RFU_C3	—	—	—	—	—
W9	R1	RFU_W9/RFU_R1	—	—	—	—	—
	AD11	RFU_AD11	—	—	—	—	—
No Connect (NC) Balls							
B4	A1	NC	—	—	—	—	—
C1	A2	NC	—	—	—	—	—
C5	A23	NC	—	—	—	—	—
D19	A24	NC	—	—	—	—	—
G4	B1	NC	—	—	—	—	—
L4	B24	NC	—	—	—	—	—
L8	E17	NC	—	—	—	—	—
M8	E19	NC	—	—	—	—	—
P4	W5	NC	—	—	—	—	—
P5	W7	NC	—	—	—	—	—
U3	W8	NC	—	—	—	—	—
U13	W9	NC	—	—	—	—	—
V2	W12	NC	—	—	—	—	—

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
W2	Y9	NC	—	—	—	—	—
AA19	AB6	NC	—	—	—	—	—
	AC1	NC	—	—	—	—	—
	AC6	NC	—	—	—	—	—
	AC24	NC	—	—	—	—	—
	AD1	NC	—	—	—	—	—
	AD2	NC	—	—	—	—	—
	AD23	NC	—	—	—	—	—
	AD24	NC	—	—	—	—	—
Internal NAND Signals							
U5		DF_NWP	DF_NWP	Input	Input	Input	Input
Power Supplies							
A10	B17	VCC_APPS	VCC_APPS	PS	Input	Input	Input
A13	C14	VCC_APPS	VCC_APPS	PS	Input	Input	Input
A15	E11	VCC_APPS	VCC_APPS	PS	Input	Input	Input
H10	H10	VCC_APPS	VCC_APPS	PS	Input	Input	Input
H11	H15	VCC_APPS	VCC_APPS	PS	Input	Input	Input
H12	K8	VCC_APPS	VCC_APPS	PS	Input	Input	Input
K14	K17	VCC_APPS	VCC_APPS	PS	Input	Input	Input
L5	L5	VCC_APPS	VCC_APPS	PS	Input	Input	Input
L14	R8	VCC_APPS	VCC_APPS	PS	Input	Input	Input
M14	R17	VCC_APPS	VCC_APPS	PS	Input	Input	Input
N5	T24	VCC_APPS	VCC_APPS	PS	Input	Input	Input
N21	U10	VCC_APPS	VCC_APPS	PS	Input	Input	Input
P10	U15	VCC_APPS	VCC_APPS	PS	Input	Input	Input
P11	AB16	VCC_APPS	VCC_APPS	PS	Input	Input	Input
P12	AC9	VCC_APPS	VCC_APPS	PS	Input	Input	Input
Y13		VCC_APPS	VCC_APPS	PS	Input	Input	Input

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AA7		VCC_APPS	VCC_APPS	PS	Input	Input	Input
AA9		VCC_APPS	VCC_APPS	PS	Input	Input	Input
AA12		VCC_APPS	VCC_APPS	PS	Input	Input	Input
C8	E8	VCC_BBATT	VCC_BBATT	PS	Input	Input	Input
D10	C9	VCC_BG	VCC_BG	PS	Input	Input	Input
Y11	AC15	VCC_CARD1	VCC_CARD1	PS	Input	Input	Input
AA14	AD18	VCC_CARD2	VCC_CARD2	PS	Input	Input	Input
P15	R22	VCC_CI	VCC_CI	PS	Input	Input	Input
P20		VCC_CI	VCC_CI	PS	Input	Input	Input
G11	Y6	VCC_DF	VCC_DF	PS	Input	Input	Input
T9	AB4	VCC_DF	VCC_DF	PS	Input	Input	Input
T10	AB7	VCC_DF	VCC_DF	PS	Input	Input	Input
T11	AB10	VCC_DF	VCC_DF	PS	Input	Input	Input
T12	AB13	VCC_DF	VCC_DF	PS	Input	Input	Input
T13	AC12	VCC_DF	VCC_DF	PS	Input	Input	Input
E15	A11	VCC_IO1	VCC_IO1	PS	Input	Input	Input
G10	C16	VCC_IO1	VCC_IO1	PS	Input	Input	Input
G15	F24	VCC_IO1	VCC_IO1	PS	Input	Input	Input
T16	AB20	VCC_IO3	VCC_IO3	PS	Input	Input	Input
K16	K19	VCC_LCD	VCC_LCD	PS	Input	Input	Input
L16		VCC_LCD	VCC_LCD	PS	Input	Input	Input
M16		VCC_LCD	VCC_LCD	PS	Input	Input	Input
D5	D2	VCC_MEM	VCC_MEM	PS	Input	Input	Input
G5	E3	VCC_MEM	VCC_MEM	PS	Input	Input	Input
G6	F3	VCC_MEM	VCC_MEM	PS	Input	Input	Input
H6	G5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
J6	J5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
K6	K5	VCC_MEM	VCC_MEM	PS	Input	Input	Input

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
L6	N5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
M6	T5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
N6	V5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
P6	Y2	VCC_MEM	VCC_MEM	PS	Input	Input	Input
R6		VCC_MEM	VCC_MEM	PS	Input	Input	Input
T6		VCC_MEM	VCC_MEM	PS	Input	Input	Input
U6		VCC_MEM	VCC_MEM	PS	Input	Input	Input
V5		VCC_MEM	VCC_MEM	PS	Input	Input	Input
G17	H20	VCC_MSL	VCC_MSL	PS	Input	Input	Input
E4	B18	VCC_MVT	VCC_MVT	PS	Input	Input	Input
G9	C21	VCC_MVT	VCC_MVT	PS	Input	Input	Input
G14	F9	VCC_MVT	VCC_MVT	PS	Input	Input	Input
H15	H6	VCC_MVT	VCC_MVT	PS	Input	Input	Input
J5	N19	VCC_MVT	VCC_MVT	PS	Input	Input	Input
J15	P6	VCC_MVT	VCC_MVT	PS	Input	Input	Input
N15	U6	VCC_MVT	VCC_MVT	PS	Input	Input	Input
R14	W16	VCC_MVT	VCC_MVT	PS	Input	Input	Input
T5	AC8	VCC_MVT	VCC_MVT	PS	Input	Input	Input
U9		VCC_MVT	VCC_MVT	PS	Input	Input	Input
D9	B8	VCC_OSC13M	VCC_OSC13M	PS	Input	Input	Input
D12	C11	VCC_PLL	VCC_PLL	PS	Input	Input	Input
AA16	AC22	VCC_PLL	VCC_PLL	PS	Input	Input	Input
B19	B21	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
C18	W11	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
AA8		VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
B3	A4	VCC_BIAS	VCC_BIAS	PS	Input	Input	Input
R16	V22	VCC_ULPI	VCC_ULPI	PS	Input	Input	Input
A1		VSS	VSS	PS	Input	Input	Input

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
A2		VSS	VSS	PS	Input	Input	Input
B1		VSS	VSS	PS	Input	Input	Input
B2		VSS	VSS	PS	Input	Input	Input
	C17	VSS	VSS	PS	Input	Input	Input
	E7	VSS	VSS	PS	Input	Input	Input
A9	E12	VSS	VSS	PS	Input	Input	Input
A20	H8	VSS	VSS	PS	Input	Input	Input
A21	H9	VSS	VSS	PS	Input	Input	Input
	H11	VSS	VSS	PS	Input	Input	Input
	H13	VSS	VSS	PS	Input	Input	Input
B13	H14	VSS	VSS	PS	Input	Input	Input
B16	H17	VSS	VSS	PS	Input	Input	Input
B20	J8	VSS	VSS	PS	Input	Input	Input
B21	J17	VSS	VSS	PS	Input	Input	Input
C2	L8	VSS	VSS	PS	Input	Input	Input
F4	L17	VSS	VSS	PS	Input	Input	Input
H8	M6	VSS	VSS	PS	Input	Input	Input
H9	M8	VSS	VSS	PS	Input	Input	Input
H13	M17	VSS	VSS	PS	Input	Input	Input
H14	N8	VSS	VSS	PS	Input	Input	Input
J14	P8	VSS	VSS	PS	Input	Input	Input
K5	T8	VSS	VSS	PS	Input	Input	Input
M5	T23	VSS	VSS	PS	Input	Input	Input
N14	U5	VSS	VSS	PS	Input	Input	Input
N20	U8	VSS	VSS	PS	Input	Input	Input
P9	U9	VSS	VSS	PS	Input	Input	Input
P13	U11	VSS	VSS	PS	Input	Input	Input
P14	U12	VSS	VSS	PS	Input	Input	Input

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
R5	U13	VSS	VSS	PS	Input	Input	Input
R8	U14	VSS	VSS	PS	Input	Input	Input
T8	U16	VSS	VSS	PS	Input	Input	Input
T14	AC10	VSS	VSS	PS	Input	Input	Input
Y7	AC16	VSS	VSS	PS	Input	Input	Input
AA13	AC17	VSS	VSS	PS	Input	Input	Input
D7	AD8	VSS	VSS	PS	Input	Input	Input
D8	F8	VSS_BBATT	VSS_BBATT	PS	Input	Input	Input
C10	F10	VSS_BG	VSS_BG	PS	Input	Input	Input
Y12	Y15	VSS_CARD1	VSS_CARD1	PS	Input	Input	Input
AA15	AC18	VSS_CARD2	VSS_CARD2	PS	Input	Input	Input
P19	T19	VSS_CI	VSS_CI	PS	Input	Input	Input
G12	W14	VSS_DF	VSS_DF	PS	Input	Input	Input
R9	Y5	VSS_DF	VSS_DF	PS	Input	Input	Input
R10	Y8	VSS_DF	VSS_DF	PS	Input	Input	Input
R11	Y10	VSS_DF	VSS_DF	PS	Input	Input	Input
R12	Y11	VSS_DF	VSS_DF	PS	Input	Input	Input
R13	Y13	VSS_DF	VSS_DF	PS	Input	Input	Input
Y1		VSS_DF	VSS_DF	PS	Input	Input	Input
Y2		VSS_DF	VSS_DF	PS	Input	Input	Input
AA1		VSS_DF	VSS_DF	PS	Input	Input	Input
AA2		VSS_DF	VSS_DF	PS	Input	Input	Input
F15	A18	VSS_IO1	VSS_IO1	PS	Input	Input	Input
G13	B11	VSS_IO1	VSS_IO1	PS	Input	Input	Input
	B22	VSS_IO1	VSS_IO1	PS	Input	Input	Input
T15	AB24	VSS_IO3	VSS_IO3	PS	Input	Input	Input
Y20		VSS_IO3	VSS_IO3	PS	Input	Input	Input
Y21		VSS_IO3	VSS_IO3	PS	Input	Input	Input

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AA20		VSS_IO3	VSS_IO3	PS	Input	Input	Input
AA21		VSS_IO3	VSS_IO3	PS	Input	Input	Input
K15	M20	VSS_LCD	VSS_LCD	PS	Input	Input	Input
L15		VSS_LCD	VSS_LCD	PS	Input	Input	Input
M15		VSS_LCD	VSS_LCD	PS	Input	Input	Input
F6	C1	VSS_MEM	VSS_MEM	PS	Input	Input	Input
F7	C2	VSS_MEM	VSS_MEM	PS	Input	Input	Input
G7	F5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
H7	G6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
J7	H5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
K7	J6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
L7	K6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
M7	L6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
N7	N6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
P7	R6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
R7	T6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
T7	V6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
U7	Y3	VSS_MEM	VSS_MEM	PS	Input	Input	Input
R15	U20	VSS_ULPI	VSS_ULPI	PS	Input	Input	Input
F17	G20	VSS_MSL	VSS_MSL	PS	Input	Input	Input
E9	C10	VSS_OSC13M	VSS_OSC13M	PS	Input	Input	Input
E11	C13	VSS_PLL	VSS_PLL	PS	Input	Input	Input
E12	AD21	VSS_PLL	VSS_PLL	PS	Input	Input	Input
W16		VSS_PLL	VSS_PLL	PS	Input	Input	Input

Table 10: PXA31x Processor Pin Usage Summary (Continued)

15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode

NOTE:
1. GPIO reset/S3/D4/C4 operation: After any reset is asserted or if PXA31x processor is in S3/D4/C4 power mode, these pins are configured as the primary function of the MFP (generally as GPIO input) and default pullup or pulldown occurs.
2. Crystal oscillator pins: These pins connect the external crystals to the on-chip oscillators and are not affected by either reset or S2/D3/C4 power mode. For more information, see the “Clocks Control and Power Management” chapter in the *PXA3xx Processor Family Vol. I: System and Timer Configuration Developers Manual.*
3. Each MFP output value is based on MFPRxx[Sleep_sel], MFPRxx[sleep_data], MFPRxx[sleep_oe_n], MFPRxx[pull_sel], MFPRxx[pullup_en] and MFPRxx[pulldown_en] following S2/D3/C4 wake-up. To prevent unnecessary current drain, ensure input signals are not floating during low-power modes. Each GPIO to be driven can be programmed to a 0/1 or be pulled up or pulled down during S2/D3/C4 power mode if the MVT and the IO (HVT) supplies are present.
4. Logic low when OSCC[TENSx] bit is cleared, CLK_TOUT when OSCC[TENSx] is set. Configure TENS2 for S2/D3/C4 mode and TENS3 for S3/D4/C4 power mode.
5. Pulldown always enabled.
6. Output functions during S2/D3/C4 power mode.
7. Pullup always enabled.
8. Pd-0 if UP2OCR[DMPDE] is set, then Pd-0, Hi-Z if UP2OCR[DMPDE] is cleared.
9. Hi-Z if UP2OCR[DPPDE] is cleared and UP2OCR[DPPUE] is cleared; Pu-1 if UP2OCR[DPPDE] is cleared and UP2OCR[DPPUE] is set; Pd-0 if UP2OCR[DPPDE] is set and UP2OCR[DPPUE] is cleared. Setting UP2OCR[DPPDE] and UP2OCR[DPPUE] at the same time is not allowed.
10. This signal’s pullup/pulldown is enabled during power-on, hardware, global watchdog and GPIO resets. The pullup/pulldown must be disabled by software by setting PCFR[PUDH] after the external devices driving these pins are configured.
11. There is no pullup or pulldown on this pin. Asserts if PCFR[SL_ROD] is clear.

4.2.3 PXA30x Processor Pin Use

Table 11 lists the mapping of signals to specific PXA30x processor package pins.

Table 11: PXA30x Pin Usage Summary

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
VCC_BBATT								
D6	B6	A6	CLK_TOUT	CLK_TOUT	OC	Clk-Out	4	4
E7	B7	E6	EXT_WAKEUP0	EXT_WAKEUP0	ICOCZ	Pd-0[11]	Pd-0[11]	Pd-0[11]
A5	C6	C6	NBATT_FAULT	nBATT_FAULT	IC	Input	Input	Input
A7	E8	E9	NGPIO_RESET	nGPIO_RESET	IC	Pu-1[11]	Pu-1[11]	Pu-1[11]
E8	D6	B6	NRESET	nRESET	IC	Input[7]	Input	Input
D9	F9	A8	NRESET_OUT	nRESET_OUT	OC	Low	12	12

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
C5	A6	E5	NTRST	nTRST	IC	Input[7]	Input[7]	Input[7]
A6	A7	A7	PWR_CAP0	PWR_CAP0	OA	-	-	-
E9	F8	F7	PWR_CAP1	PWR_CAP1	OA	-	-	-
E4	D3	C5	PWR_EN	PWR_EN	OC	Low	Low	Low
B6	C7	B7	PWR_OUT	PWR_OUT	OA	-	-	-
B5	D4	F6	SYS_EN	SYS_EN	OC	Low	Low	Low
E6	C4	A5	TCK	TCK	IC	Input	Input	Input
E5	E3	B5	TDI	TDI	IC	Input[7]	Input[7]	Input[7]
D5	D2	C4	TDO	TDO	OCZ	Hi-Z	Hi-Z	Hi-Z
D4	C3	D3	TMS	TMS	IC	Input[7]	Input[7]	Input[7]
D8	A8	C7	TXTAL_IN	TXTAL_IN	IA	2	2	2
C7	B8	C8	TXTAL_OUT	TXTAL_OUT	OA	2	2	2
VCC_MVT								
B8	B9	A9	PXTAL_IN	PXTAL_IN	IA	2	2	2
C8	C9	B9	PXTAL_OUT	PXTAL_OUT	OA	2	2	2
VCC_IO1								
B12	A11	A13	GPIO0_2	GPIO0_2	ICOCZ	Pd-0[1]	Float[1]	3
A11	D11	A12	GPIO1_2	GPIO1_2	ICOCZ	Pd-0[1]	Float[1]	3
E21	E18	D22	GPIO91	GPIO91	ICOCZ	Pu-1[1]	Float[1]	3
D22	E21	C22	GPIO92	GPIO92	ICOCZ	Pu-1[1]	Float[1]	3
C23	E20	E24	GPIO93	GPIO93	ICOCZ	Pd-0[1]	Float[1]	3
E20	D21	C23	GPIO94	GPIO94	ICOCZ	Pd-0[1]	Float[1]	3
D21	C20	D24	GPIO95	GPIO95	ICOCZ	Pd-0[1]	Float[1]	3
C22	A19	B23	GPIO96	GPIO96	ICOCZ	Pd-0[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
C21	D20	A22	GPIO97	GPIO97	ICOCZ	Pd-0[1]	Float[1]	3
D20	C21	C24	GPIO98	GPIO98	ICOCZ	Pd-0[1]	Float[1]	3
E18	A18	B16	GPIO99	GPIO99	ICOCZ	Pd-0[1]	Float[1]	3
B20	B18	A21	GPIO100	GPIO100	ICOCZ	Pd-0[1]	Float[1]	3
A21	C19	B19	GPIO101	GPIO101	ICOCZ	Pu-1[1]	Float[1]	3
A20	A17	A20	GPIO102	GPIO102	ICOCZ	Pu-1[1]	Float[1]	3
B19	D18	C20	GPIO103	GPIO103	ICOCZ	Pu-1[1]	Float[1]	3
D17	E19	C19	GPIO104	GPIO104	ICOCZ	Pu-1[1]	Float[1]	3
C18	D17	F17	GPIO105	GPIO105	ICOCZ	Pu-1[1]	Float[1]	3
A19	B17	B20	GPIO106	GPIO106	ICOCZ	Pu-1[1]	Float[1]	3
C17	C16	A17	GPIO107	GPIO107	ICOCZ	Pu-1[1]	Float[1]	3
B18	C17	C18	GPIO108	GPIO108	ICOCZ	Pu-1[1]	Float[1]	3
A18	D16	F16	GPIO109	GPIO109	ICOCZ	Pd-0[1]	Float[1]	3
B17	A16	A19	GPIO110	GPIO110	ICOCZ	Pu-1[1]	Float[1]	3
C16	F14	E15	GPIO111	GPIO111	ICOCZ	Pu-1[1]	Float[1]	3
A17	B15	H16	GPIO112	GPIO112	ICOCZ	Pd-0[1]	Float[1]	3
E15	C15	B15	GPIO113	GPIO113	ICOCZ	Pd-0[1]	Float[1]	3
B16	D15	E16	GPIO114	GPIO114	ICOCZ	Pu-1[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
A16	C13	A15	GPIO115	GPIO115	ICOCZ	Pd-0[1]	Float[1]	3
C15	A14	A16	GPIO116	GPIO116	ICOCZ	Pd-0[1]	Float[1]	3
B15	E14	E14	GPIO117	GPIO117	ICOCZ	Pd-0[1]	Float[1]	3
C14	D14	C15	GPIO118	GPIO118	ICOCZ	Pd-0[1]	Float[1]	3
D15	E13	B14	GPIO119	GPIO119	ICOCZ	Pd-0[1]	Float[1]	3
A15	B14	F15	GPIO120	GPIO120	ICOCZ	Pd-0[1]	Float[1]	3
B14	F13	E13	GPIO121	GPIO121	ICOCZ	Pd-0[1]	Float[1]	3
A14	C14	F14	GPIO122	GPIO122	ICOCZ	Pd-0[1]	Float[1]	3
D14	D13	B13	GPIO123	GPIO123	ICOCZ	Pu-1[1]	Float[1]	3
B13	B12	F13	GPIO124	GPIO124	ICOCZ	Pd-0[1]	Float[1]	3
A13	F12	F12	GPIO125	GPIO125	ICOCZ	Pd-0[1]	Float[1]	3
C12	A12	A14	GPIO126	GPIO126	ICOCZ	Pu-1[1]	Float[1]	3
A12	C12	C12	GPIO127	GPIO127	ICOCZ	Pu-1[1]	Float[1]	3
A9	F10	A10	PWR_SCL	PWR_SCL	ICOCZ	Pu-1[11]	Pu-1[11]	Float[1]
C10	B10	F11	PWR_SDA	PWR_SDA	ICOCZ	Pu-1[11]	Pu-1[11]	Float[1]
A10	B11	H12	TEST	TEST	IC	Input[5]	Input[5]	Input[5]
B10	F11	E10	TESTCLK	TESTCLK	IC	Input[5]	Input[5]	Input[5]
E12	E10	B10	VCTCXO_EN	VCTCXO_EN	OC	Low	6	6
C11	C11	B12	CLK_POUT	CLK_POUT	OC	Low	Float	Low

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
VCC_DF								
Y5	AA4	AC4	DF_ADDR0	DF_ADDR0	OCZ	Pd-0[1]	Float[1]	3
Y2	V6	AB5	DF_ADDR1	DF_ADDR1	OCZ	Pd-0[1]	Float[1]	3
Y1	W6	AD4	DF_ADDR2	DF_ADDR2	OCZ	Pd-0[1]	Float[1]	3
Y6	Y4	AC5	DF_ADDR3	DF_ADDR3	OCZ	Pd-0[1]	Float[1]	3
AA1	AA5	Y7	DF_IO0	DF_IO0	ICOCZ	Pd-0[1]	Float[1]	3
AA3	AA6	AC7	DF_IO1	DF_IO1	ICOCZ	Pd-0[1]	Float[1]	3
AA4	W7	AD6	DF_IO2	DF_IO2	ICOCZ	Pd-0[1]	Float[1]	3
AB5	Y8	AB9	DF_IO3	DF_IO3	ICOCZ	Pd-0[1]	Float[1]	3
AC3	V10	AD12	DF_IO4	DF_IO4	ICOCZ	Pd-0[1]	Float[1]	3
AC4	W13	AD13	DF_IO5	DF_IO5	ICOCZ	Pd-0[1]	Float[1]	3
AA10	W12	AD14	DF_IO6	DF_IO6	ICOCZ	Pd-0[1]	Float[1]	3
AB9	V11	Y12	DF_IO7	DF_IO7	ICOCZ	Pd-0[1]	Float[1]	3
AA2	U8	AD5	DF_IO8	DF_IO8	ICOCZ	Pd-0[1]	Float[1]	3
Y7	Y5	AB8	DF_IO9	DF_IO9	ICOCZ	Pd-0[1]	Float[1]	3
Y8	Y6	AD7	DF_IO10	DF_IO10	ICOCZ	Pd-0[1]	Float[1]	3
AB4	W8	AD9	DF_IO11	DF_IO11	ICOCZ	Pd-0[1]	Float[1]	3
AB8	U15	W13	DF_IO12	DF_IO12	ICOCZ	Pd-0[1]	Float[1]	3
AC5	W10	AB12	DF_IO13	DF_IO13	ICOCZ	Pd-0[1]	Float[1]	3
AC6	W11	Y14	DF_IO14	DF_IO14	ICOCZ	Pd-0[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AC7	W15	AD15	DF_IO15	DF_IO15	ICOCZ	Pd-0[1]	Float[1]	3
Y3	V7	AC2	DF_ALE_NWE	DF_ALE	OCZ	Pu-1[1]	Float[1]	3
AB6	V9	W10	DF_NCS0	DF_nCS0	OCZ	Pu-1[1]	Float[1]	3
AB10	U10	AC13	DF_NCS1	DF_nCS1	OCZ	Pu-1[1]	Float[1]	3
W4	W5	AB3	DF_NRE	DF_nOE	OCZ	Pu-1[1]	Float[1]	3
W3	W4	AB2	DF_NWE	DF_nWE	OCZ	Pu-1[1]	Float[1]	3
W2	W3	AA3	DF_INT_RNB	DF_RnB	ICZ	Pu-1[1]	Float[1]	3
AB3	V8	W6	DF_CLE_NOE	ND_CLE	OCZ	Pu-1[1]	Float[1]	3
AA9	AA10	AC11	DF_SCLK_E	DF_SCLK_E	OCZ	Pd-0[1]	Float[1]	3
V1	V3	W1	GPIO0	GPIO0	ICOCZ	Pd-0[1]	Float[1]	3
V2	U4	AA2	GPIO1	GPIO1	ICOCZ	Pu-1[1]	Float[1]	3
V3	V1	Y1	GPIO2	GPIO2	ICOCZ	Pu-1[1]	Float[1]	3
W5	Y3	AD3	NBE0	nBE0	OCZ	Pu-1[1]	Float[1]	3
Y4	AA3	AC3	NBE1	nBE1	OCZ	Pu-1[1]	Float[1]	3
AB7	Y10	AB11	NLLA	nLLA	OCZ	Pu-1[1]	Float[1]	3
AA8	Y9	AD10	NLUA	nLUA	OCZ	Pu-1[1]	Float[1]	3
W1	W1	AB1	NCS0	nCS0	OC	High	High	High
U5	V4	AA1	NCS1	nCS1	OC	High	High	High
VCC_IO3								
AC15	W17	AC21	GPIO17	GPIO17	ICOCZ	Pd-0[1]	Float[1]	3
AB15	W18	W17	GPIO18	GPIO18	ICOCZ	Pd-0[1]	Float[1]	3
Y16	U17	AB21	GPIO19	GPIO19	ICOCZ	Pd-0[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AC16	V18	AB23	GPIO20	GPIO20	ICOCZ	Pu-1[1]	Float[1]	3
AC17	W19	Y22	GPIO21	GPIO21	ICOCZ	Pu-1[1]	Float[1]	3
AB17	AA17	AC23	GPIO22	GPIO22	ICOCZ	Pu-1[1]	Float[1]	3
AA17	Y17	AB22	GPIO23	GPIO23	ICOCZ	Pu-1[1]	Float[1]	3
Y17	AA18	AD22	GPIO24	GPIO24	ICOCZ	Pd-0[1]	Float[1]	3
W17	Y18	AA23	GPIO25	GPIO25	ICOCZ	Pd-0[1]	Float[1]	3
AC18	Y19	AA24	GPIO26	GPIO26	ICOCZ	Pd-0[1]	Float[1]	3
U19	V21	W19	GPIO27	GPIO27	ICOCZ	Pd-0[1]	Float[1]	3
AC20	U21	Y23	GPIO28	GPIO28	ICOCZ	Pd-0[1]	Float[1]	3
AC21	V19	Y24	GPIO29	GPIO29	ICOCZ	Pd-0[1]	Float[1]	3
W20	V20	AA22	GPIO30	GPIO30	ICOCZ	Pd-0[1]	Float[1]	3
Y21	U18	W22	GPIO31	GPIO31	ICOCZ	Pd-0[1]	Float[1]	3
AB21	U20	W23	GPIO32	GPIO32	ICOCZ	Pu-1[1]	Float[1]	3
AA21	U19	W18	GPIO33	GPIO33	ICOCZ	Pu-1[1]	Float[1]	3
AA22	T20	W24	GPIO34	GPIO34	ICOCZ	Pu-1[1]	Float[1]	3
AA23	T18	V20	GPIO35	GPIO35	ICOCZ	Pu-1[1]	Float[1]	3
V21	T21	V23	GPIO36	GPIO36	ICOCZ	Pu-1[1]	Float[1]	3
Y22	R17	V19	GPIO37	GPIO37	ICOCZ	Pu-1[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
Y23	T17	U22	GPIO38	GPIO38	ICOCZ	Pd-0[1]	Float[1]	3
AB18	E6	W15	GPIO2_2	GPIO2_2	ICOCZ	Pu-1[1]	Float[1]	3
AA18	E5	W20	GPIO3_2	GPIO3_2	ICOCZ	Pd-0[1]	Float[1]	3
Y18	G8	Y18	GPIO4_2	GPIO4_2	ICOCZ	Pd-0[1]	Float[1]	3
AC19	F5	Y20	GPIO5_2	GPIO5_2	ICOCZ	Pd-0[1]	Float[1]	3
W18	E7	Y19	GPIO6_2	GPIO6_2	ICOCZ	Pu-1[1]	Float[1]	3
VCC_CI								
W22	R18	U19	GPIO39	GPIO39	ICOCZ	Pd-0[1]	Float[1]	3
W23	T19	V24	GPIO40	GPIO40	ICOCZ	Pd-0[1]	Float[1]	3
T20	R20	U23	GPIO41	GPIO41	ICOCZ	Pd-0[1]	Float[1]	3
V22	R19	T22	GPIO42	GPIO42	ICOCZ	Pd-0[1]	Float[1]	3
V23	P16	U24	GPIO43	GPIO43	ICOCZ	Pd-0[1]	Float[1]	3
U21	R21	T20	GPIO44	GPIO44	ICOCZ	Pd-0[1]	Float[1]	3
U22	P17	R20	GPIO45	GPIO45	ICOCZ	Pd-0[1]	Float[1]	3
U23	P18	T17	GPIO46	CIF_DD7	ICOCZ	Pd-0[1]	Float[1]	3
T21	N16	P22	GPIO47	GPIO47	ICOCZ	Pd-0[1]	Float[1]	3
T22	P21	R19	GPIO48	GPIO48	ICOCZ	Pd-0[1]	Float[1]	3
T23	N17	P20	GPIO49	CIF_MCLK	ICOCZ	Pd-0[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
R21	N18	R24	GPIO50	CIF_PCLK	ICOCZ	Pd-0[1]	Float[1]	3
R22	N19	N24	GPIO51	CIF_HSYNC	ICOCZ	Pd-0[1]	Float[1]	3
P20	M20	N20	GPIO52	CIF_VSYNC	ICOCZ	Pd-0[1]	Float[1]	3
VCC_LCD								
R23	M17	R23	GPIO53	GPIO53	ICOCZ	Pu-1[1]	Float[1]	3
N20	M21	P23	GPIO54	GPIO54	ICOCZ	Pd-0[1]	Float[1]	3
P21	M18	N22	GPIO55	GPIO55	ICOCZ	Pd-0[1]	Float[1]	3
P22	L18	P24	GPIO56	GPIO56	ICOCZ	Pd-0[1]	Float[1]	3
N19	M19	N23	GPIO57	GPIO57	ICOCZ	Pd-0[1]	Float[1]	3
P23	L20	P19	GPIO58	GPIO58	ICOCZ	Pd-0[1]	Float[1]	3
N21	L17	M19	GPIO59	GPIO59	ICOCZ	Pd-0[1]	Float[1]	3
N22	L21	L19	GPIO60	GPIO60	ICZ	Pd-0[1]	Float[1]	3
N23	K19	M22	GPIO61	GPIO61	ICOCZ	Pd-0[1]	Float[1]	3
M23	L19	M23	GPIO62	GPIO62	ICOCZ	Pu-1[1]	Float[1]	3
M21	K20	J19	GPIO63	GPIO63	ICOCZ	Pd-0[1]	Float[1]	3
M22	K17	M24	GPIO64	GPIO64	ICOCZ	Pd-0[1]	Float[1]	3
L21	J17	L22	GPIO65	GPIO65	ICOCZ	Pd-0[1]	Float[1]	3
L23	K21	K22	GPIO66	GPIO66	ICOCZ	Pd-0[1]	Float[1]	3
L20	J18	L23	GPIO67	GPIO67	ICOCZ	Pd-0[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
L22	K18	L20	GPIO68	GPIO68	ICOCZ	Pd-0[1]	Float[1]	3
L19	J19	K20	GPIO69	GPIO69	ICOCZ	Pd-0[1]	Float[1]	3
K23	J20	L24	GPIO70	GPIO70	ICOCZ	Pd-0[1]	Float[1]	3
K21	J16	H19	GPIO71	GPIO71	ICOCZ	Pd-0[1]	Float[1]	3
K22	J21	K23	GPIO72	GPIO72	ICOCZ	Pd-0[1]	Float[1]	3
J23	H16	K24	GPIO73	GPIO73	ICOCZ	Pd-0[1]	Float[1]	3
J22	H17	J22	GPIO74	GPIO74	ICOCZ	Pd-0[1]	Float[1]	3
J19	H18	G19	GPIO75	GPIO75	ICOCZ	Pd-0[1]	Float[1]	3
J21	H20	J23	GPIO76	GPIO76	ICOCZ	Pd-0[1]	Float[1]	3
VCC_MEM								
E3	G3	F2	DQM0	DQM0	OC	High	High	High
T1	T4	U1	DQM1	DQM1	OC	High	High	High
D2	F3	G3	DQS0	DQS0	ISOCZ	Pd-0	Pd-0	Pd-0
T2	R4	V3	DQS1	DQS1	ISOCZ	Pd-0	Pd-0	Pd-0
L3	L3	M1	MA0	MA0	OC	High	High	High
N1	N4	R5	MA1	MA1	OC	High	High	High
J4	H3	H2	MA2	MA2	OC	High	High	High
N4	M1	P5	MA3	MA3	OC	High	High	High
H3	H4	K3	MA4	MA4	OC	High	High	High
M1	M3	P3	MA5	MA5	OC	High	High	High
H2	K4	J1	MA6	MA6	OC	High	High	High
M2	M2	N3	MA7	MA7	OC	High	High	High

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
H1	J1	K2	MA8	MA8	OC	High	High	High
M3	L2	N1	MA9	MA9	OC	High	High	High
L2	M4	N2	MA11	MA11	OC	High	High	High
J3	K3	L3	MA12	MA12	OC	High	High	High
L1	H5	M5	MA13	MA13	OC	High	High	High
G1	H2	J3	MA14	MA14	OC	High	High	High
G2	J4	J2	MA15	MA15	OC	High	High	High
D3	D1	D1	MD0	MD0	ICSO CZ	Pd-0	Pd-0	Pd-0
C2	E1	E1	MD1	MD1	ICSO CZ	Pd-0	Pd-0	Pd-0
C1	E2	E2	MD2	MD2	ICSO CZ	Pd-0	Pd-0	Pd-0
G4	F1	F1	MD3	MD3	ICSO CZ	Pd-0	Pd-0	Pd-0
F3	F2	G1	MD4	MD4	ICSO CZ	Pd-0	Pd-0	Pd-0
E1	G1	G2	MD5	MD5	ICSO CZ	Pd-0	Pd-0	Pd-0
F2	G2	H3	MD6	MD6	ICSO CZ	Pd-0	Pd-0	Pd-0
F1	H1	H1	MD7	MD7	ICSO CZ	Pd-0	Pd-0	Pd-0
R1	P3	T2	MD8	MD8	ICSO CZ	Pd-0	Pd-0	Pd-0
R2	R3	T1	MD9	MD9	ICSO CZ	Pd-0	Pd-0	Pd-0
R3	R1	U3	MD10	MD10	ICSO CZ	Pd-0	Pd-0	Pd-0
R4	T2	U2	MD11	MD11	ICSO CZ	Pd-0	Pd-0	Pd-0
T3	T1	V2	MD12	MD12	ICSO CZ	Pd-0	Pd-0	Pd-0
U1	U2	V1	MD13	MD13	ICSO CZ	Pd-0	Pd-0	Pd-0

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
U2	T3	W2	MD14	MD14	ICSOCZ	Pd-0	Pd-0	Pd-0
U3	U1	W3	MD15	MD15	ICSOCZ	Pd-0	Pd-0	Pd-0
N3	N3	T3	NSDCAS	nSDCAS	OC	High	High	High
K1	L1	M3	NSDCS0	nSDCS0	OC	High	High	High
K2	J2	M2	NSDCS1	nSDCS1	OC	High	High	High
N2	P2	P2	NSDRAS	nSDRAS	OC	High	High	High
P1	P1	R3	NSDWE	nSDWE	OC	High	High	High
N5	N1	P1	RCOMP_DDR	RCOMP_DDR	OA	-	-	-
P2	R2	R2	SDCKE	SDCKE	OC	Low	Low	Low
K3	K1	L1	SDCLK0	SDCLK0	OC	Low	Low	Low
K4	K2	L2	SDCLK1	SDCLK1	OC	High	High	High
K5	J3	K1	SDMA10	SDMA10	OC	High	High	High
VCC_MSL								
H23	H19	H22	GPIO77	GPIO77	ICOCZ	Pd-0[1]	Float[1]	3
H22	G16	J24	GPIO78	GPIO78	ICOCZ	Pd-0[1]	Float[1]	3
J20	F16	J20	GPIO79	GPIO79	ICOCZ	Pd-0[1]	Float[1]	3
G23	H21	H23	GPIO80	GPIO80	ICOCZ	Pd-0[1]	Float[1]	3
G22	G18	G23	GPIO81	GPIO81	ICOCZ	Pd-0[1]	Float[1]	3
H21	G20	G22	GPIO82	GPIO82	ICOCZ	Pd-0[1]	Float[1]	3
F23	G19	F23	GPIO83	GPIO83	ICOCZ	Pd-0[1]	Float[1]	3
G21	G21	F20	GPIO84	GPIO84	ICOCZ	Pu-1[1]	Float[1]	3
F22	F19	F22	GPIO85	GPIO85	ICOCZ	Pd-0[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
E23	E16	H24	GPIO86	GPIO86	ICOCZ	Pd-0[1]	Float[1]	3
E22	F18	E23	GPIO87	GPIO87	ICOCZ	Pd-0[1]	Float[1]	3
F21	F20	E22	GPIO88	GPIO88	ICOCZ	Pd-0[1]	Float[1]	3
F20	E17	G24	GPIO89	GPIO89	ICOCZ	Pu-1[1]	Float[1]	3
D23	F21	D23	GPIO90	GPIO90	ICOCZ	Pu-1[1]	Float[1]	3
VCC_USB								
A3	A5	C3	USBH1_N	USBH1_N	IAOA	Pd-0 [8]	Pd-0[8]	Pd-0[8]
A4	B5	B4	USBH1_P	USBH1_P	IAOA	Pd-0[8]	Pd-0[8]	Pd-0[8]
C3	A3	B3	USBOTG_N	USBOTG_N	IAOA	Hi-Z	Hi-Z or Pd-0[9]	Hi-Z or Pd-0[9]
B3	A4	A3	USBOTG_P	USBOTG_P	IAOA	Hi-Z	Hi-Z or Pd-0 or Pu-1[8, 10]	Hi-Z or Pd-0 or Pu-1[8, 10]
VCC_CARD1								
AA11	U11	AB14	GPIO3	GPIO3	ICOCZ	Pd-0[1]	Float[1]	3
AC8	AA11	AC14	GPIO4	GPIO4	ICOCZ	Pd-0[1]	Float[1]	3
AB11	V12	AB15	GPIO5	GPIO5	ICOCZ	Pd-0[1]	Float[1]	3
AC9	V13	AD17	GPIO6	GPIO6	ICOCZ	Pu-1[1]	Float[1]	3
AC10	W14	AB17	GPIO7	GPIO7	ICOCZ	Pd-0[1]	Float[1]	3
AA13	U14	Y16	GPIO8	GPIO8	ICOCZ	Pd-0[1]	Float[1]	3
VCC_CARD2								
AC11	U12	AD16	GPIO9	GPIO9	ICOCZ	Pd-0[1]	Float[1]	3
AC12	Y14	AB18	GPIO10	GPIO10	ICOCZ	Pd-0[1]	Float[1]	3

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AB13	V14	AB19	GPIO11	GPIO11	ICOCZ	Pd-0[1]	Float[1]	3
AC13	U16	AC20	GPIO12	GPIO12	ICOCZ	Pu-1[1]	Float[1]	3
AB14	V15	AC19	GPIO13	GPIO13	ICOCZ	Pd-0[1]	Float[1]	3
AC14	Y15	AD20	GPIO14	GPIO14	ICOCZ	Pd-0[1]	Float[1]	3
Y15	Y16	Y17	GPIO15	GPIO15	ICOCZ	Pu-1[1]	Float[1]	3
AA15	V16	AD19	GPIO16	GPIO16	ICOCZ	Pu-1[1]	Float[1]	3
RFU Balls								
P4	J8	E18	RFU_P4/ RFU_J8/ RFU_E18					
B21	K8	E20	RFU_B21/ RFU_K8/ RFU_E20					
C19	N2	F18	RFU_C19/ RFU_N2/ RFU_F18					
C20	N8	F19	RFU_C20/ RFU_N8/ RFU_F19					
D18	P8	N17	RFU_D18/ RFU_P8/ RFU_N17	—	—	—	—	—
	R15	P17	RFU_R15/RFU_P17	—	—	—	—	—
	R16	R1	RFU_R16/RFU_R1	—	—	—	—	—
	V17	U17	RFU_V17/RFU_U17	—	—	—	—	—
	W9	AD11	RFU_W9/RFU_AD11	—	—	—	—	—
	W20		RFU_W20	—	—	—	—	—

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
	W21		RFU_W21	—	—	—	—	—
No Connect (NC) Balls								
A1	B4	A1	NC	—	—	—	—	—
A2	C1	A2	NC	—	—	—	—	—
B1	C5	A23	NC	—	—	—	—	—
B2	D19	A24	NC	—	—	—	—	—
A22	G4	B1	NC	—	—	—	—	—
A23	L4	B24	NC	—	—	—	—	—
B22	L8	E17	NC	—	—	—	—	—
B23	M8	E19	NC	—	—	—	—	—
V19	P4	W5	NC	—	—	—	—	—
V20	P5	W7	NC	—	—	—	—	—
W10	U3	W8	NC	—	—	—	—	—
W19	V2	W9	NC	—	—	—	—	—
Y19	U13	W12	NC	—	—	—	—	—
Y20	W2	Y9	NC	—	—	—	—	—
AA19	AA19	AB6	NC	—	—	—	—	—
AA20		AC1	NC	—	—	—	—	—
AB19		AC6	NC	—	—	—	—	—
AB20		AC24	NC	—	—	—	—	—
AB1		AD1	NC	—	—	—	—	—
AB2		AD2	NC	—	—	—	—	—
AC1		AD23	NC	—	—	—	—	—
AC2		AD24	NC	—	—	—	—	—
AB22			NC	—	—	—	—	—
AB23			NC	—	—	—	—	—
AC22			NC	—	—	—	—	—
AC23			NC	—	—	—	—	—

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
AA5			NC	—	—	—	—	—
Internal NAND Signals								
	U5		DF_NWP	DF_NWP	Input	Input	Input	Input
Power Supplies								
E11	A10	B17	VCC_APPS	VCC_APPS	PS	Input	Input	Input
E14	A13	C14	VCC_APPS	VCC_APPS	PS	Input	Input	Input
L4	A15	E11	VCC_APPS	VCC_APPS	PS	Input	Input	Input
R20	H10	H10	VCC_APPS	VCC_APPS	PS	Input	Input	Input
W9	H11	H15	VCC_APPS	VCC_APPS	PS	Input	Input	Input
W13	H12	K8	VCC_APPS	VCC_APPS	PS	Input	Input	Input
Y12	K14	K17	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	L5	L5	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	L14	R8	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	M14	R17	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	N5	T24	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	N21	U10	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	P10	U15	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	P11	AB16	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	P12	AC9	VCC_APPS	VCC_APPS	PS	Input	Input	Input
	Y13		VCC_APPS	VCC_APPS	PS	Input	Input	Input
	AA7		VCC_APPS	VCC_APPS	PS	Input	Input	Input
	AA9		VCC_APPS	VCC_APPS	PS	Input	Input	Input
	AA12		VCC_APPS	VCC_APPS	PS	Input	Input	Input
D7	C8	E8	VCC_BBATT	VCC_BBATT	PS	Input	Input	Input
B9	D10	C9	VCC_BG	VCC_BG	PS	Input	Input	Input
AA12	Y11	AC15	VCC_CARD1	VCC_CARD1	PS	Input	Input	Input
Y14	AA14	AD18	VCC_CARD2	VCC_CARD2	PS	Input	Input	Input

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
R19	P15	R22	VCC_CI	VCC_CI	PS	Input	Input	Input
	P20		VCC_CI	VCC_CI	PS	Input	Input	Input
V4	G11	Y6	VCC_DF	VCC_DF	PS	Input	Input	Input
W6	T9	AB4	VCC_DF	VCC_DF	PS	Input	Input	Input
W8	T10	AB7	VCC_DF	VCC_DF	PS	Input	Input	Input
Y11	T11	AB10	VCC_DF	VCC_DF	PS	Input	Input	Input
	T12	AB13	VCC_DF	VCC_DF	PS	Input	Input	Input
	T13	AC12	VCC_DF	VCC_DF	PS	Input	Input	Input
B11	E15	A11	VCC_IO1	VCC_IO1	PS	Input	Input	Input
E16	G10	C16	VCC_IO1	VCC_IO1	PS	Input	Input	Input
F19	G15	F24	VCC_IO1	VCC_IO1	PS	Input	Input	Input
W21		V22	VCC_IO3	VCC_IO3	PS	Input	Input	Input
AA16	T16	AB20	VCC_IO3	VCC_IO3	PS	Input	Input	Input
K19	K16	K19	VCC_LCD	VCC_LCD	PS	Input	Input	Input
M19	L16		VCC_LCD	VCC_LCD	PS	Input	Input	Input
	M16		VCC_LCD	VCC_LCD	PS	Input	Input	Input
D1	D5	D2	VCC_MEM	VCC_MEM	PS	Input	Input	Input
G3	G5	E3	VCC_MEM	VCC_MEM	PS	Input	Input	Input
G5	G6	F3	VCC_MEM	VCC_MEM	PS	Input	Input	Input
J1	H6	G5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
M5	J6	J5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
R5	K6	K5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
T5	L6	N5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
	M6	T5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
	N6	V5	VCC_MEM	VCC_MEM	PS	Input	Input	Input
	P6	Y2	VCC_MEM	VCC_MEM	PS	Input	Input	Input
	R6		VCC_MEM	VCC_MEM	PS	Input	Input	Input
	T6		VCC_MEM	VCC_MEM	PS	Input	Input	Input

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
	U6		VCC_MEM	VCC_MEM	PS	Input	Input	Input
	V5		VCC_MEM	VCC_MEM	PS	Input	Input	Input
H20	G17	H20	VCC_MSL	VCC_MSL	PS	Input	Input	Input
D10	E4	B18	VCC_MVT	VCC_MVT	PS	Input	Input	Input
E17	G9	C21	VCC_MVT	VCC_MVT	PS	Input	Input	Input
G20	G14	F9	VCC_MVT	VCC_MVT	PS	Input	Input	Input
H5	H15	H6	VCC_MVT	VCC_MVT	PS	Input	Input	Input
P3	J5	N19	VCC_MVT	VCC_MVT	PS	Input	Input	Input
P19	J15	P6	VCC_MVT	VCC_MVT	PS	Input	Input	Input
W14	N15	U6	VCC_MVT	VCC_MVT	PS	Input	Input	Input
AA7	R14	W16	VCC_MVT	VCC_MVT	PS	Input	Input	Input
	T5	AC8	VCC_MVT	VCC_MVT	PS	Input	Input	Input
	U9		VCC_MVT	VCC_MVT	PS	Input	Input	Input
A8	D9	B8	VCC_OSC13M	VCC_OSC13M	PS	Input	Input	Input
C13	D12	C11	VCC_PLL	VCC_PLL	PS	Input	Input	Input
W16	AA16	AC22	VCC_PLL	VCC_PLL	PS	Input	Input	Input
D19	B19	B21	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
Y9	C18	W11	VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
	AA8		VCC_SRAM	VCC_SRAM	PS	Input	Input	Input
B4	B3	A4	VCC_USB	VCC_USB	PS	Input	Input	Input
J9	A9	C17	VSS	VSS	PS	Input	Input	Input
J10	A20	E7	VSS	VSS	PS	Input	Input	Input
J11	A21	E12	VSS	VSS	PS	Input	Input	Input
J12	B13	H8	VSS	VSS	PS	Input	Input	Input
J13	B16	H9	VSS	VSS	PS	Input	Input	Input
J14	B20	H11	VSS	VSS	PS	Input	Input	Input
J15	B21	H13	VSS	VSS	PS	Input	Input	Input
E10	C2	H14	VSS	VSS	PS	Input	Input	Input

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
E13	F4	H17	VSS	VSS	PS	Input	Input	Input
G19	H8	J8	VSS	VSS	PS	Input	Input	Input
J5	H9	J17	VSS	VSS	PS	Input	Input	Input
L5	H13	L8	VSS	VSS	PS	Input	Input	Input
K9	H14	L17	VSS	VSS	PS	Input	Input	Input
K10	J14	M6	VSS	VSS	PS	Input	Input	Input
K11	K5	M8	VSS	VSS	PS	Input	Input	Input
K12	M5	M17	VSS	VSS	PS	Input	Input	Input
K13	N14	N8	VSS	VSS	PS	Input	Input	Input
K14	N20	P8	VSS	VSS	PS	Input	Input	Input
K15	P9	T8	VSS	VSS	PS	Input	Input	Input
L9	P13	T23	VSS	VSS	PS	Input	Input	Input
L10	P14	U5	VSS	VSS	PS	Input	Input	Input
L11	R5	U8	VSS	VSS	PS	Input	Input	Input
L12	R8	U9	VSS	VSS	PS	Input	Input	Input
L13	T8	U11	VSS	VSS	PS	Input	Input	Input
L14	T14	U12	VSS	VSS	PS	Input	Input	Input
L15	Y7	U13	VSS	VSS	PS	Input	Input	Input
M9	AA13	U14	VSS	VSS	PS	Input	Input	Input
M10	D7	U16	VSS	VSS	PS	Input	Input	Input
M11		AC10	VSS	VSS	PS	Input	Input	Input
M12		AC16	VSS	VSS	PS	Input	Input	Input
M13		AC17	VSS	VSS	PS	Input	Input	Input
M14		AD8	VSS	VSS	PS	Input	Input	Input
M15			VSS	VSS	PS	Input	Input	Input
N9			VSS	VSS	PS	Input	Input	Input
N10			VSS	VSS	PS	Input	Input	Input
N11			VSS	VSS	PS	Input	Input	Input

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
N12			VSS	VSS	PS	Input	Input	Input
N13			VSS	VSS	PS	Input	Input	Input
N14			VSS	VSS	PS	Input	Input	Input
N15			VSS	VSS	PS	Input	Input	Input
P9			VSS	VSS	PS	Input	Input	Input
P10			VSS	VSS	PS	Input	Input	Input
P11			VSS	VSS	PS	Input	Input	Input
P12			VSS	VSS	PS	Input	Input	Input
P13			VSS	VSS	PS	Input	Input	Input
P14			VSS	VSS	PS	Input	Input	Input
P15			VSS	VSS	PS	Input	Input	Input
R9			VSS	VSS	PS	Input	Input	Input
R10			VSS	VSS	PS	Input	Input	Input
R11			VSS	VSS	PS	Input	Input	Input
R12			VSS	VSS	PS	Input	Input	Input
R13			VSS	VSS	PS	Input	Input	Input
R14			VSS	VSS	PS	Input	Input	Input
R15			VSS	VSS	PS	Input	Input	Input
W12			VSS	VSS	PS	Input	Input	Input
Y10			VSS	VSS	PS	Input	Input	Input
AA6			VSS	VSS	PS	Input	Input	Input
Y13			VSS	VSS	PS	Input	Input	Input
C6			VSS	VSS	PS	Input	Input	Input
B7	D8	F8	VSS_BBATT	VSS_BBATT	PS	Input	Input	Input
D11	C10	F10	VSS_BG	VSS_BG	PS	Input	Input	Input
AA14	Y12	Y15	VSS_CARD1	VSS_CARD1	PS	Input	Input	Input
AB12			VSS_CARD1	VSS_CARD1	PS	Input	Input	Input

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
	AA15	AC18	VSS_CARD2	VSS_CARD2	PS	Input	Input	Input
T19	P19	T19	VSS_CI	VSS_CI	PS	Input	Input	Input
V5	G12	W14	VSS_DF	VSS_DF	PS	Input	Input	Input
W7	R9	Y5	VSS_DF	VSS_DF	PS	Input	Input	Input
W11	R10	Y8	VSS_DF	VSS_DF	PS	Input	Input	Input
	R11	Y10	VSS_DF	VSS_DF	PS	Input	Input	Input
	R12	Y11	VSS_DF	VSS_DF	PS	Input	Input	Input
	R13	Y13	VSS_DF	VSS_DF	PS	Input	Input	Input
	Y1		VSS_DF	VSS_DF	PS	Input	Input	Input
	Y2		VSS_DF	VSS_DF	PS	Input	Input	Input
	AA1		VSS_DF	VSS_DF	PS	Input	Input	Input
	AA2		VSS_DF	VSS_DF	PS	Input	Input	Input
D12	F15	A18	VSS_IO1	VSS_IO1	PS	Input	Input	Input
D16	G13	B11	VSS_IO1	VSS_IO1	PS	Input	Input	Input
E19		B22	VSS_IO1	VSS_IO1	PS	Input	Input	Input
U20	T15	U20	VSS_IO3	VSS_IO3	PS	Input	Input	Input
AB16	Y20	AB24	VSS_IO3	VSS_IO3	PS	Input	Input	Input
	Y21		VSS_IO3	VSS_IO3	PS	Input	Input	Input
	AA20		VSS_IO3	VSS_IO3	PS	Input	Input	Input
	AA21		VSS_IO3	VSS_IO3	PS	Input	Input	Input
K20	K15	M20	VSS_LCD	VSS_LCD	PS	Input	Input	Input
M20	L15		VSS_LCD	VSS_LCD	PS	Input	Input	Input
	M15		VSS_LCD	VSS_LCD	PS	Input	Input	Input
E2	F6	C1	VSS_MEM	VSS_MEM	PS	Input	Input	Input
F4	F7	C2	VSS_MEM	VSS_MEM	PS	Input	Input	Input
F5	G7	F5	VSS_MEM	VSS_MEM	PS	Input	Input	Input
H4	H7	G6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
J2	J7	H5	VSS_MEM	VSS_MEM	PS	Input	Input	Input

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode
M4	K7	J6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
P5	L7	K6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
T4	M7	L6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
U4	N7	N6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
	P7	R6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
	R7	T6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
	T7	V6	VSS_MEM	VSS_MEM	PS	Input	Input	Input
	U7	Y3	VSS_MEM	VSS_MEM	PS	Input	Input	Input
H19	F17	G20	VSS_MSL	VSS_MSL	PS	Input	Input	Input
C9	E9	C10	VSS_OSC13M	VSS_OSC13M	PS	Input	Input	Input
D13	E11	C13	VSS_PLL	VSS_PLL	PS	Input	Input	Input
W15	E12	AD21	VSS_PLL	VSS_PLL	PS	Input	Input	Input
	W16		VSS_PLL	VSS_PLL	PS	Input	Input	Input
C4	A1	B2	VSS_USB	VSS_USB	PS	Input	Input	Input
	A2		VSS_USB	VSS_USB	PS	Input	Input	Input
	B1		VSS_USB	VSS_USB	PS	Input	Input	Input
	B2		VSS_USB	VSS_USB	PS	Input	Input	Input

Table 11: PXA30x Pin Usage Summary (Continued)

19mm² Ball #	15mm² Ball #	13mm² Ball #	Ball Name	Function After Reset	Type	Reset State	S3/D4/C4 Power Mode	S2/D3/C4 Power Mode

1. GPIO reset/S3 operation: After any reset is asserted or if PXA30x processor is in S3/D4/C4 power mode, these pins are configured as the primary function of the MFP (generally as GPIO input) and default pullup or pulldown occurs.
2. Crystal oscillator pins: These pins connect the external crystals to the on-chip oscillators and are not affected by either reset or S2/D3/C4 power mode. For more information, For more information, see the “Clocks Control and Power Management” chapter in the *PXA3xx Processor Family Vol. I: System and Timer Configuration Developers Manual.*
3. Each MFP output value is based on MFPRxx[Sleep_sel], MFPRxx[sleep_data], MFPRxx[sleep_oe_n], MFPRxx[pull_sel], MFPRxx[pullup_en] and MFPRxx[pulldown_en] following S2/D3/C4 wake-up. To prevent unnecessary current drain, ensure input signals are not floating during low-power modes. Each GPIO to be driven can be programmed to a 0/1 or be pulled up or pulled down during S2/D3/C4 power mode if the MVT and the IO (HVT) supplies are present.
4. Logic low when OSCC[TENSx] bit is cleared, CLK_TOUT when OSCC[TENSx] is set. Configure TENS2 for S2/D3/C4 mode and TENS3 for S3/D4/C4 power mode.
5. Pulldown always enabled.
6. Output functions during S2/D3/C4 power mode.
7. Pullup always enabled.
8. 20 KΩ nominal, 14.5 KΩ min - 24.5 KΩ max
9. Pd-0 if UP2OCR[DMPDE] is set, then Pd-0, Hi-Z if UP2OCR[DMPDE] is cleared.
10. Hi-Z if UP2OCR[DPPDE] is cleared and UP2OCR[DPPUE] is cleared; Pu-1 if UP2OCR[DPPDE] is cleared and UP2OCR[DPPUE] is set; Pd-0 if UP2OCR[DPPDE] is set and UP2OCR[DPPUE] is cleared. Setting UP2OCR[DPPDE] and UP2OCR[DPPUE] at the same time is not allowed.
11. This signal’s pullup/pulldown is enabled during power-on, hardware, global watchdog and GPIO resets. The pullup/pulldown must be disabled by software by setting PCFR[PUDH] after the external devices driving these pins are configured.
12. There is no pullup or pulldown on this pin. Asserts if PCFR[SL_ROD] is clear.

4.2.4 Signal Type Definitions

Table 12 contains the signal type definitions for Table 9, Table 10 and Table 11.

Table 12: Signal Types

Abbreviation	Type Description	Abbreviation	Type Description
IC	CMOS input	ISOCZ	SSTL input, CMOS output, three-stateable
OC	CMOS output	OA	Analog output
OCZ	CMOS output, three-stateable	IAOA	Analog bidirectional
ICOCZ	CMOS bidirectional, three-stateable	IAOAZ	Analog bidirectional - three-stateable
IA	Analog input	PS	Power supply
OS	SSTL output	IS	SSTL Input
ICSOCZ	CMOS or SSTL input, CMOS output, three-stateable		

5 Maximum Ratings and Operation Conditions

5.1 Absolute Maximum Ratings

The absolute maximum ratings (shown in Table 13) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the PXA3xx Processor Family.

Note

Absolute maximum ratings are *not* operating ranges. Operation at absolute maximum ratings is *not* guaranteed.

Table 13: Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
T_S	Storage temperature	–40	125	°C
	Voltage applied to VCC_BBATT	2.0	4.0	V
V_{CC_HV}	Voltage applied to high-voltage supply pins VCC_MSL, VCC_CARD2, VCC_CARD1, VCC_IO1, VCC_CI, VCC_DF, VCC_LCD).VCC_IO3	VSS–0.3	VSS+4.0	V
	VCC_IO4, VCC_IO6, VCC_TSI (PXA32x Only)			V
	VCC_USB (PXA32x and PXA30x only)			V
	VCC_BIAS (PXA31x only)			V
	VCC_ULPI (PXA31x only)	VSS–0.3	VSS+2.0	V
V_{CC_MV}	Voltage applied to low-voltage supply pins (VCC_MVT, VCC_BG, VCC_PLL, VCC_OSC13M, VCC_MEM)	VSS–0.3	VSS+2.0	V
V_{CC_LV}	Voltage applied to low-voltage supply pins (VCC_APPS, VCC_SRAM)	VSS–0.3	VSS+1.54	V
V_{IP}	Voltage applied to non-supply pins except PXTAL_IN, PXTAL_OUT, TXTAL_IN, and TXTAL_OUT pins	VSS–0.3	VSS+4.0	V
V_{IP_X}	Voltage applied to XTAL pins (PXTAL_IN, PXTAL_OUT, TXTAL_IN, TXTAL_OUT)	VSS–0.3	VSS+1.9	V

Table 13: Absolute Maximum Ratings (Continued)

Symbol	Description		Min	Max	Units
V_{ESD}	Maximum ESD stress voltage, three stresses maximum: • Any pin to any supply pin, either polarity, or • Any pin to all non-supply pins together, either polarity	HBM[1]	—	2000	V
		CDM[2]	—	700	V
I_{EOS}	Maximum DC input current (electrical overstress) for any non-supply pin		—	5	mA

NOTE:
1. HBM = human body model
2. CDM = charge device model

5.2 Operating Conditions

This section discusses operating voltage, frequency, and temperature specifications for the PXA3xx Processor Family.

Table 14 shows each power domains supported voltages. Table 14 also shows the application core frequency and supply voltage operating ranges for VCC_SRAM and VCC_APPS of the PXA32x processor, PXA31x processor and the PXA30x processor. Each frequency range is specified in one of the following formats:

(turbo frequency / run frequency / internal switch bus frequency / internal system bus frequency)

or

(turbo frequency / run frequency / internal switch bus frequency / internal system bus frequency / SRAM frequency)

or

(Power Mode (Sx/Dx/Cx) / SRAM frequency (optional))

Refer to the “Clocks Controller and Power Management Unit” chapter of the *PXA3xx Processor Family Vol. I: System and Timer Configuration Developers Manual* for supported frequencies and clock-register settings as listed in Table 14.

Table 14: Voltage, Temperature, and Frequency Electrical Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
Operating Temperature						
Tcase	Package operating temperature (Standard Temp)	-25	—	+85	°C	1
Tcase	Package operating temperature (Extended Temp) **(PXA32x Only)**	-40	—	+85	°C	1
Theta Jc	Junction-to-case temperature gradient (VF-BGA)	—	2.00	—	°C / watt	—
VCC_BBATT Voltage						
Vccbatt	Voltage applied on VCC_BBATT	2.40	3.00	3.60	V	—

Table 14: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
Tbbattramp	Ramp Rate	5.0 µV/µs	—	20.00	V/µs	—
VCC_MVT Voltage						
Vccmvt_0	Voltage applied on VCC_MVT in S3/D4/C4	—	0	—	V	—
Vccmvt_1	Voltage applied on VCC_MVT	1.70	1.80	1.90	V	—
Vccmvt_2	Voltage applied on VCC_MVT	1.80	1.90	2.00	V	3
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	—
VCC_BG Voltage						
Vccbg_0	Voltage applied on VCC_BG in S3/D4/C4	—	0	—	V	—
Vccbg_1	Voltage applied on VCC_BG	1.70	1.80	1.90	V	—
Vccbg_2	Voltage applied on VCC_BG	1.80	1.90	2.00	V	3
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	—
VCC_PLL Voltage						
Vccpll_0	Voltage applied on VCC_PLL in S3/D4/C4	—	0	—	V	—
Vccpll_1	Voltage applied on VCC_PLL	1.70	1.80	1.90	V	—
Vccpll_2	Voltage applied on VCC_PLL	1.80	1.90	2.00	V	3
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	—
VCC_OSC13M Voltage						
Vccosc13m_0	Voltage applied on VCC_OSC13M in S3/D4/C4	—	0	—	V	—
Vccosc13m_1	Voltage applied on VCC_OSC13M	1.70	1.80	1.90	V	—
Vccosc13m_2	Voltage applied on VCC_OSC13M	1.80	1.90	2.00	V	3
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	—
VCC_APPS Voltage at Frequency Ranges (Turbo/Run/Switch/System Bus), (Power Mode (Sx/Dx/Cx)) (Standard BIN Only)						
Vccapps_0	Voltage applied on VCC_APPS in S3/D4/C4, S2/D3/C4	—	0	—	V	—
Vccapps_1	Voltage applied on VCC_APPS at S0/D0CS/C0, 104/104/104/104, 208/208/208/104	1.05	1.10	1.2	V	2, 5
Vccapps_2	Voltage applied on VCC_APPS at 416/208/208/156	1.05	1.10	1.2	V	2

Table 14: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
Vccapps_3	Voltage applied on VCC_APPS at 624/312/312/208	1.31	1.375	1.475	V	2
Vccapps_4	Voltage applied on VCC_APPS in S0/D2/C2, S0/D1/C2 or at 806/403/403/208[7]	1.33	1.40	1.50	V	2
Tpwrramp	Ramp Rate	2.00	10.00	12.00	mV/µs	—
VCC_SRAM Voltage at Frequency Range (Turbo/Run/Switch/System Bus/SRAM), (Power Mode (Sx/Dx/Cx) @ SRAM frequency) (Standard BIN Only)						
Vccsram_0	Voltage applied on VCC_SRAM in S3/D4/C4 or S2/D3/C4	—	0	—	V	—
Vccsram_1	Voltage applied on VCC_SRAM at S0/D0CS/C0, 104/104/104/104 or 208/208/208/104	1.05	1.10	1.20	V	2, 5
Vccsram_2	Voltage applied on VCC_SRAM at 416/208/208/156	1.05	1.10	1.2	V	2
Vccsram_3	Voltage applied on VCC_SRAM at 624/312/312/208	1.31	1.375	1.475	V	2, 5
Vccsram_4	Voltage applied on VCC_SRAM in S2/D3/C4[4], S0/D2/C2, S0/D1/C2, or 806/403/403/208[7]	1.33	1.40	1.5	V	2, 5
Tpwrramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_APPS Voltage at Frequency Ranges (Turbo/Run/Switch/System Bus), (Power Mode (Sx/Dx/Cx)) (Low Power BIN Only)						
Vccapps_0	Voltage applied on VCC_APPS in S3/D4/C4, or S2/D3/C4	—	0	—	V	—
Vccapps_1	Voltage applied on VCC_APPS at S0/D0CS/C0, 104/104/104/104, 208/208/208/104	0.975	1.00	1.10	V	2, 5
Vccapps_2	Voltage applied on VCC_APPS at 416/208/208/156	1.05	1.10	1.2	V	2
Vccapps_3	Voltage applied on VCC_APPS at 624/312/312/208	1.31	1.375	1.475	V	2
Vccapps_4	Voltage applied on VCC_APPS in S0/D2/C2, S0/D1/C2 or at 806/403/403/208[7]	1.33	1.40	1.50	V	2
Tpwrramp	Ramp Rate	2.00	10.00	12.00	mV/µs	—
VCC_SRAM Voltage at Frequency Range (Turbo/Run/Switch/System Bus/SRAM), (Power Mode (Sx/Dx/Cx) @ SRAM frequency) (Low Power BIN Only)						
Vccsram_0	Voltage applied on VCC_SRAM in S3/D4/C4 or S2/D3/C4	—	0	—	V	—

Table 14: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
Vccsram_1	Voltage applied on VCC_SRAM at S0/D0CS/C0, 104/104/104/104 or 208/208/208/104	0.975	1.00	1.20	V	2, 5
Vccsram_2	Voltage applied on VCC_SRAM at 416/208/208/156	1.05	1.10	1.2	V	2
Vccsram_3	Voltage applied on VCC_SRAM at 624/312/312/208	1.31	1.375	1.475	V	2, 5
Vccsram_4	Voltage applied on VCC_SRAM in S2/D3/C4[4], S0/D2/C2, S0/D1/C2 or at 806/403/403/208[7]	1.33	1.40	1.5	V	2, 5
Tpwrramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_MEM Voltage						
Vccmem_0	Voltage applied on VCC_MEM in S3/D4/C4	—	0	—	V	—
Vccmem_1	Voltage applied on VCC_MEM	1.70	1.80	1.90	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_IO1 Voltage						
Vccio1_0	Voltage applied on VCC_IO1 in S3/D4/C4	—	0	—	V	—
Vccio1_1	Voltage applied on VCC_IO1	1.70	1.80	1.98	V	—
Vccio1_2	Voltage applied on VCC_IO1	2.70	3.00	3.30	V	—
Vccio1_3	Voltage applied on VCC_IO1	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_IO3 Voltage						
Vccio3_0	Voltage applied on VCC_IO3 in S3/D4/C4	—	0	—	V	—
Vccio3_1	Voltage applied on VCC_IO3	1.70	1.80	1.98	V	—
Vccio3_2	Voltage applied on VCC_IO3	2.70	3.00	3.30	V	—
Vccio3_3	Voltage applied on VCC_IO3	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_IO4 Voltage (PXA32x Only)						
Vccio4_0	Voltage applied on VCC_IO4 in S3/D4/C4	—	0	—	V	—
Vccio4_1	Voltage applied on VCC_IO4	1.70	1.80	1.98	V	—
Vccio4_2	Voltage applied on VCC_IO4	2.70	3.00	3.30	V	—
Vccio4_3	Voltage applied on VCC_IO4	2.97	3.30	3.63	V	—

Table 14: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
Tsysramp	Ramp Rate	—	10.00	12.00	mV/µs	—
VCC_IO6 Voltage (PXA32x Only)						
Vccio6_0	Voltage applied on VCC_IO6 in S3/D4/C4	—	0	—	V	—
Vccio6_1	Voltage applied on VCC_IO6	1.70	1.80	1.98	V	—
Vccio6_2	Voltage applied on VCC_IO6	2.70	3.00	3.30	V	—
Vccio6_3	Voltage applied on VCC_IO6	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	—	10.00	12.00	mV/µs	—
VCC_MSL Voltage						
Vccmsl_0	Voltage applied on VCC_MSL in S3/D4/C4	—	0	—	V	—
Vccmsl_1	Voltage applied on VCC_MSL	1.70	1.80	1.98	V	—
Vccmsl_2	Voltage applied on VCC_MSL	2.70	3.00	3.30	V	—
Vccmsl_3	Voltage applied on VCC_MSL	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_LCD Voltage						
Vcclcd_0	Voltage applied on VCC_LCD in S3/D4/C4	—	0	—	V	—
Vcclcd_1	Voltage applied on VCC_LCD	1.70	1.80	1.98	V	—
Vcclcd_2	Voltage applied on VCC_LCD	2.70	3.00	3.30	V	—
Vcclcd_3	Voltage applied on VCC_LCD	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_BIAS Voltage (PXA310 only)						
Vccbias_0	Voltage applied on VCC_BIAS in S3/D4/C4	—	0	—	V	—
Vccbias_1	Voltage applied on VCC_BIAS	1.80	3.30	3.6	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_USB Voltage (PXA32x and PXA30x only)						
Vccusb_0	Voltage applied on VCC_USB in S3/D4/C4	—	0	—	V	—
Vccusb_1	Voltage applied on VCC_USB	3.00	3.30	3.6	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_ULPI Voltage (PXA31x only)						

Table 14: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
Vcculpi_0	Voltage applied on VCC_ULPI in S3/D4/C4	—	0	—	V	—
Vcculpi_1	Voltage applied on VCC_ULPI	1.70	1.80	1.98	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_CARD1 Voltage						
Vcccard1_0	Voltage applied on VCC_CARD1 in S3/D4/C4	—	0	—	V	—
Vcccard1_1	Voltage applied on VCC_CARD1	1.70	1.80	1.98	V	—
Vcccard1_2	Voltage applied on VCC_CARD1	2.70	3.00	3.30	V	—
Vcccard1_3	Voltage applied on VCC_CARD1	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_CARD2 Voltage						
Vcccard2_0	Voltage applied on VCC_CARD2 in S3/D4/C4	—	0	—	V	—
Vcccard2_1	Voltage applied on VCC_CARD2	1.70	1.80	1.98	V	—
Vcccard2_2	Voltage applied on VCC_CARD2	2.70	3.00	3.30	V	—
Vcccard2_3	Voltage applied on VCC_CARD2	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_DF Voltage						
Vccdf_0	Voltage applied on VCC_DF in S3/D4/C4	—	0	—	V	—
Vccdf_1	Voltage applied on VCC_DF	1.70	1.80	1.98	V	—
Vccdf_2	Voltage applied on VCC_DF	2.70	3.00	3.30	V	—
Vccdf_3	Voltage applied on VCC_DF	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_CI Voltage						
Vccci_0	Voltage applied on VCC_CI in S3/D4/C4	—	0	—	V	—
Vccci_1	Voltage applied on VCC_CI	1.70	1.80	1.98	V	—
Vccci_2	Voltage applied on VCC_CI	2.70	3.00	3.30	V	—
Vccci_3	Voltage applied on VCC_CI	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	2.00	10.00	12.00	mV/µs	6
VCC_TSI Voltage (PXA32x Only)						

Table 14: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
Vcctsi_0	Voltage applied on VCC_TSI in S3/D4/C4	—	0	—	V	—
Vcctsi_1	Voltage applied on VCC_TSI	2.97	3.30	3.63	V	—
Tsysramp	Ramp Rate	—	10.00	12.00	mV/µs	—

NOTE:
1. System design must ensure that the device case temperature is maintained within the specified limits. In some system applications it may be necessary to use external thermal management (for example, a package-mounted heat spreader) or configure the device to limit power consumption and maintain acceptable case temperatures.
2. The voltage ranges specified for VCC_APPS and VCC_SRAM are the targeted voltage ranges for the product. These ranges may extend or narrow depending on actual product performance and product skews. Marvell recommends that extended voltage and current capabilities be designed into the power management IC to accommodate future changes to this specification without requiring changes to the power management IC.
3. VCC_MVT requires the capability to increase from the normal operating voltage of 1.8 V to 1.9 V during certain times. This increased voltage is required under certain conditions, not during normal operation. When VCC_MVT is raised to 1.9 V, it is operating in “boost mode”. Boost mode is only used during factory programming. If VCC_PLL, VCC_OSC13M and VCC_BG are supplied by the same PMIC supply, which is the method Marvell recommends, these other voltages also operate at 1.9 V. Maximum current capabilities and voltage tolerances are identical in boost mode and normal operation.
4. This option allows one or more 128 Kbyte SRAM banks to retain state during S2/D3/C4 mode.
5. Reset voltage for VCC_APPS and VCC_SRAM is 1.4 V and the startup frequency is 104/104/104/104 MHz.
6. Min ramp rate = (Maximum voltage transition) / (LPM_DEL - ((Power I2C command execution time))
7. PXA32x Only

6 Electrical Specifications

This chapter includes DC voltage and current characteristics as well as crystal and oscillator specifications for the PXA3xx Processor Family.

6.1 DC Voltage and Current Characteristics

The DC characteristics for each pin include input-sense levels, output-drive levels, current and pullup/down resistive values. These parameters can be used to determine maximum DC loading and to determine maximum transition times for a given load.

Table 15 shows the DC operating conditions for the input, output, and I/O pins used by the EMPI bus controlled by the DMEMC. Table 16 applies to all signals powered by VCC_high. VCC_high is not a physical supply on the PXA3xx processors, but the term used to refer to the collective groups of high voltage supplies which consist of VCC_IO1, VCC_IO3, VCC_IO4 (PXA32x Only), VCC_IO6 (PXA32x Only), VCC_DF, VCC_CI, VCC_CARD1, VCC_CARD2, VCC_LCD, VCC_USB (PXA32x and PXA30x Only), VCC_BIAS (PXA31x Only), VCC_ULPI (PXA31x Only) and VCC_MSL.

Table 15: DDR Input, Output, and I/O Pins AC/DC Operating Conditions

Symbols	Description	Min	Typical	Max	Unit	Notes
Input DC Operating Conditions (SSTL receiver)[1]						
$Vih_{(dc)}$	Input high voltage	0.7 * VCC_MEM	—	VCC_MEM + 0.3	V	2
$V_{il(dc)}$	Input low voltage	-0.3	—	0.3 * VCC_MEM	V	2
$Vih_{(ac)}$	Input high voltage	0.8 * VCC_MEM	—	VCC_MEM + 0.3	V	—
$V_{il(ac)}$	Input low voltage	-0.3	—	0.2 * VCC_MEM	V	—
R_{PULLUP}	Pullup Resistance	65[3]	100	160[4]	KΩ	5, 6
$R_{PULLDOWN}$	Pulldown Resistance	55[3]	100	175[4]	KΩ	5, 6
Output DC Operating Conditions (VCC_MEM = 1.8 V)						
V_{OH}	High-level output voltage Absolute Load Current achieving Voh	0.9 * VCC_MEM	—	VCC_MEM	V	I_{OH} = (min) -6.5 mA
V_{OL}	Low-level output voltage Absolute Load Current achieving Vol	VSS	—	0.1 * VCC_MEM	V	I_{OL} = (min) 6.5 mA

Table 15: DDR Input, Output, and I/O Pins AC/DC Operating Conditions (Continued)

Symbols	Description	Min	Typical	Max	Unit	Notes

NOTE:
1. Use values when SSTL (differential) receiver is enabled. See EMPI[SSTL_DMEM_EN] and EMPI[SST_SMEM_EN] register definitions in the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual*.
2. The Schmidt trigger must be disabled for SSTL mode. EMPI[SCHM_DMEM_EN] must be cleared. Register definitions are found in the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual*.
3. Max voltage, Minimum temperature
4. Min voltage, Maximum temperature
5. Enabled during reset, S2/D3/C4 power state, and S3/D4/C4 power mode. Not enabled through software control.
6. Enabled and disabled using EMPI[PW_DQN] and EMPI[PD_DQS]. See EMPI[PW_DQN] and EMPI[PD_DQS] register definitions in the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual*.

Table 16: MFP Input, Output, and I/O Pins DC Operating Conditions

Symbols	Description	Min	Typical	Max	Unit	Notes
Input DC Operating Conditions (vcc = 1.8 V Typical)						
Vih	Input high voltage	VCC_high * 0.8	—	VCC_high + 0.3	V	3
V_{il}	Input low voltage	-0.3	—	VCC_high * 0.2	V	3
V_{hys}	Hysteresis (V_{IT+} - V_{IT-})	0.4	—	VCC_high * 0.5	V	3
R_{PULLUP}	Pullup Resistance	40[1]	110	200[2]	KΩ	4
$R_{PULLDOWN}$	Pulldown Resistance	40[1]	110	200[2]	KΩ	5
Input DC Operating Conditions (vcc = 3.0 and 3.3 V Typical)						
Vih	Input high voltage	0.8 * VCC_high	—	VCC_high + 0.3	V	3
V_{il}	Input low voltage	-0.3	—	VCC_high * 0.2	V	3
V_{hys}	Hysteresis (V_{IT+} - V_{IT-})	0.4	—	VCC_high * 0.5	V	3
R_{PULLUP}	Pullup Resistance	20[1]	45	100[2]	KΩ	4
$R_{PULLDOWN}$	Pulldown Resistance	20[1]	45	100[2]	KΩ	5

Table 16: MFP Input, Output, and I/O Pins DC Operating Conditions (Continued)

Symbols	Description	Min	Typical	Max	Unit	Notes
Output DC Operating Conditions (VCC = 1.8 V Typical)						
V_{OH}[6] 1X 2X 3X 4X 6X 8X 10X 12X	High-level output voltage Absolute Load Current achieving Voh	0.9 * VCC_high	—	VCC_high	V	I_{OH} = (mA min) -0.4 -0.8 -1.2 -1.6 -2.4 -3.2 -4.0 -4.8
V_{OL}[6] 1X 2X 3X 4X 6X 8X 10X 12X	Low-level output voltage Absolute Load Current achieving Vol	VSS	—	0.1 * VCC_high	V	I_{OL} = (mA min) 0.5 1.0 1.5 2.0 3.0 4.0 5.0 6.0
Output DC Operating Conditions (vccp = 3.0 and 3.3 V Typical)						
V_{OH}[6] 1X 2X 3X 4X 6X 8X 10X 12X	High-level output voltage Absolute Load Current achieving Voh	VCC_high * 0.9	—	VCC_high	V	I_{OH} = (mA min) -1.5 -3.0 -4.5 -6.0 -9.0 -12.0 -15.0 -18.0
V_{OL}[6] 1X 2X 3X 4X 6X 8X 10X 12X	Low-level output voltage Absolute Load Current achieving Vol	VSS	—	0.1 * VCC_high	V	I_{OL} = (mA min) 1.25 2.5 3.75 5 7.5 10 12.5 15
Output DC Operating Conditions (VCC = 1.8, 3.0 and 3.3 V Typical)						
I_{OZ}	Three-state output leakage current	—	—	40	nA	—
I_{DDQ}	Quiescent supply current	—	—	1	nA	—

Table 16: MFP Input, Output, and I/O Pins DC Operating Conditions (Continued)

Symbols	Description	Min	Typical	Max	Unit	Notes

NOTE:
1. Max voltage, Minimum temperature
2. Min voltage, Maximum temperature
3. VCC_high references to VCC_IO1, VCC_IO3, VCC_IO4, VCC_IO6, VCC_DF, VCC_CI, VCC_CARD1, VCC_CARD2, VCC_LCD, VCC_USB supplies.
4. Use MFPRxx[pull_sel] and MFPRxx[pullup_en] bits to enable or disable pullups.
5. Use MFPRxx[pull_sel] and MFPRxx[pulldown_en] bits to enable or disable pulldowns.
6. Multi-Function Pin (MFP) drive strength is programmable using MFPRxx[drive] bitfield. MFPR register definitions are found in the PXA3xx Processor Family Vol. I: System and Timer Configuration Developers Manual.

6.2 Oscillator Electrical Specifications

The PXA3xx processors contains two oscillators: a 32.768 kHz oscillator and a 13.000 MHz oscillator. Each oscillator requires a specific crystal.

6.2.1 32.768 kHz Oscillator Specifications

The 32.768 kHz crystal is connected between the TXTAL_IN (amplifier input) and TXTAL_OUT (amplified output). Table 17 lists example 32.768 kHz crystal specifications.

To drive the 32.768 kHz crystal pins from an external source:

1. Drive the TXTAL_IN pin with a digital signal that has low and high levels as listed in Table 17.
2. Ground the TXTAL_OUT pin.

Table 18 lists example 32.768 kHz oscillator specifications.

Table 17: Typical 32.768 kHz Crystal Requirements [1]

Parameter	Minimum	Typical	Maximum	Units
Frequency range	—	32.768	—	kHz
Frequency tolerance	–30	—	+30	ppm
Frequency stability, parabolic coefficient	—	—	–0.04	ppm/$(\Delta°C)^2$
Drive level	—	—	1.0	uW
Load capacitance (C_L)	—	12.5	—	pf
Series resistance (R_S)	—	18	85	kΩ

NOTE:
1. A capacitor is required from TXTAL_IN to ground and from TXTAL_OUT to ground. The capacitors must be 22.0 pF, 5%, +/-30ppm/C temperature coefficient.

Table 18: Typical External 32.768 kHz Oscillator Requirements

Symbol	Description	Min	Typical	Max	Units
Amplifier Specifications					

Table 18: Typical External 32.768 kHz Oscillator Requirements (Continued)

Symbol	Description	Min	Typical	Max	Units
VIH_X	Input high voltage, TXTAL_IN	0.8	—	1.0	V
VIL_X	Input low voltage, TXTAL_IN	–0.10	0.00	0.10	V
IIN_XT	Input leakage, TXTAL_IN	—	—	10	µA
CIN_XT	Input capacitance, TXTAL_IN/TXTAL_OUT	—	18	25	pf
tS_XT	Stabilization time	—	—	2	s
SR_XT	Slew Rate	46	—	—	mV/µs
Board Specifications					
RP_XT	Parasitic resistance, TXTAL_IN/TXTAL_OUT to any node	20	—	—	MΩ
CP_XT	Parasitic capacitance, TXTAL_IN/TXTAL_OUT, total	—	—	5	pf
COP_XT	Parasitic shunt capacitance, TXTAL_IN to TXTAL_OUT	—	—	0.4	pf

6.2.2 13.000 MHz Oscillator Specifications

The 13.000 MHz crystal is connected between the PXTAL_IN (amplifier input) and PXTAL_OUT (amplified output). Table 19 lists the 13.000 MHz crystal specifications.

To drive the 13.000 MHz crystal pins from an external source:

1. Drive the PXTAL_IN pin with a digital signal with low and high levels as listed in Table 20.
2. Float the PXTAL_OUT pin

Table 20 lists the 13.000 MHz oscillator specifications.

Table 19: Typical 13.000 MHz Crystal Requirements

Parameter	Minimum	Typical	Maximum	Units
Frequency range	12.997	13.000	13.002	MHz
Frequency tolerance at 25°C	–50	—	+50	ppm
Oscillation mode	Fundamental			—
Maximum change over temperature range	–50	—	+50	ppm
Drive level	—	10	100	uW
Load capacitance (C_L)	—	10	—	pf
Series resistance (R_S)	—	50	—	Ω

NOTE: No external capacitors are needed on the PXTAL_IN or PXTAL_OUT pins for use with a 13.000 MHz crystal. The device provides an effective internal load capacitance of 10.0pF which is the load capacitance defined for the frequency tolerance specification.

Table 20: Typical External 13.000 MHz Oscillator Requirements

Symbol	Description	Min	Typical	Max	Units
Amplifier Specifications					
VIH_X	Input high voltage, PXTAL_IN	1.7	1.8	1.9	V
VIL_X	Input low voltage, PXTAL_IN	–0.10	0.00	0.10	V
IIN_XP	Input leakage, PXTAL_IN	—	—	10	µA
CIN_XP	Input capacitance, PXTAL_IN/PXTAL_OUT	—	20	25	pf
tS_XP	Stabilization time	—	—	7	ms
SR_XP	Slew Rate	1	—	—	V/ns
Board Specifications					
RP_XP	Parasitic resistance, PXTAL_IN/PXTAL_OUT to any node	20	—	—	MΩ
CP_XP	Parasitic capacitance, PXTAL_IN/PXTAL_OUT, total	—	—	5	pf
COP_XP	Parasitic shunt capacitance, PXTAL_IN to PXTAL_OUT	—	—	0.4	pf

6.2.3 Clock Outputs

6.2.3.1 CLK_POUT - 13 MHz Clock Output

CLK_POUT can be used to drive a buffered version of the PXTAL_IN oscillator input. Refer to Table 21 for CLK_POUT specifications.

Note CLK_POUT is available only when software sets the OSCC[PEN] bit.

Table 21: CLK_POUT Specifications

Parameter	Specifications
Frequency	13 MHz
Frequency Accuracy (derived from 13 MHz crystal)	+/-200 ppm
Symmetry/Duty Cycle variation	30/70 to 70/30% at VCC
Jitter	+/-20pS max
Load capacitance (C_L)	50 pf max
Rise and Fall time (Tr & Tf)	15 nS max with 50 pF load

6.2.3.2 CLK_TOUT - 32.768 kHz Clock Output

A buffered and inverted version of the TXTAL_IN oscillator output is driven out on CLK_TOUT. Refer to Table 22 for CLK_TOUT specifications.

Do not route CLK_TOUT close to the 32 kHz crystal or the 32 kHz crystal signals TXTAL_IN and TXTAL_OUT. Incorrect layout can cause the 32 kHz crystal to not lock, or to lock at an incorrect frequency.

Note

CLK_TOUT is enabled by default. CLK_TOUT can be disabled by writing to the OSCC[TENSx] bits.

Table 22: CLK_TOUT Specifications

Parameter	Specifications
Frequency	32.768 kHz
Frequency Accuracy (derived from 32 kHz crystal)	+/-200 ppm
Symmetry/Duty Cycle variation	30/70 to 70/30% at VCC
Jitter	+/-20 pS max
Load capacitance (C_L)	50 pf max
Rise and Fall time (Tr & Tf)	15 nS max with 50 pF load

7 AC Characteristics

This chapter includes AC characteristics, timing diagrams and timing parameters for the PXA3xx Processor Family controllers/interfaces listed below. All memory devices connect to either the External-Memory Pin Interface (EMPI) or the Data-Flash Interface (DFI).

- EMPI:DDR SDRAM Timing Diagrams and Specifications
- DFI: Variable Latency I/O (VLIO) Timing Diagrams and Specifications
- DFI: Flash Memory Timing Diagrams and Specifications
- DFI: SRAM Timing Diagrams and Specifications
- DFI: Compact Flash Timing Diagrams and Specifications
- DFI: NAND Timing Diagrams and Specifications
- Quick Capture Camera Interface Timing Diagrams and Specifications
- LCD Timing Diagrams and Specifications
- SSP Timing Diagrams and Specifications
- AC '97 Timing Diagrams and Specifications
- USB 2.0 Timing Diagrams and Specifications (PXA32x and PXA30x only)
- MultiMedia Card Timing Diagrams and Specifications
- Secure Digital (SD/SDIO) Timing Diagrams and Specifications
- JTAG Boundary Scan Timing Diagrams and Specifications

A pin's alternating-current (AC) characteristics include input and output capacitance. These factors determine the loading for external drivers and other load analyses. The AC characteristics also include a derating factor, which indicates how much the AC timings might vary with different loads.

Table 23 shows the AC operating conditions for the high- and low-strength input, output, and I/O pins. All AC specification values are valid for the device's entire temperature range.

Table 23: Standard Input, Output, and I/O-Pin AC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
C_{IN}	Input capacitance, all standard input and I/O pins	—	—	10	pf
C_{OUT_H}	Output capacitance, all standard high-strength output and I/O pins	20	—	50	pf
C_{OUT_L}	Output capacitance, all standard low-strength output and I/O pins	20	—	50	pf

7.1 External Memory Pin Interface (EMPI) Memory Timings

This section describes the timing diagrams and timing parameters for the Dynamic Memory Controller (DMEMC) on the External Memory Pin Interface (EMPI). The following diagrams are included in this section:

- Figure 52, DDR SDRAM Timing Diagrams
- Figure 53, MD<31:0> to DQS Write Skew
- Figure 54, CLK to Address/Command Write Skew

- Figure 55, DQS to CLK Write Skew
- Figure 56, MD<31:0> to DQS Read Skew

7.1.1 DDR SDRAM Timing Diagrams and Specifications

Figure 52 Shows the DDR SDRAM timings that are programmable through the MDCNFG[DTC[1:0]] register. Refer the *LP DDR JEDEC Spec* for complete timing diagrams and specifications.

Figure 52: DDR SDRAM Timing Diagrams

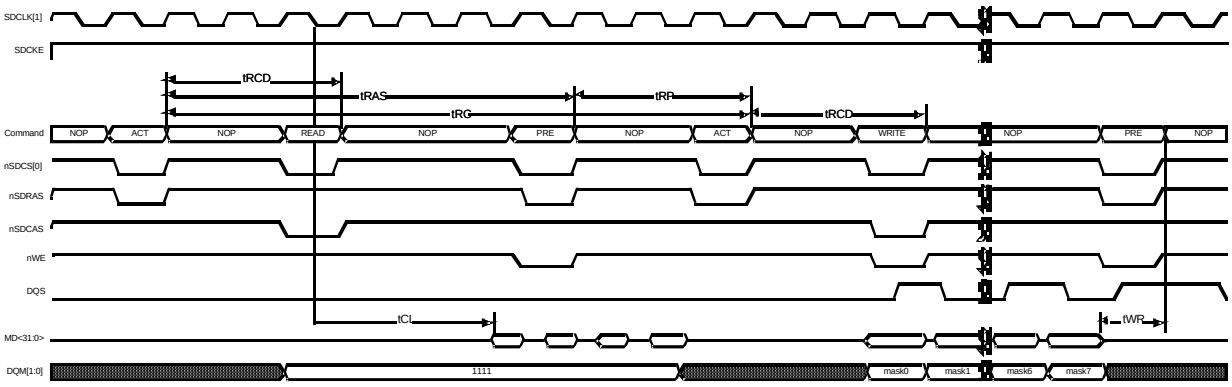


Figure 53 Shows the DQ to DQS skew during write cycles.

Figure 53: MD<31:0> to DQS Write Skew

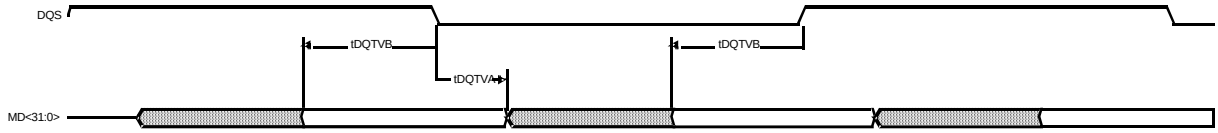


Figure 54 Shows the CLK to Address/Command skew during write cycles.

Figure 54: CLK to Address/Command Write Skew

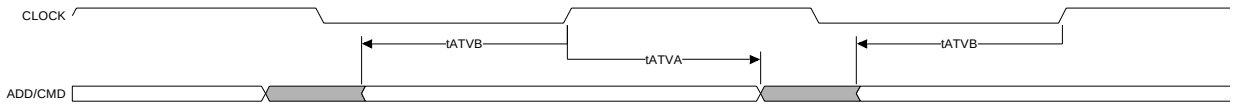


Figure 55 Shows the DQS to CLK skew during write cycles.

Figure 55: DQS to CLK Write Skew

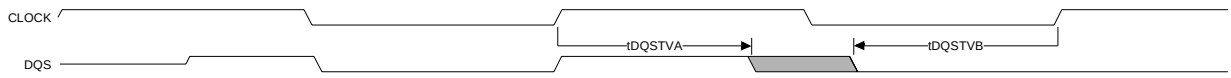


Figure 56 Shows the DQ to DQS allowable skew during read cycles.

Figure 56: MD<31:0> to DQS Read Skew

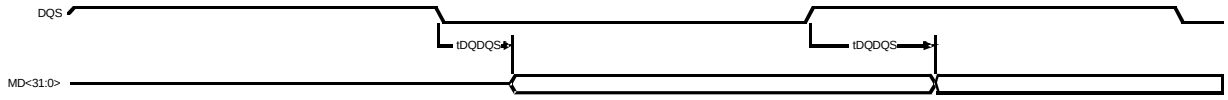


Table 24: DDR Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t_{RC}	nSDRAS cycle time	5	MDCNFG[DTCx]	10	SDCLK	1
t_{RP}	nSDRAS Precharge	2	MDCNFG[DTCx]	4	SDCLK	1
t_{CL}	nSDRAS to first data valid delay	2	MDCNFG[DTCx]	3	SDCLK	1
t_{RAS}	nSDRAS active time (min)	3	MDCNFG[DTCx]	6	SDCLK	1
t_{RCD}	nSDRAS assert to nSDCAS assert delay	2	MDCNFG[DTCx]	4	SDCLK	1
t_{WR}	Write recovery time		2		SDCLK	2
t_{DQTVB}	DQ Valid time before DQS	1.38	—	—	ns	
t_{DQTVA}	DQ Valid time after DQS	1.16	—	—	ns	
t_{ATVB}	CMD/CTL Valid time before CLK	3.2	—	—	ns	
t_{ATVA}	CMD/CTL Valid time after CLK	3.0	—	—	ns	
t_{DQSTVB}	DQS Falling edge before CLK	3.14	—	—	ns	
t_{DQSTVA}	DQS Falling edge after CLK	2.98	—	—	ns	
t_{DQDQS}	Skew between DQ and DQS permitted at the input.	-1.2	—	1.2	ns	

NOTE:
1. SDCLK frequency is one half of the DDR controller frequency. The DDR controller frequency is configured using ACCR[DMCFS] bits.
2. The write recovery time is hardcoded to two SDCLKs.
3. Refer to the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual* for more information on the MDCNFG register.

7.2 Data-Flash Interface (DFI) Memory Timing Specifications

This section describes the timing diagrams and timing parameters for all supported memory devices on the Data-Flash Interface (DFI). The following diagrams are included in this section:

7.2.1 Variable Latency I/O (VLIO) Timing Diagrams and Specifications

The variable-latency I/O (VLIO) interface allows the use of a data-ready input signal, RDY, to insert a variable number of memory-cycle wait states. The data-bus width for VLIO on the DFI for each chip-select region supports 16-bit memory devices. DF_nOE is asserted for all reads; DF_nWE is asserted for all writes.

In addition, VLIO read accesses differ from SRAM read accesses in that the DF_nOE toggles for each beat of a burst.

The memory controller waits indefinitely for the RDY signal to be asserted. This wait period hangs the system if the external VLIO is not responding. To prevent indefinite system hangs, set the watchdog timer when starting a VLIO transfer, and reset the system if no response is received from the VLIO.

For Reads, nBE<1:0> are asserted to 0b00. During Writes, data pins are actively driven by the processor (that is, they are not three-stated), regardless of the state of the individual nBE pins. For these Writes, the nBE pins are used as Byte Enables.

7.2.1.1 VLIO Read Timing

Figure 57 illustrates a full Latch-addressing mode Read cycle for a VLIO device. Figure 58 illustrates a full Latch-addressing mode Read cycle for a VLIO device using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 25 for detailed timing parameters. Only one Byte Enable (nBE[1:0]) is asserted on a single byte Read.

Figure 57: VLIO Read Timing Diagram

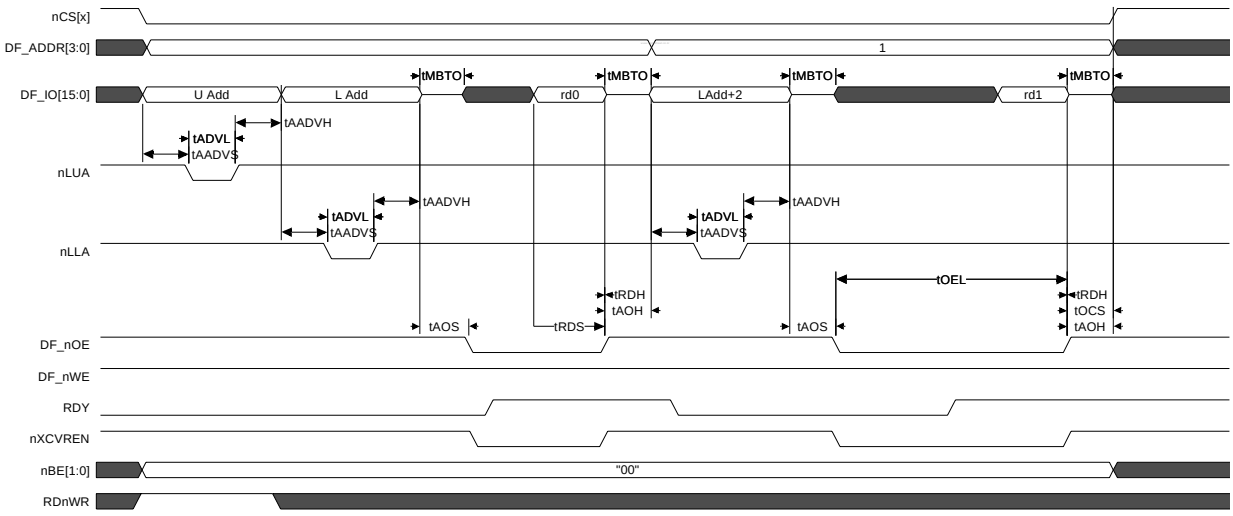
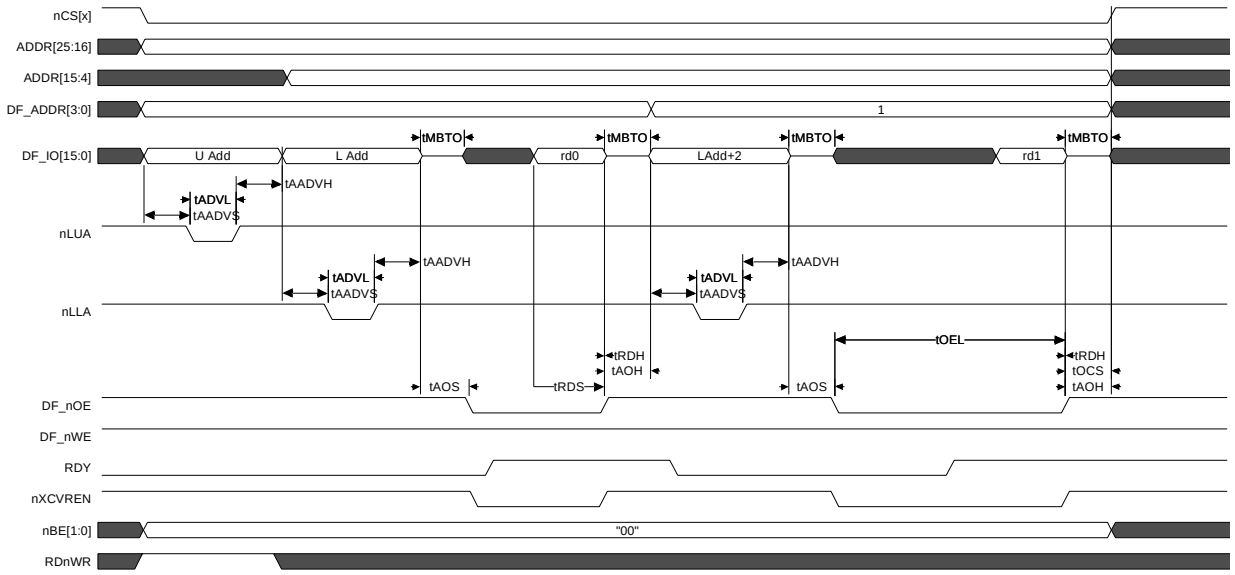


Figure 58: VLIO Read Timing Diagram (Latched Addressing Mode)



7.2.1.2 VLIO Low-Order Addressing Read Timing

Figure 59 illustrates a Low-order Addressing mode Read cycle for a VLIO device. Figure 60 illustrates a Low-order Addressing mode Read cycle for a VLIO device using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 25 for detailed timing parameters. Only one Byte Enable (nBE[1:0]) is asserted on a single byte Read.

Figure 59: VLIO Low Order Addressing Read Timing Diagram

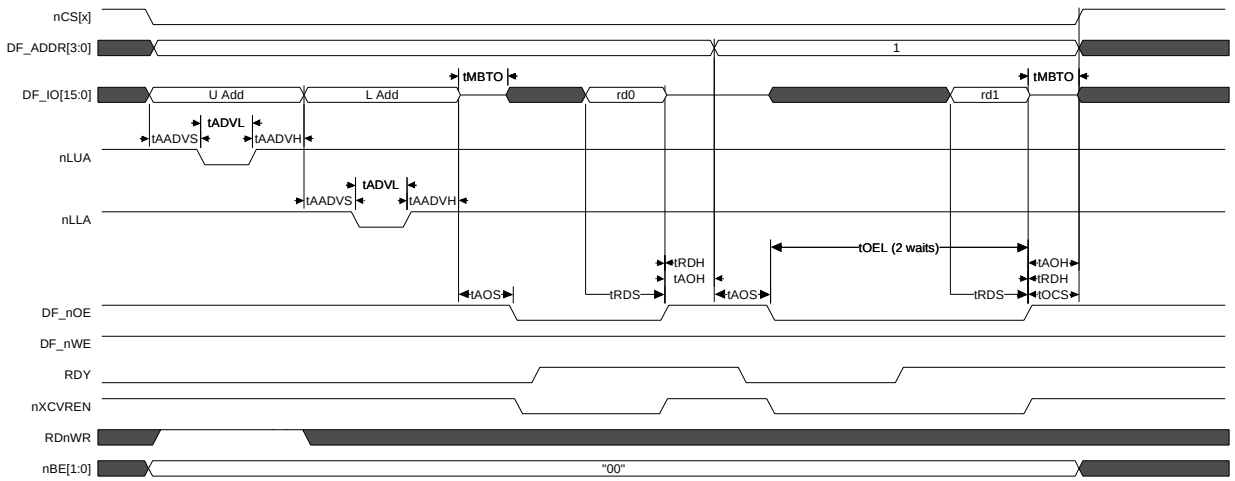
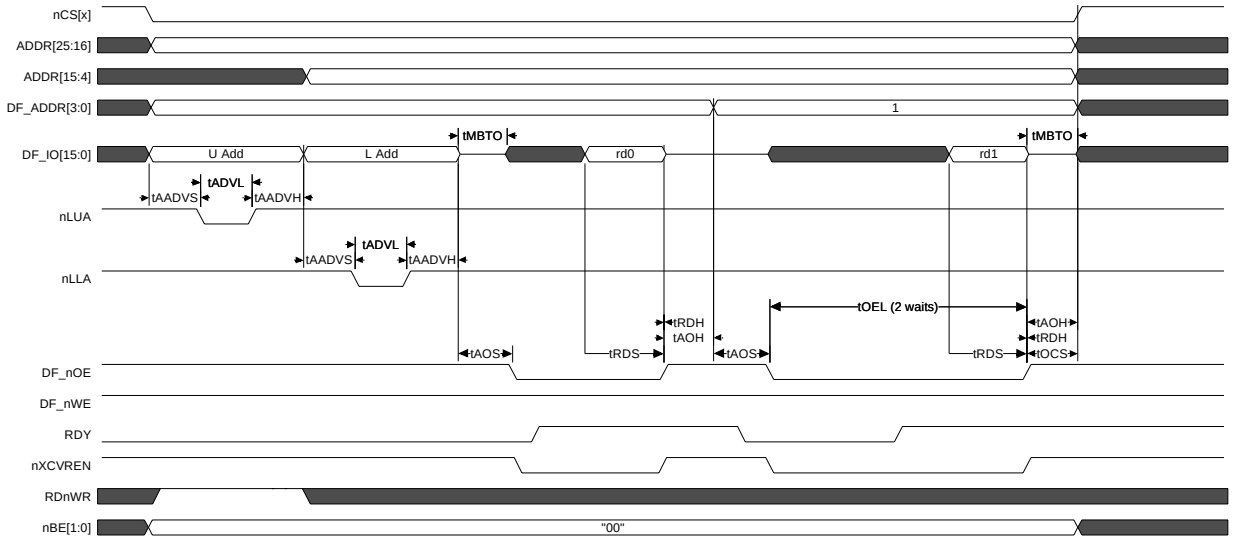


Figure 60: VLIO Low Order Addressing Read Timing Diagram (Latched Addressing Mode)



7.2.1.3 VLIO Write Timing

Figure 61 illustrates a full Latch-addressing mode Write cycle for a VLIO device. Figure 62 illustrates a full Latch-addressing mode Write cycle for a VLIO device using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 25 for detailed timing parameters.

Figure 61: VLIO Write Timing Diagram

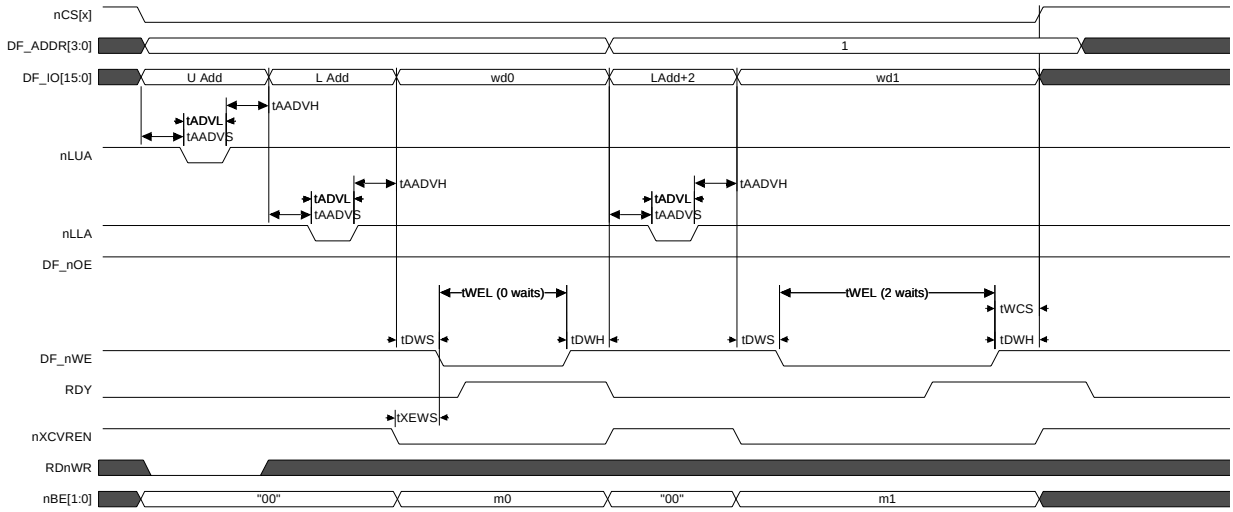
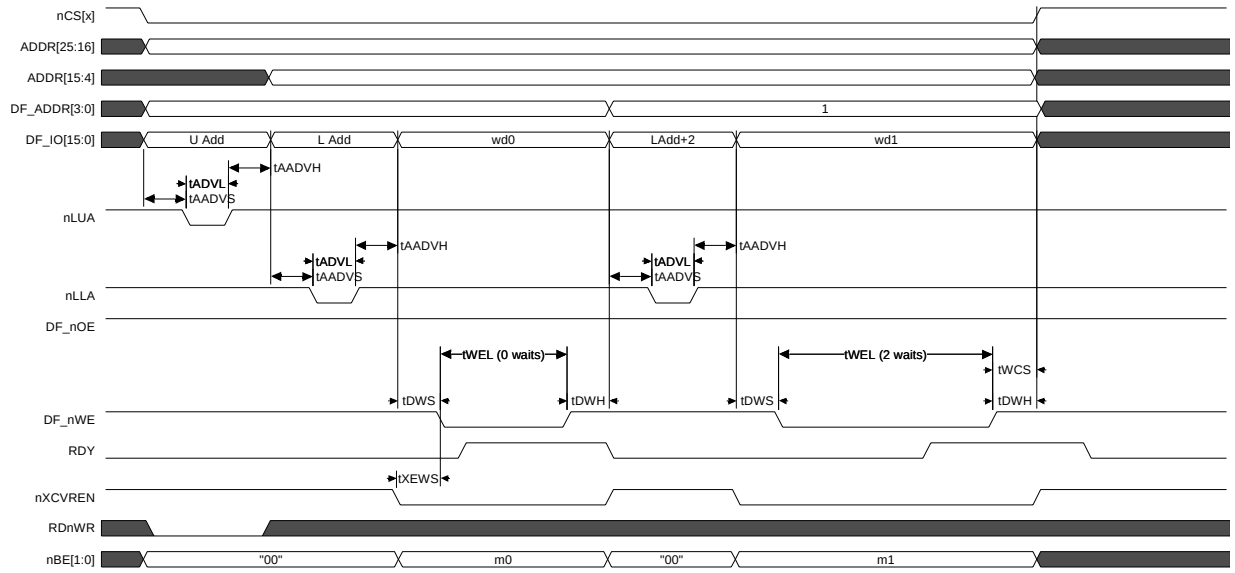


Figure 62: VLIO Write Timing Diagram (Latched Addressing Mode)



7.2.1.4 VLIO Low Order Addressing Write Timing

Figure 63 illustrates a Low-order Addressing mode Write cycle for a VLIO device. Figure 64 illustrates a Low-order Addressing mode Write cycle for a VLIO using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 25 for detailed timing parameters.

Figure 63: VLIO Low Order Addressing Write Timing Diagram

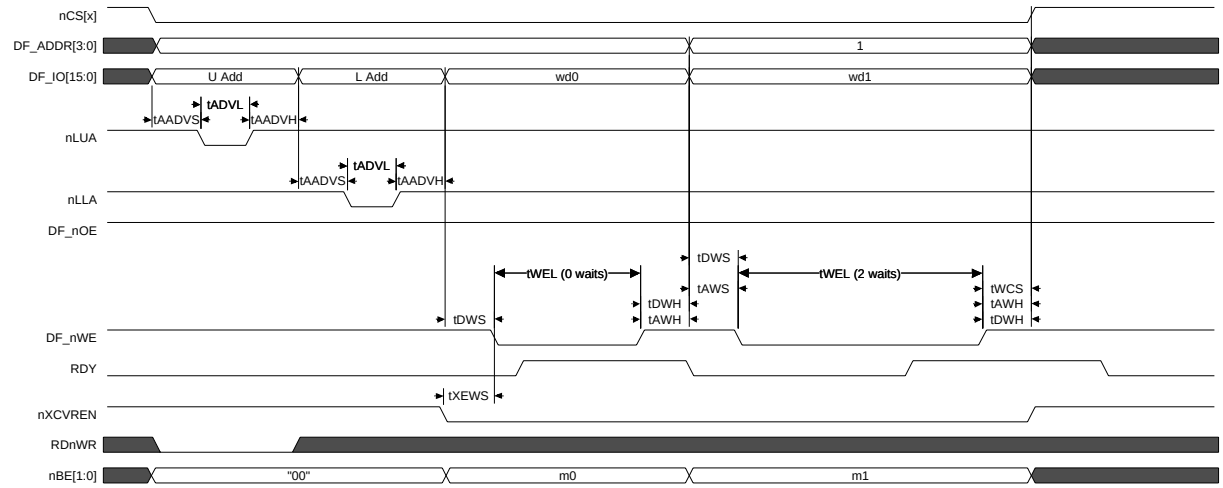


Figure 64: VLIO Low Order Addressing Write Timing Diagram (Latched Addressing Mode)

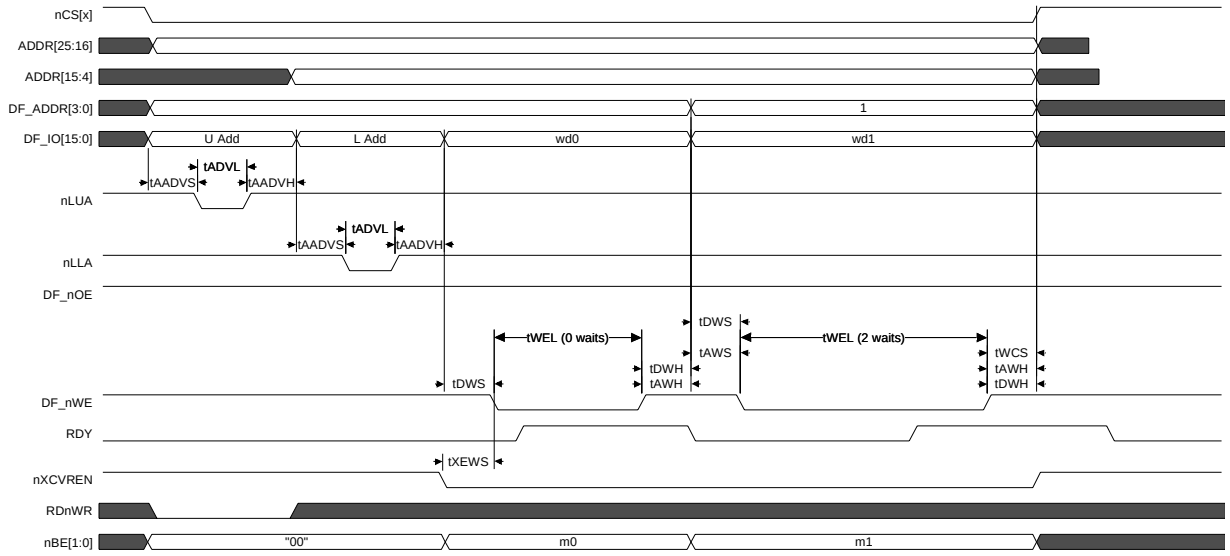


Table 25: VLIO Timing Specifications

Symbol	Description	Min[2]	Min[3]	Min[4]	Typical	Max	Units	Notes
t_{AADVS}	Address setup to nLLA/nLUA asserted	0	1	1	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{AADVH}	Address hold from nLLA/nLUA deasserted	0	1	1	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{tADVL}	nLLA/nLUA assert time	1	1	2	CSADRCFGx[ALW]	7	DF_SCLK	1
t_{XEWS}	nXCVREN setup to DF_nWE asserted	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{DWS}	Byte Enables and Write Data setup to DF_nWE asserted	—	—	—	1	—	DF_SCLK	1
t_{DWH}	Write Data, Byte Enables and nXCVREN hold from DF_nWE de-asserted	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{AOH}	Address hold from DF_nOE de-asserted	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{WCS}	DF_nWE de-asserted to nCS de-asserted	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{OCS}	DF_nOE de-asserted to nCS de-asserted	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1

Table 25: VLIO Timing Specifications (Continued)

Symbol	Description	Min[2]	Min[3]	Min[4]	Typical	Max	Units	Notes
t_{WEL}	DF_nWE assert time	3	4	7	MCS0/1[RDF]+ 1 + Waits[5]	16	DF_SCLK	1
t_{OEL}	DF_nOE assert time	3	4	7	MCS0/1[RDF]+ 1 + Waits[5]	16	DF_SCLK	1
t_{AWS}	Address setup to DF_nWE assert	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{AWH}	Address hold from DF_nWE de-assert	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{AOS}	Address setup to DF_nOE assert	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{AOH}	Address hold from DF_nOE de-assert	1	1	1	MCS0/1[RDN]	15	DF_SCLK	1
t_{RDH}	Read data hold from sample	—	—	—	0	—	ns	1
t_{RDS}	Read data setup time	30	30	30	—	—	ns	1
tMBTO	Minimum Bus Turnover time	—	—	—	1	—	DF_SCLK	1

NOTE:
1. DF_SCLK frequency depends on the ACCR[SMCFS] and MEMCLKCFG[DF_CLKDIV] programmed value.
2. DF_SCLK = 52MHz
3. DF_SCLK = 104MHz
4. DF_SCLK = 208MHz
5. Waits are cycles inserted while the RDY signal is low.
6. Refer to the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual* for more information on the CSADRCFGx and MCS0/1 registers.

7.2.2 Flash Memory Timing Diagrams and Specifications

The DFI bus uses the Static Memory Controller (SMEMC) to interface to 16-bit AA/D muxed Flash memory. Figure 65 through Figure 76 show the timing diagrams for asynchronous Reads, synchronous Reads, asynchronous Writes, and synchronous Writes.

An asynchronous Flash Read timing is shown in Figure 65. For Reads, nBE<1:0> are asserted to 0b00. During Flash Writes, nBE<1:0> are asserted to 0b00. Flash accesses are always 16-bit, so they are not used.

7.2.2.1 Flash Asynchronous Read Timing

Figure 65 illustrates a full Latch-addressing mode asynchronous Read cycle for a flash device. Figure 66 illustrates a full Latch-addressing mode asynchronous Read cycle for a flash device using the latched addressing mode (PXA31x and PXA30x only). Refer to Table 26 for detailed timing parameters.

Figure 65: Flash Asynchronous Read Timing Diagram

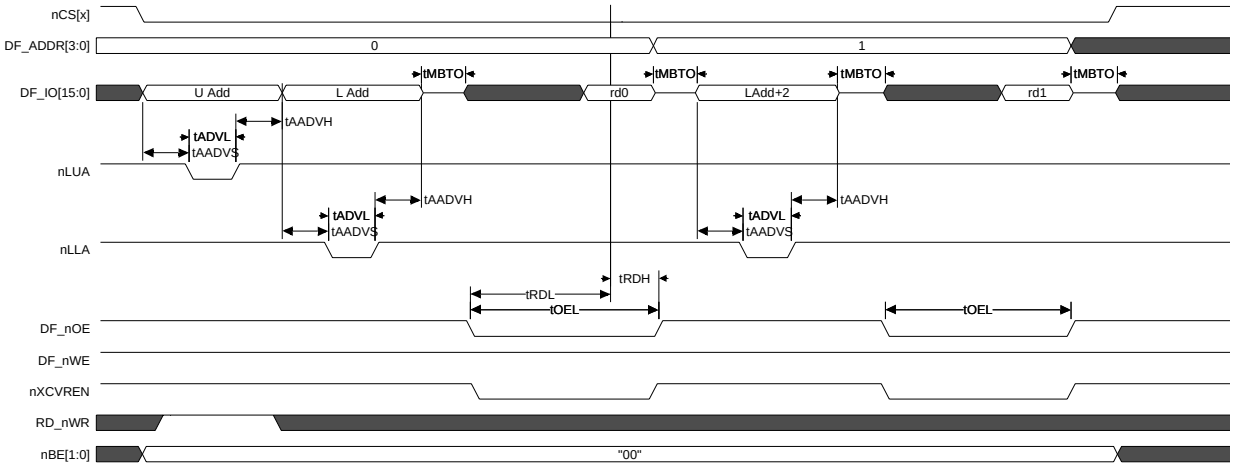
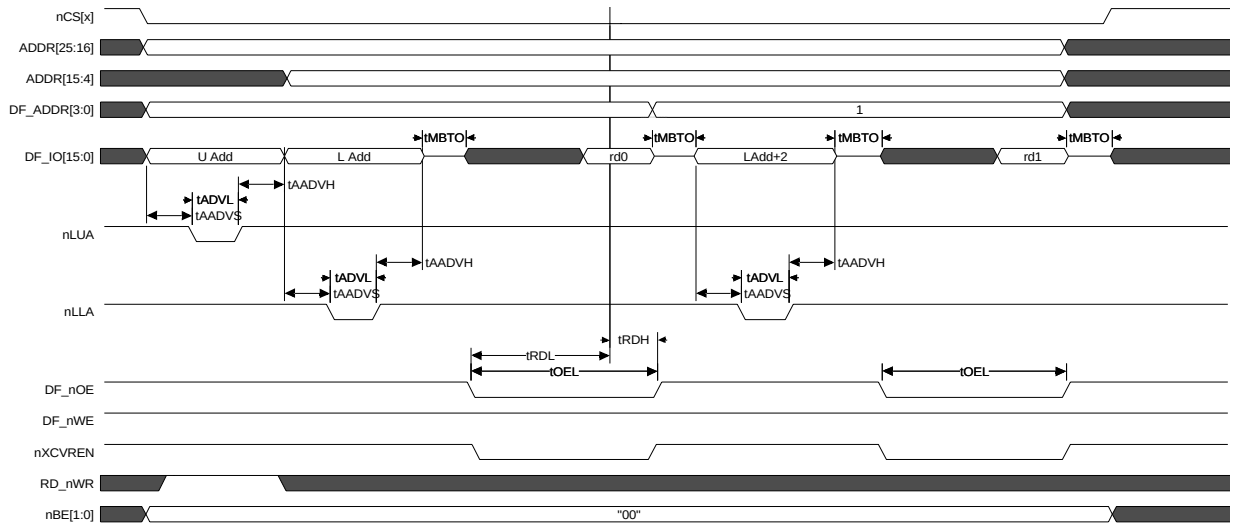


Figure 66: Flash Asynchronous Read Timing Diagram (Latched Addressing Mode)



7.2.2.2 Flash Asynchronous Low-Order Read Timing

Figure 67 illustrates a Low-order Addressing mode asynchronous Read cycle for a flash device. Figure 68 illustrates a Low-order Addressing mode asynchronous Read cycle for a flash device using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 26 for detailed timing parameters.

Figure 67: Flash Asynchronous Low-Order Read Timing Diagram

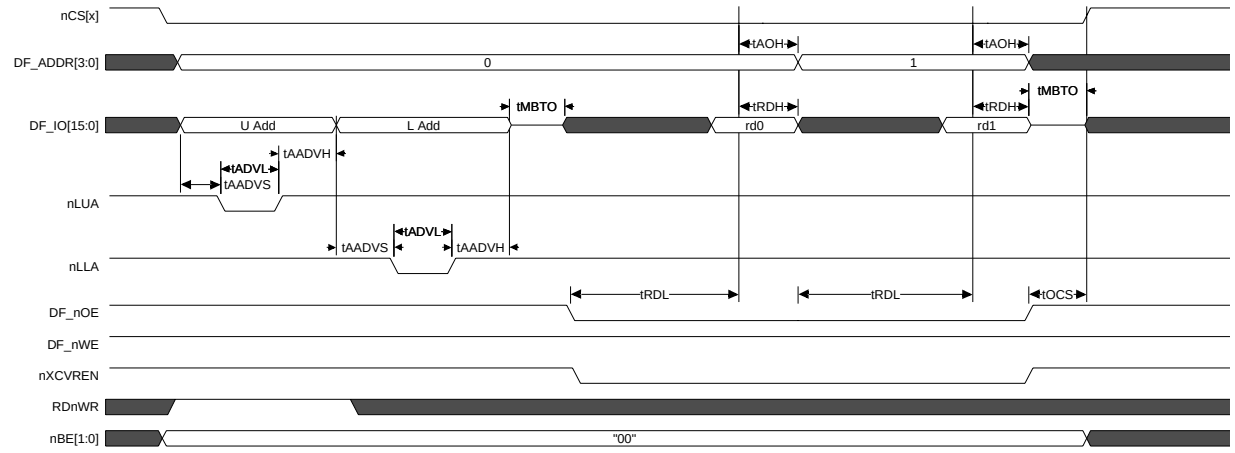
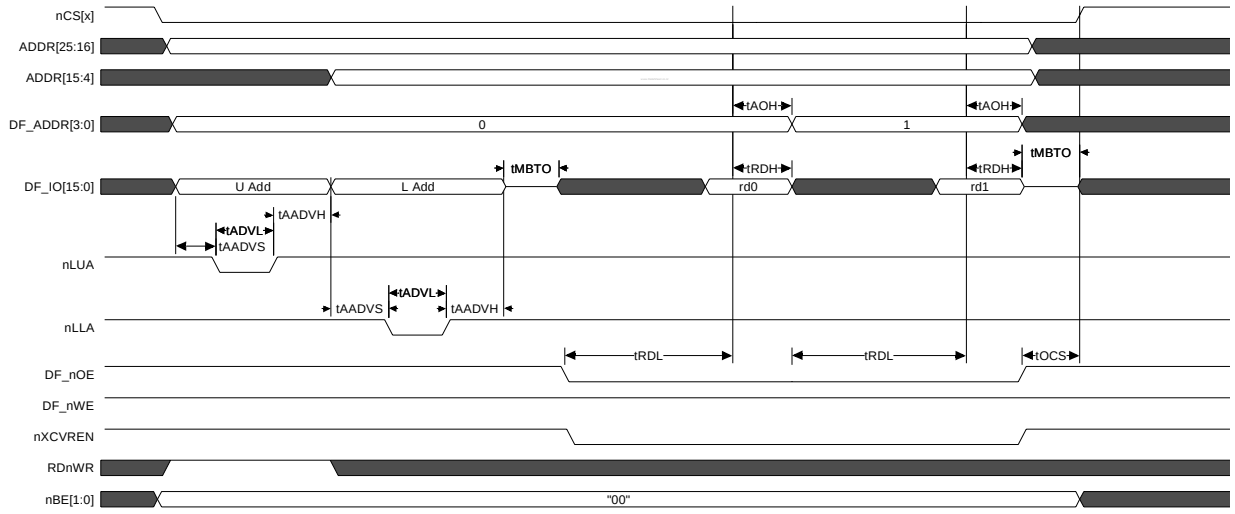


Figure 68: Flash Asynchronous Low-Order Read Timing Diagram (Latched Addressing Mode)



7.2.2.3 Flash Synchronous Read Timing

Figure 69 illustrates Continuous-word Burst mode Flash-Read cycles. Figure 70 illustrates Continuous-word Burst mode Flash-Read cycles using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 26 for detailed timing parameters.

Figure 69: Flash Synchronous Read Timing Diagram

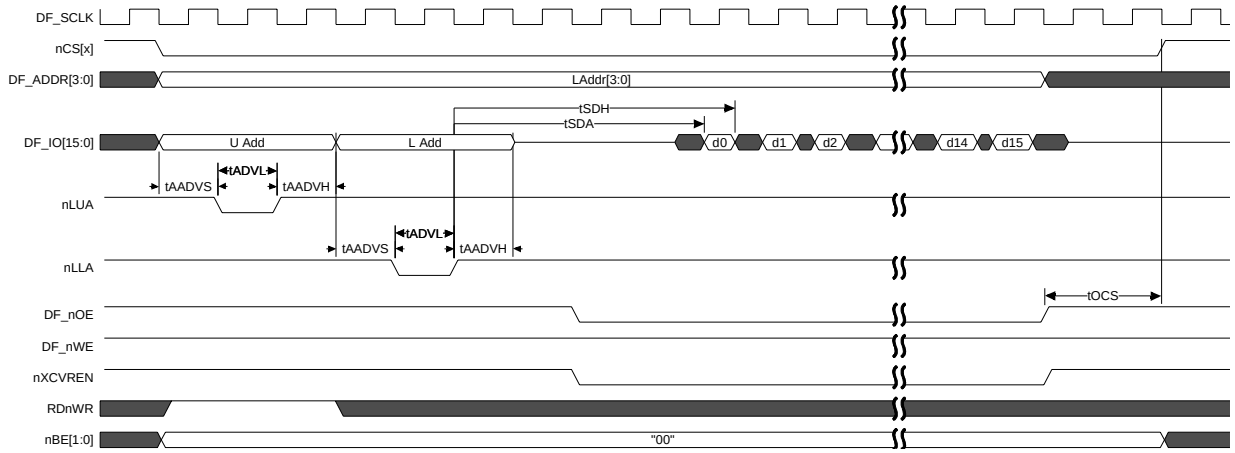
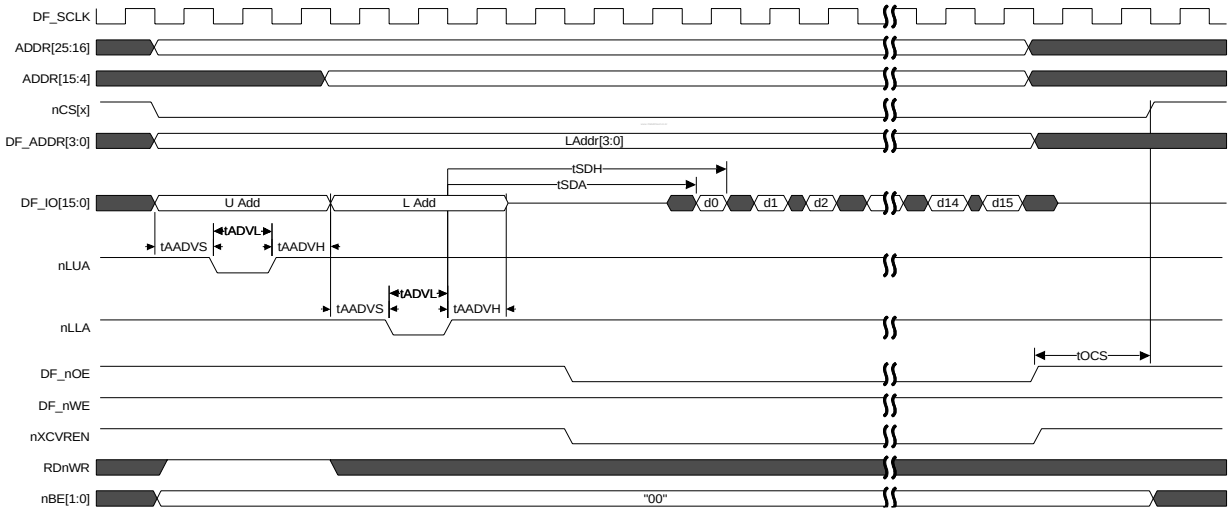


Figure 70: Flash Synchronous Read Timing Diagram (Latched Addressing Mode)



7.2.2.4 Flash Asynchronous Write Timing

Figure 71 illustrates full Latch-mode asynchronous Flash-Write cycles. Figure 72 illustrates full Latch-mode asynchronous Flash-Write cycles using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 26 for detailed timing parameters.

Figure 71: Flash Asynchronous Write Timing Diagrams

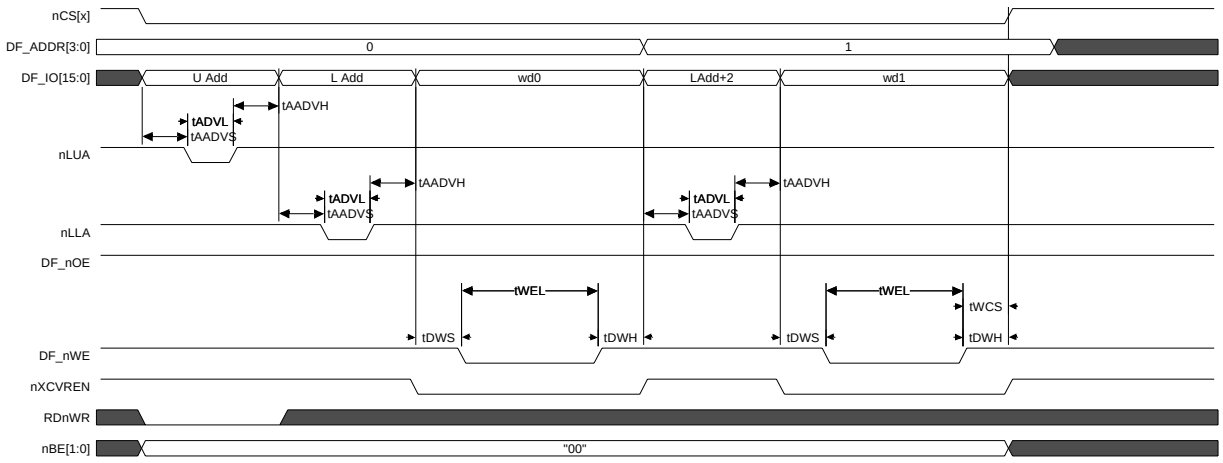
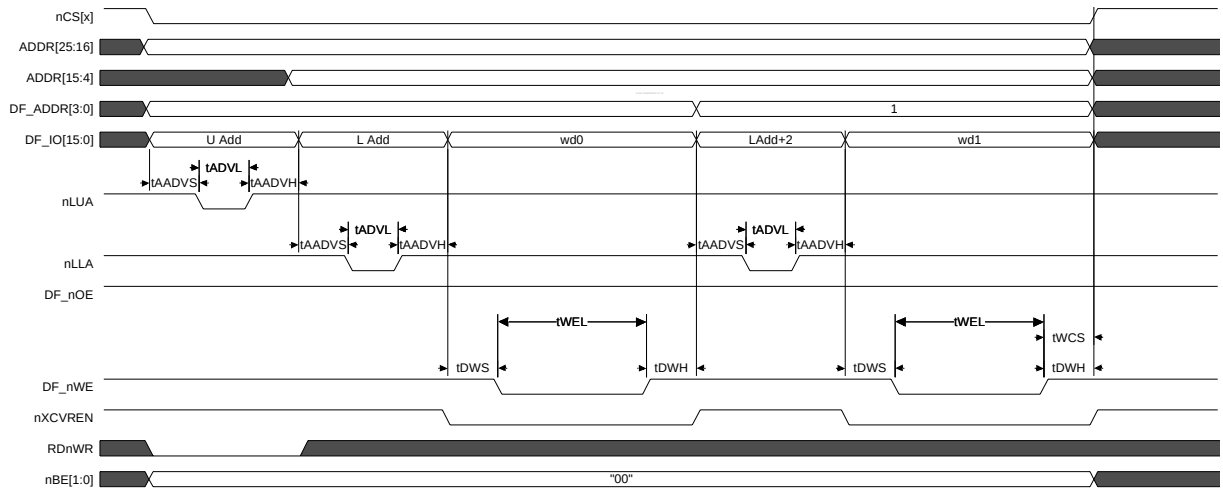


Figure 72: Flash Asynchronous Write Timing Diagrams (Latched Addressing Mode)



7.2.2.5 Flash Asynchronous Low-Order Addressing Write Timing

Figure 73 illustrates a Low-order Addressing mode asynchronous Flash-Write cycle. Figure 74 illustrates a Low-order Addressing mode asynchronous Flash-Write cycle using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 26 for detailed timing parameters.

Figure 73: Flash Asynchronous Low-Order Addressing Write Timing Diagrams

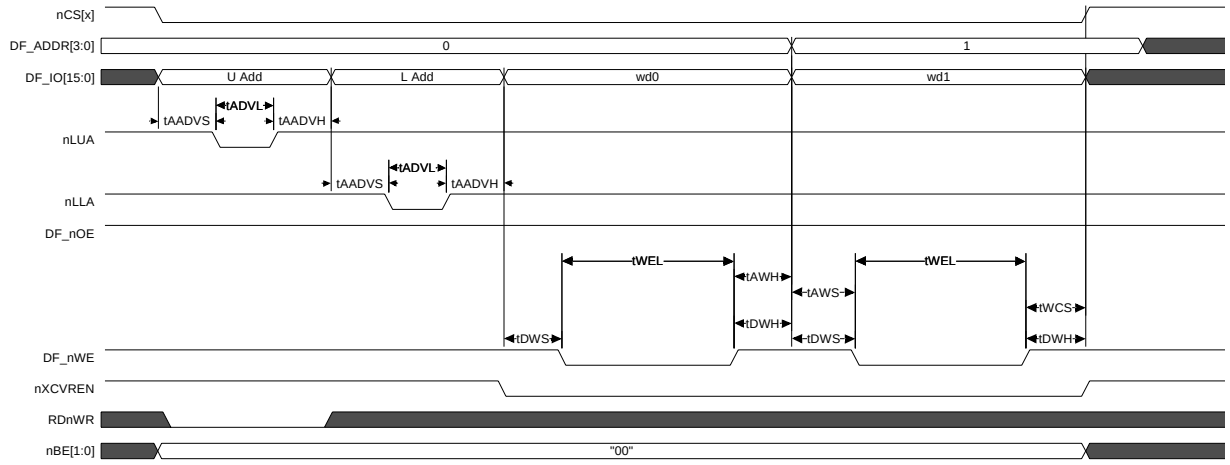
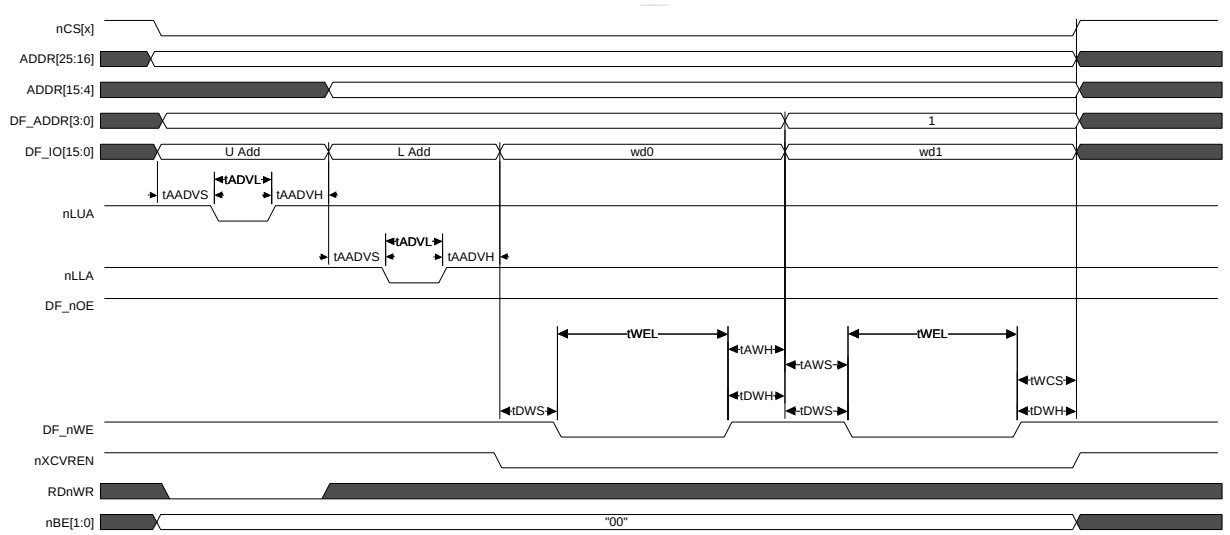


Figure 74: Flash Asynchronous Low-Order Addressing Write Cycle Timing Diagram



7.2.2.6 Synchronous Write Timings

Figure 75 illustrates synchronous Flash-Write cycles. Figure 76 illustrates synchronous Flash-Write cycles using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 26 for detailed timing parameters.

Figure 75: Synchronous Write Timings Diagrams

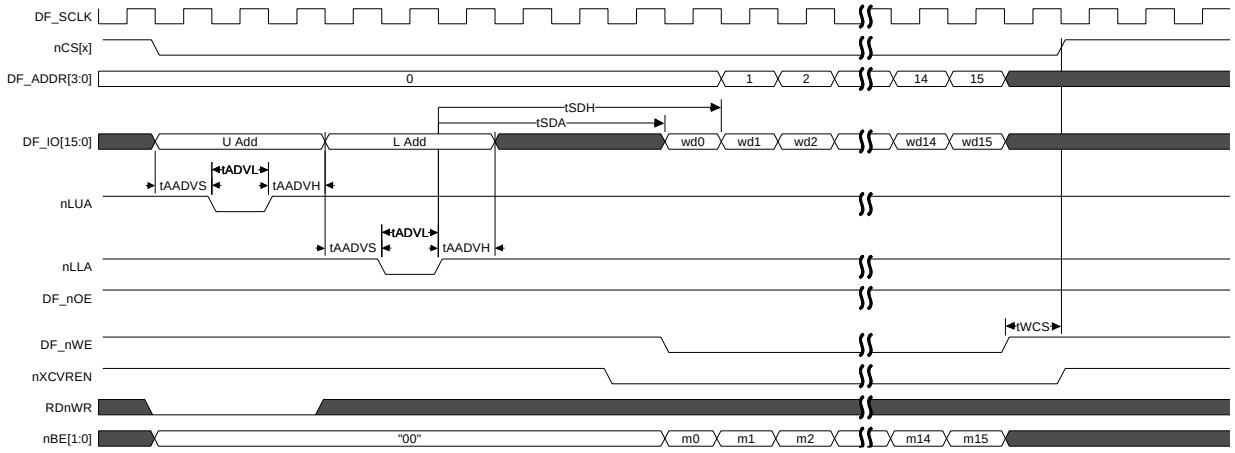


Figure 76: Synchronous Write Timings Diagrams (Latched Addressing Mode)

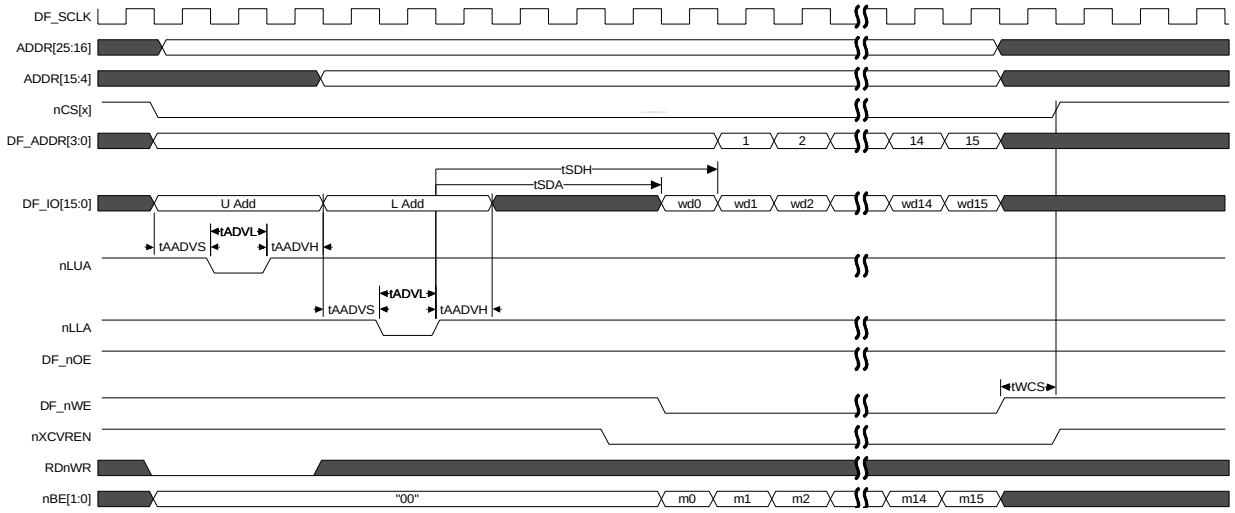


Table 26: DFI Flash Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t_{AADVH}	Address hold from nLLA/nLUA de-asserted	0	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{AADVS}	Address setup to nLLA/nLUA asserted	0	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{ADVL}	nLLU/nLLA assert time	1	CSADRCFGx[ALW]	7	DF_SCLK	1

Table 26: DFI Flash Timing Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
t_{DWS}	Data, Byte enables, and XCVREN setup to DF_nWE asserted	—	1	—	DF_SCLK	1
t_{DWH}	Data, Byte enables, and XCVREN hold from DF_nWE de-asserted	—	1	—	DF_SCLK	1
t_{WCS}	DF_nWE de-asserted to nCS de-asserted	—	1	—	DF_SCLK	1
t_{OCS}	DF_nOE de-asserted to nCS de-asserted	—	6	—	DF_SCLK	1
t_{WEL}	DF_nWE assert time	1	MCS0/1[RDF] +1	16	DF_SCLK	1
t_{OEL}	DF_nOE assert time	2	MCS0/1[RDF] + 2	17	DF_SCLK	1
t_{RDL}	DF_nOE assertion to read data latch	1	MCS0/1[RDF] + 1	16	DF_SCLK	1
t_{AOS}	Address setup to DF_nOE assert	—	1	—	DF_SCLK	1
t_{AWH}	Address hold from DF_nWE de-assert	—	1	—	DF_SCLK	1
t_{AWS}	Address setup to DF_nWE assert	—	1	—	DF_SCLK	1
t_{AOH}	Address hold from data sample	—	1	—	DF_SCLK	1
t_{RDH}	Read data hold from sample (Asynchronous Reads)	—	1	—	DF_SCLK	1
t_{SDH}	Synchronous Flash Read Data hold time	4	SXCNFG[SXCL2] + 1	11	DF_SCLK	1
t_{SDA}	Synchronous Flash Read Data access time	3	SXCNFG[SXCL2]	10	DF_SCLK	1
t_{SDH}	Synchronous write data hold time	4	SXCNFG[SXWRCL2] + 1	11	DF_SCLK	1
t_{SDA}	Synchronous write data access time	3	SXCNFG[SXWRCL2]	10	DF_SCLK	1
t_{MBTO}	Minimum Bus Turnover time	—	1	—	DF_SCLK	1

NOTE:
1. DF_SCLK frequency depends on the ACCR[SMCFS] and MEMCLKCFG[DF_CLKDIV] programmed values.
2. The maximum DF_SCLK frequency for synchronous accesses is 52 MHz.
3. Refer to the PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual for more information on the CSADRCFGx, SXCNFG and MCS0/1 registers.

7.2.3 SRAM Timing Diagrams and Specifications

An SRAM Read timing is shown in Figure 77. For Reads, nBE<1:0> are asserted to 0b00. During Writes, data pins are actively driven by the processor (that is, they are not three-stated), regardless of the state of the individual nBE pins. The nBE pins are used as Byte Enables for these Writes.

The SRAM accesses shown in Figure 77 and Figure 84 illustrate the Low-order Address mode that uses the DF_ADDR<3:0> bus to change the address without having to go through the time-consuming address-latching process that uses the nLUA and nLLA signals.

7.2.3.1 SRAM Asynchronous Read Timing

Figure 77 illustrates a full Latch-addressing mode asynchronous-SRAM Read cycle. Figure 78 illustrates a full Latch-addressing mode asynchronous-SRAM Read cycle using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 27 for detailed timing parameters.

Figure 77: SRAM Asynchronous Read Timing Diagram.

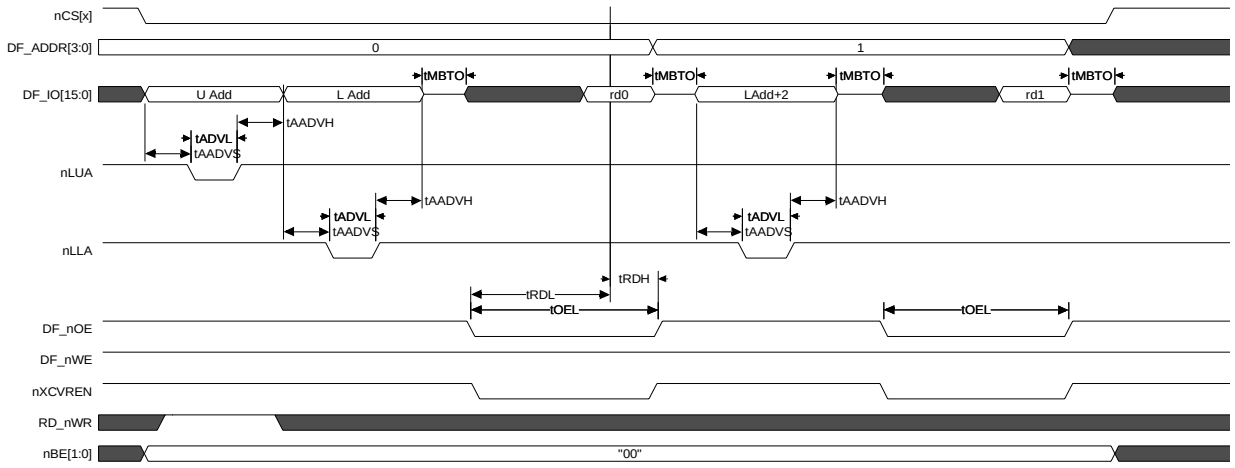
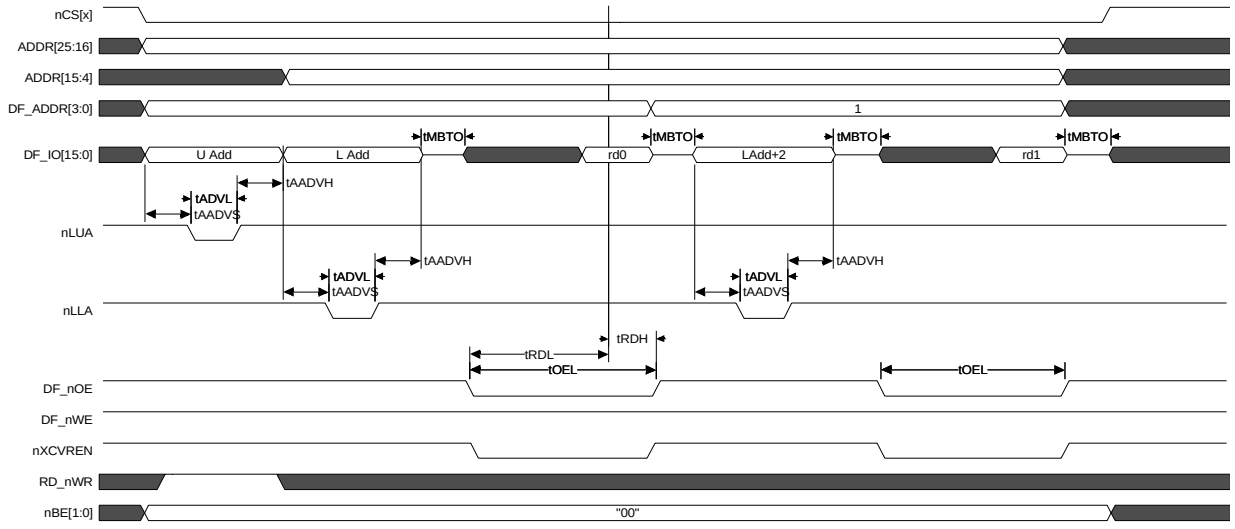


Figure 78: SRAM Asynchronous Read Timing Diagram (Latched Addressing Mode)



7.2.3.2 SRAM Asynchronous Low-Order Addressing Read Timing

Figure 79 illustrates a Low-order Addressing mode asynchronous-SRAM Read cycle. Figure 79 illustrates a Low-order Addressing mode asynchronous-SRAM Read cycle using the Latched-addressing mode (PXA31x and PXA30x only). Refer to Table 27 for detailed timing parameters.

Figure 79: SRAM Asynchronous Low-Order Addressing Read Timing Diagram

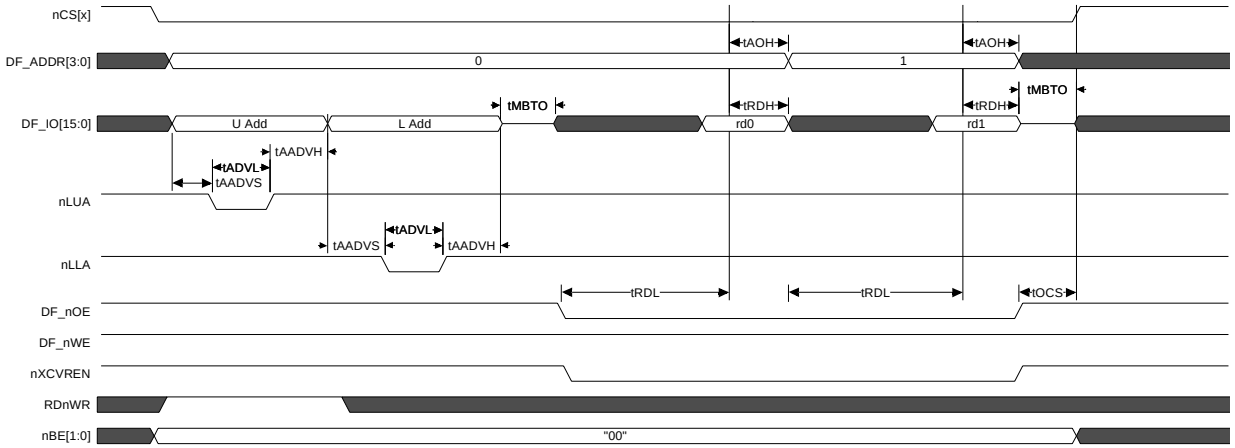
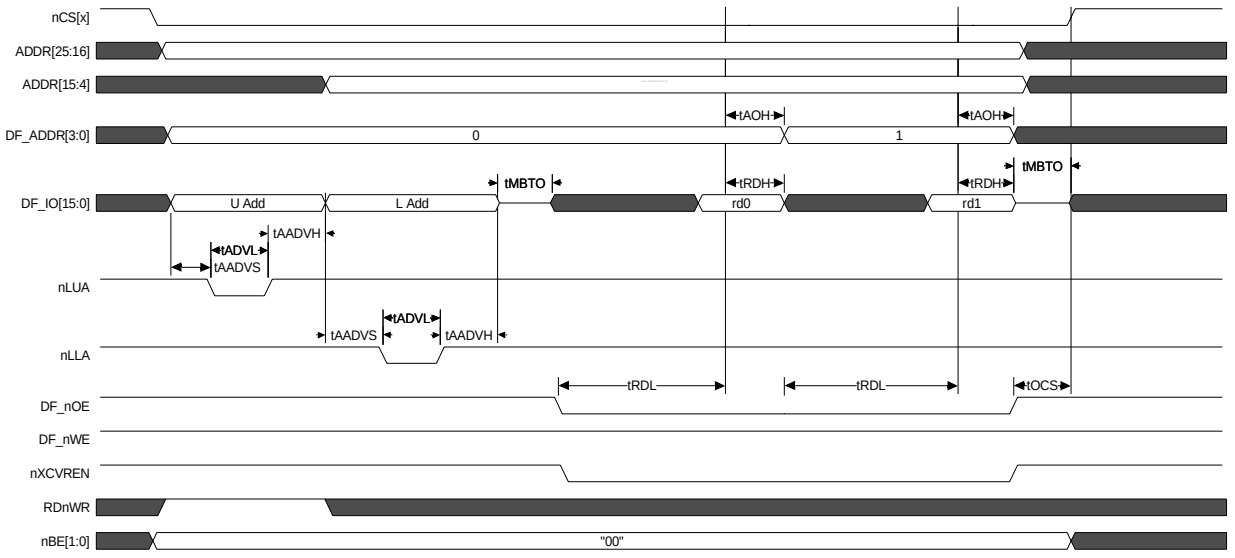


Figure 80: SRAM Asynchronous Read Timing Diagram (Non-AA/D Addressing Mode)



7.2.3.3 SRAM Asynchronous Write Timing

Figure 81 illustrates a full Latch-addressing mode asynchronous-SRAM Write cycle. Figure 82 illustrates a full Latch-addressing mode asynchronous-SRAM Write cycle using the Latched-addressing mode (PXA31x and PXA30x Only). Refer to Table 27 for detailed timing parameters.

Figure 81: SRAM Asynchronous Write Timing Diagram

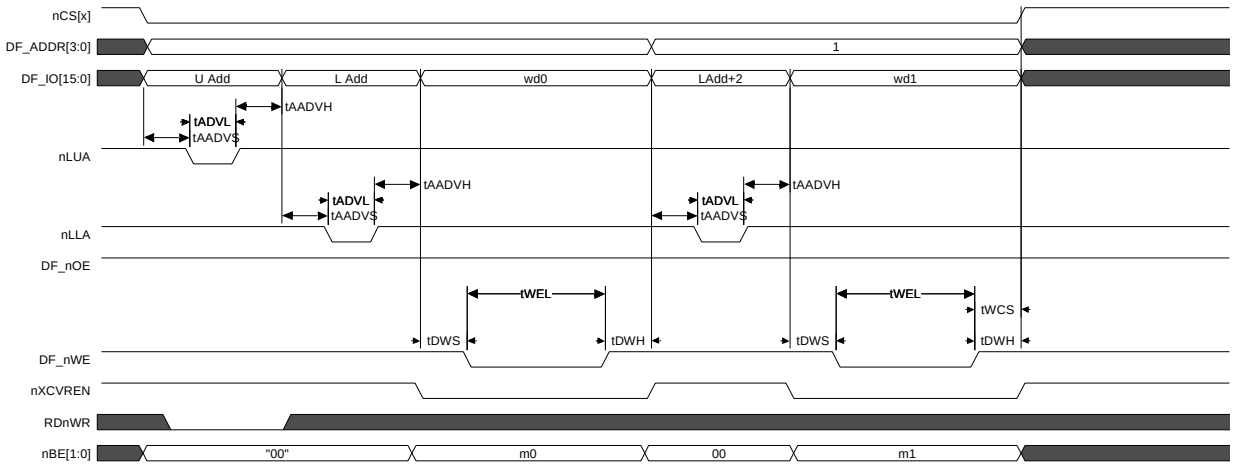
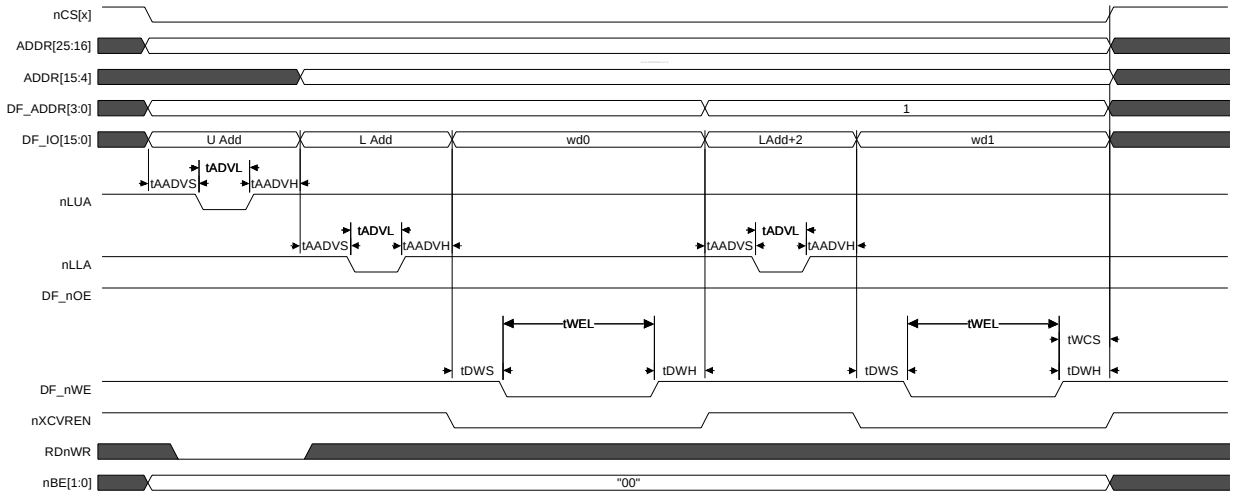


Figure 82: SRAM Asynchronous Write Timing Diagram (Latched Addressing Mode)



7.2.3.4 SRAM Asynchronous Low-Order Addressing Write Timing

Figure 83 illustrates a Low-order Addressing mode asynchronous-SRAM Write cycle. Figure 84 illustrates a Low-order Addressing mode asynchronous-SRAM Write cycle using the latched addressing mode (PXA31x and PXA30x Only). Refer to Table 27 for detailed timing parameters.

Figure 83: SRAM Asynchronous Low-Order Addressing Write Timing Diagram

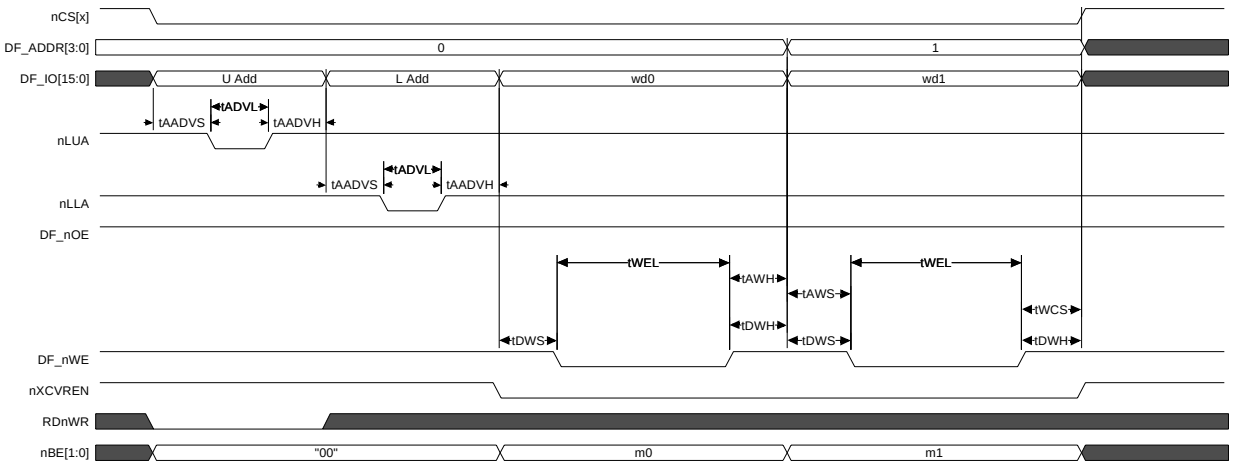


Figure 84: SRAM Asynchronous Low-Order Addressing Write Timing Diagram (Latched Addressing Mode)

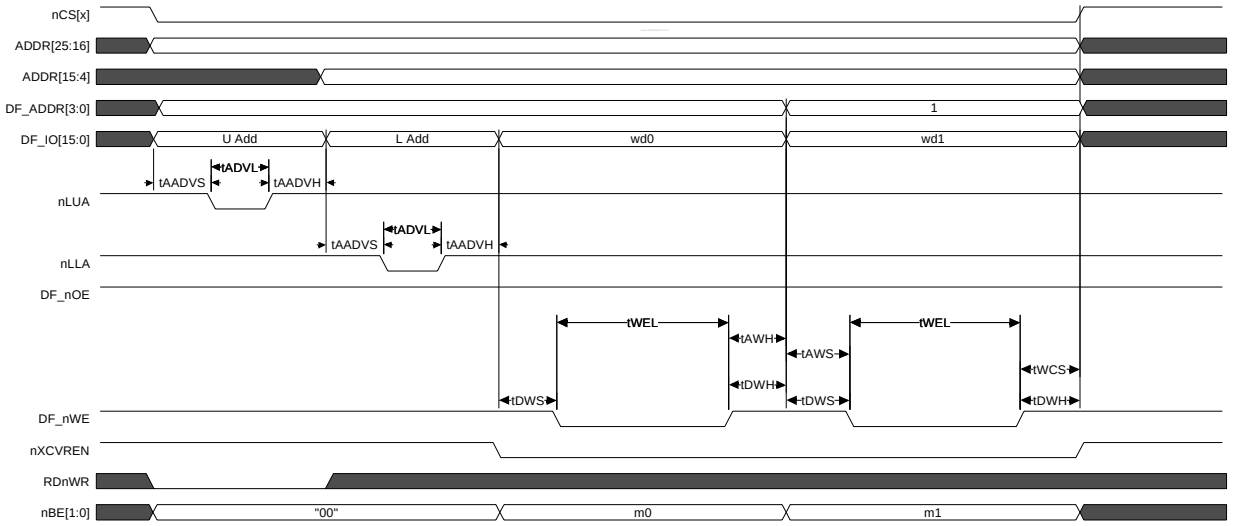


Table 27: DFI SRAM Timing Specifications

Symbol	Description	Min[2]	Min[3]	Min[4]	Typical	Max	Units	Notes
t_{AADVS}	Address setup to nLLA/nLUA asserted	1	1	1	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{AADVH}	Address hold from nLLA/nLUA deasserted	1	1	1	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{ADVL}	nLLA/nLUA assert time	1	1	2	CSADRCFGx[ALW]	7	DF_SCLK	1
t_{DWS}	Data, Byte enables, and XCVREN setup to DF_nWE asserted	—	—	—	1	—	DF_SCLK	1
t_{DWH}	Data, Byte enables, and XCVREN hold from DF_nWE deasserted	—	—	—	1	—	DF_SCLK	1
t_{WCS}	DF_nWE de-asserted to nCS de-asserted	—	—	—	1	—	DF_SCLK	1
t_{OCS}	DF_nOE de-asserted to nCS de-asserted	—	—	—	1	—	DF_SCLK	1
t_{WEL}	DF_nWE assert time	2	2	3	MCS0/1[RDN] + 1	16	DF_SCLK	1
t_{OEL}	DF_nOE assert time	3	4	7	MCS0/1[RDF] + 2	17	DF_SCLK	1
t_{RDL}	DF_nOE assertion to read data latch	2	3	6	MCS0/1[RDF] + 1	16	DF_SCLK	1
t_{AWS}	Address setup to DF_nWE assert	—	—	—	1	—	DF_SCLK	1
t_{AWH}	Address hold from DF_nWE de-assert	—	—	—	1	—	DF_SCLK	1
t_{AOH}	Address hold from data sample	—	—	—	1	—	DF_SCLK	1
t_{RDH}	Read data hold from sample	—	—	—	1	—	DF_SCLK	1
t_{MBTO}	Minimum Bus Turnover time	—	—	—	1	—	DF_SCLK	1

NOTE:
1. DF_SCLK frequency depends on the ACCR[SMCFS] and MEMCLKCFG[DF_CLKDIV] programmed values.
2. DF_SCLK = 52 MHz
3. DF_SCLK = 104 MHz
4. DF_SCLK = 208 MHz
5. Refer to the PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual for more information on the CSADRCFGx and MCS0/1 registers.

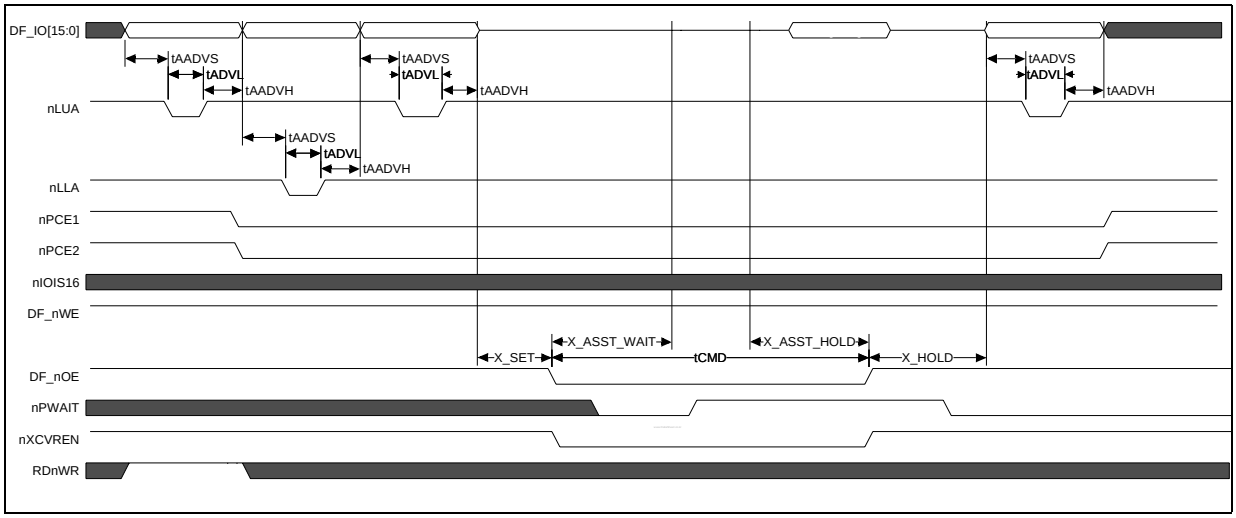
7.2.4 Compact Flash Timing Diagrams and Specifications

The PXA32x processor card interface provides control for one card, supports 8- and 16-bit peripherals, and handles common memory, I/O, and attribute-memory accesses. The duration of each access is based on programmed values per address space by fields within the MCMEMx, MCATTx, and MCIOx registers. The processors are described in detail in the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual*.

7.2.4.1 Compact Flash 16-Bit Common Memory Read Timing.

Table 85 illustrates a read cycle from Compact Flash common memory. Refer to Table 28 for detailed timing parameters.

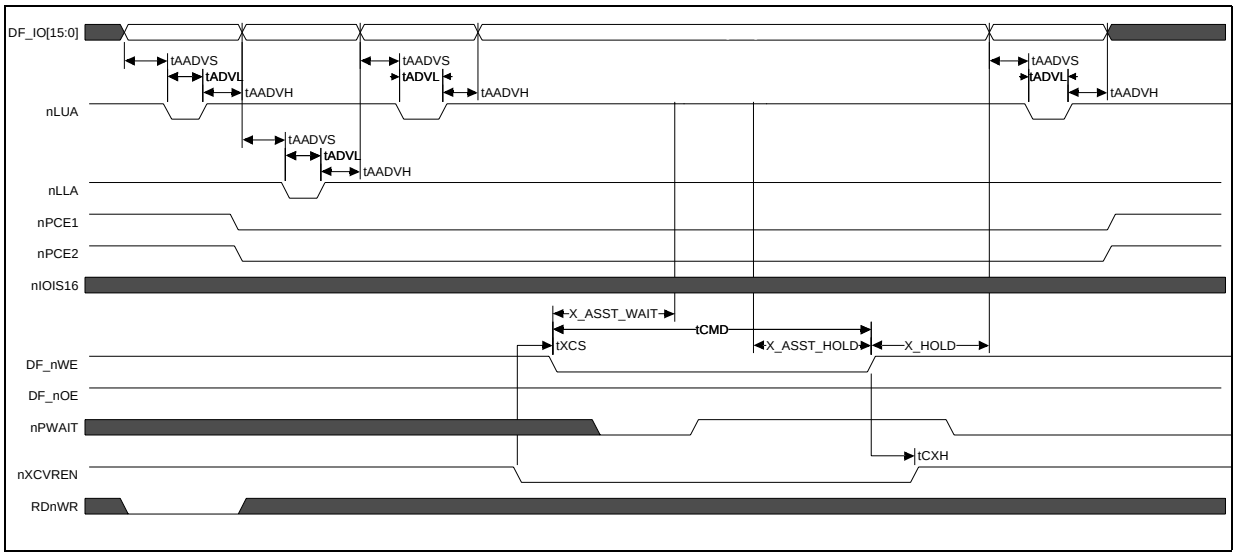
Figure 85: Compact Flash 16-Bit Common Memory Read Timing Diagram



7.2.4.2 Compact Flash 16-Bit Common Memory Write Timing.

Table 86 illustrates a write cycle to Compact Flash common memory. Refer to Table 28 for detailed timing parameters.

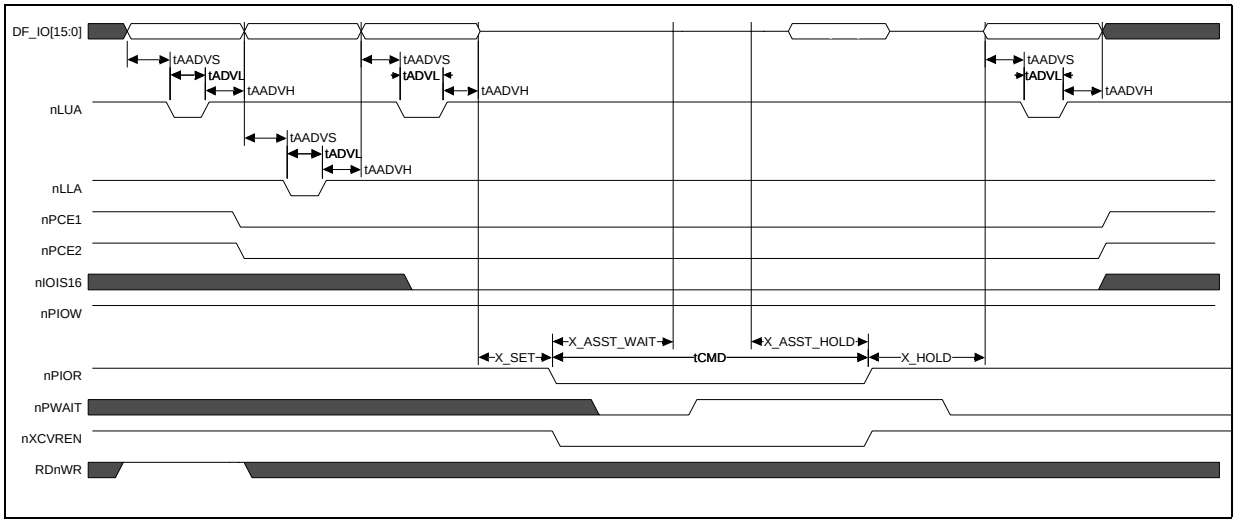
Figure 86: Compact Flash 16-Bit Common Memory Write Timing Diagram.



7.2.4.3 Compact Flash 16-Bit I/O Space Read Timing

Table 87 illustrates a 16-bit read cycle from Compact Flash I/O space memory. Refer to Table 28 for detailed timing parameters.

Figure 87: Compact Flash 16-Bit I/O Memory Read Timing Diagram



7.2.4.4 Compact Flash 8-Bit I/O Space Write Timing.

Table 88 illustrates a 8-bit write cycle to Compact Flash I/O space memory. Refer to Table 28 for detailed timing parameters.

Figure 88: Compact Flash 8-Bit I/O Space Write Timing Diagram.

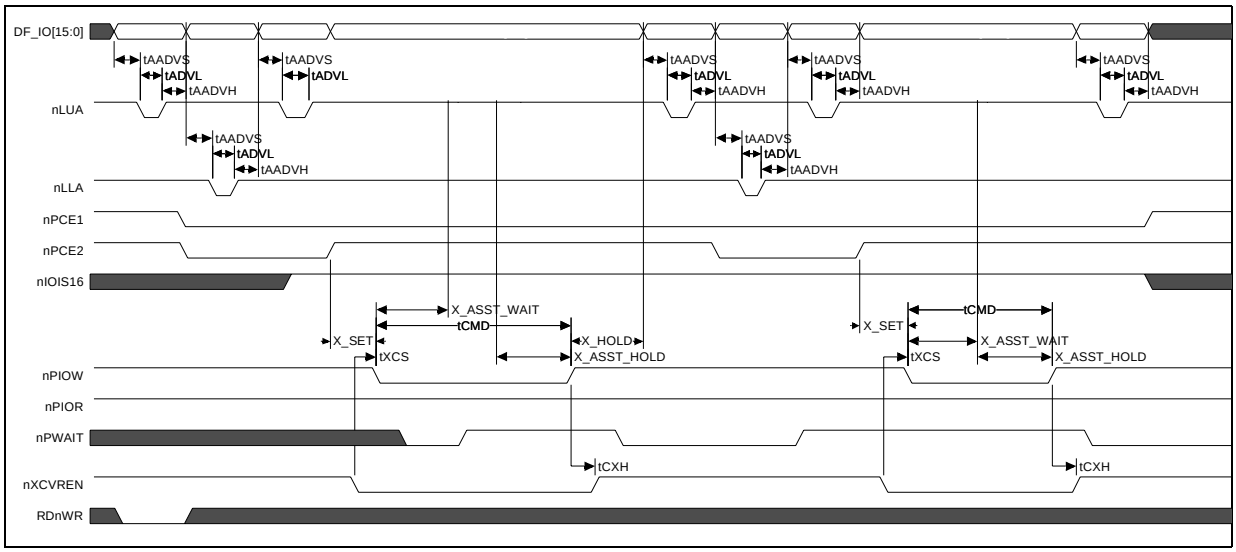


Table 28: Compact Flash Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t_{AADVS}	Address setup to nLLA/nLUA asserted	0	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{AADVH}	Address hold from nLLA/nLUA de-asserted	0	CSADRCFGx[ALT]	1	DF_SCLK	1
t_{ADVL}	nLLA/nLUA assert time	1	CSADRCFGx[ALW]	7	DF_SCLK	1
t_{X_HOLD}	Command de-assert to nPCE de-assert via nLUA command	1	MCx0[HOLD]	63	DF_SCLK	1
t_{X_SET}	Address valid to command assert	1	MCx0[SET]	127	DF_SCLK	1
$t_{X\_ASST\_WAIT}$	Command assert to when nPWAIT is sampled	1	MCx0[0_ASST]+1	32	DF_SCLK	1
$t_{X\_ASST\_HOLD}$	nPWAIT sample high to command de-asserted	1	(2*MCx0[0_ASST])+1	63	DF_SCLK	1
t_{XCS}	nXCVREN assert to command assert	1	MCx0[SET]	127	DF_SCLK	1
t_{CXH}	Command de-assert to nXCVREN de-assert	1	MCx0[HOLD]	63	DF_SCLK	1
t_{CMD}	Command assertion time	3	(3*MCx0[0_ASST])+3+ waits	96	DF_SCLK	1

Table 28: Compact Flash Timing Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes

NOTE:
1. DF_SCLK frequency depends on the ACCR[SMCFS] and MEMCLKCFG[DF_CLKDIV] programmed values.
6. Refer to the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual* for more information on the CSADRCFGx, MCMEMx, MCATTx, and MCIOx registers.

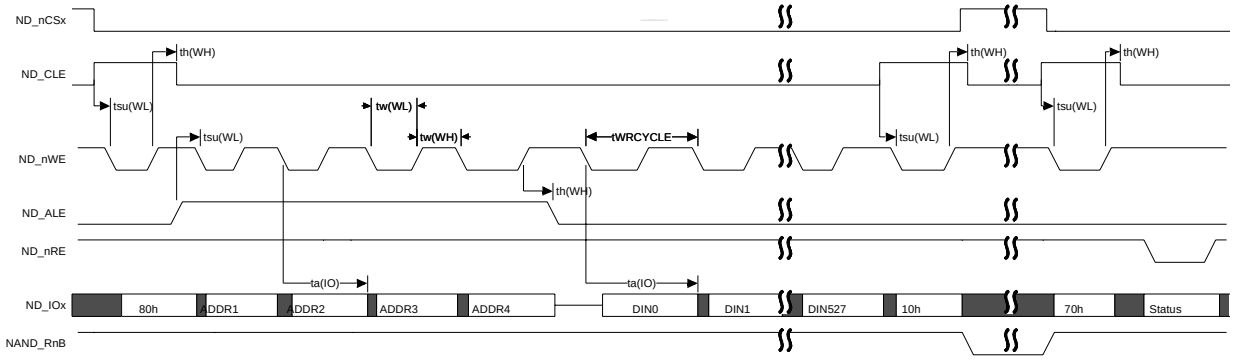
7.2.5 NAND Timing Diagrams and Specifications

This section describes the timing diagrams for NAND flash programming, erase, read, status read, and ID read with timing parameters.

7.2.5.1 NAND Flash Program Timing

Data-flash program operation writes data to the Flash. Figure 89 illustrates the programming sequence for a Flash device with a page size of 512 bytes, and a spare area of 16 bytes. The Flash device is addressed in four cycles. Refer to Table 29 for the detailed descriptions of the timing parameters. If the Auto-read Status bit (AUTO_RS) is set in the command, the NAND Flash Controller performs a status check (command 0x70) to determine whether the program operation was successful.

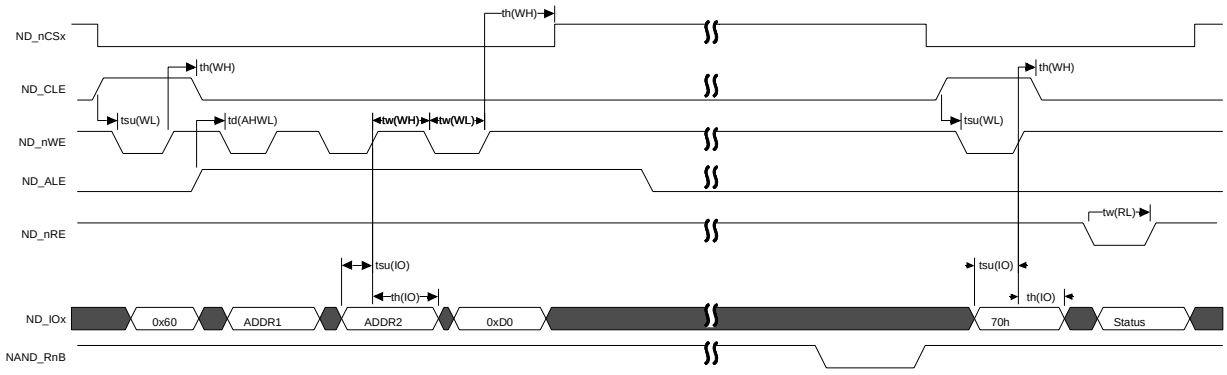
Figure 89: NAND Flash Program Timing Diagram



7.2.5.2 NAND Flash Erase Timing

Figure 90 illustrates the erase sequence for a Flash device. The block to be erased in the Flash device is addressed in two cycles. Refer to Table 29 for the detailed descriptions of the timing parameters. If the Auto-read Status bit (AUTO_RS) is set in the command, the Data Flash Controller performs a status check (Command 0x70) to determine whether the Erase operation was successful.

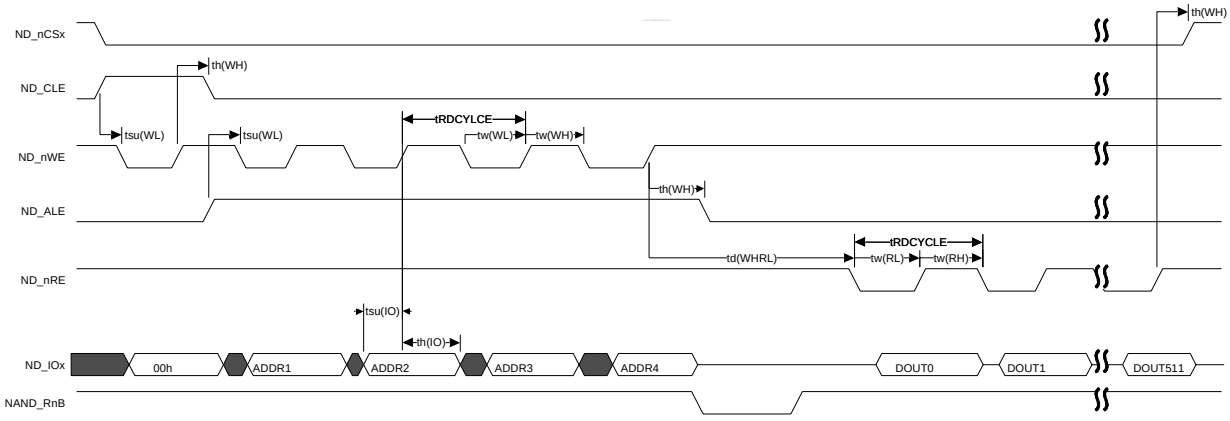
Figure 90: NAND Flash Erase Timing Diagram



7.2.5.3 Small Block NAND Flash Read Timing

Figure 91 illustrates the Read sequence for a Small-block Flash device. The Flash device is addressed in four cycles. Refer to Table 29 for detailed descriptions of the timing parameters.

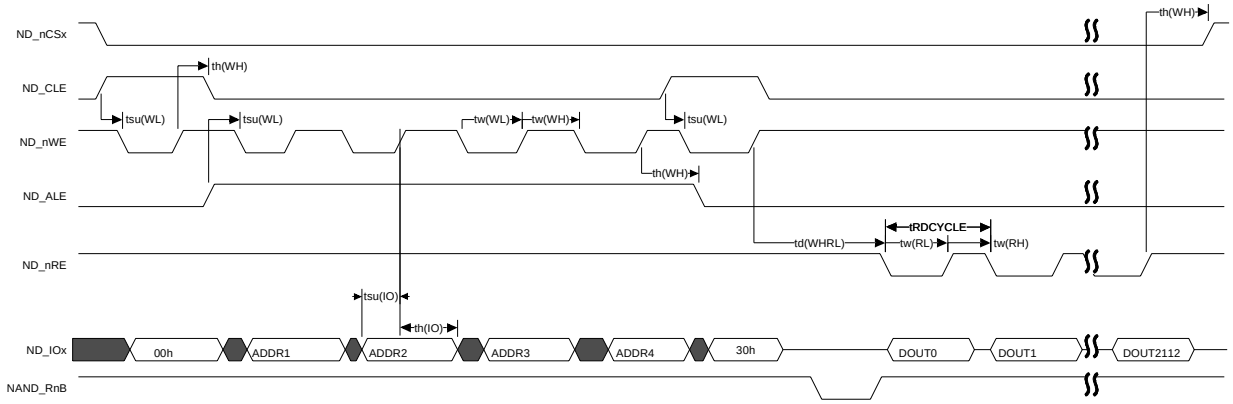
Figure 91: NAND Flash Small Block Read Timing Diagram



7.2.5.4 Large Block NAND Flash Read Timing

Figure 92 illustrates the Read sequence for a Large-block Flash device. The Flash device is addressed in four cycles. Refer to Table 29 for detailed descriptions of the timing parameters.

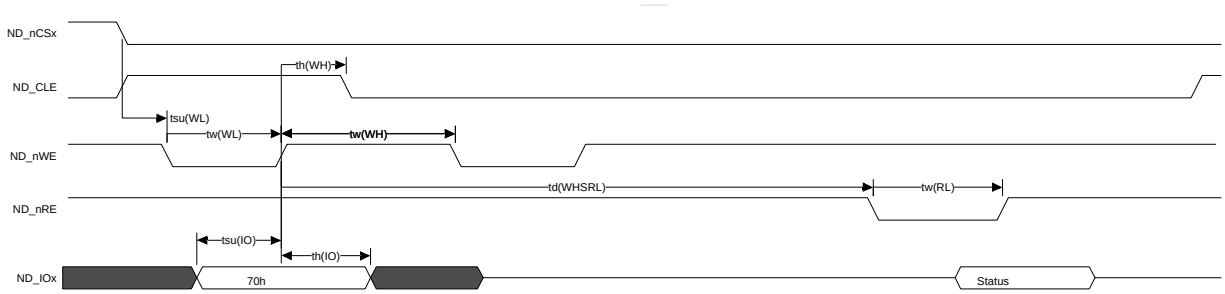
Figure 92: NAND Flash Large Block Read Timing Diagram



7.2.5.5 NAND Flash Status Read Timing

Figure 93 illustrates the Status-read sequence for a Flash device. Refer to Table 29 for detailed descriptions of the timing parameters.

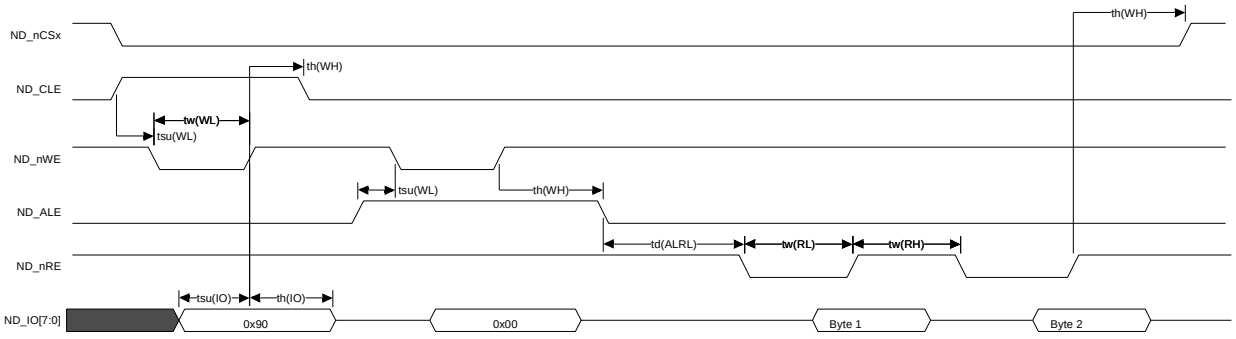
Figure 93: NAND Flash Status Read Timing Diagram



7.2.5.6 NAND Flash ID Read Timing

Figure 94 illustrates the ID read sequence for a Flash device. Refer to Table 29 for detailed descriptions of the timing parameters.

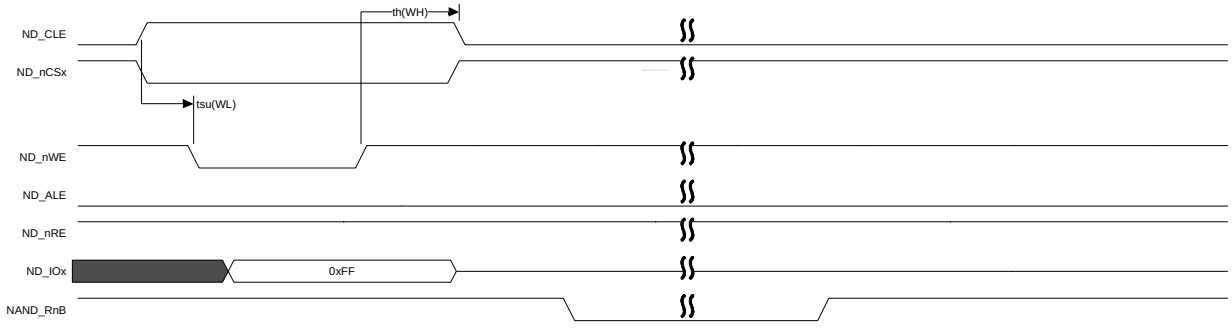
Figure 94: NAND Flash ID Read Timing Diagram



7.2.5.7 NAND Flash Reset Timing

Figure 95 illustrates the reset sequence for a Flash device. Refer to Table 29 for detailed descriptions of the timing parameters.

Figure 95: NAND Flash Reset Timing Diagram



7.2.5.8 NAND Flash Timing Parameters

Table 29 provides the values for the timing parameters seen in Figure 89, Figure 90, Figure 91, Figure 92, Figure 92, Figure 93, Figure 94 and Figure 95.

Table 29: NAND Flash Interface Program Timing Specifications

Symbol	Description	Min[1]	Min[2]	Typical	Max	Units	Notes
$t_{su(WL)}$	Setup time for ND_ALE, ND_CLE and ND_CSx with respect to ND_nWE assertion	1	1	NDTR0CS0[tCS] + 1	8	NCLK	3, 4

Table 29: NAND Flash Interface Program Timing Specifications (Continued)

Symbol	Description	Min[1]	Min[2]	Typical	Max	Units	Notes
$t_{h(WH)}$	Hold time for ND_ALE, ND_CLE and ND_CSx with respect to ND_nWE de-assertion.	2	1	NDTR0CS0[tCH] + 1	8	NCLK	3, 4
$t_{w(WL)}$	ND_nWE pulse width during assertion delay	2	1	NDTR0CS0[tWP] + 1	8	NCLK	3, 4
$t_{w(WH)}$	ND_nWE pulse width during de-assertion delay	2	1	NDTR0CS0[tWH] + 1	8	NCLK	3, 4
$t_{w(RL)}$	ND_nRE pulse width during assertion delay	4	1	NDTR0CS0[tRP] + 1	16	NCLK	3, 4
$t_{w(RH)}$	ND_nRE pulse width during de-assertion delay	3	1	NDTR0CS0[tRH] + 1	8	NCLK	3, 4
$t_{d(WHRL)}$	ND_nWE high to ND_nRE low delay for read	3	3	(NDTR1CS0[tR] + 2) + (NDTR0CS0[tCH] + 1)	65536	NCLK	3, 4
$t_{d(WHSRL)}$	ND_nWE high to ND_nRE low delay for status read	1	1	NDTR1CS0[tWHR][5, 6]	32	NCLK	3, 4
$t_{d(ALRL)}$	ND_ALE high to ND_nRE low delay for ID read	1	1	NDTR1CS0[tAR][7, 8]	16	NCLK	3, 4
$t_{a(IO)}$	ND_IOx data access time	2.5	2.5	—	10	ns	—
$t_{su(IO)}$	ND_IOx setup time constraint	23	23	—	—	ns	—
$t_{h(IO)}$	ND_IOx hold time constraint	23	23	—	—	ns	—
$t_{RDCYCLE}$	Read cycle times	67.31	30	—	—	ns	—
$t_{WRCYCLE}$	Write cycle times	38.46	30	—	—	ns	—

NOTE:
1. PXA32x processor only
2. PXA31x processor and PXA30x processor only
3. NCLK represents the clock period using a 156 MHz clock on the PXA31x processor and PXA30x processor.
4. NCLK represents the clock period using a 104 MHz clock on the PXA32x processor
5. If NDTR0CS1[tAR] + NDTR0CS0[tCH] >= NDTR0CS1[tWHR] Delay = NDTR0CS0[tCH] + (NDTR0CS1[tAR] + 2)
6. If NDTR0CS1[tAR] + NDTR0CS0[tCH] < NDTR0CS1[tWHR] Delay = (NDTR0CS1[tWHR] + 1)
7. If NDTR0CS1[tAR] + NDTR0CS0[tCH] >= NDTR0CS1[tWHR] Delay = NDTR0CS1[tAR] + 1
8. If NDTR0CS1[tAR] + NDTR0CS0[tCH] < NDTR0CS1[tWHR] Delay = (NDTR0CS1[tWHR] - NDTR0CS0[tCH])
9. Refer to the *PXA3xx Processor Family Vol. II: Memory Controller Configuration Developers Manual* for more information on the NDTR0CS0 and NDTR0CS1 registers.

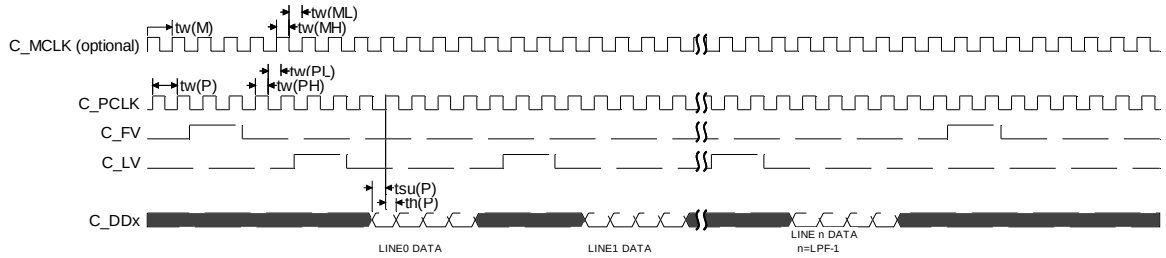
7.3 Quick Capture Camera Interface Timing Diagrams and Specifications

This section describes the timing diagrams for master-parallel mode of operation with timing parameters.

7.3.1 Master-Parallel Timing

The master-parallel interface timing is shown in Figure 96. See Table 30 for camera timing parameters. The frame clock (C_FV) must first be asserted to indicate that a new frame has begun. The valid data is then captured with the active edge of PCLK, after Beginning of Line Wait Count (CICR2[BLW]) PCLK cycles have elapsed from the assertion of C_LV. At the end of the capture of the last line of a frame, the Quick Capture Interface waits for the assertion of C_FV to begin the next frame-capture sequence.

Figure 96: Camera Master-Parallel Timing Diagram



7.3.2 Master-Parallel Interface Timing Specifications

Table 30 describes the camera timing parameters for Figure 96.

Table 30: Master-Parallel Timing Specifications (PXA32x Processor and PXA30x Processor Only)

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{w(M)}$	C_MCLK pulse width frequency	0.48	—	52	MHz	
$t_{w(P)}$	C_PCLK pulse width frequency	3.0	—	48	MHz	1
$t_{w(MH)}$	C_MCLK pulse width high time	9.5	—	4352	nS	
$t_{w(ML)}$	C_MCLK pulse width low time	9.5	—	4352	nS	
$t_{w(PH)}$	C_PCLK pulse width high time	10	—	158.3	nS	
$t_{w(PL)}$	C_PCLK pulse width low time	10	—	158.3	nS	
$t_{su(P)}$	C_DDx to C_PCLK setup time constraint	2.2	—	—	ns	
$t_{h(P)}$	C_PCLK to C_DDx hold time constraint	3.0	—	—	ns	

Table 30: Master-Parallel Timing Specifications (Continued)(PXA32x Processor and PXA30x

Symbol	Description	Min	Typical	Max	Units	Notes
NOTE: 1. Maximum allowable frequency of C_PCLK is 1/4 of System bus #1 (Application Subsystem Clock Configuration Register (ACCR[HSS])).						

Table 31: Master-Parallel Timing Specifications (PXA31x Processor Only)

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{w(M)}$	C_MCLK pulse width frequency	0.48	—	52	MHz	
$t_{w(P)}$	C_PCLK pulse width frequency	3.0	—	96	MHz	1
$t_{w(MH)}$	C_MCLK pulse width high time	9.5	—	4352	nS	
$t_{w(ML)}$	C_MCLK pulse width low time	9.5	—	4352	nS	
$t_{w(PH)}$	C_PCLK pulse width high time	4.95	—	158.3	nS	
$t_{w(PL)}$	C_PCLK pulse width low time	4.95	—	158.3	nS	
$t_{su(P)}$	C_DDx to C_PCLK setup time constraint	2.2	—	—	ns	
$t_{h(P)}$	C_PCLK to C_DDx hold time constraint	3.0	—	—	ns	
NOTE: 1. Maximum allowable frequency of C_PCLK is 1/2 of System bus #1 (Application Subsystem Clock Configuration Register (ACCR[HSS]))						

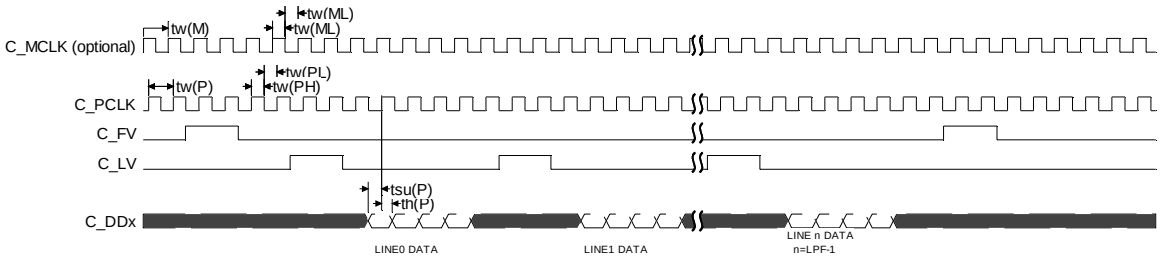
7.3.3 Slave-Parallel Timing

Figure 97 shows the timing for slave-parallel mode of operation. See Table 32 for the slave-parallel timing parameters. The timing is very similar to that of master-slave, except that in Slave-Parallel mode, the Quick Capture Interface drives the synchronization signals C_LV and C_FV. C_FV and C_LV are driven for the duration specified by Vertical Sync Width (CICR3[VSW]) and Horizontal Sync Width (CICR2[HSW]), respectively. The delay (in PCLK cycles) between C_FV being asserted and C_LV being asserted is configured with CICR2[BFPW]. The number of frame clock (C_FV) periods to wait before valid data is output is configured with CICR2[FSW].

Note

Before the Quick Capture Interface starts operating in this mode, configure the sensor to float the synchronization pins.

Figure 97: Camera Slave-Parallel Timing Diagram



7.3.4 Slave-Parallel Interface Timing Parameters

Table 32 describes the camera timing parameters for Figure 97.

Table 32: Slave-Parallel Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{w(M)}$	C_MCLK pulse width frequency	0.203	—	52	MHz	
$t_{w(P)}$	C_PCLK pulse width frequency	3.0	—	6.25	MHz	
$t_{w(MH)}$	C_MCLK pulse width high time	9.5	—	2338	ns	
$t_{w(ML)}$	C_MCLK pulse width low time	9.5	—	2338	ns	
$t_{w(PH)}$	C_PCLK pulse width high time	76	—	158.3	ns	
$t_{w(PL)}$	C_PCLK pulse width low time	76	—	158.3	ns	
$t_{su(P)}$	C_DDx to C_PCLK setup time constraint	3.7	—	—	ns	
$t_{h(P)}$	C_PCLK to C_DDx hold time constraint	0.0	—	—	ns	

7.4 LCD Timing Diagrams and Specifications

This section describes the timing diagrams for interfacing to Passive, Active, and Smart LCD panels with timing parameters.

7.4.1 LCD Passive Timing

For Passive (and Active) LCD panels, the line-clock pin (L_LCLK_A0) is toggled when an entire line of pixels has been output to the LCD Controller screen. Likewise, the frame-clock pin (L_FCLK_RD) is toggled when an entire frame of pixels has been output to the LCD Controller screen.

Switch the power and ground supplies periodically to prevent a DC charge from building within a Passive display. The LCD controller signals the display to switch the polarity by toggling the AC bias pin (L_BIAS). Program the number of line-clock transitions between each toggle to control the frequency of the bias pin.

The programmable timing of the line- and frame-clock pins supports both Passive and Active mode. Programming options include: wait-state insertion both at the beginning and end of each line and frame; pixel clock; line clock; frame clock; output-enable signal polarity; and frame-clock pulse width.

Figure 98 and Figure 99 illustrate the LCD timing parameters. Table 33 provides the values for the parameters.

Figure 98: LCD Passive Panel Synchronous Timing Diagram

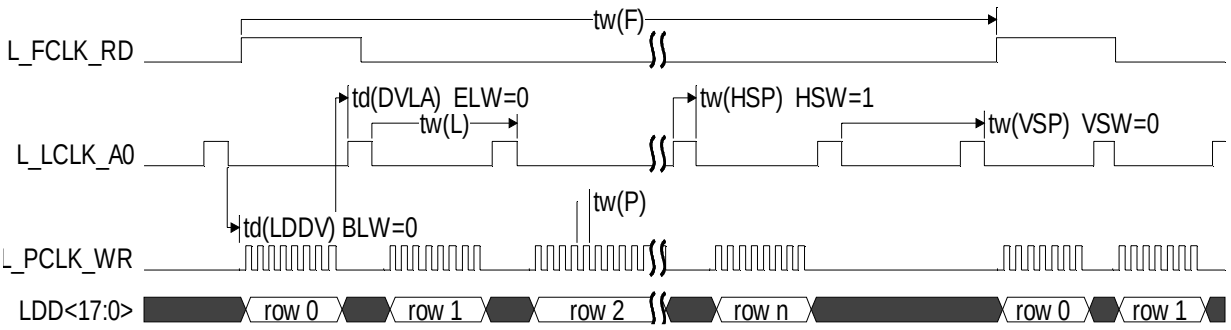


Figure 99: LCD Passive Panel Data Timing Diagram

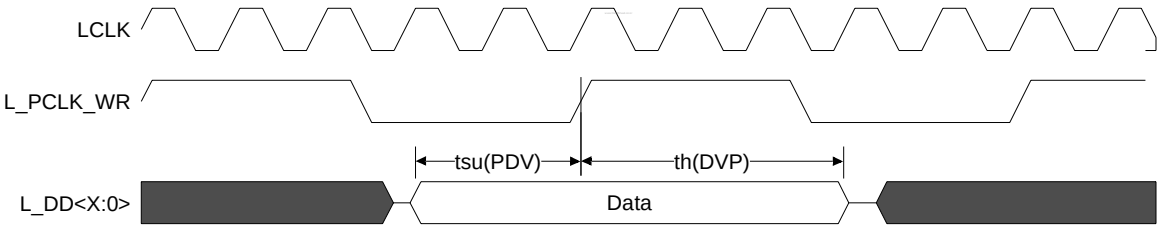


Table 33: LCD Passive Panel Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{w(P)}$	L_PCLK_WR period (Pixel Clock Pulse Width)	9.6	LCLK /(2*(LCCR3[PCD] +1))	4920	ns	1, 2, 5, 8
$t_{w(L)}$	L_LCLK_A0 pulse width duration (Horizontal Sync (Line Clock) Pulse Width)	12	td(LDDV) + LCCR1[PPL] + td(DVLA) + tw(HSP)	1312	tw(P)	1, 3
$t_{w(F)}$	L_FCLK_RD pulse width duration (Vertical Sync (Frame Clock) Pulse Width)	2	LCCR2[LPP] + 1 + tw(VSP)	864	tw(L)	1, 3

Table 33: LCD Passive Panel Timing Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{w(HSP)}$	Horizontal Sync Pulse Width	1	LCCR1[HSW] + 1	64	tw(P)	1, 4
$t_{w(VSP)}$	Vertical Sync Pulse Width	1	LCCR2[VSW] + 1	64	tw(L)	1
$t_{d(LDDV)}$	Beginning-of-Line L_PCLK_WR wait delay	1	LCCR1[BLW] + 1	256	tw(P)	1,5
$t_{d(DVLA)}$	End-of-Line L_PCLK_WR wait delay	1	LCCR1[ELW] + 1	256	tw(P)	1
$t_{su(PDV)}$	L_PCLK_WR to Data valid set up time when PCLK divisor is an even number	—	—	2^9 + 0.5ns	LCLK	5,6,7
$t_{su(PDV)}$	L_PCLK_WR to Data valid set up time when PCLK divisor is an odd number	—	—	(divisor - 1))/2)^9 + 0.5ns	LCLK	5,6,7
$t_{h(DVP)}$	End-of-Line L_PCLK_WR hold time when PCLK divisor is an even number.	2^9 + 0.5ns	—	—	LCLK	5,6,7
$t_{h(DVP)}$	End-of-Line L_PCLK_WR hold time when PCLK divisor is an odd number	(((divisor - 1)/2) + 1)^9 + 0.5ns	—	—	LCLK	5,6,7

NOTE:
1. PCLK is short for pixel clock.
2. Pixel clock is programmable based off LCLK. LCLK frequency depends on the ACCR[HSS] programmed value.
3. In this example, horizontal-sync polarity as shown is active high, inactive low. Use LCCR3[HSP] for configuring polarity.
4. In this example vertical-sync polarity is active high, inactive low. Use LCCR3[VSP] for configuring polarity.
5. In this example pixel-clock polarity is configured to sample data on the rising edge of L_PCLK_WR (LCCR3[PCP]=0).
6. In this example the LCLK is 104 MHz and the divisor is 5 (20.8 MHz).
7. The divisor is determined by the LCCR3[PCD] register. The setup and hold times are different depending on the divisor value.
8. LCLK can vary from104 MHz to 208 MHz. Refer to the *PXA3xx Processor Family Vol. III: Graphics and Input Controller Configuration Developers Manual*, for more information.
9. LCLK clock cycles
10. There are no Beginning-of-Frame LCLK wait to End-of-Frame LCLK wait delay timings for passive panels. LCCR2[BFW] and LCCR2[EFW] must be zero for passive panels.

7.4.2 LCD Active Panel Timing

For Active (and Passive) LCD panels, the line clock pin (L_LCLK_A0) is toggled when an entire line of pixels has been output to the LCD Controller screen. Likewise, the frame-clock pin (L_FCLK_RD) is toggled when an entire frame of pixels has been output to the LCD Controller screen.

The pixel clock toggles continuously in this mode as long as the LCD is enabled. The AC bias pin (L_BIAS) functions as an Output Enable. When L_BIAS is asserted, the display latches data from the LCD pins using the pixel clock. The line-clock pin (L_LCLK_A0) is used as the horizontal synchronization signal, and the frame clock (L_FCLK_RD) as the vertical synchronization signal.

The programmable timing of the line- and frame-clock pins supports both Passive and Active mode. Programming options include: wait-state insertion both at the beginning and end of each line and frame; pixel clock; line clock; frame clock; output-enable signal polarity; and frame-clock pulse width.

Figure 100 and Figure 101 illustrate the LCD timing parameters. Table 34 provides the values for the parameters.

Figure 100:LCD Active Panel Timing Diagram

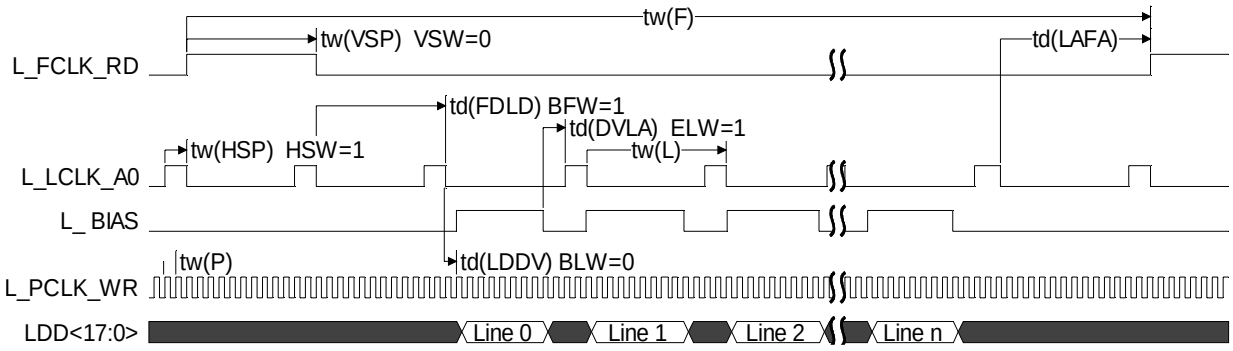


Figure 101:LCD Active Panel Timing Diagram

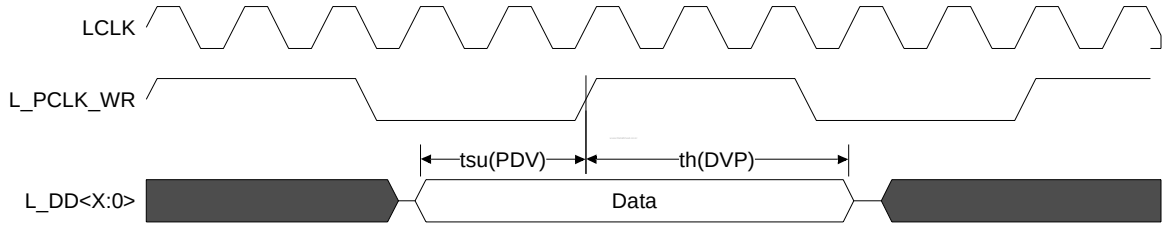


Table 34: LCD Active Panel Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{w(P)}$	L_PCLK_WR period (Pixel Clock Pulse Width)	9.6	LCLK /(2*(LCCR3[PCD]+1))	4920	ns	1, 2, 5, 6
$t_{w(L)}$	L_LCLK_A0 pulse width duration (Horizontal Sync (Line Clock) Pulse Width)	12	td(LDDV) + LCCR1[PPL] + td(DVLA) + tw(HSP)	1312	tw(P)	1, 3
$t_{w(F)}$	L_FCLK_RD pulse width duration (Vertical Sync (Frame Clock) Pulse Width)	2	LCCR2[LPP] + 1 + tw(VSP)	1174	tw(L)	1, 3
$t_{w(HSP)}$	Horizontal Sync Pulse Width	1	LCCR1[HSW] + 1	64	tw(P)	1, 4
$t_{w(VSP)}$	Vertical Sync Pulse Width	1	LCCR2[VSW] + 1	64	tw(L)	1

Table 34: LCD Active Panel Timing Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{d(LDDV)}$	Beginning-of-Line L_PCLK_WR wait delay	1	LCCR1[BLW] + 1	256	tw(P)	1,5
$t_{d(DVLA)}$	End-of-Line L_PCLK_WR wait delay	1	LCCR1[ELW] + 1	256	tw(P)	1
$t_{d(FDLD)}$	Beginning-of-Frame LCLK wait delay	0	LCCR2[BFW]	255	PCLK	1
$t_{d(LAFA)}$	End-of-Frame LCLK wait delay	0	LCCR2[EFW]	255	ns	—
$t_{su(PDV)}$	L_PCLK_WR to Data valid set up time when PCLK divisor is an even number	—	—	2^{11} + 0.5ns	LCLK	5,6,7
$t_{su(PDV)}$	L_PCLK_WR to Data valid set up time when PCLK divisor is an odd number	—	—	(divisor - 1))/2)[11] + 0.5ns	LCLK	8,9,10
$t_{h(DVP)}$	End-of-Line L_PCLK_WR hold time when PCLK divisor is an even number.	2^{11} + 0.5ns	—	—	LCLK	8,9,10
$t_{h(DVP)}$	End-of-Line L_PCLK_WR hold time when PCLK divisor is an odd number	(((divisor - 1)/2) + 1)[11] + 0.5ns	—	—	LCLK	8,9,10

NOTE:
1. PCLK is shortened form of pixel clock.
2. Pixel clock is programmable based off LCLK. LCLK frequency depends on the ACCR[HSS] programmed value.
3. In this example, horizontal-sync polarity as shown is active high, inactive low. Use LCCR3[HSP] for configuring polarity.
4. In this example vertical-sync polarity is active high, inactive low. Use LCCR3[VSP] for configuring polarity.
5. In this example pixel-clock polarity is configured to sample data on the rising edge of L_PCLK_WR (LCCR3[PCP]=0).
6. In this example the LCLK is 104 MHz and the divisor is 5 (20.8 MHz).
7. The divisor is determined by the LCCR3[PCD] register. The setup and hold times are different depending on the divisor value.
8. In this example pixel-clock polarity is configured to sample data on the rising edge of L_PCLK_WR (LCCR3[PCP]=0).
9. In this example the LCLK is 104 MHz and the divisor is 5 (20.8 MHz).
10. The divisor is determined by the LCCR3[PCD] register. The setup and hold times are different depending on the divisor value.
11. LCLK clock cycles
12. LCLK can vary from104 MHz to 208 MHz. Refer to the *PXA3xx Processor Family Vol. III: Graphics and Input Controller Configuration Developers Manual*, for more information.

7.4.3 LCD Smart Panel Timing

Figure 102 illustrates the LCD timing parameters for Smart panels. Table 35 provides the values for the parameters.

Figure 102:LCD Smart Panel Timing Diagram

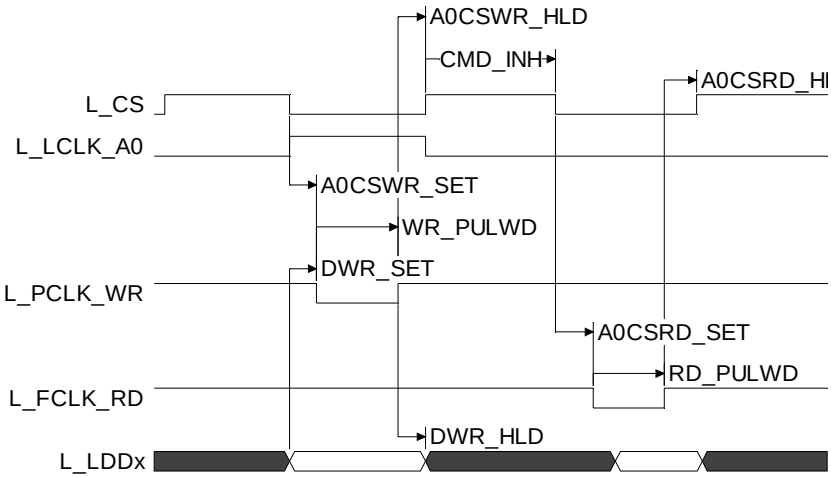


Table 35: LCD Smart Panel Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t_{A0CSWR_SET}	L_CS low to L_PCLK_WR low delay	1	LCCR1[ELW] + 1	256	LCLK	1
t_{WR_PULWD}	L_PCLK_WR pulse width duration	1	LCCR1[BLW] + 1	256	LCLK	1
t_{DWR_SET}	LDDx write data setup before PCLK_WR low	1	LCCR1[ELW] + 1	256	LCLK	1
t_{A0CSWR_HLD}	L_PCLK_WR high to L_CS high delay	1	LCCR1[ELW] + 1	256	LCLK	1
t_{DWR_HLD}	L_LDDx write data hold after L_PCLK_WR high	1	LCCR1[ELW] + 1	256	LCLK	1
t_{CMD_INH}	L_CS recover time for two consecutive read or writes (include write/read and read/write)	1	LCCR3[PCD] + 1	256	LCLK	1
t_{A0CSRD_SET}	L_CS low to L_FCLK_RD low delay	1	LCCR1[ELW] + 1	256	LCLK	1
t_{RD_PULWD}	L_FCLK_RD pulse width duration	1	LCCR1[BLW] + 1	256	LCLK	1
t_{A0CSRD_HLD}	L_FCLK_RD high to L_CS high delay	1	LCCR1[ELW] + 1	256	LCLK	1

NOTE:
1. LCLK frequency depends on the ACCR[HSS] programmed value.

7.5 SSP Timing Diagrams and Specifications

Figure 103 and Table 36 convey the SSP timing parameters with SSP in Master mode. The processor drives SSPSCLK and SSPSFRM when in Master mode. Figure 104 and Table 37 convey the SSP timing parameters with SSP in Slave mode. The processor receives SSPSCLK and SSPSFRM when in Slave mode.

The processor can also provide SSPSCLK while the external peripheral sources SSPSFRM, which is termed a “mixed mode” as in shown in Figure 105 with the timing parameters specified in Table 38. Similarly, the processor can also receive SSPSCLK while the external peripheral provides SSPSFRM, which is termed a “mixed mode” as in shown in Figure 106 with the timing parameters specified in Table 39.

SSP Master Mode Timing

Figure 103:SSP Master Mode Timing Diagram

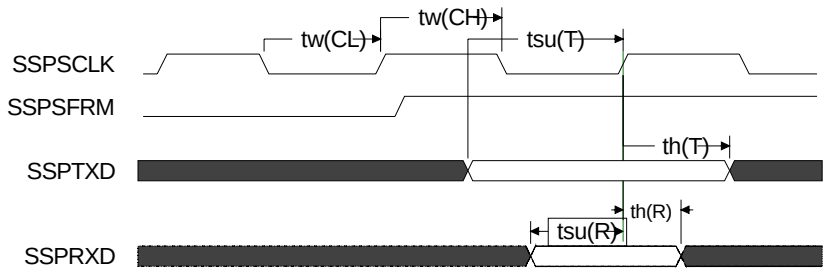


Table 36: SSP Master Mode Timing Specifications

Symbol	Description	Min	Max	Units	Notes
$t_{w(CH)}$	SSPSCLK pulse width high duration	38.46	—	ns	1
$t_{w(CH)}$	SSPSCLK pulse width high duration	19.23	—	ns	2
$t_{w(CL)}$	SSPSCLK pulse width low duration	38.46	—	ns	1
$t_{w(CL)}$	SSPSCLK pulse width low duration	19.23	—	ns	2
$t_{su(T)}$	SSPTXD to SSPSCLK setup time	35	—	ns	
$t_{h(T)}$	SSPSCLK to SSPTXD hold time	33	—	ns	
$t_{su(R)}$	SSPRXD to SSPSCLK setup time	4	—	ns	
$t_{h(R)}$	SSPSCLK to SSPRXD hold time	3.6	—	ns	

NOTE:
1. Timing for PXA32x and PXA30x only
2. Timing for PXA31x only

7.5.1 SSP Slave Mode Timing

Figure 104:SSP Slave Mode Timing Definitions

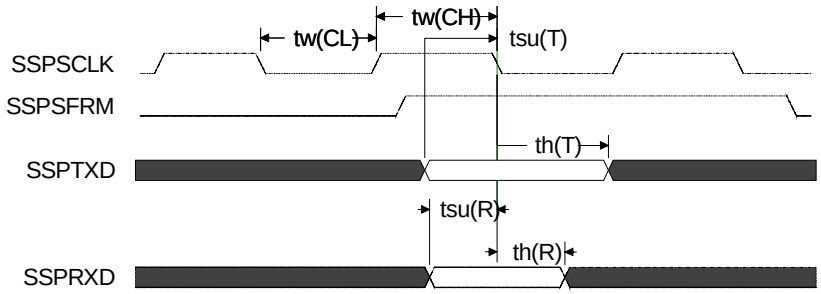


Table 37: SSP Slave Mode Timing Specifications

Symbol	Description	Min	Max	Units
$t_{w(CH)}$	SSPSCLK pulse width high duration	38.46	—	ns
$t_{w(CL)}$	SSPSCLK pulse width low duration	38.46	—	ns
$t_{su(T)}$	SSPTXD to SSPSCLK setup time	35	—	ns
$t_{h(T)}$	SSPSCLK to SSPTXD hold time	33	—	ns
$t_{su(R)}$	SSPSRXD to SSPSCLK setup time	4	—	ns
$t_{h(R)}$	SSPSRXD to SSPSSCLK hold time	3.6	—	ns

7.5.2 SSP Mixed Mode Timing - Processor Master to Clock

Figure 105:SSP Mixed Mode, Processor Master to Clock Timing Definitions

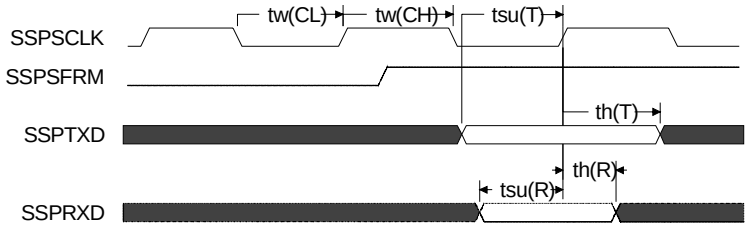


Table 38: SSP Mixed Mode, Processor Master to Clock Timing Specifications

Symbol	Description	Min	Max	Units	Notes
$t_{w(CH)}$	SSPSCLK pulse width high duration	38.46	—	ns	1
$t_{w(CH)}$	SSPSCLK pulse width high duration	19.23	—	ns	2
$t_{w(CL)}$	SSPSCLK pulse width low duration	38.46	—	ns	1
$t_{w(CL)}$	SSPSCLK pulse width low duration	19.23	—	ns	2
$t_{su(T)}$	SSPTXD to SSPSCLK setup time	35	—	ns	
$t_{h(T)}$	SSPSCLK to SSPTXD hold time	33	—	ns	
$t_{su(R)}$	SSPSRXD to SSPSCLK setup time	4	—	ns	
$t_{h(R)}$	SSPSRXD to SSPSSCLK hold time	3.6	—	ns	

NOTE:
1. Timing for PXA32x and PXA30x only
2. Timing for PXA31x only

7.5.3 SSP Mixed Mode Timing - Processor Master to Frame

Figure 106:SSP Mixed Mode, Processor Master to Frame Timing Definitions

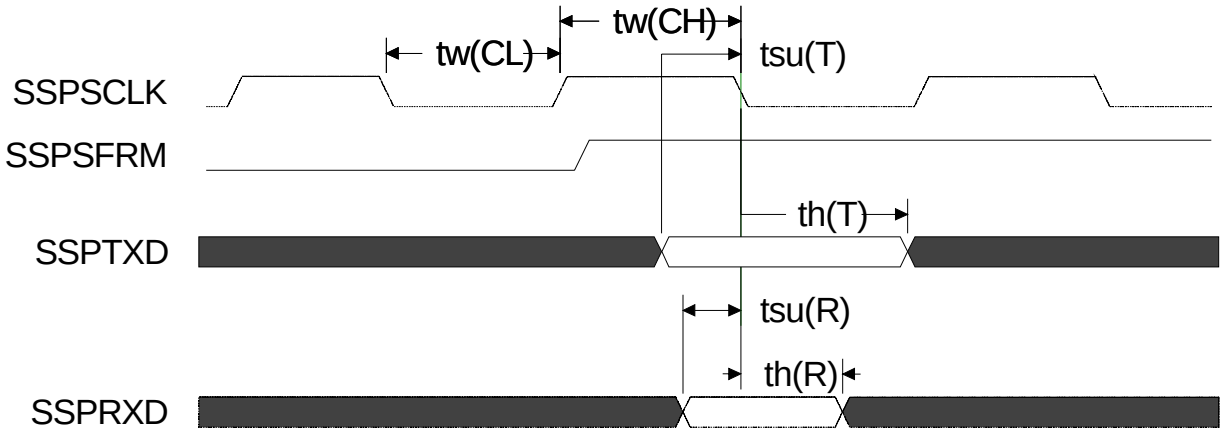


Table 39: SSP Mixed Mode, Processor Master to Frame Timing Specifications

Symbol	Description	Min	Max	Units	Notes
$t_{w(CH)}$	SSPSCLK pulse width high duration	38.46	—	ns	1
$t_{w(CH)}$	SSPSCLK pulse width high duration	19.23	—	ns	2
$t_{w(CL)}$	SSPSCLK pulse width low duration	38.46	—	ns	1
$t_{w(CL)}$	SSPSCLK pulse width low duration	19.23	—	ns	2
$t_{su(T)}$	SSPTXD to SSPSCLK setup time	35	—	ns	
$t_{h(T)}$	SSPSCLK to SSPTXD hold time	33	—	ns	
$t_{su(R)}$	SSPSRXD to SSPSCLK setup time	4	—	ns	
$t_{h(R)}$	SSPSRXD to SSPSSCLK hold time	3.6	—	ns	

NOTE:
1. 0Timing for PXA32x and PXA30x only
2. 0Timing for PXA31x only

7.6 AC '97 Timing Diagrams and Specifications

Figure 107 and Table 40 defines the AC '97 CODEC interface AC timing specifications.

Figure 107:AC '97 CODEC Timing Diagram

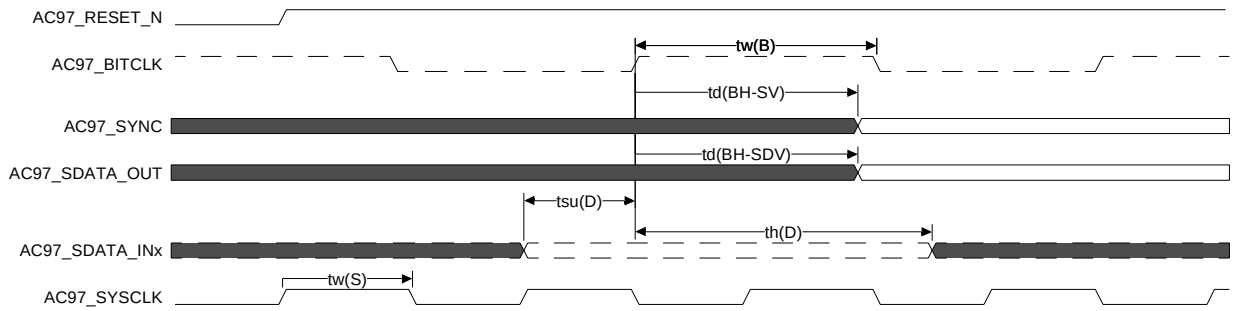


Table 40: AC '97 CODEC Timing Specifications

Symbol	Parameter	Min	Max	Units	Notes
$t_{w(B)}$	AC97_BITCLK pulse width constraint	40.69	—	ns	1
$t_{d(BH-SV)}$	AC97_BITCLK high to AC97_SYNC valid delay	8.18	22.68	ns	1
$t_{d(BH-SDV)}$	AC97_BITCLK high to AC97_SDATA_OUT valid delay	7.78	23.08	ns	1
$t_{su(D)}$	AC97_SDATA_INx to AC97_BITCLK setup time constraint	4.33	—	ns	1
$t_{h(D)}$	AC97_BITCLK to AC97_SDATA_INx hold time constraint	0.93	—	ns	1
$t_{w(S)}$	AC97_SYSCLK pulse width delay	20.34	—	ns	

NOTE:
1. Slew rate for incoming BITCLK is 0.5 V/ns

7.7 USB 2.0 Timing Diagrams and Specifications (PXA32x and PXA30x only)

Figure 108 and Table 41 defines the AC characteristics for the USB 2.0 timing specifications.

Figure 108:USB 2.0 Timing Diagram

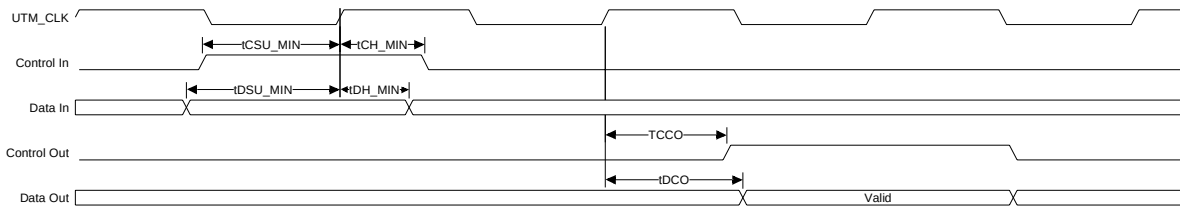


Table 41: USB 2.0 Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
t_{CSU_MIN}	Minimum setup time for TxValid	4.8	15.5	ns	—
t_{CH_MIN}	Minimum Hold time for TxValid	1	—	ns	—
t_{DSU_MIN}	Minimum setup time for Data in (Transmit)	4.8	15.5	ns	—
t_{DH_MIN}	Minimum hold time for Transmit Data	1	—	ns	—
t_{CCO}	Clock to Control Out time for TxReady, RxValid, RxActive and RxError	1	8	ns	—
t_{CDO}	Clock to Data Out time (receive)	1	8	ns	—

7.8 MultiMedia Card Timing Diagrams and Specifications

Figure 109 and Table 42 define the MultiMedia Card controller AC timing specifications.

Figure 109:MultiMedia Card Timing Diagrams

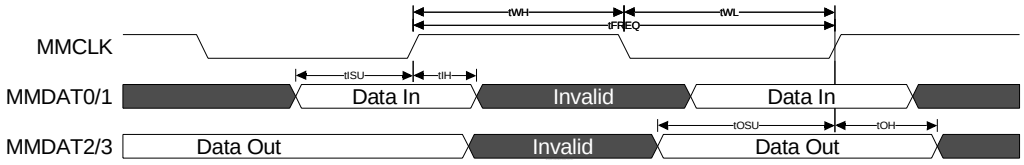


Table 42: MultiMedia Card Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
t_{FREQ}	MMCLK Frequency Data Transfer Mode	0	19.5	MHz	2
t_{FREQ}	MMCLK Frequency Data Transfer Mode	0	26	MHz	3
t_{FREQ}	MMCLK Frequency Identification Mode	0	400	kHz	
t_{WH}	Clock high time	10	—	ns	1
t_{WL}	Clock low time	10	—	ns	1
t_{rise}	Clock rise time	—	10	ns	1
t_{fall}	Clock fall time	—	10	ns	1
t_{ISU}	Data input setup time	3	—	ns	1
t_{IH}	Data input hold time	3	—	ns	1
t_{OSU}	Output data setup time	13.1	—	ns	1

Table 42: MultiMedia Card Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Notes
t_{OH}	Output data hold time	9.7	—	ns	1

NOTE:
1. Rise and fall times measured from 10% - 90% of voltage level.
2. Timing for PXA32x processor only.
3. Timing for PXA31x processor and PXA30x processor only.
4. 0 KHz is when the clock is stopped. The minimum 100 KHz frequency range is where a continous clock is required.

7.9 Secure Digital (SD/SDIO) Timing Diagrams and Specifications

Figure 110 and Table 43 define the Secure Digital (SD/SDIO) controller AC timing specifications.

Figure 110:SD/SDIO Timing Diagrams

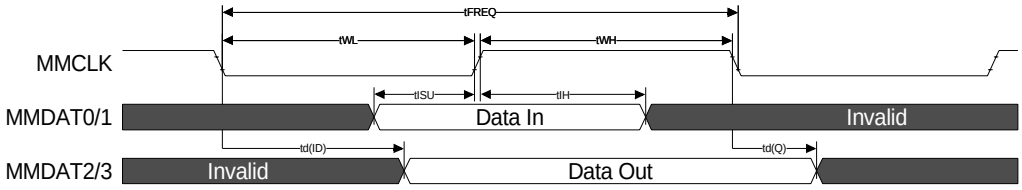


Table 43: SD/SDIO Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
t_{FREQ}	MMCLK Frequency Data Transfer Mode	0	19.5	MHz	2
t_{FREQ}	MMCLK Frequency Data Transfer Mode	0	26	MHz	3
t_{FREQ}	MMCLK Frequency Identification Mode	0[1]/100	400	kHz	
t_{WH}	Clock high time	50	—	ns	—
t_{WL}	Clock low time	50	—	ns	—
t_{rise}	Clock rise time	—	10	ns	4
t_{fall}	Clock fall time	—	10	ns	4
t_{ISU}	Data input setup time	5	—	ns	—
t_{IH}	Data input hold time	5	—	ns	—
$t_{d(Q)}$	Output Delay time during Data Transfer Mode	0	14	ns	—
$t_{d(ID)}$	Output Delay time during Identification Mode	0	50	ns	—

NOTE:
1. 0 KHz is when the clock is stopped. The minimum 100 KHz frequency range is where continuous clock is required.
2. Timing for PXA32x processor only.
3. Timing for PXA31x processor and PXA30x processor only.
4. Rise and fall times measured from 10% - 90% of voltage level.

7.10 JTAG Boundary Scan Timing Diagrams and Specifications

Figure 111 and Table 44 defines the AC specifications for the JTAG boundary-scan test signals.

Figure 111:JTAG Boundary-Scan Timing Diagram

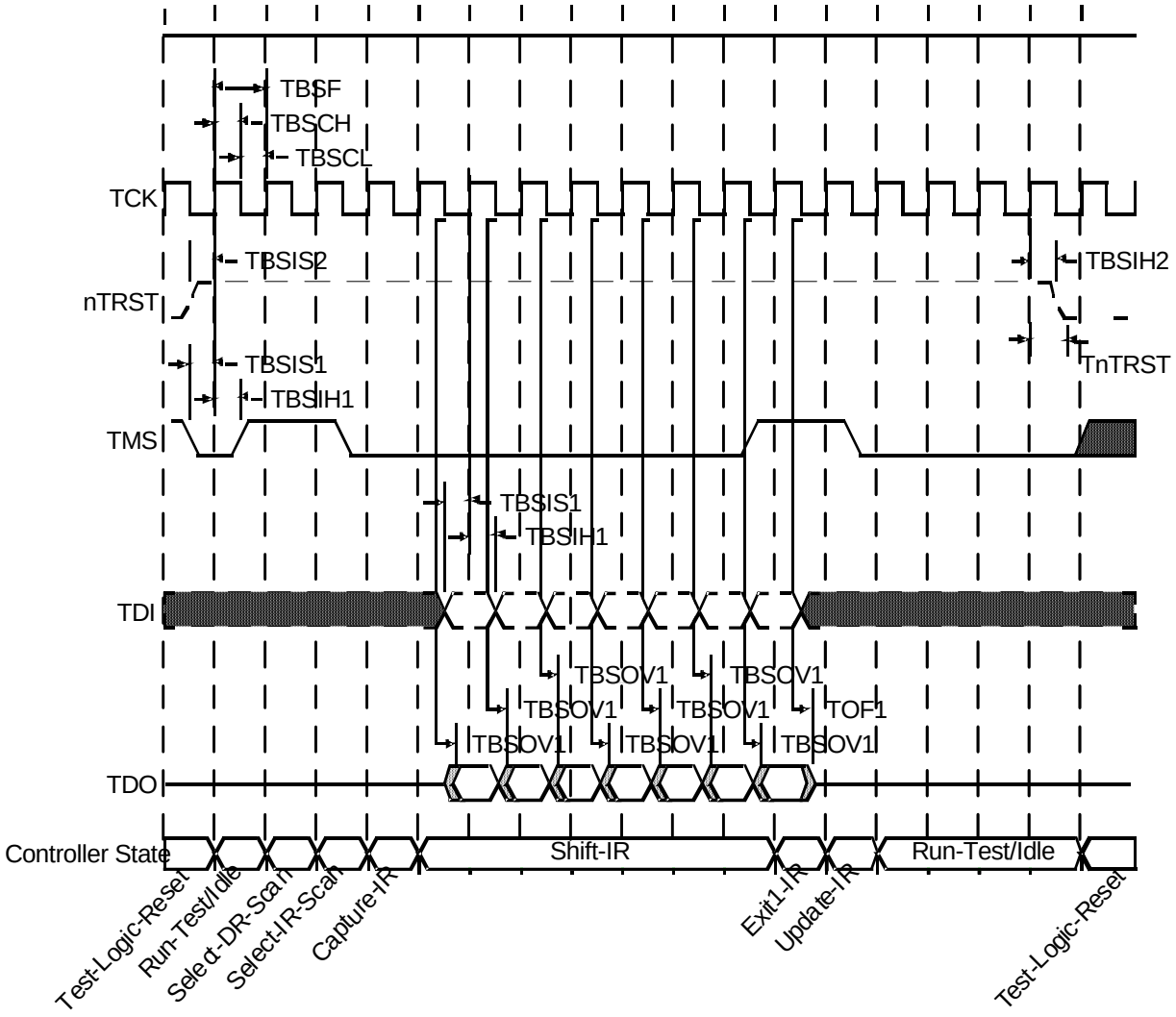


Table 44: Boundary Scan Timing Specifications

Symbol	Parameter	Min	Max	Units	Notes
TBSF	TCK Frequency	0.0	13	MHz	—
TBSCH	TCK High Time	15.0	—	ns	3
TBSCL	TCK Low Time	15.0	—	ns	3
TBSCR	TCK Rise Time	—	5.0	ns	1
TBSCF	TCK Fall Time	—	5.0	ns	2

Table 44: Boundary Scan Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Units	Notes
TBSIS1	Input Setup to TCK TDI, TMS	4.0	—	ns	—
TBSIH1	Input Hold from TCK TDI, TMS	6.0	—	ns	—
TBSIS2	Input Setup to TCK nTRST	25.0	—	ns	—
TBSIH2	Input Hold from TCK nTRST	3.0	—	ns	—
TnTRST	Assertion time of nTRST	6	—	ms	—
TBSOV1	TDO Valid Delay	1.5	6.9	ns	4
TOF1	TDO Float Delay	1.1	5.4	ns	4

NOTE:
1. Not shown in diagram. This is the transition time for TCK from 0.8 V to 2.0 V.
2. Not shown in diagram. This is the transition time for TCK from 2.0 V to 0.8 V.
3. Measured at 1.5 V
4. Relative to falling edge of TCK

8 Power and Reset Specifications

This section includes specifications for the following:

- Power up
- Power down
- Reset timing
- Power consumption

8.1 Power Up Timings

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation. Figure 112 shows this sequence and is detailed in Table 45.

Figure 112:Power Up Reset Timing

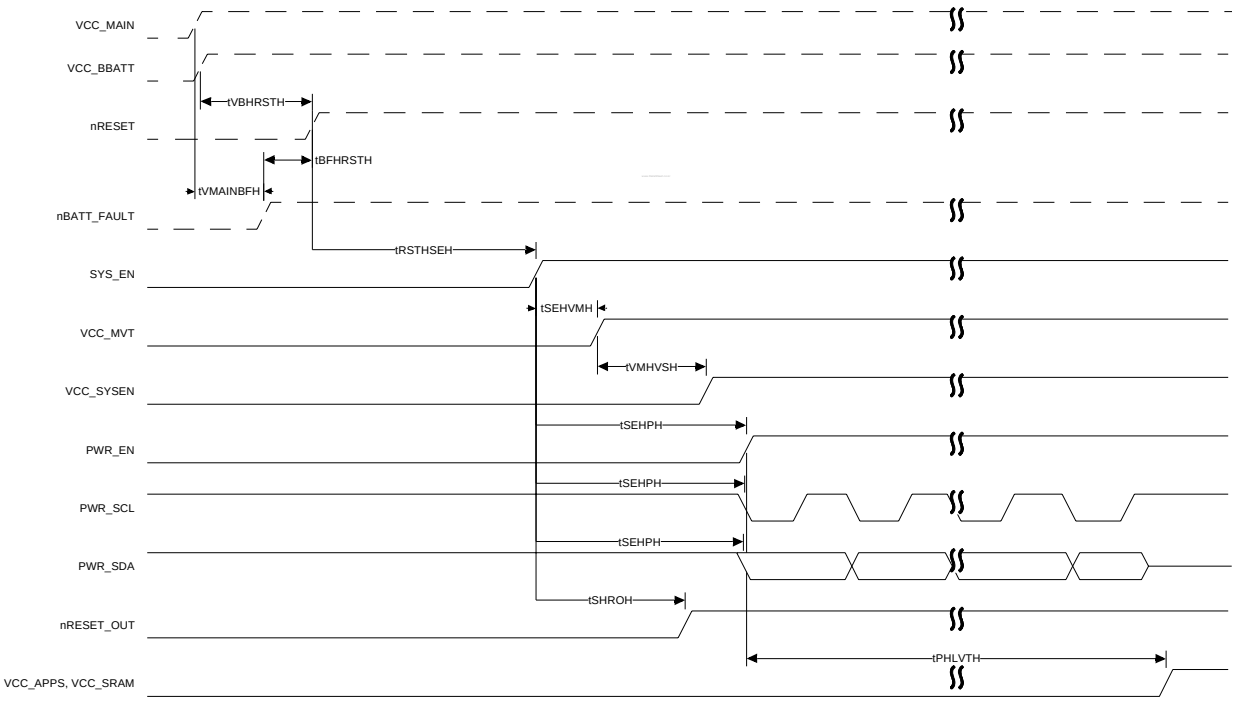


Table 45: Power Up Timing Specifications

Symbol	Description	Min	Max	Units	Notes
$t_{VBHRSTH}$	VCC_BBATT enabled to nRESET high constraint	8 + PMIC ramp rate	—	ms	1
$t_{VMAINBFH}$	VCC_MAIN enabled to nBATT_FAULT high constraint	0	—	ms	2
$t_{BFHRSTH}$	nBATT_FAULT high to nRESET high constraint	165	—	µs	3
$t_{RSTHSEH}$	nRESET high to SYS_EN high delay	—	2.005	s	—
t_{SEHVMH}	SYS_EN high to VCC_MVT stable	0	SYS_DEL time	µs	5
t_{VMHVSH}	VCC_MVT enabled to VCC_SYSEN stable	0	SYS_DEL time - t_{SEHVMH}	µs	4, 5
t_{SEHPH}	SYS_EN high to PWR_EN high delay	182	SYS_DEL time + 183	µs	5
t_{SHROH}	SYS_EN high to nRESET_OUT high delay	SYS_DEL time + 213	SYS_DEL time + 214	µs	5
t_{PHLVTH}	PWR_EN high to VCC_APPS and VCC_SRAM supplies stable	0	PWR_DEL time	µs	6

NOTE:
1. PMIC Ramp Rate is the time for PMIC voltages to ramp to the preferred voltage levels. Increasing the ramp rate decreases the overall power-up timing.
2. VCC_MAIN is the main battery supply voltage
3. nBATT_FAULT is the signal that is used to determine if the main power supply is connected. If nBATT_FAULT occurs after nRESET, the processor enters an S3/D4/C4 before going into S0/D0/C0.
4. VCC_SYSEN = All supplies except VCC_BBATT, VCC_APPS, VCC_SRAM and VCC_MVT.
5. Defined by programming PCFR[SYS_DEL]
6. Defined by programming PCFR[PWR_DEL]

8.2 Powerdown Timings

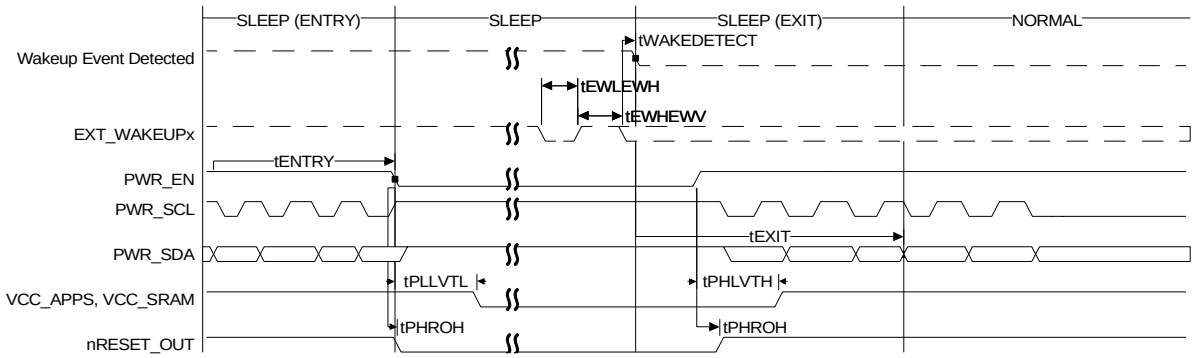
This section has the following powerdown timings:

- S2/D3/C4 - Sleep
- S3/D4/C4 - Deep Sleep

8.2.1 S2/D3/C4 Mode Timings

During S2/D3/C4 (Sleep) mode, the nRESET_OUT and PWR_EN signals change state. The sequence indicated in Figure 113 and detailed in Table 46 is the required timing parameters for S2/D3/C4 mode.

Figure 113:S2/D3/C4 Timing



NOTE:

1. nRESET _OUT assertion is an option for S2/D3/C4 entry. By clearing the PCFR[SL_ROD], nRESET_OUT is asserted upon entry into S2/D3/C4.

Table 46: S2/D3/C4 Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t_{ENTRY}	PWRMODE S2/D3/C4 state command issued to PWR_EN low delay		78		µs	4
t_{PLLVTL}	PWR_EN low to VCC_APPS and VCC_SRAM supplies disabled constraint	0	—	—	s	—
t_{PLROL} / t_{PHROH}	PWR_EN low to nRESET_OUT low and PWR_EN high to nRESET_OUT high delay	-62.5	—	62.5	µs	2
t_{EWLEWH}	EXT_WAKEUPx low pulse width constraint	5	—	—	ns	1, 3
t_{EWHEWV}	EXT_WAKEUPx high pulse width constraint	5	—	—	ns	1, 3
t_{PHLVTH}	PWR_EN high to VCC_APPS and VCC_SRAM supplies stable	—	—	PWR_DEL time	µs	2
$t_{WAKEDETECT}$	Acknowledge the external wake-up edge and to begin the wake-up sequence delay	—	—	150	µs	—
t_{EXIT}	Wake-up event to the run mode delay	—	7.9	—	ms	4

Table 46: S2/D3/C4 Timing Specifications (Continued)

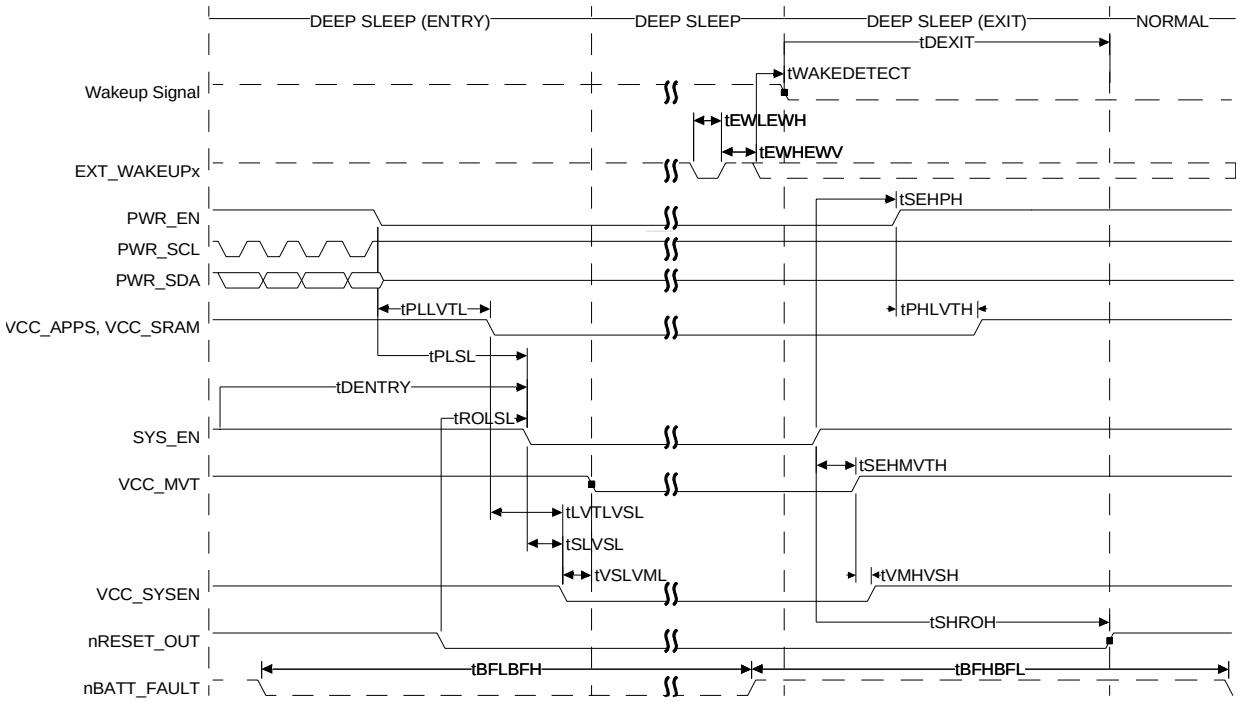
Symbol	Description	Min	Typical	Max	Units	Notes

NOTE:
1. EXT_WAKEUPx signal shown in the diagram is for falling edge detect. However, either edge or both edge detect can be enabled. PWER[WERx] and FWER[WEFx] configures which edge is used for detection.
2. S2/D3/C4 state nRESET_OUT Disable (PCFR[SL_ROD]) — Prevents the nRESET_OUT pin from asserting upon entry into S2/D3/C4 or S3/D4/C4 modes.
3. EXT_WAKEUPx signal shown in this diagram is based of PWER[EDF] bit being set.
4. Time with PCFR[PWR_DEL] = 0b0 and no Power I^2C commands.

8.2.2 S3/D4/C4 Mode Timings

During S3/D4/C4 (Deep Sleep) mode, nRESET_OUT, PWR_EN and SYS_EN change state. The sequence indicated in Figure 114 and detailed in Table 47 is the required timing parameters for S3/D4/C4 (Deep Sleep) mode.

Figure 114:S3/D4/C4 Timing



NOTE:
1. VCC_SYSEN = All supplies except VCC_BBATT, VCC_APPS, VCC_SRAM and VCC_MVT.
2. nRESET _OUT assertion is an option for S3/D4/C4 entry. By clearing the PCFR[SL_ROD], nRESET_OUT is asserted upon entry into S3/D4/C4.

Table 47: S3/D4/C4 (Deep Sleep) Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t_{DENTRY}	PWRMODE S3/D4/C4 state command issued to SYS_EN low delay	—	1.4	—	ms	3,7
t_{PLLVTL}	PWR_EN low to VCC_APPS and VCC_SRAM supplies disabled constraint	0	—	—	s	—
t_{PLSL}	PWR_EN low to SYS_EN low delay	—	—	62	µs	—
t_{ROLSL}	nRESET_OUT low to SYS_EN low delay	—	—	123	µs	4
t_{BFLBFH}	nBATT_FAULT low pulse width constraint	100	—	—	µs	
$t_{LVTLVSL}$	VCC_APPS and VCC_SRAM supplies disabled to VCC_SYSEN disabled constraint	0	—	—	s	2
t_{SLVSL}	SYS_EN low to VCC_SYSEN supplies disabled constraint	0	—	—	ns	2,3
t_{VSLVML}	VCC_SYSEN supplies disabled to VCC_MVT supply disabled constraint	0	—	100	ns	2
t_{EWLEWH}	EXT_WAKEUPx low to EXT_WAKEUPx high constraint	5	—	—	ns	1
t_{EWHEWV}	EXT_WAKEUPx high to EXT_WAKEUPx valid delay	5	—	—	ns	1
$t_{WAKEDETECT}$	Acknowledge the external wake-up edge and to begin the wake-up sequence delay	—	—	150	µs	4
t_{BFHSEH}	nBATT_FAULT high to SYS_EN high delay	—	—	150	µs	—
t_{PHLVTH}	PWR_EN high to VCC_APPS and VCC_SRAM supplies stable	0	—	PWR_DEL time	µs	—
$t_{SEHMVTH}$	SYS_EN to VCC_MVT supply stable	0	—	SYS_DEL time	µs	—
t_{SEHPH}	SYS_EN high to PWR_EN high delay	182	—	SYS_DEL time + 183	µs	—
t_{DEXIT}	Wakeup event to run mode delay	—	OSCC[VCXOST] + SYS_DEL + PWR_DEL + 1ms		ms	6,7

Table 47: S3/D4/C4 (Deep Sleep) Timing Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
t_{VMHVSH}	VCC_MVT supply enabled to VCC_SYSEN supplies stable	0	—	SYS_DEL time - t_{SEHVMH}	µs	2
t_{SHROH}	SYS_EN high to nRESET_OUT high delay	SYS_DEL time + 213	—	SYS_DEL time + 214	µs	4
t_{BFHBFL}	nBATT_FAULT high pulse width constraint	0	—	—	s	

NOTE:
1. EXT_WAKEUPx signal shown in the diagram is for falling edge detect. However, edge detection can be enabled for either edge or both edges. PWER[WERx] and FWER[WEFx] configures which edge(s) is/are used for detection.
2. VCC_SYSEN = All supplies except VCC_BBATT, VCC_APPS, VCC_SRAM and VCC_MVT.
3. To get the most power savings, Marvell recommends turning off VCC_SYSEN as close to the SYS_EN assertion as possible
4. S2/D3/C4 state nRESET_OUT Disable (PCFR[SL_ROD]) — Prevents the nRESET_OUT pin from asserting upon entry into S2/D3/C4 or S3/D4/C4 modes.
5. The time interval between the software Write to Core PWRMODE register (CP14 Register 7) to initiate a Low-power mode and the wake-detection window activation is 1µs (max).
6. The following are the assumptions for exit times -
- There are no transfers pending within the system that cause exit sequence to stall
- There are no external transfers pending that cause exit sequence to stall
- All counters that are user programmable that can cause exit sequence to stall are set to minimum values: including sys_del, pwr_del, lpm_del and vctost
- Exit times provided are typical
7. Time with PCFR[PWR_DEL] = 0b0 and no Power I^2C commands.

8.3 Reset Timing

The processor asserts the nRESET_OUT pin in one of several different reset modes:

- Hardware reset timing
- Watchdog reset timing
- GPIO reset timing (Can be configured by software)

The following sections provide the timing and specifications for the entry and exit of these modes.

8.3.1 Hardware Reset Timing

Hardware reset timing sequences assume stable power supplies at the assertion of nRESET. They follow the timings indicated in Section 8.1, Power Up Timings. Refer to Figure 112.

8.3.2 Watchdog Reset Timing

Watchdog reset is an internally generated reset and therefore has no external-pin dependencies. The nRESET_OUT pin is the only indicator of watchdog reset, and it stays asserted for t_{GRLGRH}. nBAUTT_FAULT and nRESET are assumed to be in their asserted states.

8.3.3 GPIO Reset Timing

GPIO reset is usually generated externally to a dedicated signal nGPIO_RESET. A GPIO reset can also occur by setting the PMCR[SWGR] register. Figure 115 shows the timing of GPIO reset.

Figure 115:GPIO Reset Timing

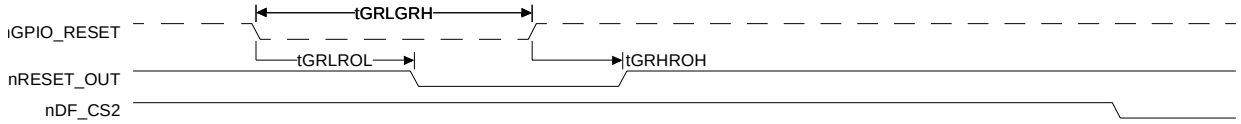


Table 48: GPIO Reset Timing Specifications

Symbol	Description	Min	Max	Units	Notes
tGRLGRH	nGPIO_RESET pulse width constraint	100	—	µs	—
tGRLROL	nGPIO_RESET low to nRESET_OUT low delay	153	—	µs	1
tGRHROH	nGPIO_RESET high to nRESET_OUT high delay	92	—	µs	1

NOTE:
1. GPIO Reset Disable (PCFR[GP_ROD])—Enables/disables assertion of nRESET_OUT during GPIO reset.

8.4 Power Consumption

Power consumption depends on the following:

- Operating voltage
- Operating frequency
- Peripherals enabled
- External switching activity
- External loading

Table 49 contains PXA32x Processor power-consumption information.

Table 50 contains PXA31x Processor power-consumption information.

Table 51 contains PXA30x Processor power-consumption information.

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Table 49: PXA32x Processor Power-Consumption Specifications[1]

Parameter Description	Low Power Typical (mW)	Low Power Maximum (mW)	Standard Typical (mW)	Standard Maximum (mW)	Test Conditions
Active Power (Turbo/Run/Switch/System Bus)					
806 MHz Active Power (806/403/403/208)	—	—	—	1950	1
208 MHz Active Power (—/208/208/104)	485[5]	—	582[4]	—	1
104 MHz Active Power (—/104/104/104)	300[5]	—	360[4]	—	1
Low Power Modes (S3/D4/C4, S2/D3/C4)					

Table 49: PXA32x Processor Power-Consumption Specifications[1] (Continued)

Parameter Description	Low Power Typical (mW)	Low Power Maximum (mW)	Standard Typical (mW)	Standard Maximum (mW)	Test Conditions
S3/D4/C4	—	—	—	0.120	2
S2/D3/C4	—	—	—	0.800	3

Test Conditions:
1. VCC_APPS = 1.4V; VCC_SRAM = 1.4V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C; 8 DMA channels with memory to memory transactions
2. VCC_BBATT = 3.0V; VCC_APPS = 0V; VCC_SRAM = 0V; VCC_PLL=0; VCC_IO=0V; VCC_MEM=0V; Ta = 0C
3. VCC_BBATT = 3.0V; VCC_APPS = 0V; VCC_SRAM = 0V; VCC_PLL=0; VCC_IO=3V; VCC_MEM=1.8V; Ta = 0°C
4. VCC_APPS = 1.1V; VCC_SRAM = 1.1V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C; 8 DMA channels with memory to memory transactions
5. VCC_APPS = 1.0V; VCC_SRAM = 1.0V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C; 8 DMA channels with memory to memory transactions

NOTE:
1. Numbers are representative of median plus 1 sigma (85% of the units will be below these numbers)
2. VCC_IO is a combination of the VCC_IO1, VCC_DF, VCC_IO3, VCC_I04, VCC_CI, VCC_IO6, VCC_LCD, VCC_MSL,VCC_USB, VCC_CARD1, VCC_CARD2 and VCC_TS voltage domains.
3. Only voltage domains listed for each test condition were used to measure power consumption.

Table 50: PXA31x Processor Power-Consumption Specifications[1]

Parameter Description	Typical (mW)	Maximum (mW)	Test Conditions
Active Power (Turbo/Run/Switch/System Bus)			
624 MHz Active Power (624/312/312/208)	—	1525	1
Low Power Modes (S3/D4/C4, S2/D3/C4, S0/D2/C2, S0/D1/C2)			
S3/D4/C4	—	0.120	2
S2/D3/C4	—	0.800	3
S0/D2/C2	—	0.975	4

Table 50: PXA31x Processor Power-Consumption Specifications[1] (Continued)

Parameter Description	Typical (mW)	Maximum (mW)	Test Conditions
S0/D1/C2	—	0.975	5

Test Conditions:
1. VCC_APPS = 1.375V; VCC_SRAM = 1.375V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C; 8 DMA channels with memory to memory transactions
2. VCC_BBATT = 3.0V; VCC_APPS = 0V; VCC_SRAM = 0V; VCC_PLL=0; VCC_IO=0V; VCC_MEM=0V;Ta = 0C
3. VCC_BBATT = 3.0V; VCC_APPS = 0V; VCC_SRAM = 0V; VCC_PLL=0; VCC_IO=3V; VCC_MEM=1.8V; Ta = 0°C
4. VCC_BBATT = 3.0V; VCC_APPS = 1.4V; VCC_SRAM =1.4V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C;
5. VCC_BBATT = 3.0V; VCC_APPS = 1.4V; VCC_SRAM =1.4V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C;

NOTE:
1. Numbers are representative of median plus 1 sigma (85% of the units will be below these numbers)
2. VCC_IO is a combination of the VCC_IO1, VCC_DF, VCC_IO3, VCC_CI, VCC_LCD, VCC_MSL,VCC_USB, VCC_CARD1 and VCC_CARD2 voltage domains.
3. Only voltage domains listed for each test condition were used to measure power consumption.

Table 51: PXA30x Processor Power-Consumption Specifications[1]

Parameter Description	Typical (mW)	Maximum (mW)	Test Conditions
Active Power (Turbo/Run/Switch/System Bus)			
624 MHz Active Power (624/312/312/208)	—	1525	1
Low Power Modes (S3/D4/C4, S2/D3/C4, S0/D2/C2, S0/D1/C2)			
S3/D4/C4	—	0.120	2
S2/D3/C4	—	0.800	3
S0/D2/C2	—	0.975	4
S0/D1/C2	—	0.975	5

Test Conditions:
1. VCC_APPS = 1.375V; VCC_SRAM = 1.375V; VCC_PLL = 1.8V; VCC_IO = .0V; VCC_MEM = 1.8V; Ta = 0C; 8 DMA channels with memory to memory transactions
2. VCC_BBATT = 3.0V; VCC_APPS = 0V; VCC_SRAM = 0V; VCC_PLL=0; VCC_IO=0V; VCC_MEM=0V;Ta = 0C
3. VCC_BBATT = 3.0V; VCC_APPS = 0V; VCC_SRAM = 0V; VCC_PLL=0; VCC_IO=3V; VCC_MEM=1.8V; Ta = 0°C
4. VCC_BBATT = 3.0V; VCC_APPS = 1.4V; VCC_SRAM =1.4V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C;
5. VCC_BBATT = 3.0V; VCC_APPS = 1.4V; VCC_SRAM =1.4V; VCC_PLL = 1.8V; VCC_IO = 3.0V; VCC_MEM = 1.8V; Ta = 0C

NOTE:
1. Numbers are representative of median plus 1 sigma (85% of the units will be below these numbers)
2. VCC_IO is a combination of the VCC_IO1, VCC_DF, VCC_IO3, VCC_CI, VCC_LCD, VCC_MSL,VCC_USB, VCC_CARD1, VCC_CARD2 and VCC_ULPI voltage domains.
3. Only voltage domains listed for each test condition were used to measure power consumption.

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A PXA30x and PXA31x Programmer Enabling

The PXA30x and PXA31x processors are high-performance, low-power microprocessors now available with additional memory chips.

A.1 Introduction

This chapter describes how to prepare the PXA30x and PXA31x processors for flash memory programming, and how to reduce programming time in a factory environment.

The PXA30x and PXA31x processors can be enabled to program flash using one of two different methods. One method focuses on programming the PXA30x and PXA31x processor prior to assembly of the system; the other focuses on waiting until after the processors have been assembled in the system before programming. Both methods may be suitable, depending on the design requirements. This chapter explains the trade-offs between different methods, thus helping reduce time in a factory environment and/or reducing cost of development.

The *direct-access programming* method requires minimum software development and takes less time to program the flash memory. Direct-access programming requires that all other memory devices along with the PXA30x and PXA31x processors be placed into high-z (by issuing a JTAG high-z instruction) while programming the NAND flash memory. All the power domains must be brought up to their required voltages to prevent damage to the part. All other memories are placed into high-z by applying power and ensuring the de-assertion of their chip-select signals.

The second method for programming flash within the PXA30x and PXA31x processors requires a greater amount of code development through the JTAG controller. It is a slower programming method but requires fewer pins. This method does not require any of the memory address, data, or control signals to be pinned out. Flash loader code is loaded into the PXA30x and PXA31x processors mini-instruction cache. The code is then executed and uses the PXA30x and PXA31x processors memory controller to program the flash and de-select the other memory devices that might be present within the package. This method is referred to as *JTAG flash programming*. All the power domains on PXA30x and PXA31x processors must be brought up to their required voltages to prevent damage to the part. All input signals not used must be driven to prevent excessive current usage. Refer to the PXA30x and PXA31x Processor Developers Manual “Debug Interface” chapter for JTAG-specific command information.

A.2 Device Configuration

The PXA30x and PXA31x processors stacked package uses a processor die combined with flash memory die and/or SDRAM memory chips all packaged together. Currently available PXA30x and PXA31x processors package configurations are as follows:

- 1 Gbits of NAND flash memory + 512 Mbits of low-power DDR (PXA30x processor)
- 2 Gbits of NAND flash memory + 1 Gbits of low-power DDR (PXA31x processor)

Note Device configurations are subject to change before final production qualification.

A.3 Procedure to Prepare PXA3xx (88AP3xx) Processor Family for Programming Flash

The following steps describe the procedure to prepare the PXA30x processor or PXA31x processor using either the direct-access programming method or the JTAG-flash programming method. To prepare for direct-access programming, the internal memories other than flash are de-selected by de-asserting the dedicated chip-select signals and the PXA30x processor or PXA31x processor must be placed into high-Z using high-Z JTAG command.

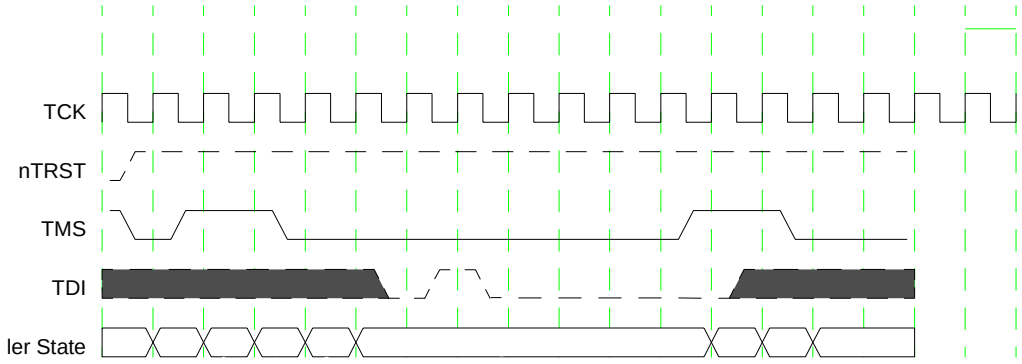
To prepare for JTAG flash programming, bring the PXA30x processor or PXA31x processor out of reset. It is responsible for controlling all the memory signals and receiving the data to program the flash devices through the JTAG controller.

A.3.1 Sequence Required for Direct-Access Programming

Follow these steps to prepare the PXA30x processor or PXA31x processor for direct-access programming. Use the power-on timing specifications with respect to applying power to the required domains.

1. If required, drive all memory chip selects (other than NAND flash) to their inactive state to guarantee the other memories are not contending with the NAND flash signals.
2. Drive EXT_WAKEUP0 pin low, NBATT_FAULT pin high, and NGPIO_RESET pin high.
3. Apply a hardware reset to the package by asserting nRESET and nTRST together.
4. Release reset by de-asserting nRESET and nTRST together.
5. Wait for nRESET_OUT to de-assert.
6. Issue the High-Z JTAG command (0x002) to place the PXA30x processor or PXA31x processor signals into high-z state.
7. Begin programming the flash devices in the package.

Figure 116:Diagram Showing Steps for Putting PXA30x Processor and PXA31x Processor into High-Z



A.3.2 Sequence Required for JTAG Flash Programming

Follow the steps below to prepare the PXA30x processor or PXA31x processor for JTAG flash programming. Use the power-on timing specifications with respect to applying power to the required domains.

1. Drive EXT_WAKEUP0 pin low, NBATT_FAULT pin high, and NGPIO_RESET pin high.
2. Apply a hardware reset to the package by asserting nRESET and nTRST together.
3. Release JTAG reset by de-asserting nTRST.
4. Follow steps documented in Download Code in the instruction cache seen in the PXA30x and PXA31x Processor Developers Manual.
5. Download the flash loader utility into the mini-instruction cache, start execution of the flash loader utility.
6. 10 µs must elapse after nTRST is de-asserted before proceeding with any JTAG operation.
7. De-assert nRESET.
8. Wait for nRESET_OUT to de-assert.
9. Begin sending raw data through the JTAG port to program the flash devices in the package.

A.4 PXA30x Processor or PXA31x Processor: Connections for Flash Programming

Table 53 describes the connections for existing PXA30x processor or PXA31x processor configurations. Table 53 shows the minimum number of balls that must be connected to program the NAND flash memory internal to the package for each of the two programming methods as described in Section A.3.

For direct-access flash programming, the balls needed are determined based on the power signals and control signals required for placing the PXA30x and PXA31x processors into a high-z state. For the JTAG-flash programming method, the signals needed are only those that power up the PXA30x and PXA31x processors such that the JTAG controller can program flash through the PXA30x and PXA31x processors memory controllers.

Table 53 shows the connections required for programming the NAND flash memory within the PXA30x and PXA31x processors. The first two columns in Table 53 show which signals must be accessed depending on the method used to program the NAND flash memory. Use the list in the next table to decode the letter representing the die within the PXA30x and PXA31x processors.

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Table 52: Abbreviations Used in Table 53

f	ball required to program flash
b	ball required by the PXA30x and PXA31x processors
s	ball required to deselect SDRAM
v	voltage supply connection required
nc	no connect
rfu	reserved for future use
dnu	do not use. do not physically connect to anything
o	optional (may not be required depending on system design)
shade	Shading indicates ball is used differently between PXA30x processor and PXA31x processor.

Table 53: Required Balls for Programming the Package Flash Memory

Required Balls (JTAG Flash Programming)	Required Balls (Direct Access Programming)	Ball #	PXA30x processor Function	PXA31x processor Function	NAND Function	Signal Instruction
Power Control Signals (VCC_BBATT)						
b	b	D3	PWR_EN	PWR_EN	—	use power-on timing specifications.
b	b	D4	SYS_EN	SYS_EN	—	
b	b	D6	nRESET_IN	nRESET_IN	—	
b	b	F9	nRESET_OUT	nRESET_OUT	—	
b	b	B7	EXT_WAKEUP0	EXT_WAKEUP0	—	Pull-down to ground. This signals internal pull-down is enabled during power-on, hardware, global watchdog and GPIO resets and is disabled when the PCFR[PUDH] bit is set.
b	b	C6	nBATT_FAULT	nBATT_FAULT	—	Pull-up to VCC_BBATT.
b	b	E8	nGPIO_RESET	nGPIO_RESET	—	Pull-up to VCC_BBATT. This signals internal pull-up is enabled during power-on, hardware, global watchdog and GPIO resets and is disabled when the PCFR[PUDH] bit is set.
b	b	A7	PWR_CAP0	PWR_CAP0	—	External 0.1 µF capacitor connected between PWR_CAP0 and PWR_CAP1. If a polarized capacitor is used, the + plate must be connected to PWR_CAP1.
b	b	F8	PWR_CAP1	PWR_CAP1	—	
b	b	C7	PWR_OUT	PWR_OUT	—	External 0.1 µF capacitor connected to ground.

Table 53: Required Balls for Programming the Package Flash Memory (Continued)

Required Balls (JTAG Flash Programming)	Required Balls (Direct Access Programming)	Ball #	PXA30x processor Function	PXA31x processor Function	NAND Function	Signal Instruction
JTAG Interface (VCC_BBATT)						
b	b	A6	nTRST	nTRST	—	JTAG interface.
b	b	C4	TCK	TCK	—	
b	b	E3	TDI	TDI	—	
b	b	D2	TDO	TDO	—	
b	b	C3	TMS	TMS	—	
Processor Clock Signals						
b	b	A8	TXTAL_IN	TXTAL_IN	—	Can be connected to an external 32.768 kHz crystal or to an external clock source. Note: The maximum voltage level on TXTAL_IN is 1.0 V.
b	b	B8	TXTAL_OUT	TXTAL_OUT	—	Can be connected to an external 32.768 kHz crystal or grounded when an external clock source is connected to TXTAL_IN.
Processor Clock Signals						
b	b	B9	PXTAL_IN	PXTAL_IN	—	Must be connected to a 13 MHz crystal or external clock source.
b	b	C9	PXTAL_OUT	PXTAL_OUT	—	Must be connected to a 13 MHz crystal or left floating when using an external clock source.
TEST Signals						
b	b	B11	TEST	TEST	—	Reserved for manufacturing test. Must be grounded for normal operation.
b	b	F11	TESTCLK	TESTCLK	—	Reserved for manufacturing test. Must be grounded for normal operation.

Table 53: Required Balls for Programming the Package Flash Memory (Continued)

Required Balls (JTAG Flash Programming)	Required Balls (Direct Access Programming)	Ball #	PXA30x processor Function	PXA31x processor Function	NAND Function	Signal Instruction
Data Flash Interface (VCC_DF)						
	f	W3	DF_INT_RNB	DF_INT_RNB	R/$\overline{B}$	NAND Read/$\overline{Busy}$. Must have an external 10 Kohm pull-up to VCC_DF.
	f	AA5	DF_IO0	DF_IO0	I/O<0:15>	NAND I/O interface.
	f	AA6	DF_IO1	DF_IO1		
	f	W7	DF_IO2	DF_IO2		
	f	Y8	DF_IO3	DF_IO3		
	f	V10	DF_IO4	DF_IO4		
	f	W13	DF_IO5	DF_IO5		
	f	W12	DF_IO6	DF_IO6		
	f	V11	DF_IO7	DF_IO7		
	f	U8	DF_IO8	DF_IO8		
	f	Y5	DF_IO9	DF_IO9		
	f	Y6	DF_IO10	DF_IO10		
	f	W8	DF_IO11	DF_IO11		
	f	U15	DF_IO12	DF_IO12		
	f	W10	DF_IO13	DF_IO13		
	f	W11	DF_IO14	DF_IO14		
	f	W15	DF_IO15	DF_IO15		
	f	V7	DF_ALE_NWE	DF_ALE_NWE	ALE	ALE - Address Latch Enable

Table 53: Required Balls for Programming the Package Flash Memory (Continued)

Required Balls (JTAG Flash Programming)	Required Balls (Direct Access Programming)	Ball #	PXA30x processor Function	PXA31x processor Function	NAND Function	Signal Instruction
	f	V9	DF_NCS0	DF_NCS0	CE	$\overline{CE}$ - Chip Enable. Note: Refer to individual package specifications to determine which chip enables to use for programming NAND.
	f	U10	DF_NCS1	DF_NCS1		
	f	W5	DF_NRE	DF_NRE	RE	RE - Read Enable
	f	W4	DF_NWE	DF_NWE	WE	WE - Write Enable
	f	V8	DF_CLE_NOE	DF_CLE_NOE	CLE	CLE - Command Latch Enable
	f	U5	DF_NWP	DF_NWP	WP	$\overline{WP}$ - Write Protect. When logic Low, provides a hardware protection against undesired modify (program / erase) operations. Must be connected to VCC_DF when programming NAND.
No Connect Signals						
	rfu	C1, N2, V2, W2, U3, B4, G4, L4, P4, C5, P5, L8, M8, D19, AA19	RFU	RFU	—	Reserved for Future Use. Treat as a No Connect.
	dnu	W9	DNU	DNU		Do Not Use. Do not physically connect to anything.
Power Supplies						

Table 53: Required Balls for Programming the Package Flash Memory (Continued)

Required Balls (JTAG Flash Programming)	Required Balls (Direct Access Programming)	Ball #	PXA30x processor Function	PXA31x processor Function	NAND Function	Signal Instruction
v	v	L5, N5, AA7, AA9, A10, H10, P10, H11, P11, H12, P12, AA12, A13, Y13, K14, L14, M14, A15, N21	VCC_APPS	VCC_APPS	—	Apply 1.41 V
v	v	AA8, C18, B19	VCC_SRAM	VCC_SRAM	—	
v	v	C8	VCC_BBATT	VCC_BBATT	—	Apply 3.3 V
v	v	D12, AA16	VCC_PLL	VCC_PLL	—	Apply 1.8 V
v	v	E4, J5, T5, G9, U9, G14, R14, H15, J15, N15	VCC_MVT	VCC_MVT	—	
v	v	D9	VCC_OSC13M	VCC_OSC13M	—	
v	v	D10	VCC_BG	VCC_BG	—	
v	v	Y11	VCC_CARD1	VCC_CARD1	—	Apply 3.3 V
v	v	AA14	VCC_CARD2	VCC_CARD2	—	
v	v	E15, G10, G15	VCC_IO1	VCC_IO1	—	
v	v	T16	VCC_IO3	VCC_IO3	—	
v	v	K16, L16, M16	VCC_LCD	VCC_LCD	—	
v	v	G17	VCC_MSL	VCC_MSL	—	

Table 53: Required Balls for Programming the Package Flash Memory (Continued)

Required Balls (JTAG Flash Programming)	Required Balls (Direct Access Programming)	Ball #	PXA30x processor Function	PXA31x processor Function	NAND Function	Signal Instruction
v	v	B3	VCC_USB	VCC_BIAS	—	Apply 3.3 V for both processors
v	v	P15, P20	VCC_CI	VCC_CI	—	Apply 3.3 V
v	v	R16	RFU	VCC_ULPI	—	Apply 1.8 V for PXA31x processor
v	v	D5, G5, V5, G6, H6, J6, K6, L6, M6, N6, P6, R6, T6, U6	VCC_MEM	VCC_MEM	—	Apply 1.8 V.
v	v	G11, T9, T10, T11, T12, T13	VCC_DF	VCC_DF	VCC (for NAND)	Apply 1.8 V.
v	v	C2, F4, K5, M5, R5, Y7, H8, R8, T8, A9, H9, P9, B13, H13, P13, AA13, H14, J14, N14, P14, T14, B16, A20, B20, N20, A21, B21	VSS	VSS	—	Connect to ground.
v	v	D8	VSS_BBATT	VSS_BBATT	—	Connect to ground.
v	v	C10	VSS_BG	VSS_BG	—	Connect to ground.
v	v	Y12	VSS_CARD1	VSS_CARD1	—	Connect to ground.
v	v	AA15	VSS_CARD2	VSS_CARD2	—	Connect to ground.
v	v	P19	VSS_CI	VSS_CI	—	Connect to ground.

Table 53: Required Balls for Programming the Package Flash Memory (Continued)

Required Balls (JTAG Flash Programming)	Required Balls (Direct Access Programming)	Ball #	PXA30x processor Function	PXA31x processor Function	NAND Function	Signal Instruction
v	v	Y1, AA1, Y2, AA2, R9, R10, R11, G12, R12, R13	VSS_DF	VSS_DF	VSS (for NAND)	Connect to ground.
v	v	G13, F15	VSS_IO1	VSS_IO1	—	Connect to ground.
v	v	T15, Y20, AA20, Y21, AA21	VSS_IO3	VSS_IO3	—	Connect to ground.
v	v	K15, L15, M15	VSS_LCD	VSS_LCD	—	Connect to ground.
v	v	F6, F7, G7, H7, J7, K7, L7, M7, N7, P7, R7, T7, U7	VSS_MEM	VSS_MEM	—	Connect to ground.
v	v	F17	VSS_MSL	VSS_MSL	—	Connect to ground.
v	v	E9	VSS_OSC13M	VSS_OSC13M	—	Connect to ground.
v	v	D7	VSS_OSC32K	VSS_OSC32K	—	Connect to ground.
v	v	E11, E12, W16	VSS_PLL	VSS_PLL	—	Connect to ground.
v	v	A1, B1, A2, B2	VSS_USB	VSS	—	Connect to ground.
v	v	R15	RFU	VSS_ULPI	—	Connect to ground for PXA31x processor.

A.5 PXA30x Processor and PXA31x Processor Processor Mechanical Drawings

Refer to Section 3 for the PXA30x and PXA31x processors mechanical drawings.

A.6 PXA30x Processor and PXA31x Processor Processor Ballouts

Refer to Section 4 for the PXA30x and PXA31x processors ballouts.

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