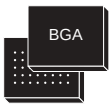
M69AW024BE

16 Mbit (1M x16) 3V Asynchronous PSRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.3V
- ACCESS TIME: 60ns
- LOW STANDBY CURRENT: 70µA
- DEEP POWER DOWN CURRENT: 10µA
- COMPATIBLE WITH STANDARD LPSRAM
- TFBGA48 PACKAGE RoHS COMPLIANT (directive 2002/95/EC of the European Parliament)

Figure 1. Package



TFBGA48 (ZB)
6x8 mm

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SUMMARY DESCRIPTION

The M69AW024BE is a 16 Mbit (16,777,216 bit) CMOS memory, organized as 1,024,576 words by 16 bits, and is supplied by a single 2.7V to 3.3V supply voltage range.

M69AW024BE is a member of STMicroelectronics PSRAM memory family, based on the one-transistor per-cell architecture. These devices are manufactured using dynamic random access memory cells, to minimize the cell size, and maximize the amount of memory that can be implemented in a given area.

However, through the use of internal control logic, the device is fully static in its operation, requiring no external clocks or timing strobes, and has a standard Asynchronous SRAM Interface.

The internal control logic of the M69AW024BE handles the periodic refresh cycle, automatically, and without user involvement.

Write cycles can be performed on a single byte by using Upper Byte Enable (UB) and Lower Byte Enable (LB).

The device can be put into standby mode using Chip Enable (E1) or in deep power down mode by using Chip Enable (E2).

Power-Down mode achieves a very low current consumption by halting all the internal activities. Since the refresh circuitry is halted, the duration of the power-down should be less than the maximum period for refresh, if the user has not finished with the data contents of the memory.

Figure 2. Logic Diagram

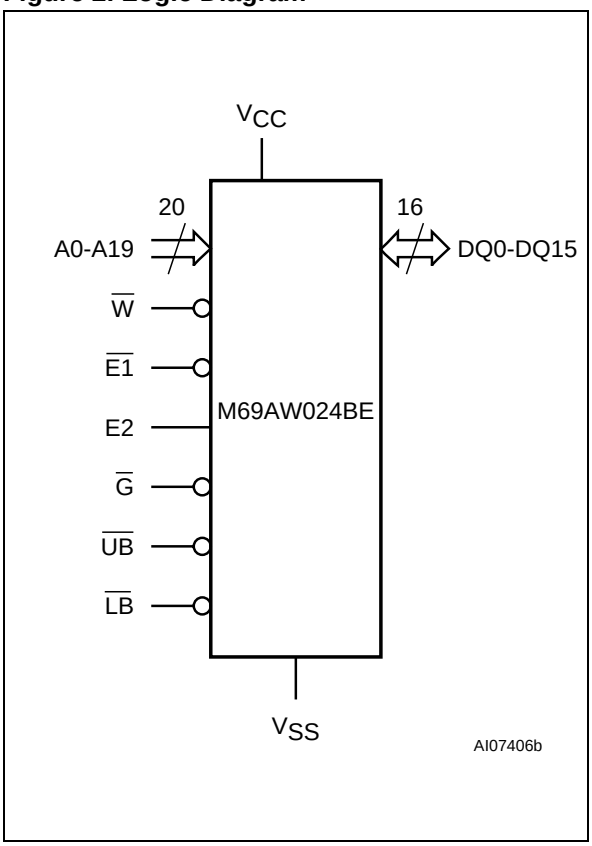
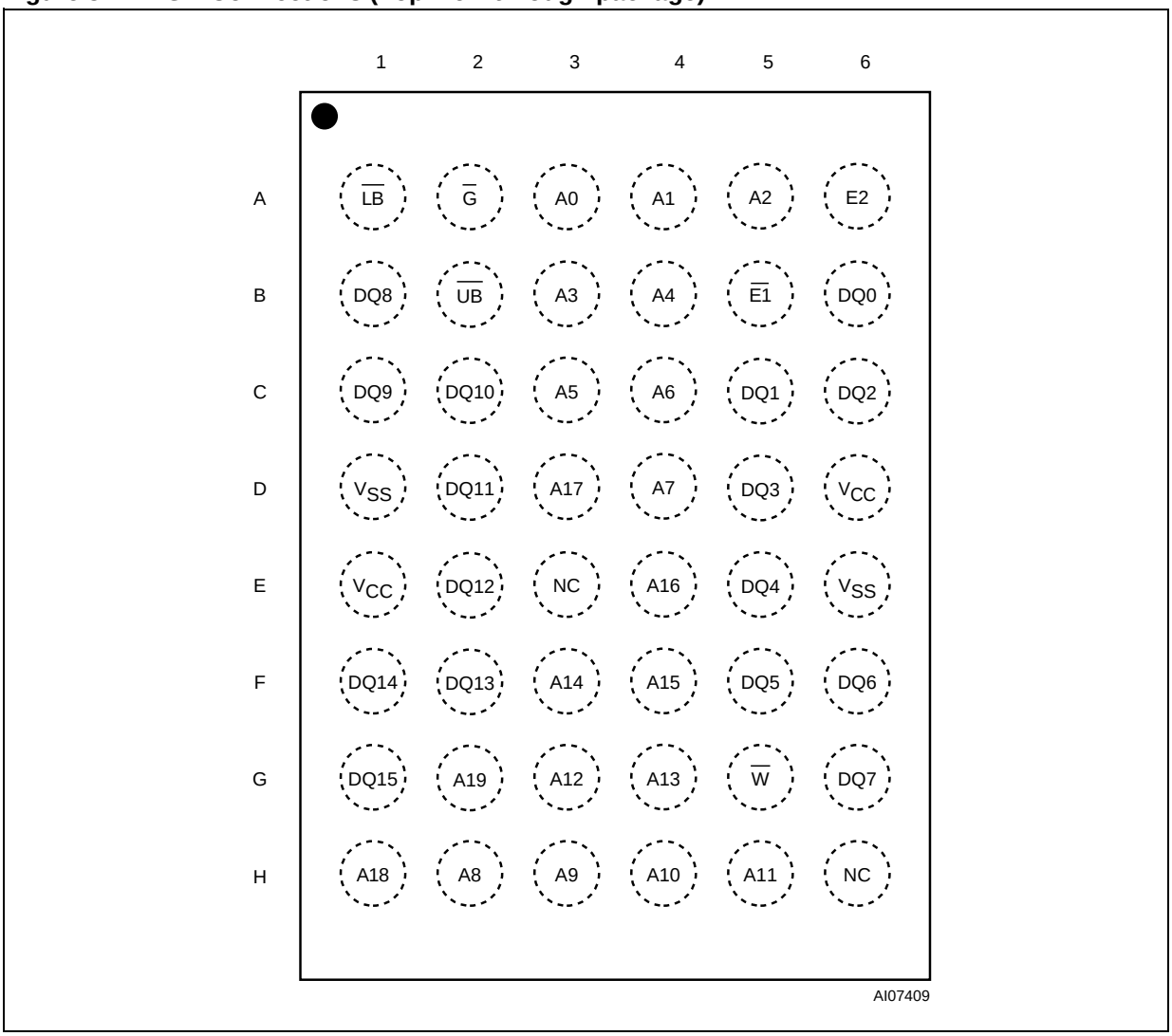


Table 1. Signal Names

A0-A19	Address Input
DQ0-DQ15	Data Input/Output
$\overline{E1}$, E2	Chip Enable, Power Down
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected (no internal connection)

Figure 3. TFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A19). The Address Inputs select the cells in the memory array to access during Read and Write operations.

Data Inputs/Outputs (DQ8-DQ15). The Upper Byte Data Inputs/Outputs carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable (UB) is driven Low.

Data Inputs/Outputs (DQ0-DQ7). The Lower Byte Data Inputs/Outputs carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable (LB) is driven Low.

Chip Enable ($\overline{E1}$). When asserted (Low), the Chip Enable, $\overline{E1}$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

Chip Enable (E2). The Chip Enable, E2, puts the device in Deep Power-down mode when it is driven Low. This is the lowest power mode.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

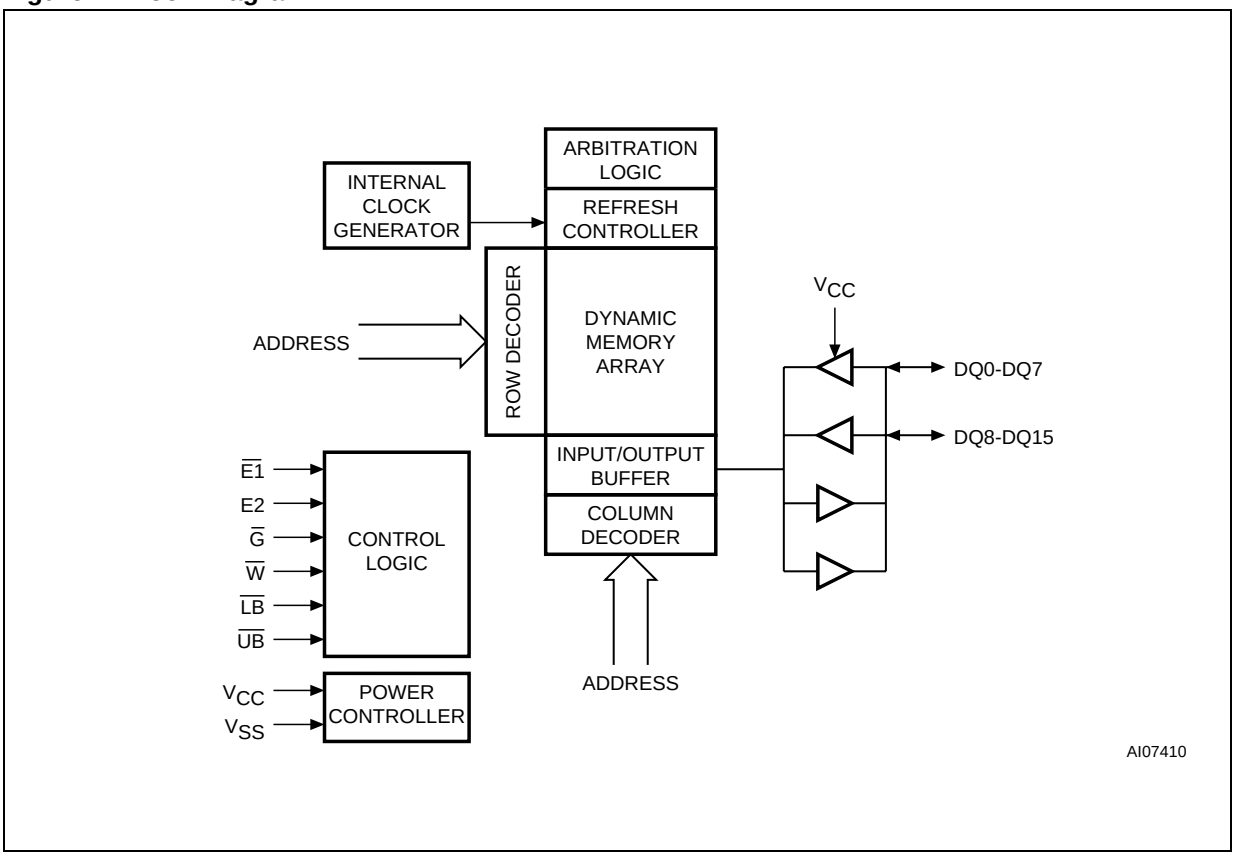
Upper Byte Enable ($\overline{UB}$). The Upper Byte Enable, $\overline{UB}$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

Lower Byte Enable ($\overline{LB}$). The Lower Byte Enable, $\overline{LB}$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read or Write) and for driving the refresh logic, even when the device is not being accessed.

V_{SS} Ground. The V_{SS} Ground is the reference for all voltage measurements.

Figure 4. Block Diagram



OPERATION

Operational modes are determined by device control inputs W, E1, E2, LB and UB as summarized in the Operating Modes table (see Table 2.).

Power On Sequence

Because the internal control logic of the M69AW024BE needs to be initialized, the following power-on procedure must be followed before the memory is used:

- Apply power and wait for V_{CC} to stabilize
- Wait t_{CHEL} while driving both Chip Enable signals (E1 and E2) High
- Activate the memory by driving Chip Enable ($\overline{E1}$) Low.

Read Mode

The device is in Read mode when:

- Write Enable ($\overline{W}$) is High and
- Output Enable ($\overline{G}$) Low and
- the two Chip Enable signals are asserted (E1 is Low, and E2 is High).

The time taken to enter Read mode (t_{ELQV}, t_{GLQV} or t_{BLQV}) depends on which of the above signals was the last to reach the appropriate level.

Data out (DQ15-DQ0) may be indeterminate during t_{ELQX}, t_{GLQX} and t_{BLQX}, but data will always be valid during t_{AVQV}.

Write Mode

The device is in Write mode when

- Write Enable ($\overline{W}$) is Low and
- Chip Enable ($\overline{E1}$) is Low and
- the two Chip Enable signals are asserted (E1 is Low, and E2 is High)
- one of Upper Byte Enable ($\overline{UB}$) or Lower Byte Enable (LB) is Low, while the other is High.

The Write cycle begins just after the event (the falling edge) that causes the last of these conditions to become true (t_{AVWL}, t_{AVEL} or t_{AVBL}).

The Write cycle is terminated by the earlier of a rising edge on Write Enable (W) or Chip Enable ($\overline{E1}$).

If the device is in Write mode (Chip Enable ($\overline{E1}$) is Low, Output Enable (G) is Low, Upper Byte Enable ($\overline{UB}$) or Lower Byte Enable ($\overline{LB}$) is Low), then Write Enable ($\overline{W}$) will return the outputs to high impedance within t_{WHDZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable (W), or for t_{DVEH} before the rising edge of Chip Enable ($\overline{E1}$), whichever occurs first, and remain valid for t_{BHDZ}, t_{WHDZ}, t_{EHDZ}.

Standby Mode

The device is in Standby mode when:

- Chip Enable ($\overline{E1}$) is High and
- Chip Enable (E2) is High.

The input/output buffers and the decoding/control logic are switched off, but the dynamic array continues to be refreshed. In this mode, the memory current consumption, I_{SB}, is reduced, and the data remains valid.

Deep Power-down Mode

The device is in Deep Power-down mode when:

- Chip Enable (E2 is Low).

Table 2. Operating Modes

Operation	E2	$\overline{E1}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	A0-A19	DQ0-DQ7	DQ8-DQ15	I_{CC}	Data Retention
Standby (Deselect)	V_{IH}	V_{IH}	X (1)	X (1)	X (1)	X (1)	X (1)	Hi-Z	Hi-Z	I_{SB}	Yes
Output Disabled (2)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X (1)	X (1)	Note (4)	Hi-Z	Hi-Z	I_{CC}	Yes
Output Disabled (No Read)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Valid	Hi-Z	Hi-Z	I_{CC}	Yes
Upper Byte Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Valid	Hi-Z	Output Valid	I_{CC}	Yes
Lower Byte Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Valid	Output Valid	Hi-Z	I_{CC}	Yes
Word Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Valid	Output Valid		I_{CC}	Yes
Upper Byte Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Valid	Invalid	Input Valid	I_{CC}	Yes
Lower Byte Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Valid	Input Valid	Invalid	I_{CC}	Yes
Word Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Valid	Input Valid	Input Valid	I_{CC}	Yes
Power-down (3)	V_{IL}	X (1)	X (1)	X (1)	X (1)	X (1)	X (1)	Hi-Z	Hi-Z	I_{PD}	No

Note: 1. X = V_{IH} or V_{IL}.
2. Output Disable mode should not be kept longer than 1µs.
3. Power-down mode can be entered from Stand-by state, and all DQ pins are in Hi-Z state.
4. Can be either VIL or VIH but must be valid before Read or Write.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
I_O	Output Current	–50	50	mA
T_A	Ambient Operating Temperature	–30	85	°C
T_{LEAD}	Lead Temperature During Soldering		(1)	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{CC}	Core Supply Voltage	–0.5	3.6	V
V_{IO}	Input or Output Voltage	–0.5	3.6	V

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	M69AW024BE		Unit
	–60		
	Min	Max	
V_{CC} Supply Voltage[1]	2.7	3.3	V
Ambient Operating Temperature	–30	85	°C
Load Capacitance (C_L)	50		pF
Output Circuit Protection Resistance (R_1)	50		Ω
Input Rise and Fall Times		4	ns
Input Pulse Voltages	0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		V
Output Transition Timing Ref. Voltages	$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$		V
Input Transition Time (tτ) between V_{IL} and V_{IH}[(2)]	5		ns

Note: 1. All voltages are referenced to V_{SS}.
2. The Input Transition Time used in AC measurements is 5ns. For other input transition times, see Table 9.

Figure 5. AC Measurement Load Circuit

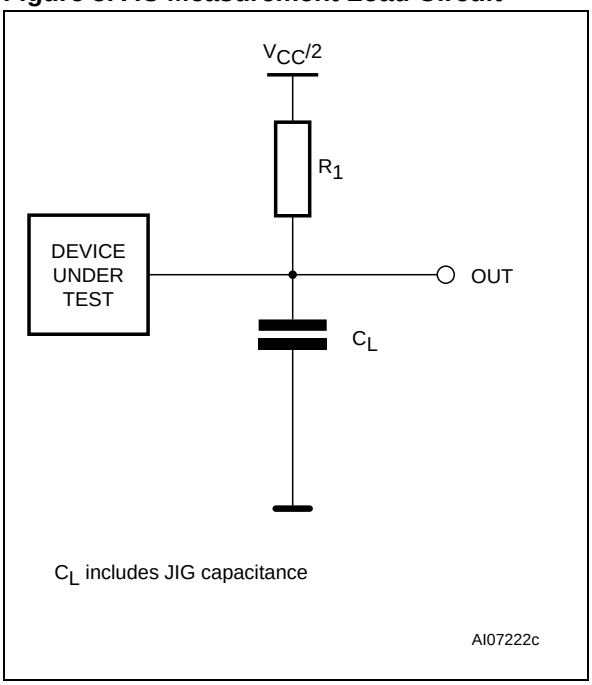
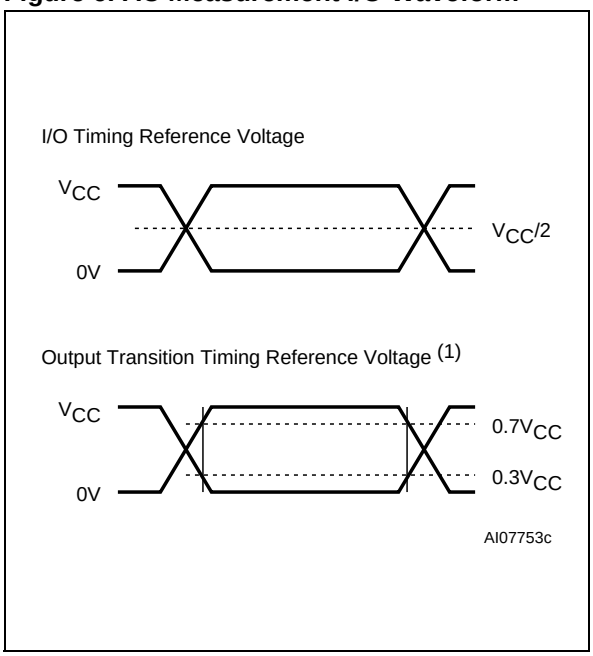


Figure 6. AC Measurement I/O Waveform



Note: 1. This waveform is given for Hi-Z and data transition AC parameters only (see Note 8. below Table 7., Read and Standby Modes AC Characteristics).

Table 5. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} (1)	Output Capacitance	V_{OUT} = 0V		8	pF

Note: 1. Outputs deselected.

Table 6. DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{CC1} (1)	Operating Supply Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IL}$, E2 = V_{IH}, I_{OUT} = 0mA	t_{RC}/t_{WC} = Min		20	mA
			t_{RC}/t_{WC} = 1µs		3.0	mA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		–1	1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		–1	1	µA
I_{PD}	Deep Power Down Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, E2 ≤ 0.2V			10	µA
I_{SB}	Standby Supply Current CMOS	3.1V ≤ V_{CC} ≤ 3.3V, V_{IN} ≤ 0.2V or ≥ V_{CC} –0.2V, $\overline{E1}$ ≥ V_{CC} –0.2V and E2 ≥ V_{CC} –0.2V), I_{OUT} = 0mA			100	µA
		2.7V ≤ V_{CC} ≤ 3.1V, V_{IN} ≤ 0.2V or ≥ V_{CC} –0.2V, $\overline{E1}$ ≥ V_{CC} –0.2V and E2 ≥ V_{CC} –0.2V), I_{OUT} = 0mA			70	µA
V_{IH} (2)	Input High Voltage	2.7V ≤ V_{CC} ≤ 3.3V		0.8V_{CC}	V_{CC} + 0.2	V
V_{IL} (3)	Input Low Voltage	2.7V ≤ V_{CC} ≤ 3.3V		–0.3	0.2V_{CC}	V
V_{OH}	Output High Voltage	3.1V ≤ V_{CC} ≤ 3.3V, I_{OH} = –0.5mA		2.5		V
		2.7V ≤ V_{CC} ≤ 3.1V, I_{OH} = –0.5mA		2.2		V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	V

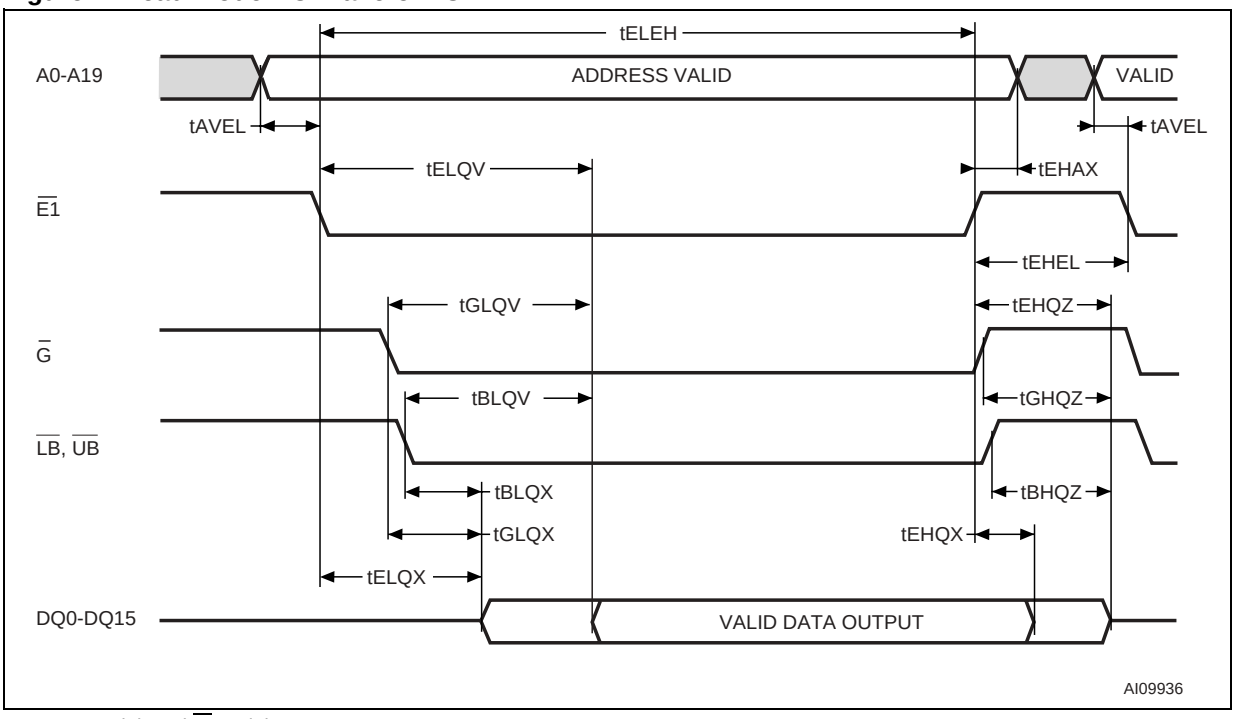
Note: 1. Average AC current, Outputs open, cycling at t_{AVAX} (min).
2. Maximum DC voltage on inputs and I/O pins is V_{CC} + 0.2V.
During voltage transitions, data inputs may overshoot to V_{CC} + 1.0V for a period of up to 5ns.
3. Minimum DC voltage on input or I/O pins is –0.3V.
During voltage transitions, data inputs may overshoot to V_{SS} + 1.0V for a period of up to 5ns.

Table 7. Read and Standby Modes AC Characteristics

Symbol	Alt.	Parameter	M69AW024BE		Unit
			–60		
			Min	Max	
t_{AVAX}, t_{ELEH} (1,2)	t_{RC}	Read Cycle Time	70	1000	ns
t_{ELQV}(3)	t_{CE}	Chip Enable Access Time		60	ns
t_{GLQV}(3)	t_{OE}	Output Enable Access Time		40	ns
t_{AVQV}(3,5)	t_{AA}	Address Access Time		60	ns
t_{BLQV}(3)	t_{BA}	$\overline{LB}$, $\overline{UB}$ Low to Output Valid		30	ns
t_{AXQX}, t_{GHQX}, t_{BHQX}, t_{EHQX} (8)	t_{OH}	Output Hold Time after Chip Enable Low	5		ns
t_{ELQX}(4,8)	t_{CLZ}	Chip Enable Low to Output Low-Z	5		ns
t_{GLQX}(4,8)	t_{OLZ}	Output Enable Low to Output Low-Z	0		ns
t_{BLQX}(4,8)	t_{BLZ}	$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	0		ns
t_{EHQZ}(8)	t_{CHZ}	Chip Enable High to Output Hi-Z		20	ns
t_{GHQZ}(8)	t_{OHZ}	Output Enable High to Output Hi-Z		20	ns
t_{BHQZ}(8)	t_{BHZ}	$\overline{LB}$, $\overline{UB}$ High to Output Hi-Z		20	ns
t_{AVEL}	t_{ASC}	Address Set-up Time to Chip Enable Low	–5		ns
t_{AVGL}	t_{ASO}	Address Valid to Output Enable Low	10		ns
t_{AXAV}(5)	t_{AX}	Address Invalid Time		10	ns
t_{EHAX}(6)	t_{CHAH}	Chip Enable High to Address Hold Time	–5		ns
t_{GHAX}	t_{OHAH}	Output Enable High to Address Hold Time	–5		ns
t_{WHGL}(7)	t_{WHOL}	Write Enable High to Output Enable Low (Read Operations)	10	1000	ns
t_{EHEL}	t_{CP}	Chip Enable High Pulse Width	10		ns

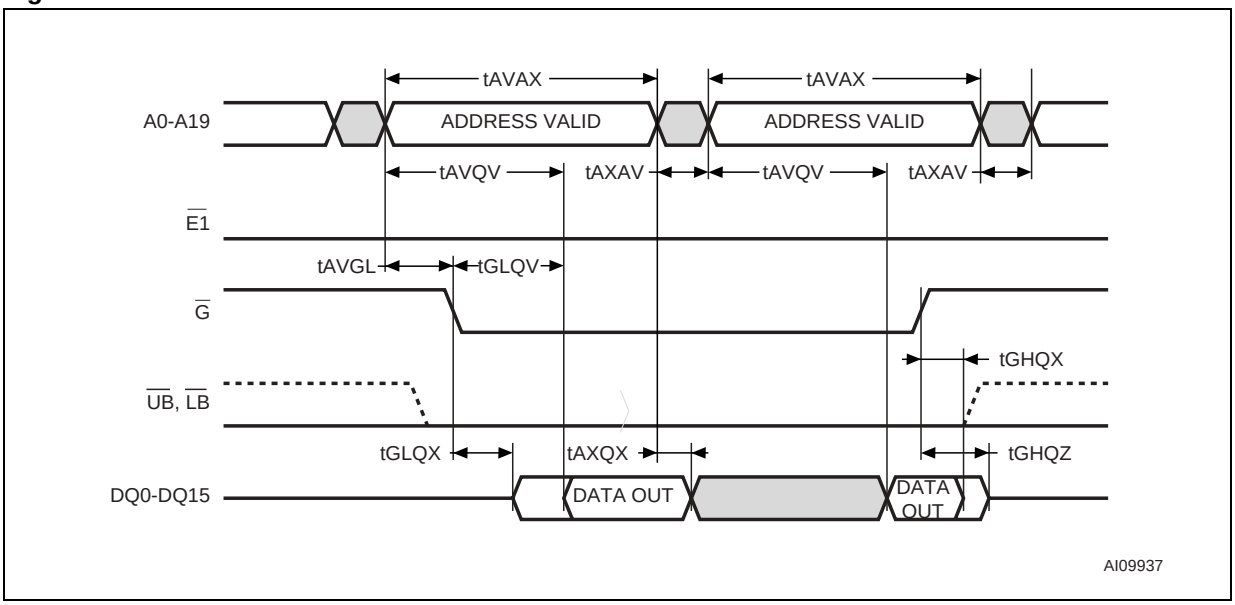
Note: 1. The maximum value of this timing is applicable if $\overline{E1}$ is kept Low with addresses unchanged.If needed by the system operation, please contact your local ST representative for relaxation of the 1000ns limitation.
2. Addresses should not be changed during t_{AVAX}(min).
3. These parameters are measured according to the conditions on input and output timing reference voltage shown on Figure 6., AC Measurement I/O Waveform.
4. The output load capacitance is 5pF without any other load.
5. These timings are given for $\overline{E1}$ Low.
6. t_{AVAX}(min) must be satisfied.
7. If the current value of t_{WHGL} is lower than the minimum value given in the above table, t_{AVQV} during the following Read operation may increase by t_{WHGL}(current) – t_{WHGL}(min).
8. All timings are measured according to the conditions for output transition timing reference voltage shown on Figure 6., AC Measurement I/O Waveform.

Figure 7. Read Mode AC Waveforms



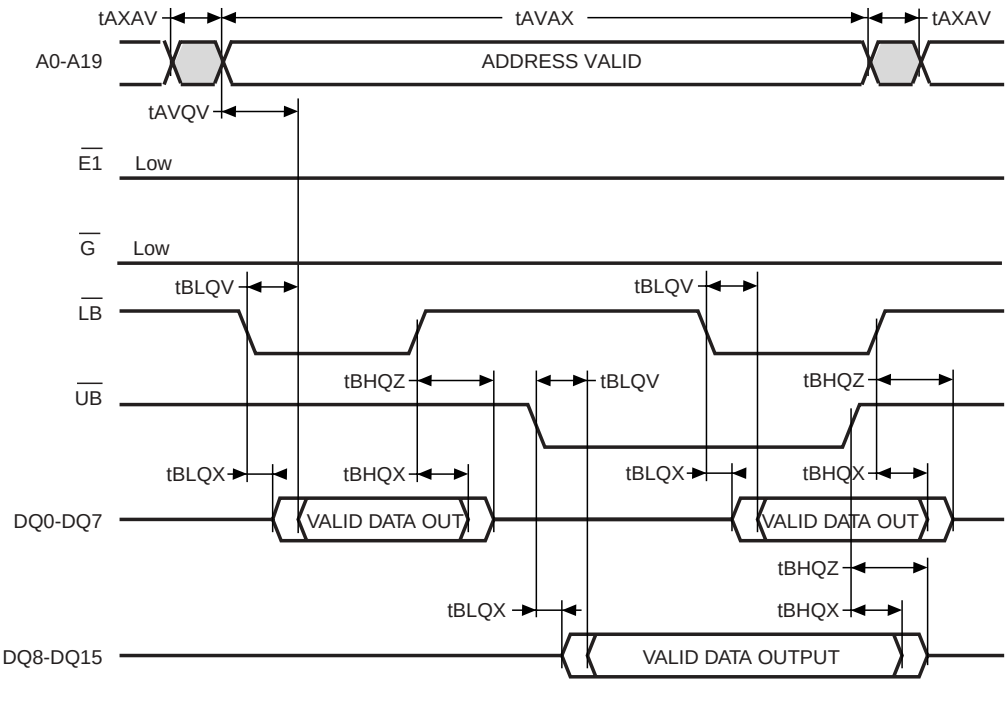
Note: E2 = High and $\overline{W}$ = High.

Figure 8. Address Access after $\overline{G}$ Controlled Read AC Waveforms



Note: 1. E2 = High and $\overline{W}$ = High.
2. During the two consecutive Read operations, the Output Enable signal, $\overline{G}$, can either remain Low, or be toggled.

Figure 9. $\overline{UB}$/$\overline{LB}$ Controlled Read AC Waveforms



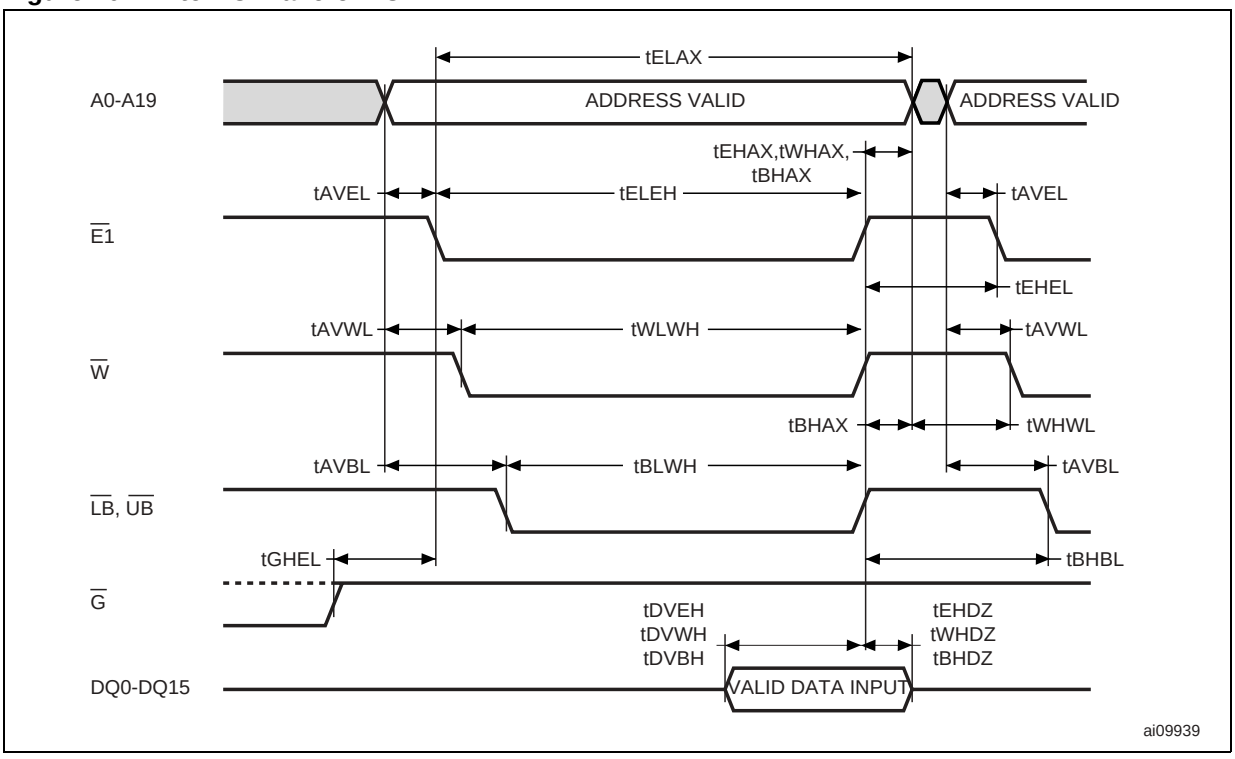
Note: E2 = High and $\overline{W}$ = High.

Table 8. Write Mode AC Characteristics

Symbol	Alt.	Parameter	M69AW024BE		Unit
			–60		
			Min	Max	
t_{AVAX}, t_{ELAX}(1,2)	t_{WC}	Chip Enable Write Cycle Time	70	1000	ns
t_{AVEL}, t_{AVBL}, t_{AVWL}(2)	t_{AS}	Address Set-up Time to Chip Enable Low	0		ns
t_{ELEH}(3)	t_{CW}	Chip Enable Write Pulse Width	45		ns
t_{WLBH}, t_{WLWH}(3)	t_{WP}	Write Enable Write Pulse Width	45		ns
t_{BLWH}, t_{BLBH}(3)	t_{BW}	$\overline{LB}$, $\overline{UB}$ Pulse (Write Operation)	45		ns
t_{BHWL}(4)	t_{BS}	$\overline{LB}$, $\overline{UB}$ Byte Masking Set-up Time	–5		ns
t_{WHBL}(5)	t_{BH}	$\overline{LB}$, $\overline{UB}$ Hold Time	–5		ns
t_{WHAX}, t_{EHAX}, t_{BHAX}(6)	t_{WR}	Write Recovery Time	0		ns
t_{EHEL}	t_{CP}	Chip Enable High Pulse	10		ns
t_{WHWL}	t_{WHP}	Write Enable High Pulse	10	1000	ns
t_{BHBL}	t_{BHP}	$\overline{LB}$, $\overline{UB}$ High Pulse	10	1000	ns
t_{DVEH}, t_{DVWH}, t_{DVBH}	t_{DS}	Data Set-up Time	15		ns
t_{EHDZ}, t_{WHDZ}, t_{BHDZ}, t_{GHDZ}	t_{DH}	Data Hold Time	0		ns
t_{GHEL}(7)	t_{OHCL}	Output Enable High to Chip Enable Low Set-up Time	–5		ns
t_{GHAV}(8)	t_{OES}	Output Enable Set-up Time	0		ns
t_{BLBH2}	t_{BWO}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High for Page Access	30		ns

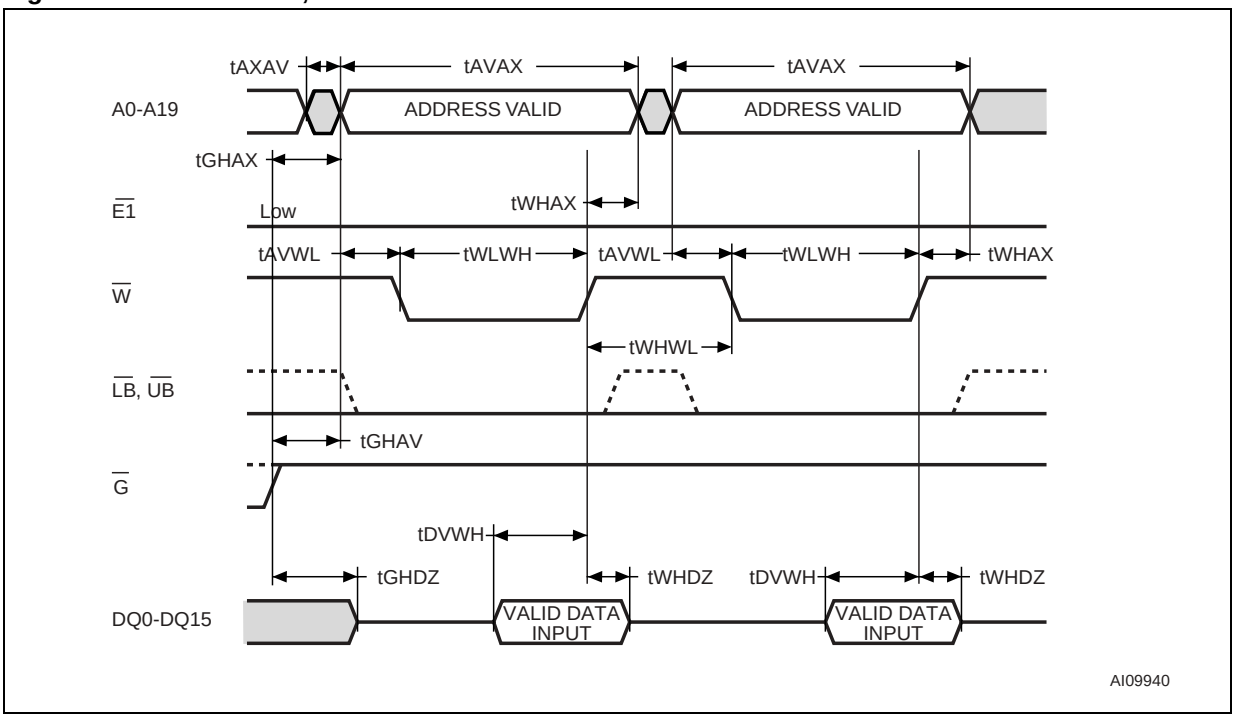
Note: 1. The maximum value of this timing is applicable if $\overline{E1}$ is kept Low without any address change. If needed by system operation, please contact your local ST representative for relaxation of the 1000ns limitation.
2. Minimum value must be equal to or greater than the sum of the write pulse (t_{ELEH}, t_{WLBH} or t_{BLBH} and the write recovery time t_{WHAV}.
3. Write pulse is defined from the falling edge of $\overline{E1}$, $\overline{W}$, or $\overline{LB}$/$\overline{UB}$, whichever occurs last.
4. Applicable to Byte Masking only. Byte Masking set-up time is defined from the falling edge of $\overline{E1}$ or $\overline{W}$ whichever occurs last.
5. Applicable to Byte Masking only. Byte Masking hold time is defined from the rising edge of $\overline{E1}$ or $\overline{W}$ whichever occurs first.
6. Write recovery is defined from the rising edge of $\overline{E1}$, $\overline{W}$, or $\overline{LB}$/$\overline{UB}$, whichever occurs first.
7. If $\overline{G}$ is Low after t_{GHEL}(min), the read cycle is initiated. In other words, $\overline{G}$ must be brought High within t_{GHEL} (min) after $\overline{E1}$ is brought Low. Once the read cycle is initiated, new write pulse should be input after t_{AVAX} or t_{ELEH} minimum value.
8. If $\overline{G}$ is Low after new address input, the read cycle is initiated. In other words, $\overline{G}$ must be brought High at the same time or before new address valid. Once the read cycle is initiated, new write pulse should be input after t_{AVAX} or t_{ELEH} minimum value.

Figure 10. Write AC Waveforms



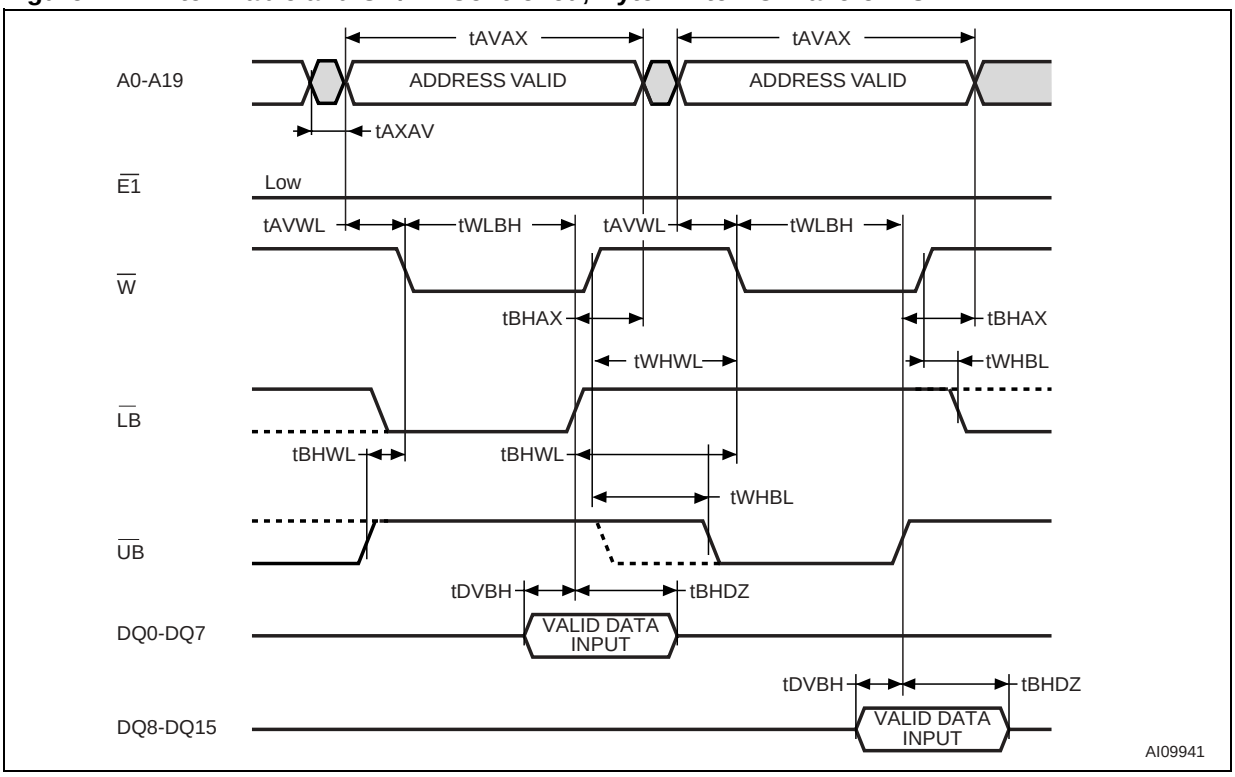
Note: 1. E2 must be High during the Write cycle.

Figure 11. $\overline{W}$ Controlled, Write AC Waveforms



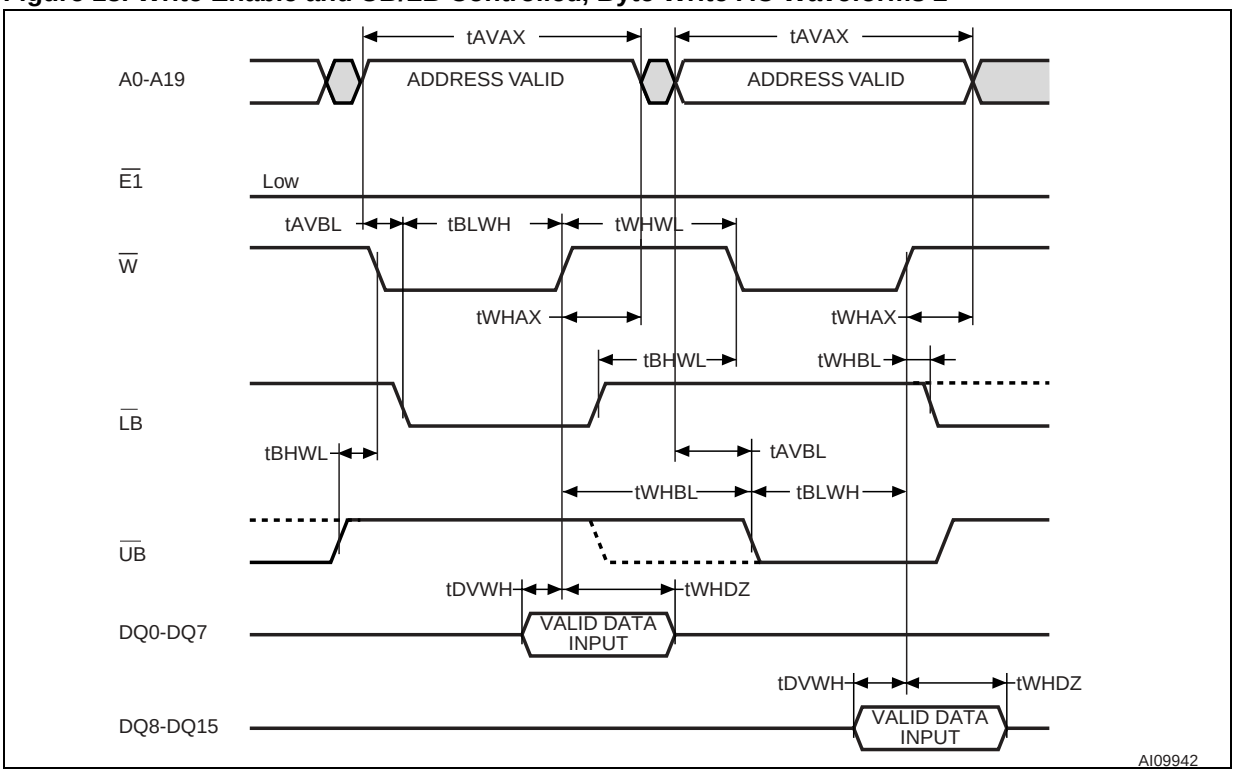
Note: 1. E2 must be High during the Write cycle.

Figure 12. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Byte Write AC Waveforms 1



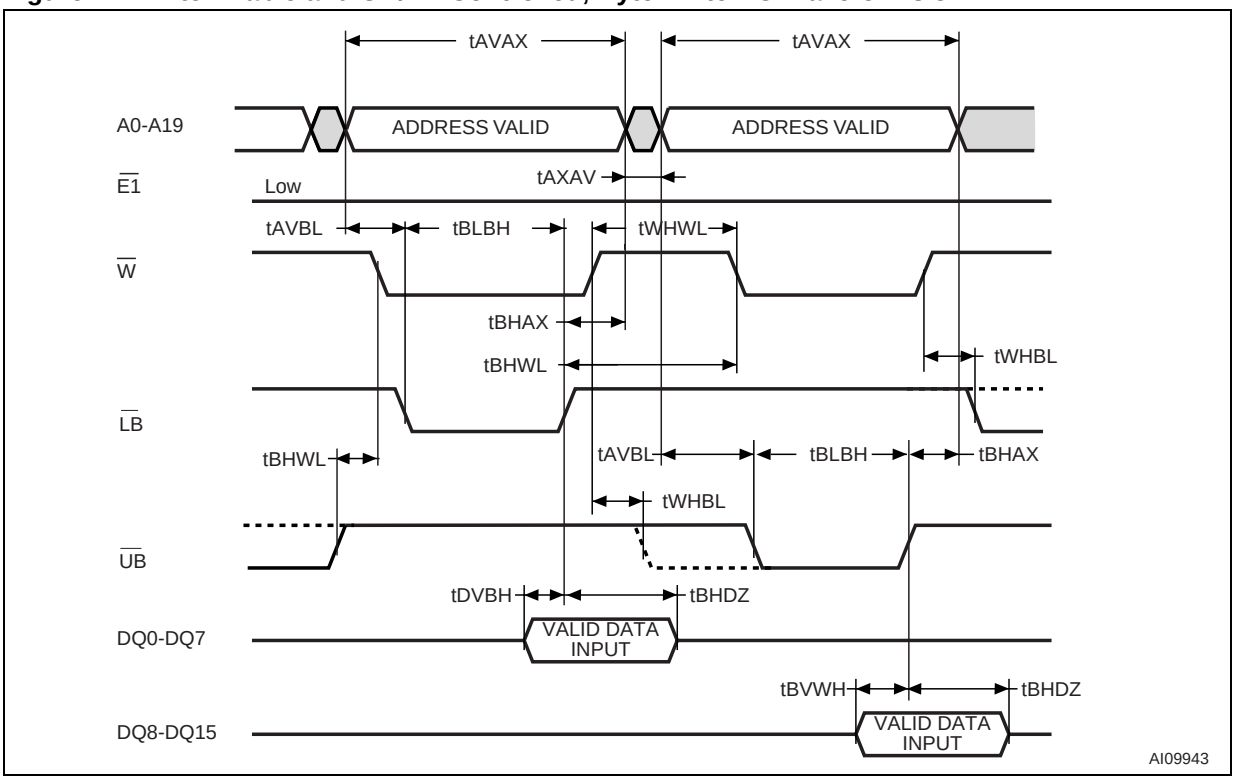
Note: 1. E2 and $\overline{G}$ must be High during the Write cycle.

Figure 13. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Byte Write AC Waveforms 2



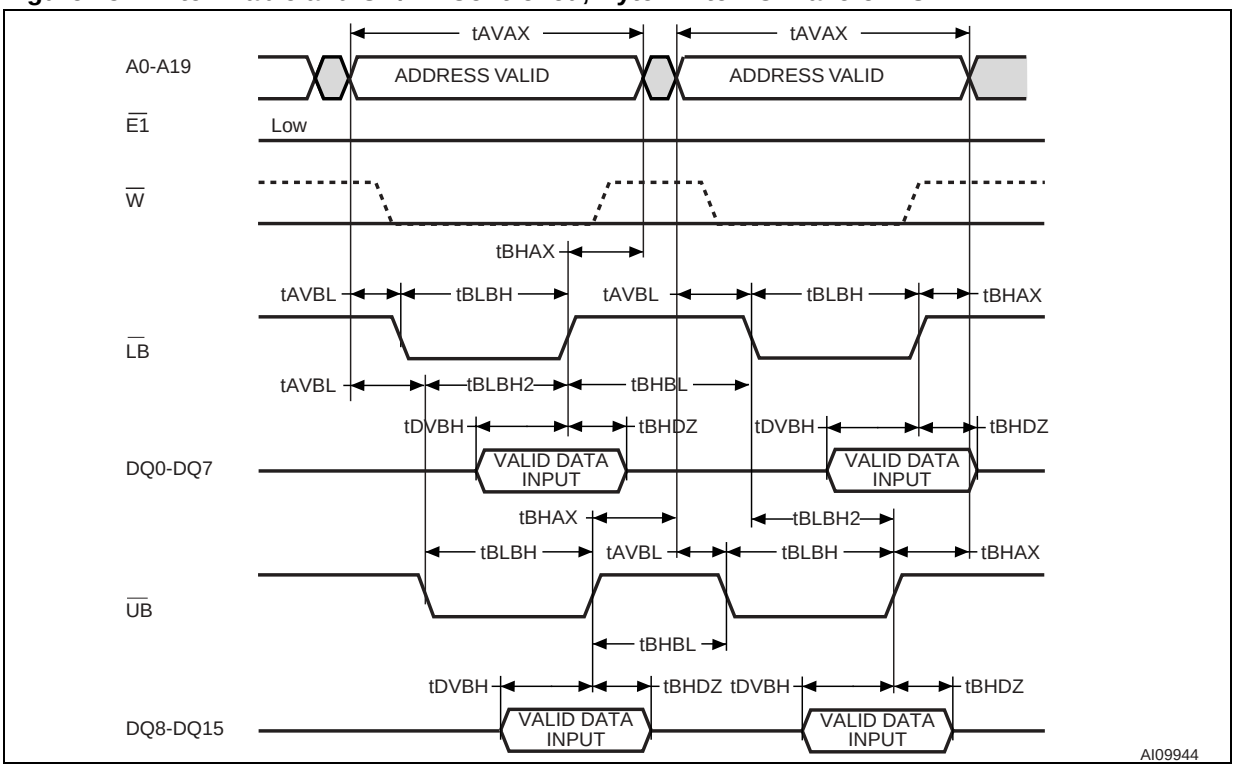
Note: 1. E2 and $\overline{G}$ must be High during the Write cycle.

Figure 14. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Byte Write AC Waveforms 3



Note: 1. E2 and $\overline{G}$ must be High during the Write cycle.

Figure 15. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Byte Write AC Waveforms 4



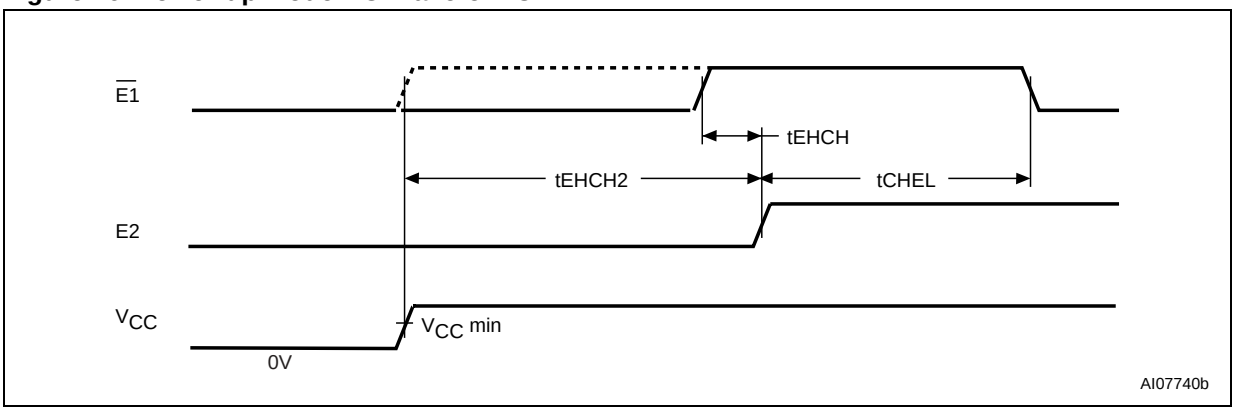
Note: 1. E2 and $\overline{G}$ must be High during the Write cycle.

Table 9. Standby, Power-Down and Power-Up AC Parameters

Symbol	Alt.	Parameter	M69AW024BE		Unit
			–60		
			Min	Max	
t_{CLEL}	t_{CSP}	E2 Low Setup Time for Power Down Entry	10		ns
t_{ELCH}	t_{C2LP}	E2 Low Hold Time after Power Down Entry	80		ns
t_{CHEL}(1)	t_{CHH}	$\overline{E1}$ High Hold Time following E2 High after Power-Down Exit $\overline{E1}$ High Hold Time following E2 High after Power-Up	300		µs
t_{EHCH}	t_{CHS}	$\overline{E1}$ High Setup Time following E2 High after Power-Down Exit	0		ns
t_{EHGH}	t_{CHOX}	$\overline{E1}$ High to $\overline{G}$ Invalid Time for Standby Entry	10		ns
t_{EHWH}(2)	t_{CHWX}	$\overline{E1}$ High to $\overline{W}$ Invalid Time for Standby Entry	10		ns
t_{τ}(3)	t_{τ}	Input Transition Time	1	25	ns
t_{EHCH2}	t_{C2LH}	Power-Up Time	50		µs

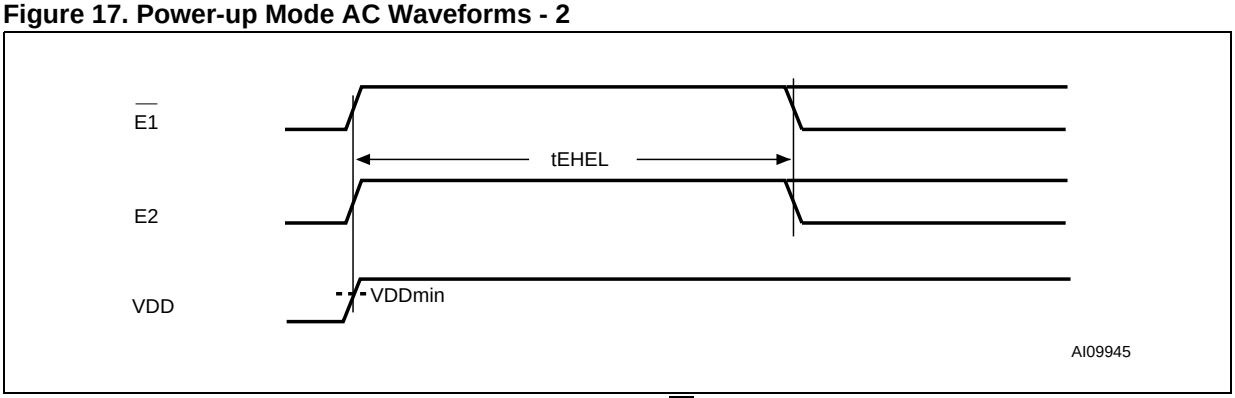
Note: 1. Applicable both to Power-Down and Power-Up.
2. Some data might be written into any address location if t_{EHWL} (min) is not satisfied.
3. The Input Transition Time used in AC measurements is 5ns.
4. TBD = to be defined.

Figure 16. Power-up Mode AC Waveforms - 1



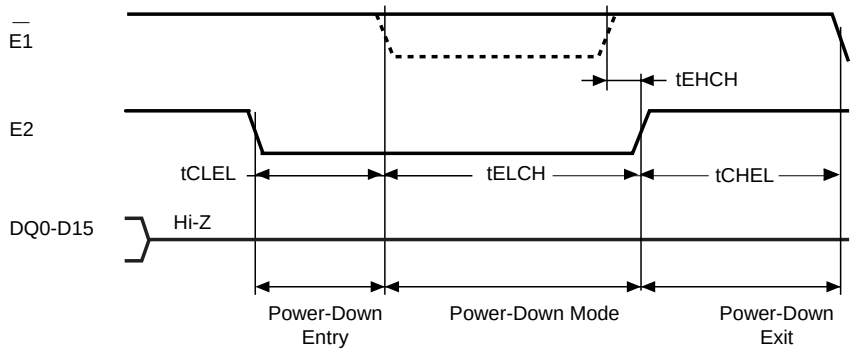
Note: t_{EHCH2} is defined from V_{CC} reaching V_{CC}(min).

Figure 17. Power-up Mode AC Waveforms - 2



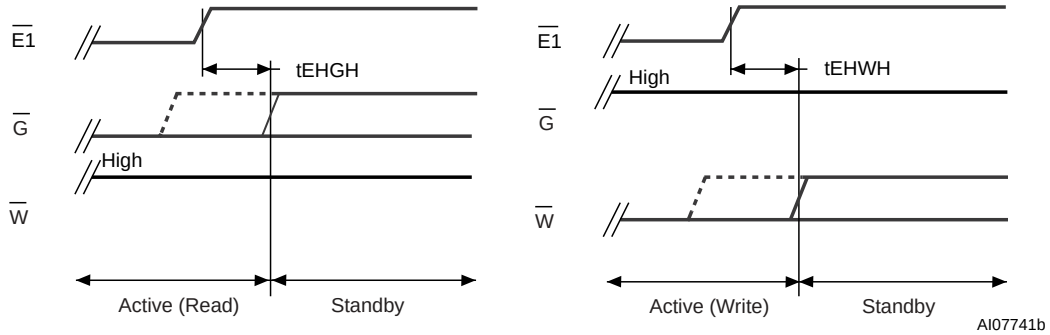
Note: t_{CHEL} is defined from V_{CC} reaching V_{CC}(min) and applicable both for $\overline{E1}$ and E2 signals.

Figure 18. Power-Down Entry ad Exit AC Waveforms



Note: The Power-Down mode timing can also be used as a Reset timing if the Power-up mode timing cannot be satisfied.

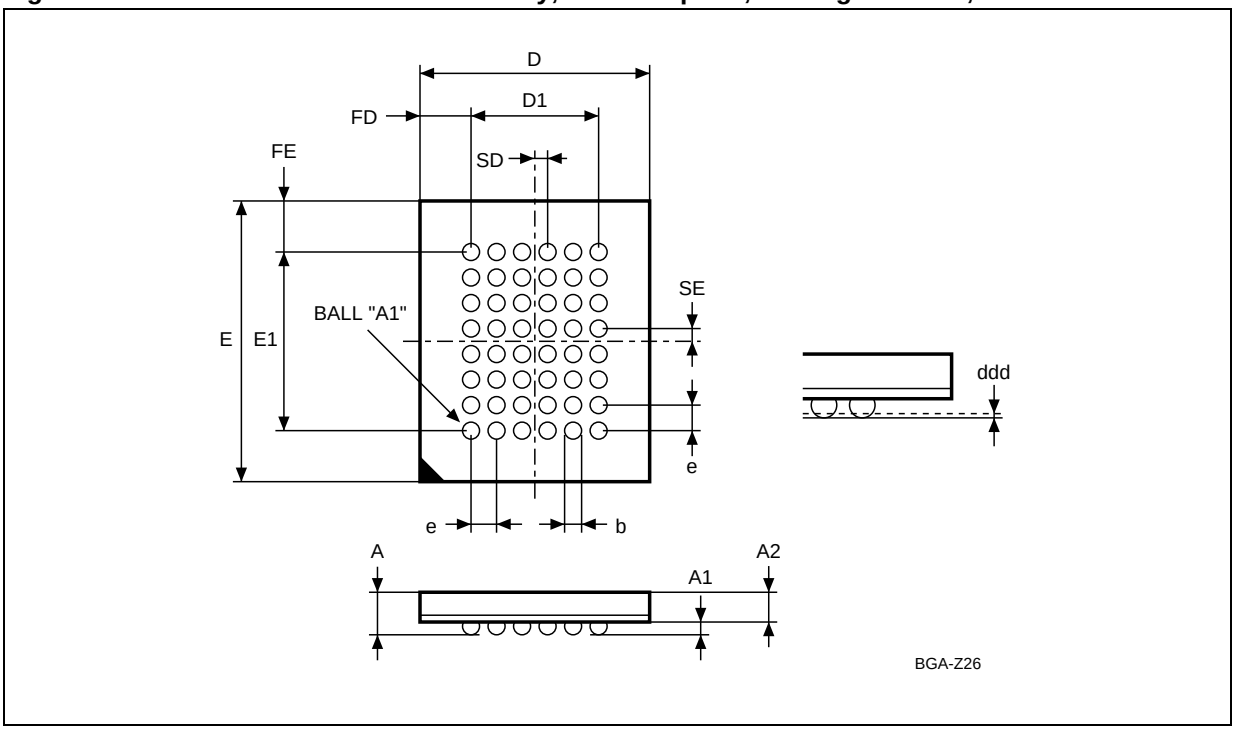
Figure 19. Standby Mode Entry AC Waveforms, after Read or Write



Note: Both t_{EHGH} and t_{EHWH} define the earliest entry timing for Standby mode. If one of these timings is not satisfied, it takes a t_{AVAX}(min) delay to enter Standby mode from $\overline{E1}$ rising edge.

PACKAGE MECHANICAL

Figure 20. TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch, Package Outline, Bottom View



Note: Drawing is not to scale.

Table 10. TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.125	–	–	0.0443	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M69AW024BE 60 ZB 8 F

Device Type
M69 = 1T/1C Memory Cell Architecture

Mode
A = Asynchronous

Operating Voltage
W = 2.7 to 3.3V

Array Organization
024 = 16 Mbit (1M x16)

Option 1
B = 2 Chip Enable

Option 2
E = E die

Speed Class
60 = 60ns

Package
ZB = TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch

Temperature Range
8 = –30 to 85 °C

Packing Option
F = RoHS Compliant Package, Tape & Reel Packing

The notation used for the device number is as shown in Table 11.. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest STMicroelectronics Sales Office.

REVISION HISTORY

Table 12. Document Revision History

Date	Rev.	Revision Details
28-Jun-2004	0.1	First Issue
29-Jun-2004	0.2	Table 11., Ordering Information Scheme updated.
22-Mar-2005	1.0	t_{EHQX} added in Table 7., Read and Standby Modes AC Characteristics. t_{GHDZ} and t_{BHDZ} added in Table 8., Write Mode AC Characteristics. Figure 19., Standby Mode Entry AC Waveforms, after Read or Write updated. RoHS Packing option added in FEATURES SUMMARY and Table 11., Ordering Information Scheme. T_{LEAD} parameter added in Table 3., Absolute Maximum Ratings
05-Apr-2005	2.0	Figure title modified and Note 2 added below Figure 8.