TDK SEMICONDUCTOR CORP.

73K224BL
V.22bis/V.22/V.21/Bell 212A/103
Single-Chip Modem w/ Integrated Hybrid

June 2001

DESCRIPTION

The 73K224BL is a highly integrated single-chip modem IC which provides the functions needed to construct a V.22bis compatible modem, capable of 2400 bit/s full-duplex operation over dial-up lines. The 73K224BL is an enhancement of the 73K224L single-chip modem which adds the hybrid hook switch control, and driver to the 73K224L. The 73K224BL integrates analog, digital, and switched-capacitor array functions on a single chip, offering excellent performance and a high level of functional integration in a 32-Lead PLCC package.

The 73K224BL operates from a single +5 V supply for low power consumption.

The 73K224BL is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular single-chip micro-processors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control simplifies address demultiplexing. Data communications normally occur through a separate serial port.

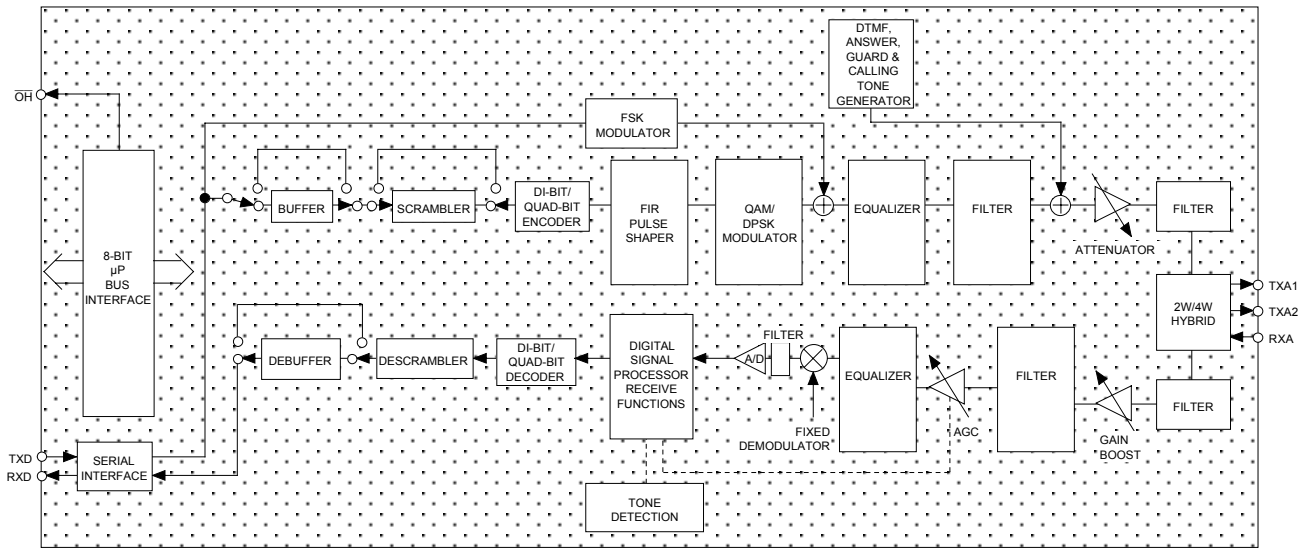
(continued)

FEATURES

- **Includes features of 73K224L single-chip modem**
- **On chip 2-wire/4-wire hybrid driver and off hook relay buffer driver**
- **One-chip multi-mode V.22bis/V.22/V.21 and Bell 212A/103 compatible modem data pump**
- **FSK (300 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Software compatible with other TDK Semiconductor K-Series one-chip modems**
- **Interfaces directly with standard micro-processors (80C51 typical)**
- **Parallel or serial bus for control**
- **Selectable internal buffer/debuffer and scrambler/descrambler functions**
- **All asynchronous and synchronous operating modes (internal, external, slave)**

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

The 73K224BL is pin and software compatible with the 73K222BL, allowing system upgrades with a single component change.

The 73K224BL is designed to be a complete V.22bis compatible modem on a chip. The complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. Many functions were included to simplify implementation of typical modem designs. In addition to the basic 2400 bit/s QAM, 600/1200 bit/s DPSK and 300 bit/s FSK modulator/demodulator sections, the device also includes synch/asynch converters, scrambler/descrambler, call progress tone detect, DTMF tone generator capabilities and handshake pattern detectors. Test features such as analog loop, digital loop, and remote digital loopback are supported. Internal pattern generators are also included for self-testing.

FEATURES (continued)

- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (16 dB, 1 dB steps), selectable receive boost (+18 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, and signal quality monitors**
- **DTMF, answer and guard tone generators**
- **Test modes available: ALB, DL, RDL, mark, space, alternating bit, S1 pattern generation and detection**
- **CMOS technology for low power consumption (typically 100 mW @ 5 V) with power-down mode (15 mW @ 5 V)**
- **TTL and CMOS compatible inputs and outputs**

FUNCTIONAL DESCRIPTION

HYBRID AND RELAY DRIVER

To make designs more cost effective and space efficient, the 73K224BL includes the 2-wire to 4-wire hybrid with sufficient drive to interface directly to the telecom coupling transformers. In addition, an off hook relay driver with 30mA drive capability is also included to allow use of commonly available mechanical telecom relays.

QAM MODULATOR/DEMODULATOR

The 73K224BL encodes incoming data into quad-bits represented by 16 possible signal points with specific phase and amplitude levels. The base-band signal is then filtered to reduce intersymbol interference on the band limited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The 73K224BL modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). Adaptive equalization is also used in DPSK modes for optimum operation with varying line conditions.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz

FUNCTIONAL DESCRIPTION (continued)

(originate mark and space) and 2225 and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the band limited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communication with asynchronous terminals which may communicate at 600,1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01% in DPSK and QAM modes. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where quad-bit/di-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking, and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The synch/asynch converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 rising edge of TXCLK the normal width.

Both the synch/asynch rate converter and the data descrambler are automatically bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted at the same rate as it is input.

PARALLEL BUS CONTROL INTERFACE MODE

Eight 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Six control registers are read/write memory. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE MODE

The serial Command mode allows access to the 73K224BL control and status registers via a serial control port. In this mode the AD0, AD1, and AD2 lines provide register addresses for data passed through the AD7 (DATA) pin under control of the RD and WR lines. A read operation is initiated when the RD line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. WR is then pulsed low and data transfer into the selected register occurs on the rising edge of WR.

DTMF GENERATOR

The DTMF generator controls the sending of the sixteen standard DTMF tone pairs. The tone pair sent is determined by selecting transmit DTMF (bit D4) and the 4 DTMF bits (D0-D3) of the Tone Register. Transmission of DTMF tones from TXA is gated by the transmit enable bit of CR0 (bit D1) as with all other analog signals.

PIN DESCRIPTION

POWER

NAME	PIN	TYPE	DESCRIPTION
GND	1	I	System ground
VDD	16	I	Power supply input, 5 V ±10% (73K224BL). Bypass with 0.1 and 22 µF capacitors to GND.
VREF	31	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to ground.
ISET	28	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR CONTROL INTERFACE MODE

ALE	13	I	ADDRESS LATCH ENABLE: The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	5-12	I/O	ADDRESS/DATA BUS: These bi-directional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	23	I	CHIP SELECT: A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	2	O	OUTPUT CLOCK: This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 times the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	20	O	INTERRUPT: This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	15	I	READ: A low requests a read of the 73K224BL internal registers. Data can not be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	30	I	RESET: An active high signal on this pin will put the chip into an inactive state. All Control Register bits (CR0, CR1, tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on-reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	PIN	TYPE	DESCRIPTION
$\overline{WR}$	14	I	WRITE: A low on this informs the 73K224BL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR CONTROL INTERFACE MODE

NAME	PIN	TYPE	DESCRIPTION
AD0-AD2	5-7	I	REGISTER ADDRESS SELECTION: These lines carry register addresses and should be valid during any read or write operation.
DATA (AD7)	12	I/O	SERIAL CONTROL DATA: Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	15	I	READ: A low on this input informs the 73K224BL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	14	I	WRITE: A low on this input informs the 73K224BL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

NOTE: The serial control mode is provided by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become the register address.

DTE USER

NAME	PIN	TYPE	DESCRIPTION
EXCLK	22	I	EXTERNAL CLOCK: This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	26	O	RECEIVE CLOCK: The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	25	O	RECEIVED DATA OUTPUT: Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	21	O	TRANSMIT CLOCK: This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In internal mode the clock is generated internally. In external mode TXCLK is phase locked to the EXCLK pin. In slave mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	24	I	TRANSMIT DATA INPUT: Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended over speed mode.

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PIN DESCRIPTION (continued)

ANALOG INTERFACE AND OSCILLATOR

NAME	PIN	TYPE	DESCRIPTION
RXA	32	I	Received modulated analog signal input from the telephone line interface.
TXA1 / TXA2	18 / 17	O	Transmit Analog (differential outputs): These pins provide the analog output signals to be transmitted to the telephone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
XTL1 / XTL2	3 / 4	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to ground. XTL2 can also be driven from an external clock.
$\overline{OH}$	27	O	OFF-HOOK RELAY DRIVER: This signal is an open drain output capable of sinking 30mA and is used for controlling a relay. The output is the complement of the OH register bit in the ID Register.

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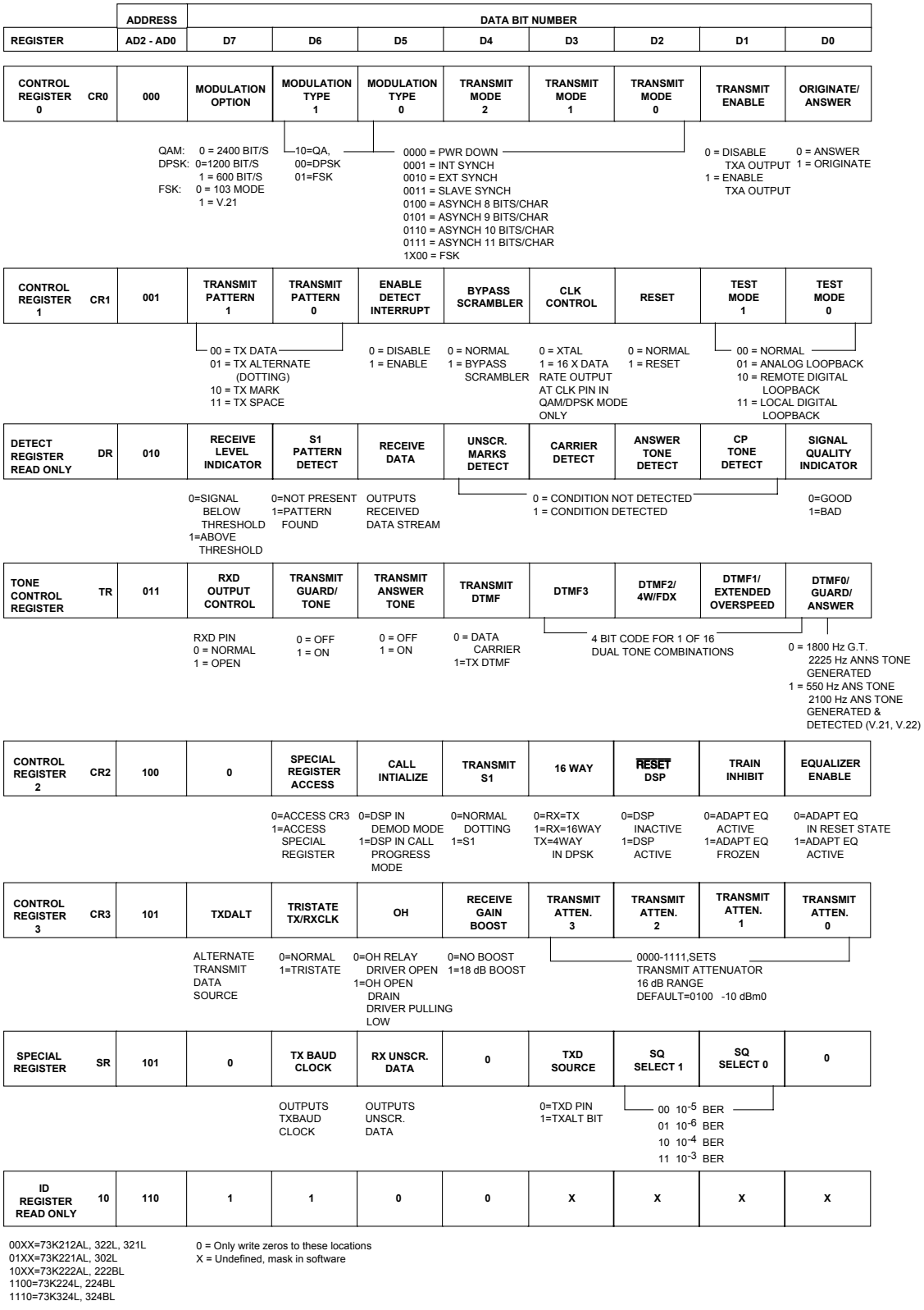
REGISTER ADDRESS TABLE



00XX=73K212AL, 322L, 321L
01XX=73K221AL, 302L
10XX=73K222AL, 222BL
1100=73K224L, 224BL
1110=73K324L, 324BL

0 = Only write zeros to these locations
X = Undefined, mask in software

CONTROL REGISTER 0

CR0	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA1 & TXA2
		1	Enables transmit output at TXA1 & TXA2
			Note: Transmit enable must be set to 1 to allow activation of answer tone or DTMF.
D5,D4 D3,D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects Power down mode. All functions disabled except digital interface..
		0 0 0 1	Internal synchronous mode in this mode TXCLK is an internally derived 600,1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 600, 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode Same operation as other synchronous modes TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects a synchronous mode 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, 1 stop bit) or 2 stop bits)..
		1 X 0 0	Selects FSK operation.
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK

CONTROL REGISTER 0 (continued)

CR0	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects 103 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

CR1	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLOCK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT	NAME	CONDITION	DESCRIPTION
D0, D1	Test Mode	D1 D0	
		0 0	Selects normal operating mode
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same carrier frequency as the transmitter. To squelch the TXA pin, transmit enable bit as well as Tone Register bit D2 must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrier at TXA pin
D2	Reset	0	Selects Normal Operations
		1	Resets modem to power-down state. All Control Register bits (CR0, CR1, CR2, CR3 and tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	Clock Control	0	Selects 11.0592 MHz crystal echo output at CLK pin
		1	Selects 16 times the data rate output at CLK pin in DPSK/QAM modes only.

CONTROL REGISTER 1 (continued)

CR1	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLOCK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK and QAM data is passed through scrambler.
		1	Selects Scrambler bypass. Bypass DPSK and QAM data is route around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power-down mode.
		1	Enables INT output. An interrupt will be generated with a change in status of DR bits D1- D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TXDTMF is activated. All interrupts will be disabled if the device is in power-down mode.
D6, D7	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXDpin.
		0 1	Selects an alternating mar/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation (see CR2 bit D4).
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

DR	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONES DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT	NAME	CONDITION	DESCRIPTION
D0	Signal Quality Indicator	0	Indicates normal received signal.
		1	Indicates low received signal quality (above average error rate). Interacts with Special Register bits D2, D1.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (continued)

DR	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONES DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	In call init mode, indicates detection of 2225 Hz answer tone in Bell mode (TR bit D0 = 0) or 2100 Hz if in CCITT mode (TR bit D0 = 1). The device must be in originate mode for detection of answer tone. Both answer tones are detected in demodulation mode.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0	No S1 pattern being received.
		1	S1 pattern detected. Should be time qualified by software. S1 pattern is defined as a double di-bit (001100..) unscrambled 1200 bit/s DPSK signal. Pattern must be aligned with baud clock to be detected.
D7	Receive Level Indicator	0	Received signal level below threshold, (typical ≈ -25 dBm0); can use receive gain boost (+18 dB).
		1	Received signal above threshold.

TONE REGISTER

TR	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4-WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER GUARD

BIT	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown
		X X 1 X	Transmit DTMF tones must be in DPSK or Bell 103 mode.
		X 1 0 0	Select Bell mode answer tone. Interacts with DR bit D2 and TR bit D5.
		X 1 0 1	Select CCITT mode answer tone. Interacts with DR bit D2 and TR bit D5.
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Extended Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM or DPSK +1% -2.5%. (normal)
		0 1	Asynchronous QAM or DPSK +2.3% -2.5%. (extended overspeed)
D2	DTMF 2/ 4 Wire FDX	D4 D2	
		0 0	Selects 2-wire duplex or half duplex
		0 1	D2 selects 4-wire full duplex in the modulation mode selected. The receive path corresponds to the receive mode selected by the ANS/ORIG bit CR0 D0 in terms of high or low band selection. The transmitter is in the same band as the receiver, but does not have magnitude filtering or equalization on its signal as in the receive path.

TONE REGISTER

TR	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4-WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER GUARD

BIT	NAME	CONDITION	DESCRIPTION		
D3, D2, D1, D0	DTMF 3, 2, 1, 0		D0 interacts with bits D6, D5, and D4 as shown		
			Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:		
		DTMF CODE D3 D2 D1 D0	KEYBOARD EQUIVALENT	TONES LOW	HIGH
		0 0 0 1	1	697	1209
		0 0 1 0	2	697	1336
		0 0 1 1	3	697	1477
		0 1 0 0	4	770	1209
		0 1 0 1	5	770	1336
		0 1 1 0	6	770	1477
		0 1 1 1	7	852	1209
		1 0 0 0	8	852	1336
		1 0 0 1	9	852	1477
		1 0 1 0	0	941	1336
		1 0 1 1	*	941	1209
		1 1 0 0	#	941	1477
		1 1 0 1	A	697	1633
		1 1 1 0	B	770	1633
		1 1 1 1	C	852	1633
		0 0 0 0	D	941	1633
D4	TX DTMF (Transmit DTMF)	0	Disable DTMF.		
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.		

NOTE: DTMF0-DTMF2 should be set to an appropriate state after DTMF dialing to avoid unintended operation.

TONE REGISTER (continued)

TR	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4-WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER GUARD

BIT	NAME	CONDITION	DESCRIPTION
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown. Also interacts with DR bit D2 in originate mode (see Detect Register description).
		0 0 X	Disables answer tone generator.
		1 0 0	In answer mode, a Bell 2225 Hz tone is transmitted continuously when the transmit enable bit is set.
		1 0 1	Likewise, a CCITT 2100 Hz answer tone is transmitted.
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator (see D0 for selection of guard tones). Bit D4 must be zero.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

CR2	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ $\overline{\text{DSP}}$	TRAIN INHIBIT	EQUALIZER ENABLE

BIT	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This bit is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET}}$ $\overline{\text{DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits.
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the modulator control mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.
D4	Transmit S1	0	The transmitter when placed in alternating mark/space mode transmits 0101..... scrambled or not dependent on the bypass scrambler bit.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, and in DPSK or QAM, an unscrambled repetitive double di-bit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is set-up to do demodulation and pattern detection based on the various mode bits. Both answer tones are detected in demodulation mode concurrently; TR-D0 is ignored.
		1	The DSP decodes unscrambled mark, answer tone and call progress tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the special register (see the special register for details).
D7	Not used at this time	0	Only write zero to this bit.

CONTROL REGISTER 3

CR3	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 101	TXDALT	TRI-STATE TX/RXCLK	OH	RECEIVE BOOST ENABLE	TRANSMIT ATTEN. 3	TRANSMIT ATEN 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 1 1 1 1	Sets the attenuation level of the transmitted signal in 1 dB steps. The default (D3 - D0 = 0100) is for a transmit level of -10 dBm0 on the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive Gain Boost	0	18 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5	OH	0	Relay driver open.
		1	Open drain driver pulling low.
D6	Tri-state TXCLK/RXCLK	0	TXCLK and RXCLK are driven.
		1	TXCLK and RXCLK are tri-stated.
D7	TXDALT	Special Register Bit D3=1	Alternate TX data source (see Special Register).

SPECIAL REGISTER

SR	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 101	0	TXBAUD CLOCK	RXUN-DSCR DATA	0	TXD SOURCE	SIGNAL QUALITY LEVEL SELECT 1	SIGNAL QUALITY LEVEL SELECT 0	0

BIT	NAME	DESCRIPTION	
D7, D4, D0		Not used at this time. Only write zeros to these bits.	
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.	
D5	RXUNDSCR Data	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.	
D3	TXD Source	This bit selects the transmit data source; either the TXD pin if zero or the TXDALT if this bit is a one. The transmit pattern bits D7 and D6 in CR1 override either of these sources.	
D2, D1	Signal Quality Level Select	The signal quality indicator is a logical zero when the signal received is acceptable for low error rate reception. It is determined by the value of the mean squared error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a one constantly. The SQI bit and threshold selection are valid for QAM and DPSK only and indicates typical error rate.	
	D2 D1	THRESHOLD VALUE	UNITS
	0 0	10^{-5}	BER (default)
	0 1	10^{-6}	BER
	1 0	10^{-4}	BER
	1 1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a one and addressing CR3. This register provides functions to the 73K224BL user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a zero.

ID REGISTER

ID	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 110	ID	ID	ID	ID	X	X	X	X

BIT	NAME	CONDITION				DESCRIPTION
D7, D6, D5, D4		D7	D6	D5	D4	Indicates Device:
		0	0	X	X	73K212L, 73K321L or 73K322L
		0	1	X	X	73K221L or 73K302L
		1	0	X	X	73K222L or 73K222BL
		1	1	0	0	73K224L, 73K224BL
		1	1	1	0	73K324L, 73K324BL

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD supply voltage	7 V
Storage temperature	-65 to 150° C
Soldering temperature (10 s)	235° C
Applied voltage	-0.3 to VDD + 0.3 V

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD supply voltage		4.5	5	5.5	V
TA, operating free-air		-40		+85	C
Clock variation	(11.0592 MHz) crystal or external clock	-0.01		+0.01	%
External components (Refer to application section for placement.)					
VREF bypass capacitor	External to GND (Note 1)	0.1			µF
Bias setting resistor	Placed between VDD and ISET pins	1.8	2	2.2	Ω
ISET bypass capacitor	ISET pin to GND	0.1			µF
VDD bypass capacitor 1	External to GND (Note 1)	0.1			µF
VDD bypass capacitor 2	External to GND (Note 1)	22			µF
XTL1 load capacitor	Depends on crystal characteristics from pin to GND			40	pF
XTL2 load capacitor	Depends on crystal characteristics from pin to GND			40	pF
Hybrid loading	see Figure 1		600		Ω
R1			600		Ω
R2			0.033		Ω
C1					µF

NOTE 1: Minimum for optimized system layout; may require higher values for noisy environments.

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	CLK = 11.0592 MHz ISET Resistor = 2 MΩ				
IDD1, Active	Operating with crystal oscillator,		20	27	mA
IDD2, Idle	< 5 pF capacitive load on CLK pin		5	7	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VDD			100	µA
IIL, Input Low Current	VI = 0V	-200			µA
Reset Pull-down Current	Reset = VDD	2		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
RXD Tri-State Pull-up Curr.	RXD = GND	-2		-50	µA
OH Output VOL	IOUT = 40 mA			TBA	V
Capacitance					
CLK	Maximum permitted load			25	pF
Input Capacitance	All digital inputs			10	pF

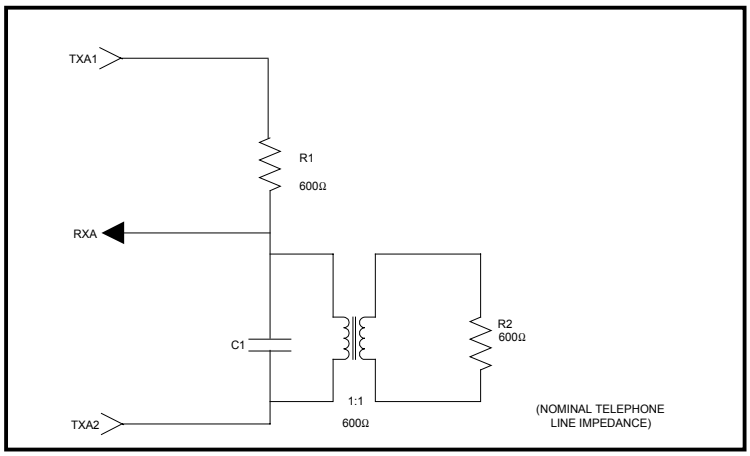


FIGURE 1: ANALOG INTERFACE HYBRID LOADING

NOTE: Parameters expressed in dBm0 refer to signals at the telephone line, i.e., across R2 in Figure 1.

The signals at TXA1 or TXA2 are each ≈ 8dB lower than at the line.

The signal at RXA is ≈ 3 dB lower than at the line.

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
QAM/DPSK Modulator					
Carrier suppression	Measured at TXA	35			dB
Output Amplitude	TX Scrambled marks ATT = 0100 (default)	-11.5	-10	-9	dBm0
FSK Modulator/Demodulator					
Output Frequency Error	CLK = 11.0592 MHz	-0.31		+0.20	%
Transmit Level	ATT = 0100 (default) transmit dotting pattern	-11.5	-10	-9	dBm0
TXA output distortion	All products through BPF			-45	dB
Output bias distortion @ RXD	Dotting pattern measured at RXD receive level -20 dBm, SNR 20 dB	-10		+10	%
Output jitter @ RXD	Integrated for 5 seconds	-15		+15	%
Sum of bias distortion and output jitter	Integrated for 5 seconds	-17		+17	%
Answer Tone Generator (2100 or 2225 Hz)					
Output amplitude	ATT = 0100 (default level)	-11.5	-10	-9	dBm0
	Not in V.21				
Output Distortion	Distortion products in receive band			-40	dB
DTMF Generator	Not in V.21				
Frequency accuracy		-0.03		+0.25	%
Output amplitude	Low band, ATT = 0100, DPSK mode	-10		-8	dBm0
Output amplitude	High band, ATT = 0100, DPSK mode	-8		-6	dBm0
Twist	High band to low band, DPSK mode	1	2	3	dB
Receiver Dynamic Range	Refer to performance curves	-43		-3	dBm0
Call Progress Detector	In call init mode				
Detect level	460 Hz test signal	-34		0	dBm0
Reject level	460 Hz test signal			-40	dBm0
Delay time	-70 dBm0 to -30 dBm0 step			25	ms
Hold time	-30 dBm0 to -70 dBm0 step			25	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Carrier Detect		Receive gain = On for lower input level measurements				
Threshold		All modes	-48		-43	dBm0
Hysteresis		All modes		2		
Delay Time	FSK	70 dBm0 to -6 dBm0 Change at input	25		37	ms
		70 dBm0 to -40 dBm0 Change at input	25		37	ms
	DPSK	-70 dBm0 to -6 dBm0 Change at input	7		17	ms
		-70 dBm0 to -40 dBm0 Change at input	7		17	ms
	QAM	-70 dBm0 to -6 dBm0 Change at input	25		37	ms
		-70 dBm0 to -40 dBm0 Change at input	25		37	ms
Hold Time	FSK	-6 dBm0 to -70 dBm0 Change at input	25		37	ms
		40 dBm0 to -70 dBm0 Change at input	15		30	ms
	DPSK	-6 dBm0 to -70 dBm0 Change at input	20		29	ms
		-40 dBm0 to -70 dBm0 Change at input	14		21	ms
	QAM	-6 dBm0 to -70 dBm0 Change at input	25		32	ms
		-40 dBm0 to -70 dBm0 Change at input	18		28	ms
Answer Tone Detectors		DPSK Mode				
Detect Level			-48		-43	dBm0
Detect Time		Call init mode, 2100 or 2225 Hz	6		50	ms
Hold Time		Call init mode, 2100 or 2225 Hz	6		50	ms
Pattern Detectors		DPSK Mode				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		55	ms
Hold Time		Demodulation mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40 call init	10		45	ms
Hold Time		mode	10		45	ms
Receive Level Indicator						
Detect On			-22		-28	dBm0
Valid after Carrier Detect		DPSK Mode	1	4	7	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Transmit Attenuator					
Range of Transmit Level	1111-0000 (Default ATT=0100)	-22		-6	dBm0
Step Accuracy		-0.15		+0.15	dB
Clock Noise					
	TXA pins; 153.6 kHz			1.5	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±5		Hz
Recovered Clock					
Capture Range	% of frequency (originate or answer)	-0.02		+0.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz		+1.2		%
	1800 Hz		-0.8		
Tone Level	550 Hz	-4.5	-3.0	-1.5	dB
(Below QAM/DPSK Output)	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion	550 Hz			-50	dB
(700 to 2900 Hz)	1800 Hz			-50	dB

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
TIMING (Refer to Timing Diagrams)		*				
TAL		$\overline{CS}$/Address setup before ALE Low	12			ns
TLA	$\overline{CS}$	$\overline{CS}$	0			ns
	AD0-AD7	Address hold after ALE Low	10			ns
TLC		ALE Low to $\overline{RD}$/$\overline{WR}$ Low	10			ns
TCL		$\overline{RD}$/$\overline{WR}$ Control to ALE High	0			ns
TRD		Data out from $\overline{RD}$ Low	0		70	ns
TLL		ALE width	15			ns
TRDF		Data float after $\overline{RD}$ High			50	ns
TRW		$\overline{RD}$ width	50			ns
TWW		$\overline{WR}$ width	150			ns
TDW		Data setup before $\overline{WR}$ High	15			ns
TWD		Data hold after $\overline{WR}$ High	12			ns
TCKD		Data out after EXCLK Low			200	ns
TCKW (serial mode)		$\overline{WR}$ after EXCLK Low	150			ns
TDCK (serial mode)		Data setup before EXCLK Low	150			ns
TAC (serial mode)		Address setup before control**	50			ns
TCA (serial mode)		Address hold after control**	50			ns
TWH (serial mode)		Data Hold after EXCLK	50			ns

* All timing parameters are targets and not guaranteed.

** Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$. Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

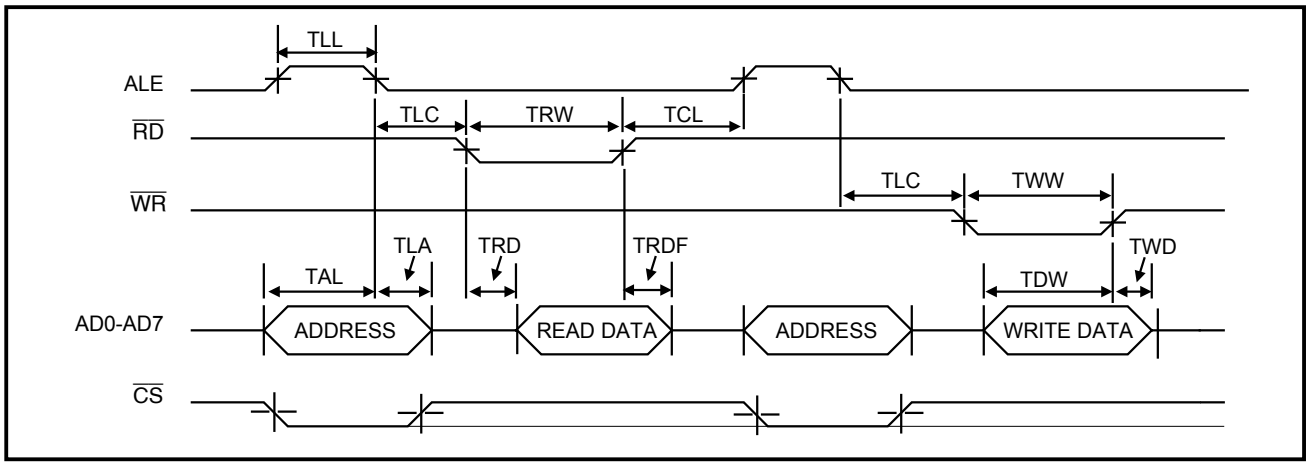


FIGURE 2: Bus Timing Diagram (Parallel Control Mode)

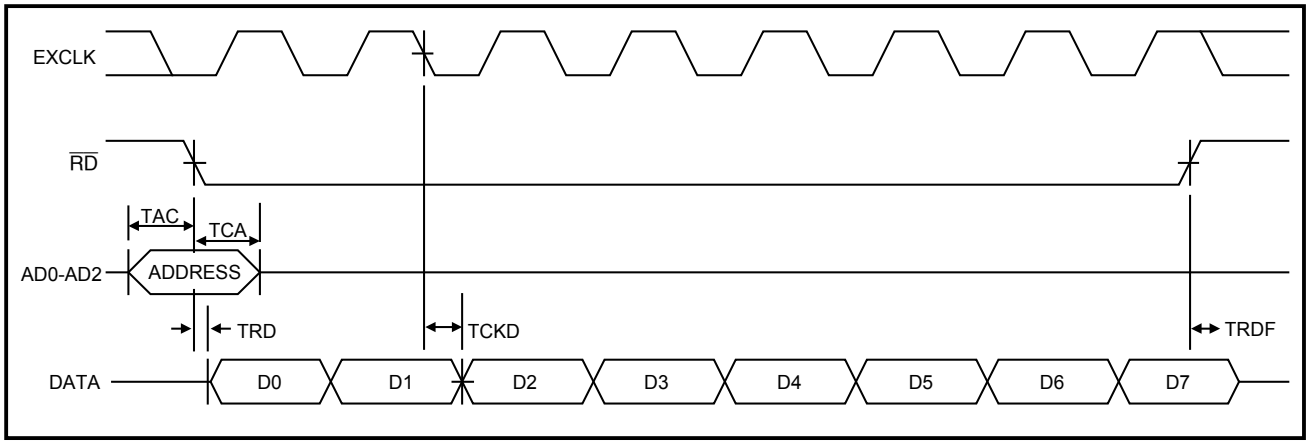


FIGURE 3: Read Timing Diagram (Serial Control Mode)

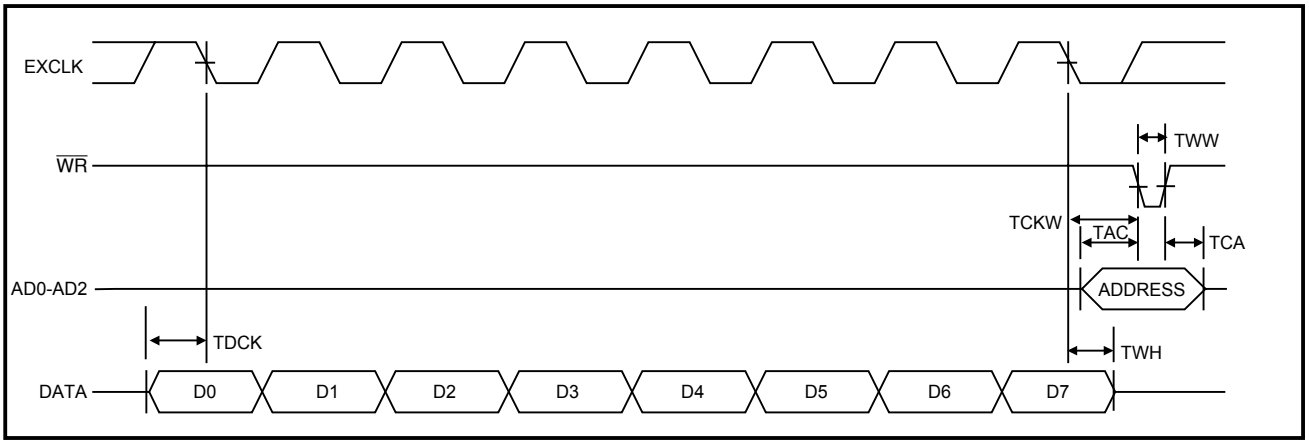


FIGURE 4: Write Timing Diagram (Serial Control Mode)

APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figure 5 shows the basic circuit diagram for a 73K224BL modem integrated circuit designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. A typical DAA arrangement is shown in Figure 5. This diagram is for reference only and does not represent a production-ready modem design.

The 73K224BL is available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 compatible microcontrollers from Intel or many other manufacturers. The serial interface mode can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

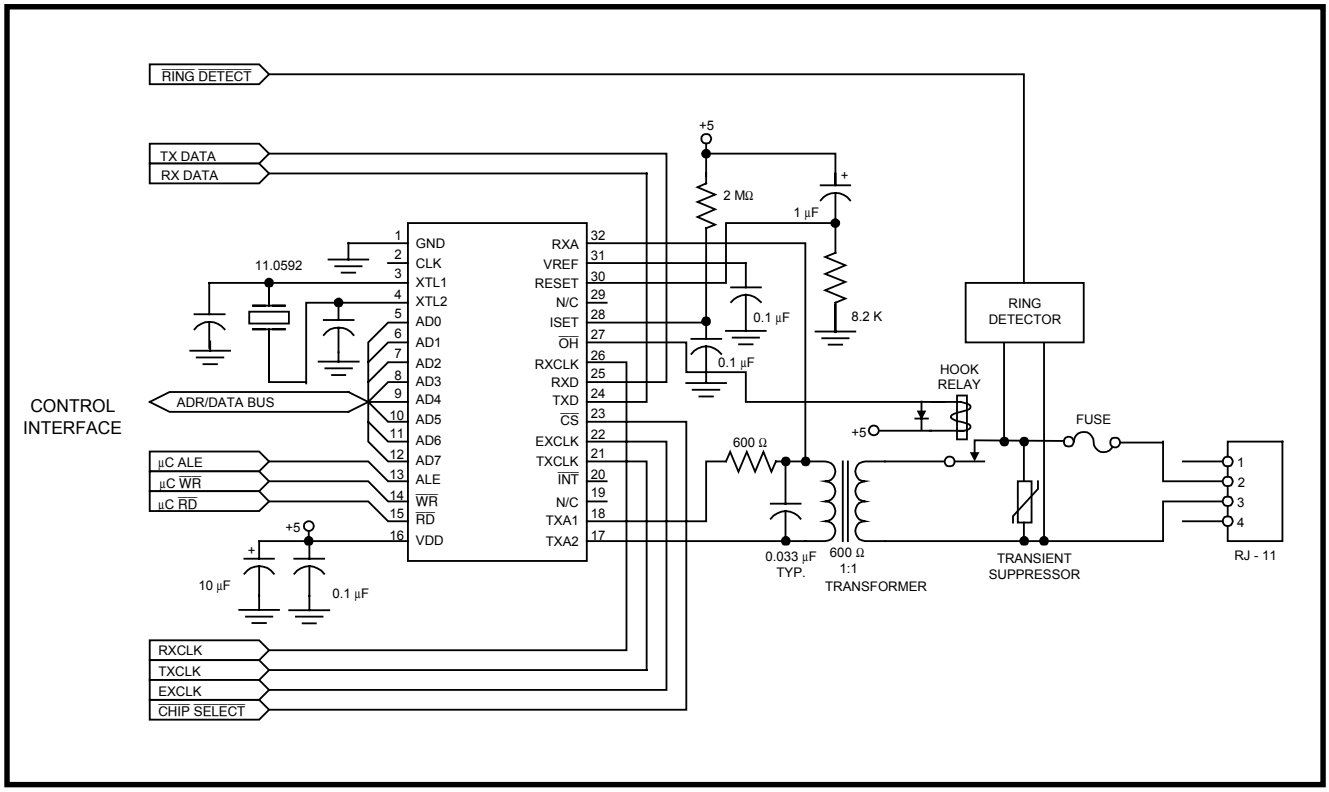


FIGURE 5: Typical 73K224BL DAA Circuit

APPLICATIONS INFORMATION (continued)

DIRECT ACCESS ARRANGEMENT (DAA)

The DAA (Direct Access Arrangement) required for the 73K224BL consists of an impedance matching resistor, telecom coupling transformer, and ring detection and fault protection circuitry.

The transformer specifications must comply with the impedance of the country in which the modem is being operated. Transformers designed specifically for use with the telephone network should be used. These may present a DC load to the network themselves (a “wet” transformer) or they may require AC coupling with a DC load provided by additional devices (a “dry” transformer). A dry transformer will generally provide higher performance and smaller size than a wet transformer. A wet transformer allows a simpler design, but must not saturate with the worst case DC current passing through it or distortion and poor performance will result.

The protection circuitry typically consists of a transient suppression device and current limiter to protect the user and the telephone network from hazardous voltages that can be present under fault conditions. The transient suppresser may be a MOV (metal oxide varistor), Sidactor® (Teccor Electronics Inc.), spark gap device, or avalanche diode. Some devices clamp the transient to their specified break down voltage and others go into low impedance crowbar state. The latter require that the fault current cease before they can return to their inactive state.

Current limiting devices can consist of a resistor, Raychem PolySwitch® resettable fuse, or slow blow fuse that can withstand the transient tests without permanent damage or replacement.

Ring detection circuitry is not required by the FCC, but may be required by the application. The ring detector usually consists of an optoisolator, capacitor, and resistor to present the proper AC load to the network to meet the REN (Ring Equivalency Number) regulations of FCC Part 68. The K-Series Design Manual contains detailed information on the design of a ring detect circuits as well as the other topics concerning the DAA.

DESIGN CONSIDERATIONS

Semiconductor's one-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (anti-resonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal’s characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high performance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located

close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem ICs should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

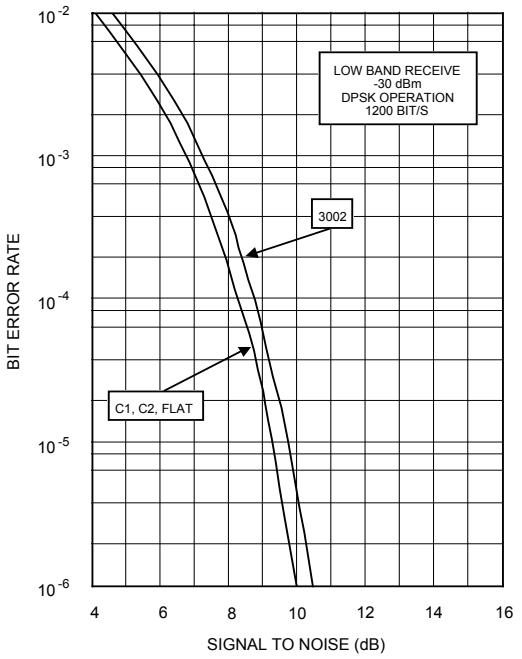
BER VS. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of operating conditions. Typically, a DPSK modem will exhibit better BER performance test curves receiving in the low band than in the high band.

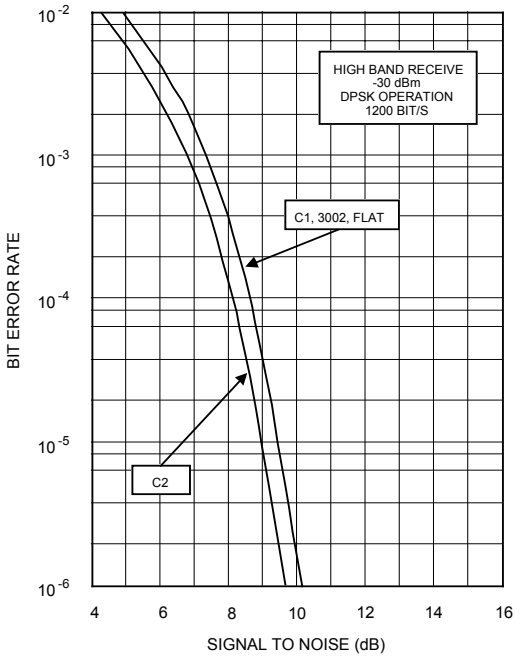
BER VS. RECEIVE LEVEL

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

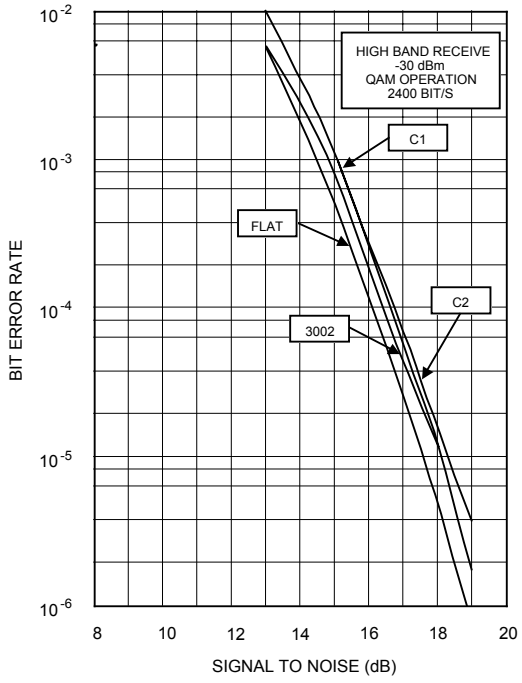
73K224BL BER vs S/N-DPSK LOW BAND



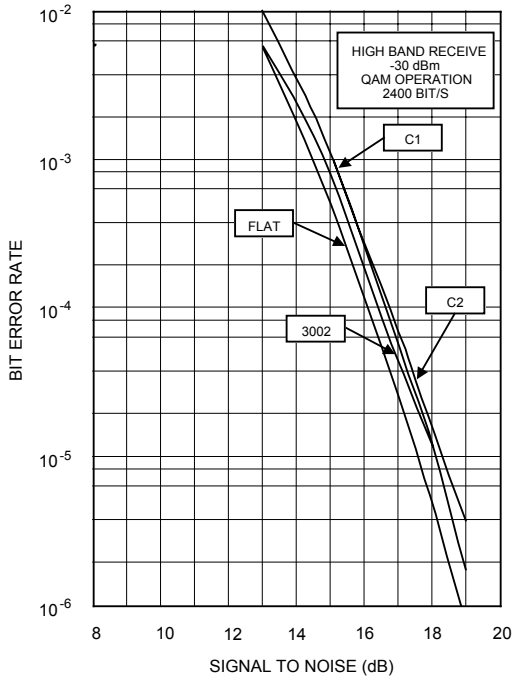
73K224BL BER vs S/N-DPSK HIGH BAND



73K224BL
BER VS S/N-QAM-LOW BAND

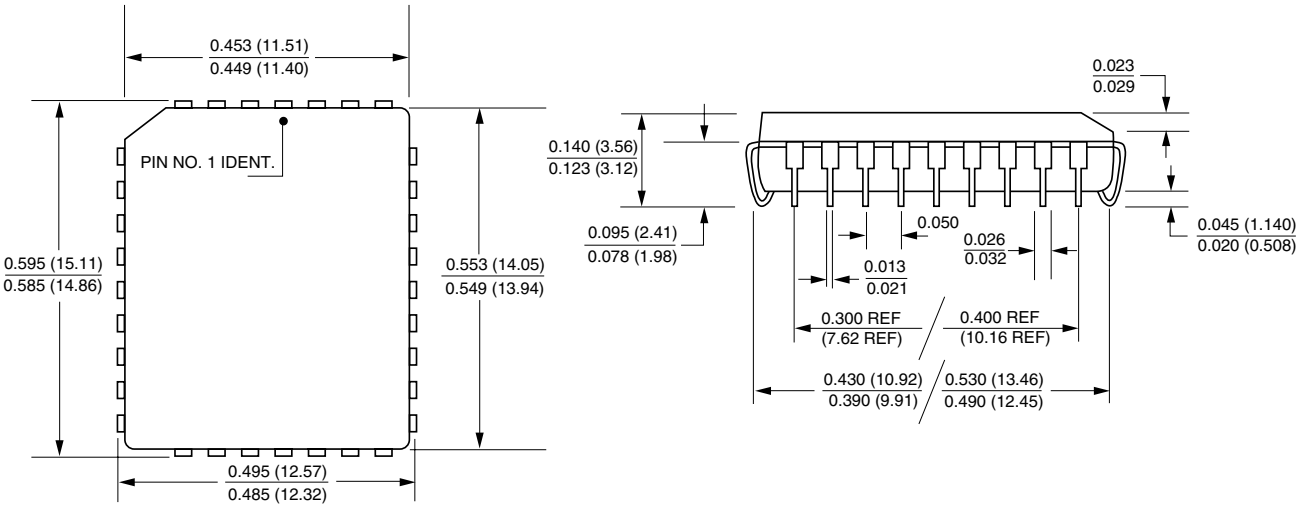


73K224BL
BER VS S/N-QAM-HIGH BAND



MECHANICAL SPECIFICATIONS

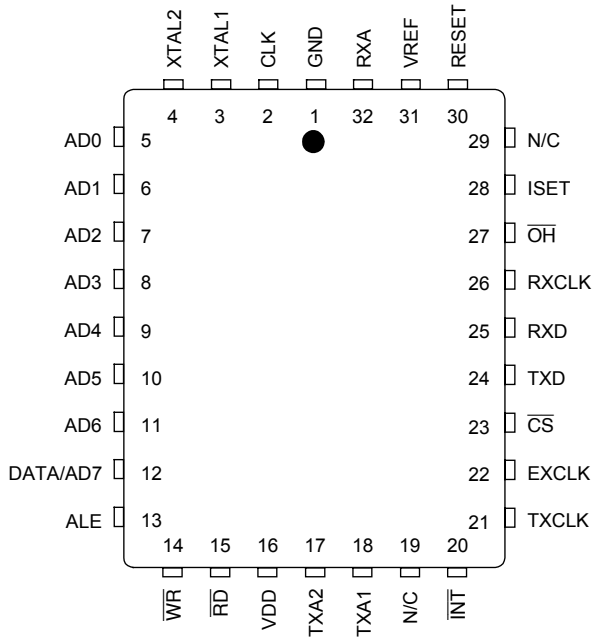
32-Lead PLCC



PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32-Lead PLCC
73K224BL-IH

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGING MARK
73K224BL	32-Lead PLCC	73K224BL-IH	73K224BL-IH

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