The Future of Analog IC Technology

## DESCRIPTION

The MPGC01 is a monolithic step-down switch mode converter with a built-in high-side power MOSFET and a gate driver for low-side external MOSFET. It achieves 8A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MPGC01 requires a minimum number of readily available standard external components and is available in a 8-pin SOIC package with exposed pad.

## FEATURES

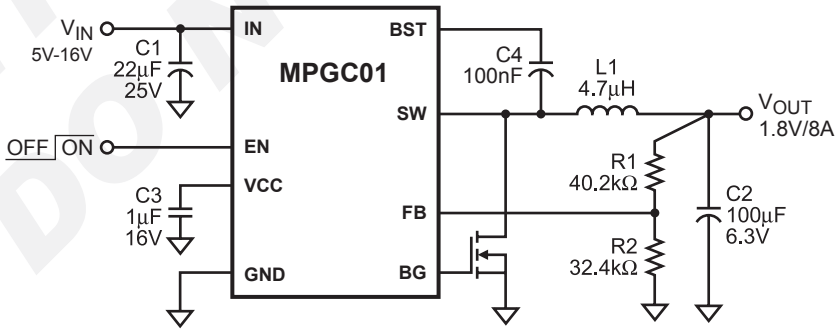
- Wide 5V to 16V Operating Input Range
- 8A Output Current
- 33mΩ Internal Power MOSFET Switch
- Synchronous Gate Driver Delivers up to 95% Efficiency
- Fixed 600KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Thermal Shutdown
- Output Adjustable from 0.8V to 5V
- Stable with Low ESR Output Ceramic Capacitors
- Available in a Thermally Enhanced 8-Pin SOIC Package

## APPLICATIONS

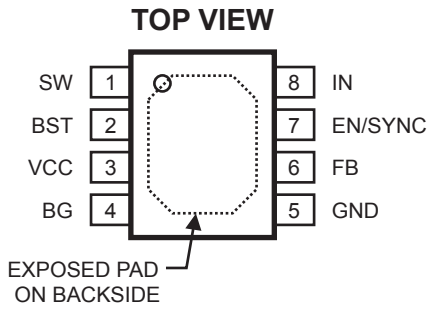
- Graphics Cards
- Distributed Power Systems
- DDR Memory
- Pre-Regulator for Linear Regulators



## TYPICAL APPLICATION



## PACKAGE REFERENCE




| Part Number* | Package | Temperature |
|---|---|---|
| MPGC01DN | SOIC8N | –40°C to +85°C |

* For Tape & Reel, add suffix –Z (eg. MPGC01DN–Z)
For RoHS Compliant Packaging, add suffix –LF
(eg. MPGC01DN–LF–Z)

## ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage $V_{IN}$ ..... 18V
$V_{SW}$ ..... –0.3V to $V_{IN}$ + 0.3V
$V_{BS}$ ..... $V_{SW}$ + 6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

### *Recommended Operating Conditions* (2)

Supply Voltage $V_{IN}$ ..... 5V to 16V
Output Voltage $V_{OUT}$ ..... 0.8V to 5V
Operating Temperature ..... –40°C to +85°C

### *Thermal Resistance* (3)

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| SOIC8N | 50 | 10 | °C/W |

**Notes:**
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $T_A$ = +25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Feedback Voltage | $V_{FB}$ | 5V ≤ $V_{IN}$ ≤ 16V | 0.790 | 0.810 | 0.830 | V |
| Feedback Current | $I_{FB}$ | $V_{FB}$ = 0.8V | | 10 | | nA |
| Switch On Resistance (4) | $R_{DS(ON)}$ | | | 33 | | mΩ |
| Switch Leakage | | $V_{EN}$ = 0V, $V_{SW}$ = 0V | | 0 | 50 | μA |
| Current Limit (4) | | | | 10 | | A |
| Oscillator Frequency | $f_{SW}$ | $V_{FB}$ = 0.6V | | 600 | | KHz |
| Fold-back Frequency | | $V_{FB}$ = 0V | | 150 | | KHz |
| Maximum Duty Cycle | | $V_{FB}$ = 0.6V | | 90 | | % |
| Minimum On Time | $t_{ON}$ | $V_{FB}$ = 1V | | 100 | | ns |
| Under Voltage Lockout Threshold Rising | | | 3.70 | 3.95 | 4.20 | V |
| Under Voltage Lockout Threshold Hysteresis | | | | 440 | | mV |
| EN Input Low Voltage | | | | | 0.4 | V |
| EN Input High Voltage | | | 1.2 | | | V |
| EN Input Current | | $V_{EN}$ = 2V | | 2 | | μA |
| | | $V_{EN}$ = 0V | | 0 | | |
| Supply Current (Shutdown) | | $V_{EN}$ = 0V | | 0 | | μA |
| Supply Current (Quiescent) | | $V_{EN}$ = 2V, $V_{FB}$ = 1V | | | 1.1 | mA |
| Thermal Shutdown | | | | 150 | | °C |
| Gate Driver Sink Impedance | $R_{SINK}$ | | | 1 | | Ω |
| Gate Driver Source Impedance | $R_{SOURCE}$ | | | 4 | | Ω |
| Gate Drive Current Sense Trip Threshold | | | | 20 | | mV |

**Note:**
4) Guaranteed by design.

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | SW | Switch Output. |
| 2 | BST | Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BS pins to form a floating supply across the power switch driver. A 0.1µF capacitor is recommended for use. |
| 3 | VCC | BG Driver Bias Supply. Decouple with a 1µF ceramic capacitor. |
| 4 | BG | Gate Driver Output. Connect this pin to the synchronous MOSFET. |
| 5 | GND | Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part. |
| 6 | FB | Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV. |
| 7 | EN | On/Off Control. |
| 8 | IN | Supply Voltage. The MPGC01 operates from a +5V to +16V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input. |

## OPERATION

The MPGC01 is a current mode buck regulator. That is, the Error Amplifier output voltage is proportional to the peak inductor current.

At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 600KHz CLK signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the Current Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and the MPGC01 reverts to its initial state (M1 off).

If the sum of the Current Sense Amplifier and the Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The EA output of the Error Amplifier integrates the voltage difference between the feedback and the 0.8V bandgap reference. The polarity is such that a FB pin voltage lower than 0.8V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage increases current delivered to the output.

An external synchronous MOSFET supplies the inductor current when M1 is off.

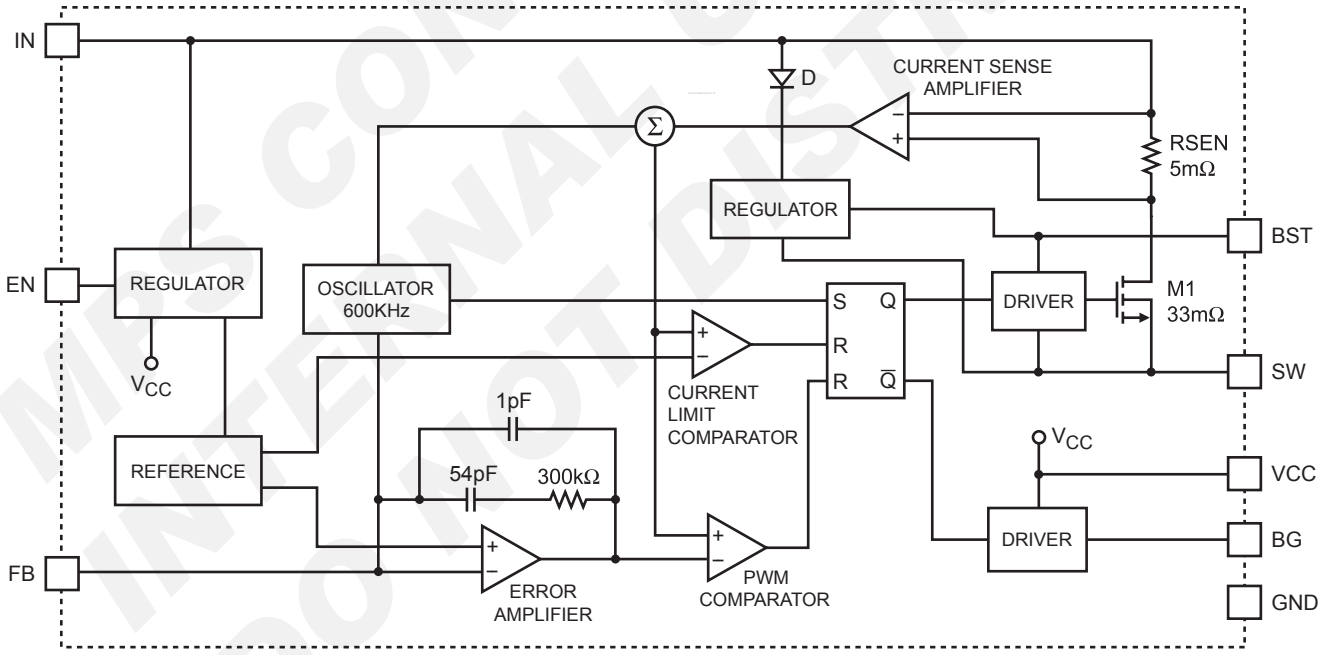



**Figure 1—Functional Block Diagram**

# APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

**Table 1—Resistor Selection for Common Output Voltages**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) |
|---|---|---|
| 1.8 | 40.2 (1%) | 32.4 (1%) |
| 2.5 | 40.2 (1%) | 19.1 (1%) |
| 3.3 | 40.2 (1%) | 13 (1%) |
| 5 | 40.2 (1%) | 7.68 (1%) |

### Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 10mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where $\Delta I_L$ is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current, 8A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

### Synchronous MOSFET

The external synchronous MOSFET is used to supply current to the inductor when the internal high-side switch is off. It significantly reduces the power loss when compared against a Schottky rectifier.

Table 2 lists example synchronous MOSFETs and manufacturers.

**Table 2—Diode Selection Guide**

| Part No. | Manufacture |
|---|---|
| FDS6670AS | Fairchild |
| IRF7821 | International Rectifier |

### Selecting the Input Capacitor

The input capacitor (C1) reduces the surge current drawn from the input and also the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from pass to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For 8A applications, a 22μF capacitor is sufficient.

### Selecting the Output Capacitor

The output capacitor (C2) keeps output voltage small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

### PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

**External Bootstrap Diode**

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.

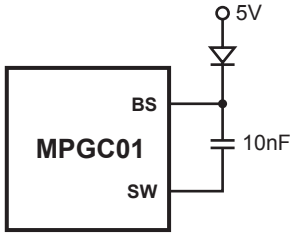
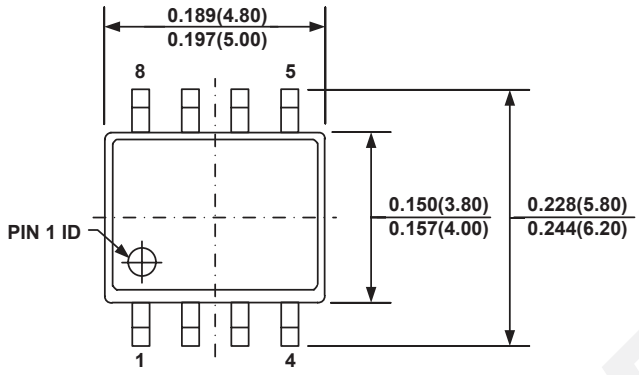



**Figure 2—External Bootstrap Diode**

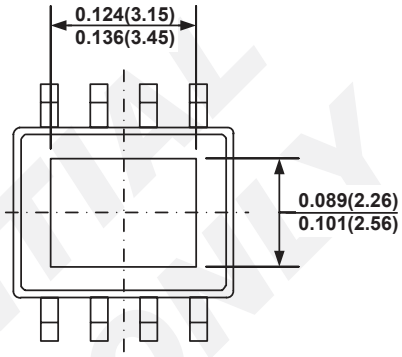
This diode is also recommended for high duty cycle operation (when $\frac{V_{OUT}}{V_{IN}}$>65%) and high output voltage ($V_{OUT}$>12V) applications.

# PACKAGE INFORMATION

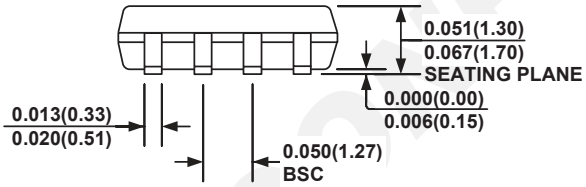
## SOIC8N (EXPOSED PAD)



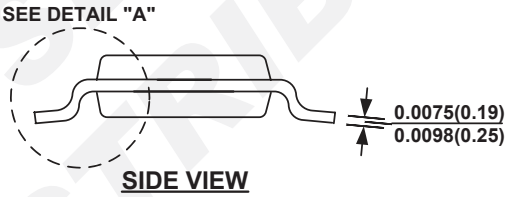

TOP VIEW



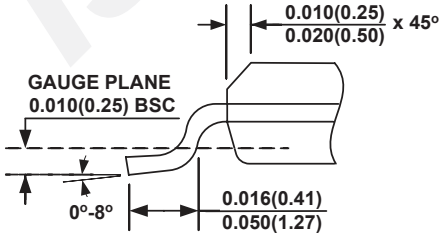

BOTTOM VIEW



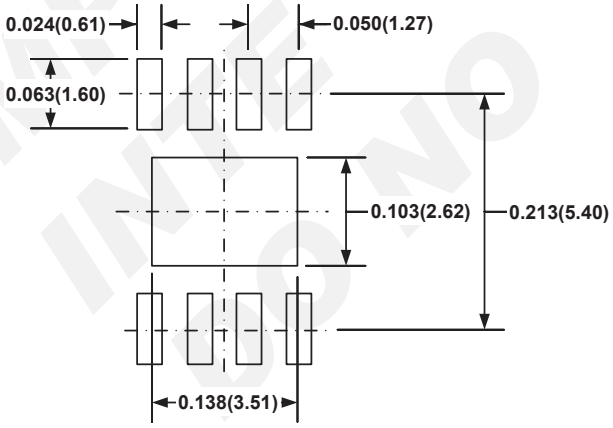

FRONT VIEW




SIDE VIEW




DETAIL "A"




RECOMMENDED LAND PATTERN

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.