

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μ PD78P078 is a member of the μ PD78078 Subseries of the 78K/0 Series, in which the on-chip mask ROM of the μ PD78078 is replaced with a one-time PROM or EPROM.

Because this device can be programmed by users, it is ideally suited for system evaluation, small-lot and multiple-device production, and early development and time-to-market.

The μ PD78P078 can be used for evaluation when a system using the μ PD78075B Subseries is developed.

- Cautions**
1. The μ PD78075B Subseries is different from the μ PD78078 Subseries in specification. To use the μ PD78P078 for evaluation of the μ PD78075B Subseries, refer to μ PD78075B, 78075BY Subseries User's Manual (planned).
 2. The μ PD78P078KL-T does not maintain planned reliability when used in your systems' mass-produced products. Please use only experimentally or for evaluation purposes during trial manufacture.

The details of functions are described in the user's manuals. Be sure to read the following manuals before designing.

μ PD78078, 78078Y Subseries User's Manual : U10641E
78K/0 Series User's Manual Instructions : U12326E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 60 Kbytes ^{Note 1}
 - μ PD78P078KL-T: Reprogrammable (ideally suited for system evaluation)
 - μ PD78P078GC, μ PD78P078GK: One-time programmable (ideally suited for small-lot production)
- Internal high-speed RAM: 1 024 bytes
- Internal expansion RAM: 1 024 bytes ^{Note 2}
- Internal buffer RAM: 32 bytes
- Operable in the same supply voltage as the mask ROM version ($V_{DD} = 1.8$ to 5.5 V)
- Corresponding to QTOP™ microcontrollers

- Notes**
1. The internal PROM capacity can be changed by setting the memory size switching register (IMS).
 2. The internal expansion RAM capacity can be changed by the internal expansion RAM size switching register (IXS).

- Remarks**
1. Refer to 1. DIFFERENCES BETWEEN μ PD78P078 AND MASK ROM VERSIONS for the differences between the PROM version and the mask ROM version.
 2. QTOP microcontroller is a general term for microcontrollers which incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening and verification).

In this document, the term PROM is used in parts common to one-time PROM versions and EPROM versions.

The information in this document is subject to change without notice.

ORDERING INFORMATION

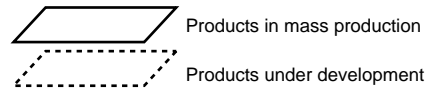
Part Number	Package	Internal ROM	Quality Grade
μ PD78P078GC-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)	One-Time PROM	Standard
★ μ PD78P078GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)	One-Time PROM	Standard
μ PD78P078GF-3BA	100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)	One-Time PROM	Standard
μ PD78P078KL-T	100-pin ceramic WQFN (14 × 20 mm)	EPROM	Not applicable

Caution The μ PD78P078GC comes in two types of packages (refer to 11. PACKAGE DRAWINGS). Please consult an NEC sales representative regarding available packages.

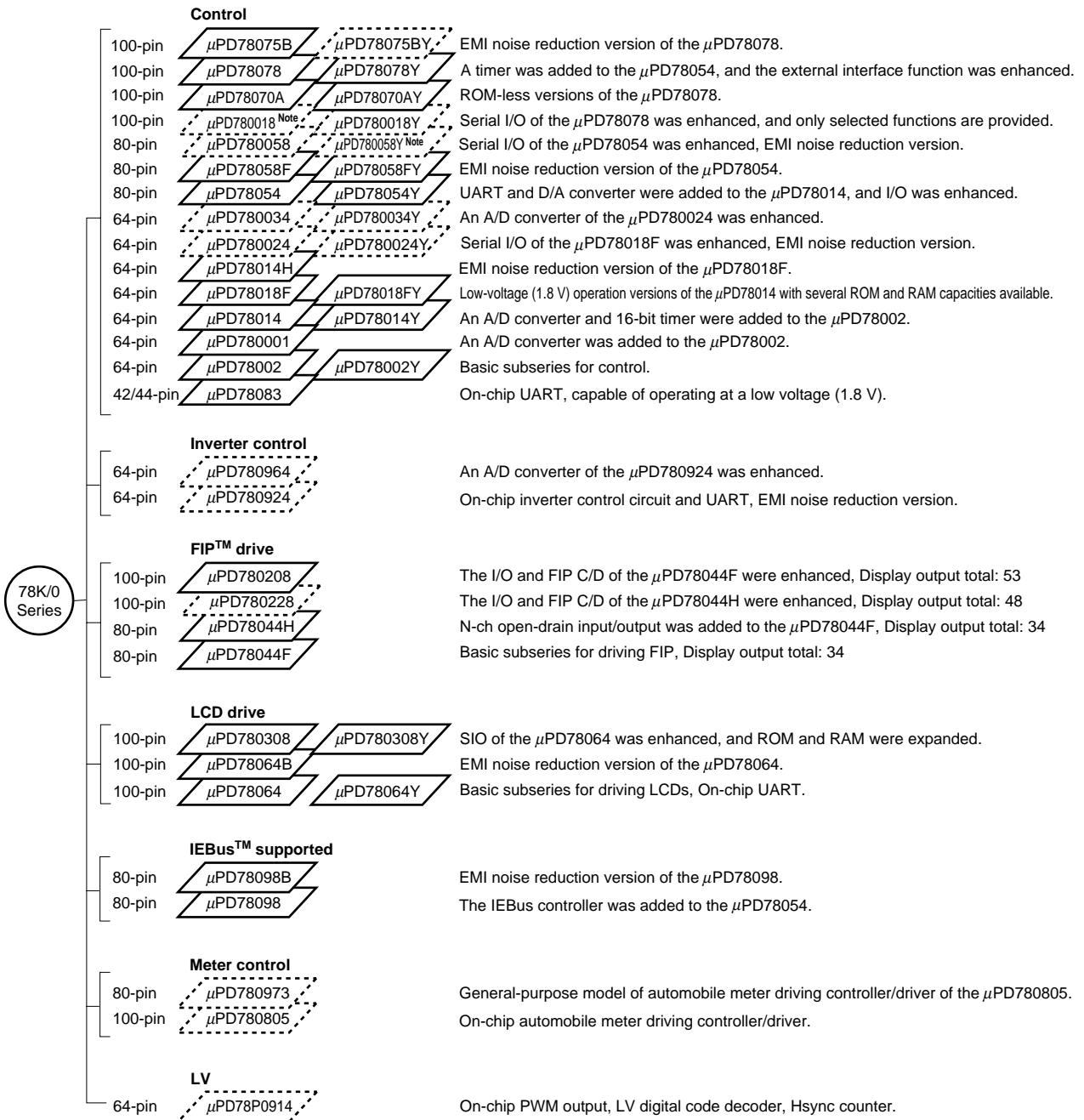
Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 Series Development

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



Y subseries products are compatible with I²C bus.



Note Under planning

The following table shows the differences among subseries functions.

Function Subseries Name		ROM Capacity	Timer				8-bit	10-bit	8-bit	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion				
			8-bit	16-bit	Watch	WDT	A/D	A/D	D/A								
Control	μPD78075B	32 K to 40 K	4ch	1ch	1ch	1ch	8ch	-	2ch	3ch (UART: 1ch)	88	1.8 V	Available				
	μPD78078	48 K to 60 K									61			2.7 V			
	μPD78070A	-									61			2.7 V			
	μPD780018	48 K to 60 K	2ch	-	-	-	-	-	-	2ch (time-division 3-wire: 1ch)	88	1.8 V	-				
	μPD780058	24 K to 60 K								3ch (time-division UART: 1ch)	68			1.8 V			
	μPD78058F	48 K to 60 K								3ch (UART: 1ch)	69			2.7 V			
	μPD78054	16 K to 60 K								2.0 V							
	μPD780034	8 K to 32 K								-	8ch			-	3ch (UART: 1ch, time-division 3-wire: 1ch)	51	1.8 V
	μPD780024									8ch	-				2ch	53	
	μPD78014H																
	μPD78018F	8 K to 60 K									2.7 V						
	μPD78014	8 K to 32 K															
	μPD780001	8 K		-	-					1ch	39		-				
	μPD78002	8 K to 16 K			1ch						53		Available				
μPD78083				-					8ch	8ch	1ch (UART: 1ch)	33	1.8 V	-			
Inverter control	μPD780964	8 K to 32 K	3ch	Note	-	1ch	-	8ch	-	2ch (UART: 2ch)	47	2.7 V	Available				
	μPD780924						8ch	-									
FIP drive	μPD780208	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	-	-	2ch	74	2.7 V	-				
	μPD780228	48 K to 60 K								3ch	-	-		1ch	72	4.5 V	
	μPD78044H	32 K to 48 K	2ch	1ch	1ch	-	-	-	-	68	2.7 V						
	μPD78044F	16 K to 40 K								2ch							
LCD drive	μPD780308	48 K to 60 K	2ch	1ch	1ch	1ch	8ch	-	-	3ch (time-division UART: 1ch)	57	2.0 V	-				
	μPD78064B	32 K								2ch (UART: 1ch)							
	μPD78064	16 K to 32 K															
IEBus supported	μPD78098B	40 K to 60 K	2ch	1ch	1ch	1ch	8ch	-	2ch	3ch (UART: 1ch)	69	2.7 V	Available				
	μPD78098	32 K to 60 K															
Meter control	μPD780973	24 K to 32 K	3ch	1ch	1ch	1ch	5ch	-	-	2ch (UART: 1ch)	56	4.5 V	-				
	μPD780805	40 K to 60 K					8ch				39	2.7 V					
LV	μPD78P0914	32 K	6ch	-	-	1ch	8ch	-	-	2ch	54	4.5 V	Available				

Note 10-bit timer: 1 channel

FUNCTION DESCRIPTION

Item	Function								
Internal memory	<ul style="list-style-type: none"> PROM: 60 Kbytes ^{Note 1} RAM <ul style="list-style-type: none"> High-speed RAM: 1 024 bytes Expansion RAM: 1 024 bytes ^{Note 2} Buffer RAM: 32 bytes 								
Memory space	64 Kbytes								
General register	8 bits × 32 registers (8 bits × 8 registers × 4 banks)								
Minimum instruction execution time	Minimum instruction execution time variable function is integrated.								
	<table border="1"> <tr> <td>When main system clock is selected</td> <td>0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz)</td> </tr> <tr> <td>When subsystem clock is selected</td> <td>122 μs (@ 32.768 kHz)</td> </tr> </table>	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz)	When subsystem clock is selected	122 μs (@ 32.768 kHz)				
When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz)								
When subsystem clock is selected	122 μs (@ 32.768 kHz)								
Instruction set	<ul style="list-style-type: none"> 16-bit operation Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) Bit manipulation (set, reset, test, Boolean operation) BCD adjust, etc. 								
I/O ports	<table border="1"> <tr> <td>Total</td> <td>: 88</td> </tr> <tr> <td>• CMOS input</td> <td>: 2</td> </tr> <tr> <td>• CMOS input/output</td> <td>: 78</td> </tr> <tr> <td>• N-ch open-drain input/output</td> <td>: 8</td> </tr> </table>	Total	: 88	• CMOS input	: 2	• CMOS input/output	: 78	• N-ch open-drain input/output	: 8
Total	: 88								
• CMOS input	: 2								
• CMOS input/output	: 78								
• N-ch open-drain input/output	: 8								
A/D converter	8-bit resolution × 8 channels								
D/A converter	8-bit resolution × 2 channels								
Serial interface	<ul style="list-style-type: none"> 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel 3-wire serial I/O mode (with max. 32-byte on-chip automatic transmit/receive function): 1 channel 3-wire serial I/O/UART mode selectable: 1 channel 								
Timer	<ul style="list-style-type: none"> 16-bit timer/event counter: 1 channel 8-bit timer/event counter: 4 channels Watch timer: 1 channel Watchdog timer: 1 channel 								
Timer output	5 pins (14-bit PWM output enable: 1 pin, 8-bit PWM output enable: 2 pins)								
Clock output	19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0 MHz with main system clock) 32.768 kHz (@ 32.768 kHz with subsystem clock)								
Buzzer output	1.2 kHz, 2.4 kHz, 4.9 kHz and 9.8 kHz (@ 5.0 MHz with main system clock)								

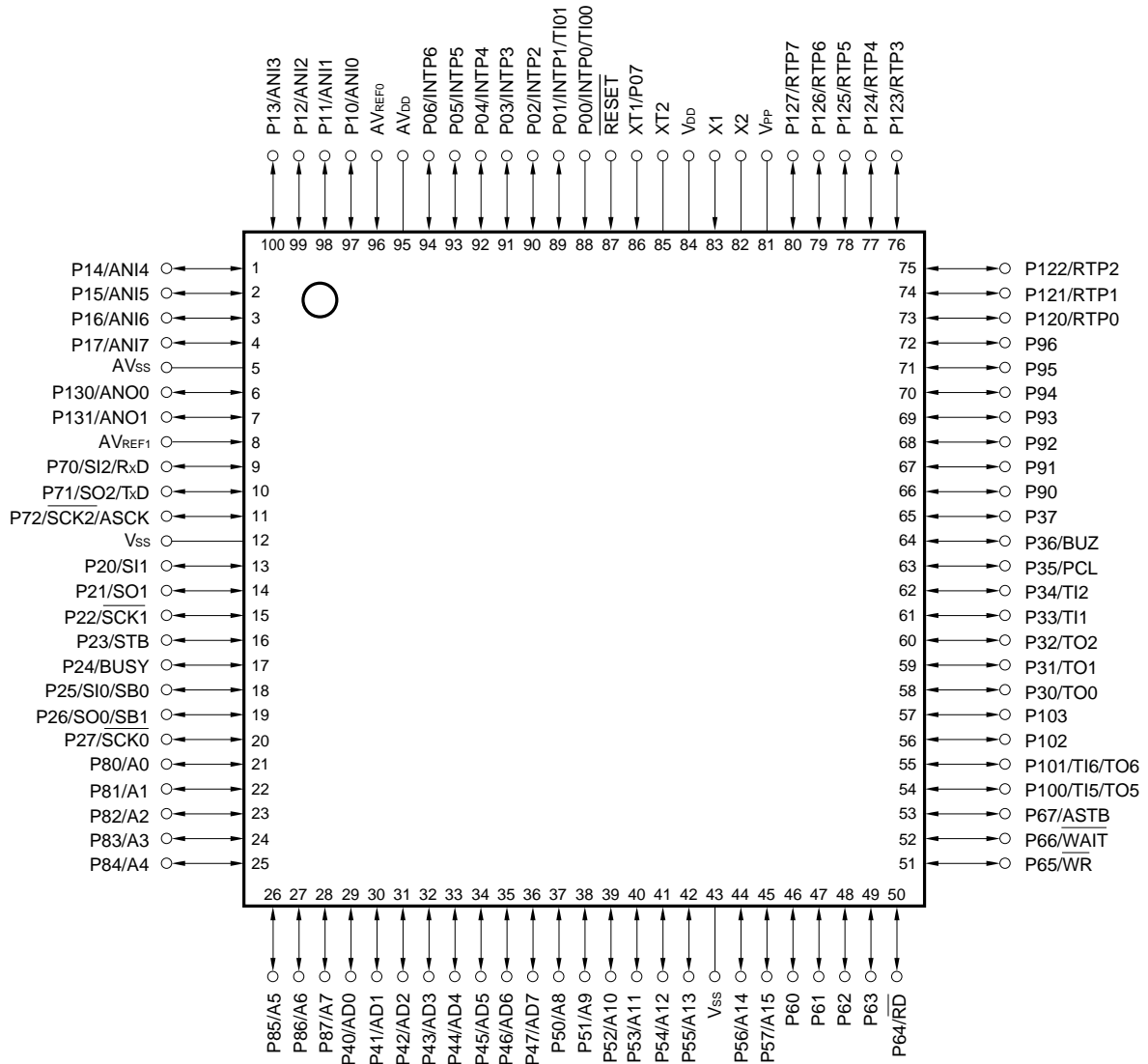
- Notes**
- Internal PROM capacity can be changed by memory size switching register (IMS).
 - Internal expansion RAM capacity can be changed by internal expansion RAM size switching register (IXS).

Item		Function
Vectored interrupt source	Maskable	Internal: 15, External: 7
	Non-maskable	Internal: 1
	Software	1
Test input		Internal: 1, External: 1
Supply voltage		V _{DD} = 1.8 to 5.5 V
★	Package	<ul style="list-style-type: none"> • 100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm) • 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm) • 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm) • 100-pin ceramic WQFN (14 × 20 mm)

PIN CONFIGURATIONS (Top View)

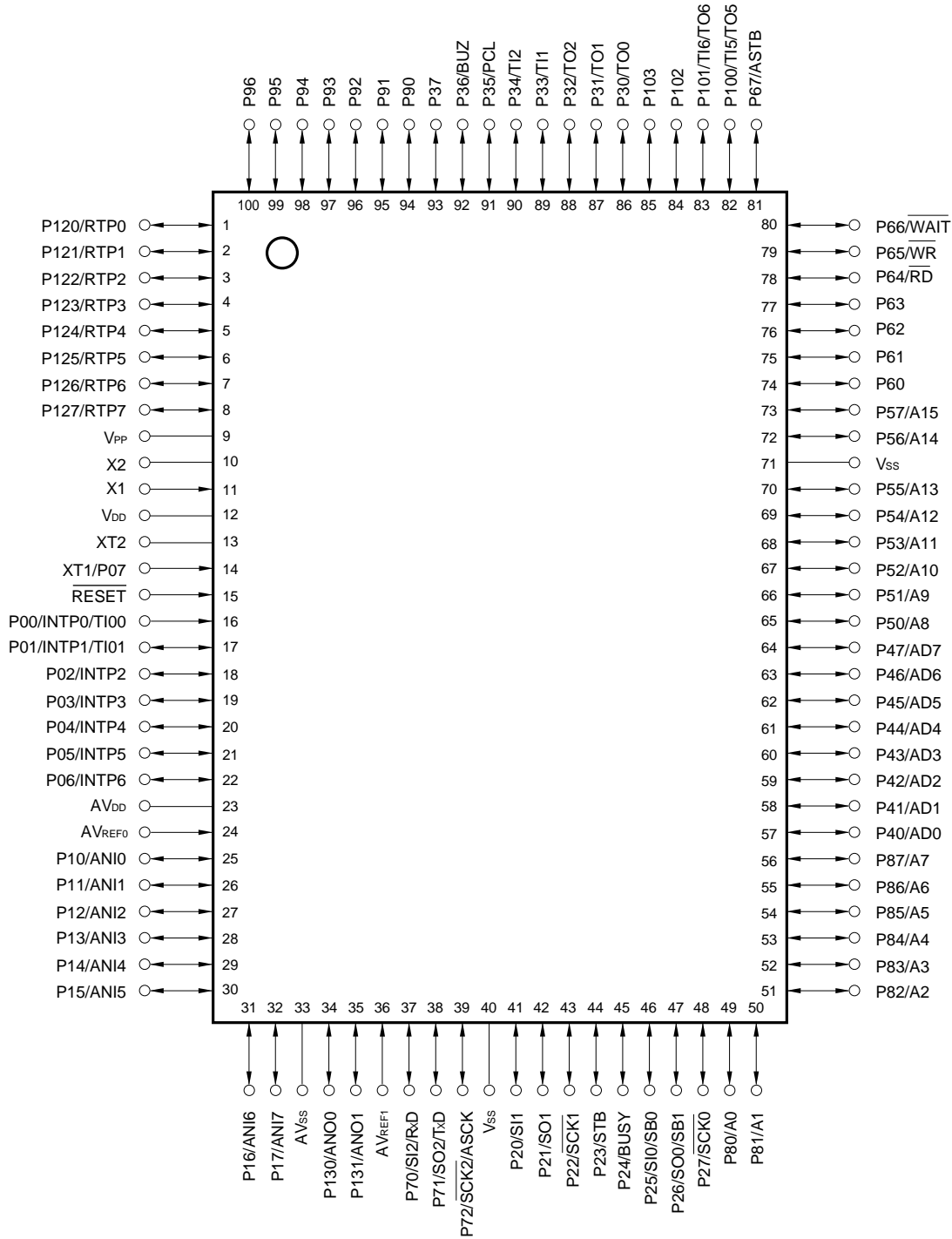
(1) Normal operating mode

- 100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)
μPD78P078GC-7EA
- ★ • 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
μPD78P078GC-8EU



- Cautions**
1. Connect V_{PP} pin directly to V_{SS}.
 2. Connect AV_{DD} pin to V_{DD}.
 3. Connect AV_{SS} pin to V_{SS}.

- 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)
μPD78P078GF-3BA
- 100-pin ceramic WQFN (14 × 20 mm)
μPD78P078KL-T

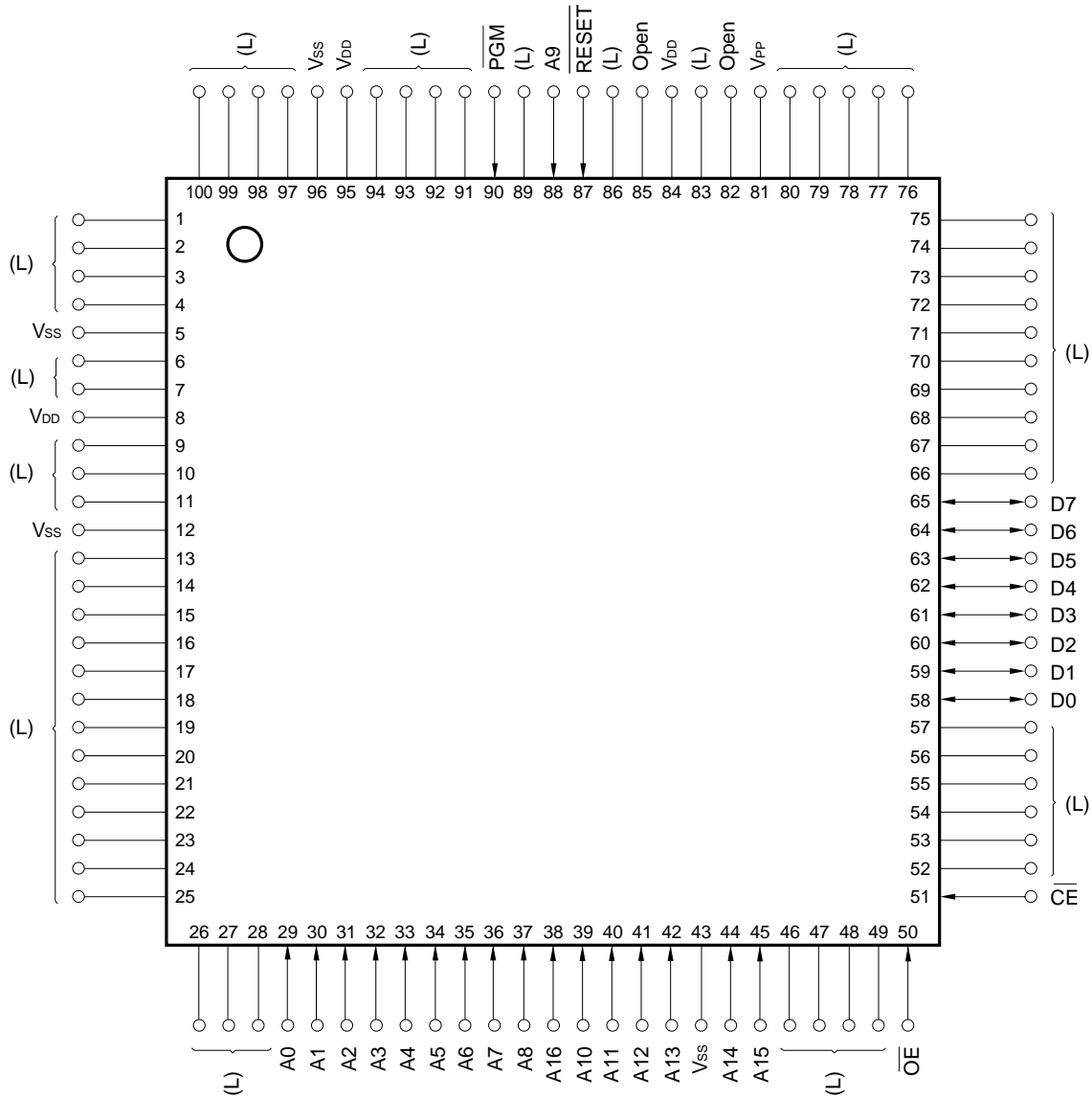


- Cautions**
1. Connect V_{PP} pin directly to V_{SS}.
 2. Connect AV_{DD} pin to V_{DD}.
 3. Connect AV_{SS} pin to V_{SS}.

A0 to A15	: Address Bus	P120 to P127	: Port12
AD0 to AD7	: Address/Data Bus	P130, P131	: Port13
ANI0 to ANI7	: Analog Input	PCL	: Programmable Clock
ANO0, ANO1	: Analog Output	\overline{RD}	: Read Strobe
ASCK	: Asynchronous Serial Clock	\overline{RESET}	: Reset
ASTB	: Address Strobe	RTP0 to RTP7	: Real-Time Output Port
AV _{DD}	: Analog Power Supply	RxD	: Receive Data
AV _{REF0} , AV _{REF1}	: Analog Reference Voltage	TxD	: Transmit Data
AV _{SS}	: Analog Ground	SB0, SB1	: Serial Bus
BUSY	: Busy	$\overline{SCK0}$ to $\overline{SCK2}$: Serial Clock
BUZ	: Buzzer Clock	SI0 to SI2	: Serial Input
INTP0 to INTP6	: Interrupt from Peripherals	SO0 to SO2	: Serial Output
P00 to P07	: Port0	STB	: Strobe
P10 to P17	: Port1	TI00, TI01	: Timer Input
P20 to P27	: Port2	TI1, TI2, TI5, TI6	: Timer Input
P30 to P37	: Port3	TO0 to TO2, TO5, TO6	: Timer Output
P40 to P47	: Port4	V _{DD}	: Power Supply
P50 to P57	: Port5	V _{PP}	: Programming Power Supply
P60 to P67	: Port6	V _{SS}	: Ground
P70 to P72	: Port7	\overline{WAIT}	: Wait
P80 to P87	: Port8	\overline{WR}	: Write Strobe
P90 to P96	: Port9	X1, X2	: Crystal (Main System Clock)
P100 to P103	: Port10	XT1, XT2	: Crystal (Subsystem Clock)

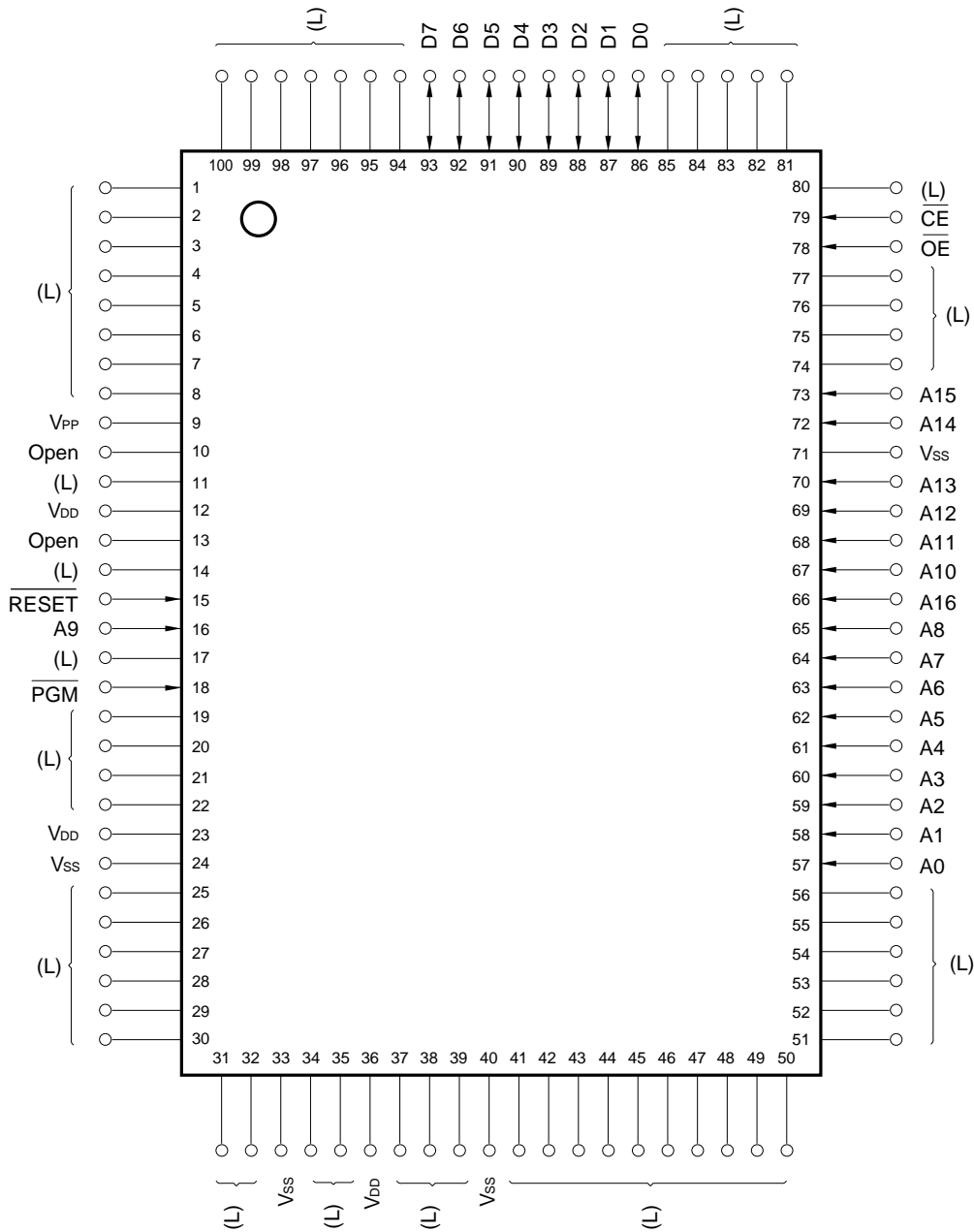
(2) PROM programming mode

- 100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)
μPD78P078GC-7EA
- ★ • 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
μPD78P078GC-8EU



- Cautions**
1. (L): Individually connect to Vss via a pull-down resistor.
 2. Vss: Connect to GND.
 3. RESET: Set to low level.
 4. Open: No connection.

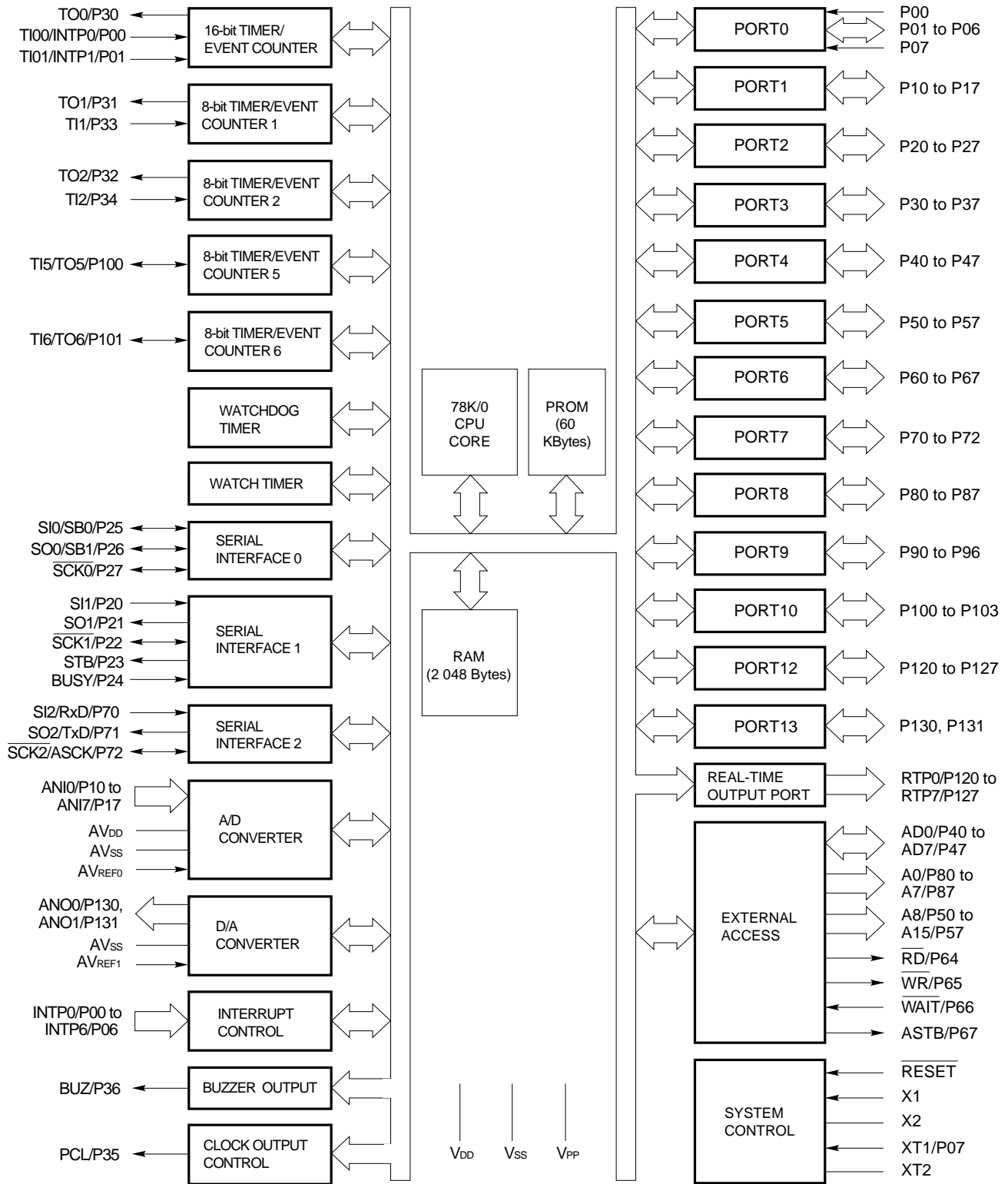
- 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)
μPD78P078GF-3BA
- 100-pin ceramic WQFN (14 × 20 mm)
μPD78P078KL-T



- Cautions**
1. (L): Individually connect to V_{SS} via a pull-down resistor.
 2. V_{SS}: Connect to GND.
 3. $\overline{\text{RESET}}$: Set to low level.
 4. Open: No connection.

A0 to A16	: Address Bus	$\overline{\text{RESET}}$: Reset
$\overline{\text{CE}}$: Chip Enable	V _{DD}	: Power Supply
D0 to D7	: Data Bus	V _{PP}	: Programming Power Supply
$\overline{\text{OE}}$: Output Enable	V _{SS}	: Ground
PGM	: Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μ PD78P078 AND MASK ROM VERSIONS	14
2. PIN FUNCTIONS	15
2.1 Pins in Normal Operating Mode	15
2.2 Pins in PROM Programming Mode	19
2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins	20
3. MEMORY SIZE SWITCHING REGISTER (IMS)	24
4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)	25
5. PROM PROGRAMMING	26
5.1 Operating Modes	26
5.2 PROM Write Procedure	28
5.3 PROM Read Procedure	32
6. PROGRAM ERASURE (μ PD78P078KL-T ONLY)	33
7. OPAQUE FILM ON ERASURE WINDOW (μ PD78P078KL-T ONLY)	33
8. ONE-TIME PROM VERSION SCREENING	33
9. ELECTRICAL SPECIFICATIONS	34
10. CHARACTERISTIC CURVES (REFERENCE VALUES)	68
11. PACKAGE DRAWINGS	70
12. RECOMMENDED SOLDERING CONDITIONS	74
APPENDIX A. DEVELOPMENT TOOLS	76
APPENDIX B. RELATED DOCUMENTS	81

1. DIFFERENCES BETWEEN μPD78P078 AND MASK ROM VERSIONS

The μPD78P078 is a single-chip microcontroller with an on-chip one-time PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

It is possible to make all the functions, except for PROM specification and mask option of P60 to P63 and P90 to P93 pins, the same as those of the mask ROM versions by setting the memory size switching register (IMS) and internal expansion RAM size switching register (IXS).

Differences between PROM version (μPD78P078) and mask ROM versions (μPD78074B, 78075B, 78076, 78078) are shown in Table 1-1.

★ **Table 1-1. Differences between μPD78P078 and Mask ROM Versions**

Parameter	μPD78P078	Mask ROM Versions
Internal ROM type	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	60 Kbytes	μPD78074B: 32 Kbytes μPD78075B: 40 Kbytes μPD78076: 48 Kbytes μPD78078: 60 Kbytes
Internal expansion RAM capacity	1 024 bytes	μPD78074B: none μPD78075B: none μPD78076: 1 024 bytes μPD78078: 1 024 bytes
Internal ROM capacity can be changed with memory size switching register	Changeable ^{Note 1}	Not changeable
Internal expansion RAM capacity can be changed with internal expansion RAM size switching register	Changeable ^{Note 2}	Not changeable
IC pin	No	Yes
V _{PP} pin	Yes	No
On-chip mask option pull-up resistor of P60 to P63 and P90 to P93 pins	Yes	No
Electrical specifications	Refer to the Data Sheet for each version.	

Notes 1. The internal PROM becomes 60 Kbytes and the internal high-speed RAM becomes 1 024 bytes by the $\overline{\text{RESET}}$ input.

2. The internal expansion RAM becomes 1 024 bytes by the $\overline{\text{RESET}}$ input.

★ **Caution** The PROM version and mask ROM version differ in noise tolerance and noise emission. When replacing a PROM version with a mask ROM version when switching from experimental production to mass production, make a thorough evaluation with a CS version (not ES version) of the mask ROM version.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins (1/3)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0 8-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 ^{Note 1}	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software. ^{Note 2}	Input	ANI0 to ANI7	
P20	Input/output	Port 2 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	SI1	
P21				SO1	
P22				SCK1	
P23				STB	
P24				BUSY	
P25				SI0/SB0	
P26				SO0/SB1	
P27				SCK0	
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	TO0	
P31				TO1	
P32				TO2	
P33				TI1	
P34				TI2	
P35				PCL	
P36				BUZ	
P37				—	

- Notes**
- When P07/XT1 pins are used as the input ports, set the processor clock control register (PCC) bit 6 (FRC) to 1 (Be sure not to use the feedback resistor of the subsystem clock oscillator).
 - When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for the A/D converter, the pull-up resistor is automatically disabled.

(1) Port pins (2/3)

Pin Name	Input/Output	Function		After Reset	Alternate Function	
P40 to P47	Input/output	Port 4 8-bit input/output port Input/output is specifiable in 8-bit units. When used as the input port, it is possible to connect an on-chip pull-up resistor by software. Set test input flag (KRIF) to 1 by falling edge detection.		Input	AD0 to AD7	
P50 to P57	Input/output	Port 5 8-bit input/output port It is possible to directly drive LEDs. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	A8 to A15	
P60	Input/output	Port 6	N-ch open-drain input/output port. It is possible to directly drive LEDs.	Input	—	
P61		8-bit input/output port Input/output is specifiable bit-wise.				
P62			When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	RD		
P63				WR		
P64				WAIT		
P65				ASTB		
P66						
P67						
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	SI2/RxD	
P71		SO2/TxD				
P72		SCK2/ASCK				
P80 to P87	Input/output	Port 8 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	A0 to A7	
P90	Input/output	Port 9	N-ch open-drain input/output port. It is possible to directly drive LEDs.	Input	—	
P91		7-bit input/output port Input/output is specifiable bit-wise.				
P92			When used as the input port, it is possible to connect an on-chip pull-up resistor by software.			
P93						
P94						
P95						
P96						

(1) Port pins (3/3)

Pin Name	Input/Output	Function	After Reset	Alternate Function
P100	Input/output	Port 10 4-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	T15/TO5
P101				T16/TO6
P102, P103				—
P120 to P127	Input/output	Port 12 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	ANO0, ANO1

(2) Non-port pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input/output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{\text{SCK0}}$	Input/output	Serial interface serial clock input/output.	Input	P27
$\overline{\text{SCK1}}$				P22
$\overline{\text{SCK2}}$				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/SCK2
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TI5		External count clock input to 8-bit timer (TM5).		P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO0		Output		16-bit timer output (TM0) (also used for 14-bit PWM output).
TO1	8-bit timer output (TM1).		P31	
TO2	8-bit timer output (TM2).		P32	
TO5	8-bit timer output (TM1) (also used for 8-bit PWM output).		P100/TI5	
TO6	8-bit timer output (TM2) (also used for 8-bit PWM output).		P101/TI6	
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120 to P127
AD0 to AD7	Input/output	Low-order address/data bus at external memory expansion.	Input	P40 to P47

(2) Non-port pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
A0 to A7	Output	Low-order address bus at external memory expansion.	Input	P80 to P87
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
RD	Output	External memory read operation strobe signal output.	Input	P64
WR		External memory write operation strobe signal output.	Input	P65
WAIT	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address data output for ports 4, 5 and 8 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AVREF0	Input	A/D converter reference voltage input.	—	—
AVREF1	Input	D/A converter reference voltage input.	—	—
AVDD	—	A/D converter analog power supply. Connected to V _{DD} .	—	—
AVSS	—	A/D converter ground potential. Connected to V _{SS} .	—	—
RESET	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V _{DD}	—	Positive power supply.	—	—
V _{PP}	—	High-voltage applied during program write/verification. Connected directly to V _{SS} in normal operating mode.	—	—
V _{SS}	—	Ground potential.	—	—

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
RESET	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the V _{PP} pin and a low level signal is applied to the RESET pin, this chip is set in the PROM programming mode.
V _{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification.
A0 to A16	Input	Address bus.
D0 to D7	Input/output	Data bus.
CE	Input	PROM enable input/program pulse input.
OE	Input	Read strobe input to PROM.
PGM	Input	Program/program inhibit input in PROM programming mode.
V _{DD}	—	Positive power supply.
V _{SS}	—	Ground potential.

2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, see Figure 2-1.

Table 2-1. Type of Input/Output Circuit of Each Pin (1/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to V _{SS} .
P01/INTP1/TI01	8-A	Input/output	Independently connect to V _{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V _{DD} .
P10/ANI0 to P17/ANI7	11	Input/output	Independently connect to V _{DD} or V _{SS} via a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/SCK1	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/SCK0			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7		5-E	Input/output
P50/A8 to P57/A15	5-A	Input/output	Independently connect to V _{DD} or V _{SS} via a resistor.
P60 to P63	13-D	Input/output	Independently connect to V _{DD} via a resistor.
P64/RD	5-A	Input/output	Independently connect to V _{DD} or V _{SS} via a resistor.
P65/WR			
P66/WAIT			
P67/ASTB			

Table 2-1. Type of Input/Output Circuit of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P70/SI2/RxD	8-A	Input/output	Independently connect to V _{DD} or V _{SS} via a resistor.
P71/SO2/TxD	5-A		
P72/SCK2/ASCK	8-A		
P80/A0 to P87/A7	5-A		
P90 to P93	13-D	Input/output	Independently connect to V _{DD} via a resistor.
P94 to P96	5-A	Input/output	Independently connect to V _{DD} or V _{SS} via a resistor.
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102, P103	5-A		
P120/RTP0 to P127/RTP7	5-A		
P130/ANO0, P131/ANO1	12-A	Input/output	Independently connect to V _{SS} via a resistor.
RESET	2	Input	—
XT2	16	—	Leave open.
AV _{REF0}	—		Connect to V _{SS} .
AV _{REF1}			Connect to V _{DD} .
AV _{DD}			
AV _{SS}			Connect to V _{SS} .
V _{PP}			Connect directly to V _{SS} .

Figure 2-1. List of Pin Input/Output Circuits (1/2)

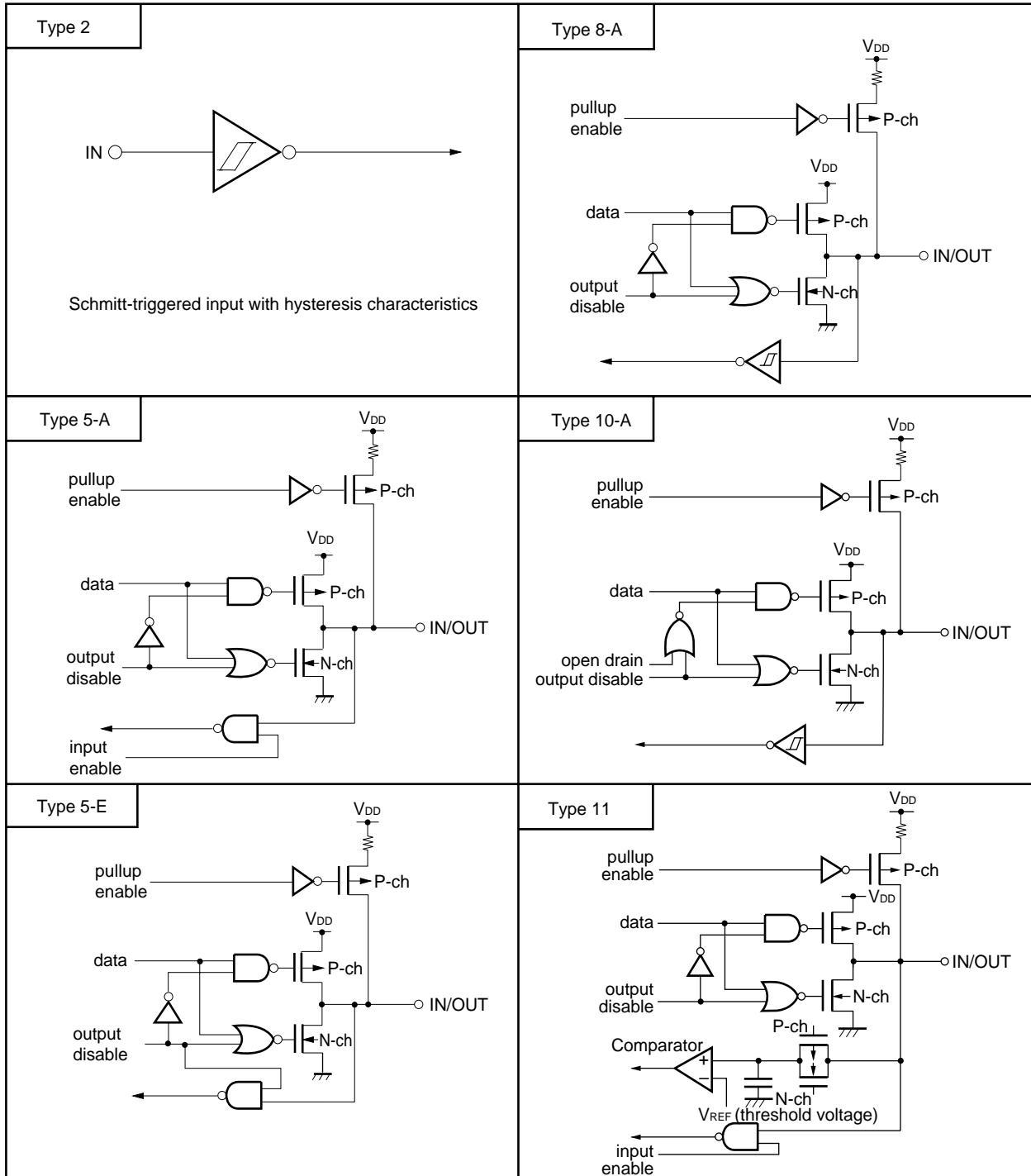
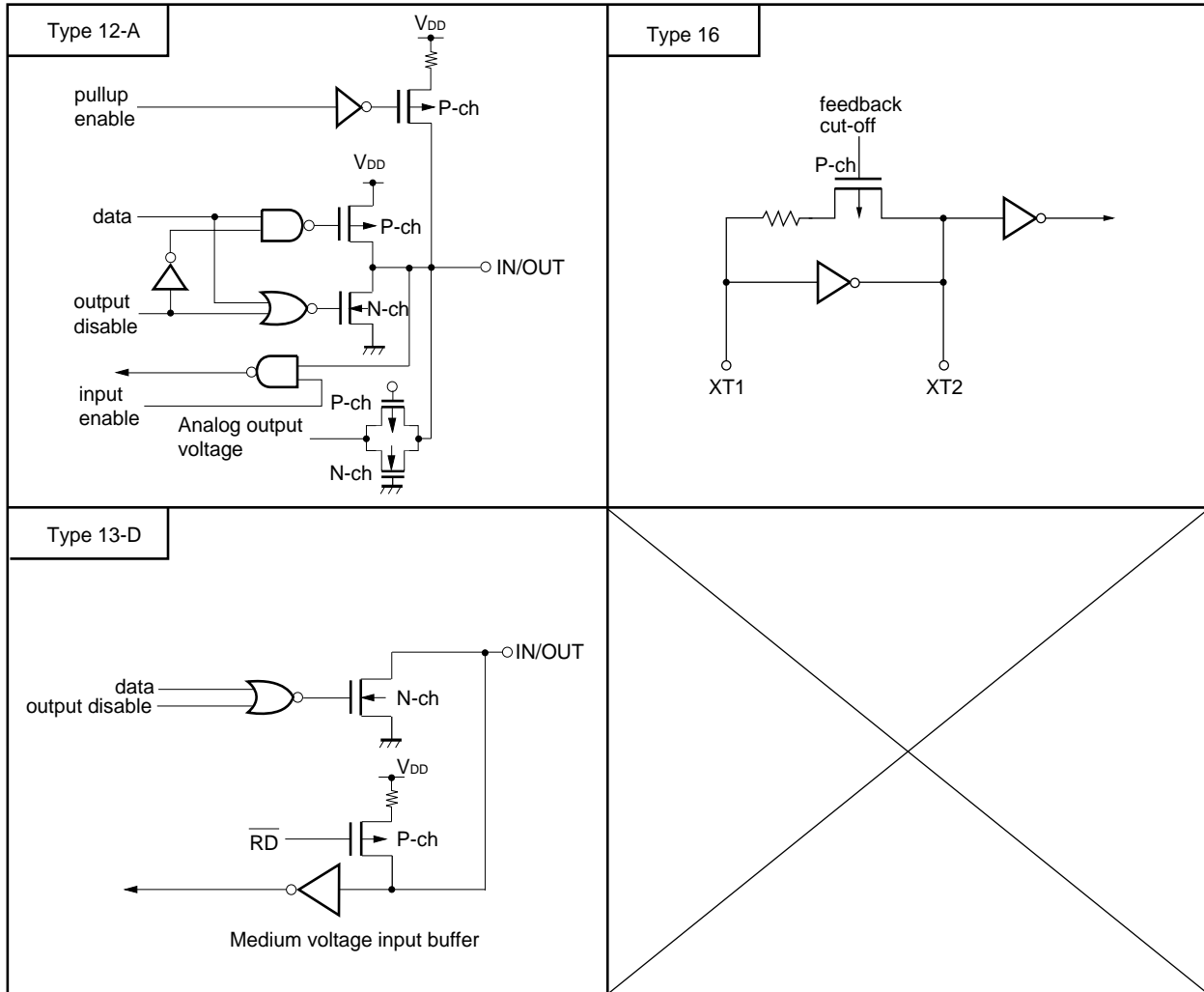


Figure 2-1. List of Pin Input/Output Circuits (2/2)



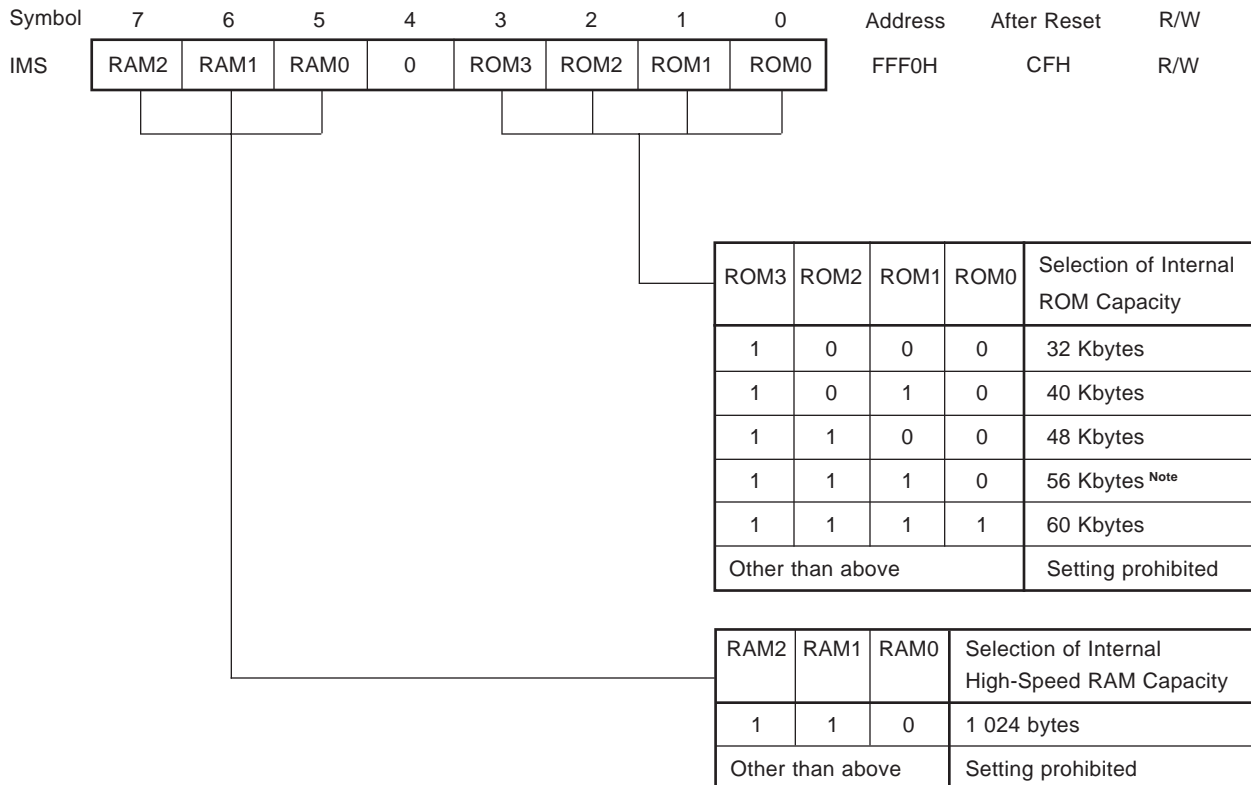
3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal memory (ROM).

IMS is set with an 8-bit memory manipulation instruction.

RESET input sets IMS to CFH.

Figure 3-1. Memory Size Switching Register Format



Note When the external device expansion function is used, internal ROM capacity should be set to 56 Kbytes or less.

Table 3-1 shows the setting values of IMS which make the memory mapping the same as that of the mask ROM version.

Table 3-1. Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting Value
μPD78074B	C8H
μPD78075B	CAH
μPD78076	CCH
μPD78078	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to set the internal expansion RAM capacity by software. By setting this internal expansion RAM size switching register (IXS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal expansion RAM.

IXS is set with an 8-bit memory manipulation instruction.

RESET input sets IXS to 0AH.

Figure 4-1. Internal Expansion RAM Size Switching Register Format

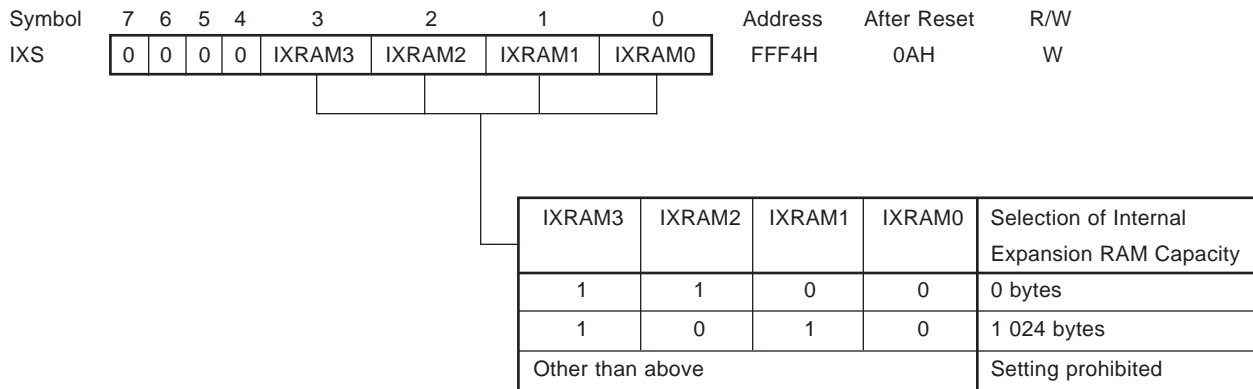


Table 4-1 shows the setting values of IXS which make the memory mapping the same as that of the mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Versions	IXS Setting Value
μPD78074B	0CH ^{Note}
μPD78075B	
μPD78076	0AH
μPD78078	

Note If a program for the μPD78P078 in which “MOV IXS, #0CH” is written is executed in the μPD78074B and μPD78075B, the operations are not affected.

5. PROM PROGRAMMING

The μPD78P078 has an on-chip 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode with the V_{PP} and \overline{RESET} pins. For the connection of unused pins, refer to “PIN CONFIGURATIONS (2) PROM programming mode.”

Caution Programs must be written in addresses 0000H to EFFFH (The last address EFFFH must be specified). They cannot be written by a PROM programmer which cannot specify the write address.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the \overline{RESET} pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the \overline{CE} , \overline{OE} and PGM pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin	\overline{RESET}	V_{PP}	V_{DD}	\overline{CE}	\overline{OE}	\overline{PGM}	D0 to D7
Operating Mode							
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read	+5 V	+5 V	L	L	H	Data output	
Output disable			L	H	×	High-impedance	
Standby			H	×	×	High-impedance	

× : L or H

(1) Read mode

Read mode is set if $\overline{CE} = L$, $\overline{OE} = L$ is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE} = H$ is set.

Therefore, it allows data to be read from any device by controlling the \overline{OE} pin, if multiple μ PD78P078s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE} = H$ is set.

In this mode, data outputs become high-impedance irrespective of the \overline{OE} status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE} = H$, $\overline{PGM} = H$, $\overline{OE} = L$ are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the \overline{PGM} pin with $\overline{CE} = H$, $\overline{OE} = H$. Then, program verification can be performed, if $\overline{CE} = L$, $\overline{OE} = L$ are set.

If programming is not performed by a one-time program pulse, X times ($X \leq 10$) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the \overline{PGM} pin with $\overline{CE} = L$, $\overline{OE} = H$. Then, program verification can be performed if $\overline{OE} = L$ is set.

If programming is not performed by a one-time program pulse, X times ($X \leq 10$) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE} = L$, $\overline{PGM} = H$, $\overline{OE} = L$ are set.

In this mode, check if a write operation is performed correctly after the write.

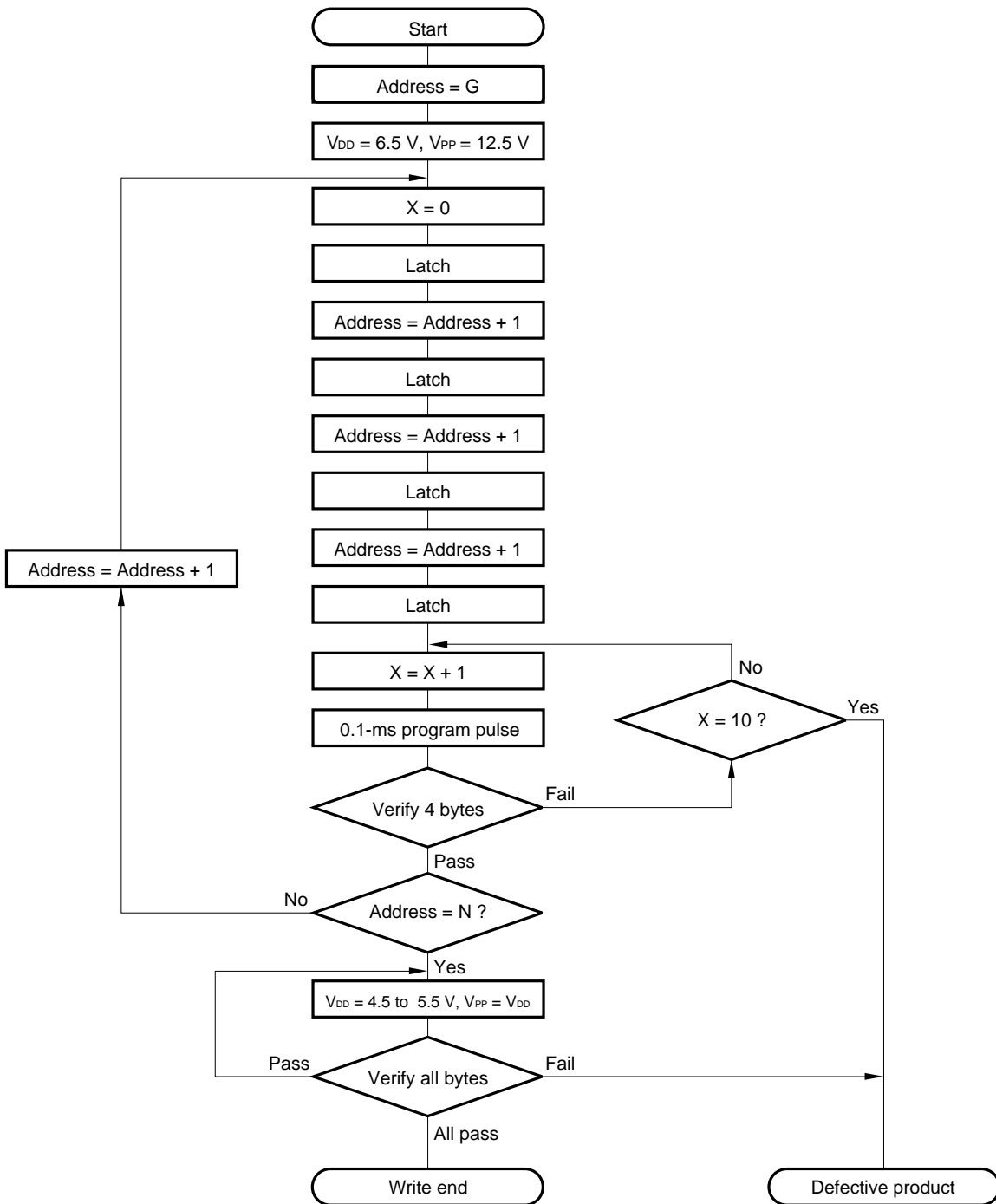
(8) Program inhibit mode

Program inhibit mode is used when the \overline{OE} pin, V_{PP} pin and D0 to D7 pins of multiple μ PD78P078s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the \overline{PGM} pin driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flow Chart



G = Start address
 N = Program last address

Figure 5-2. Page Program Mode Timing

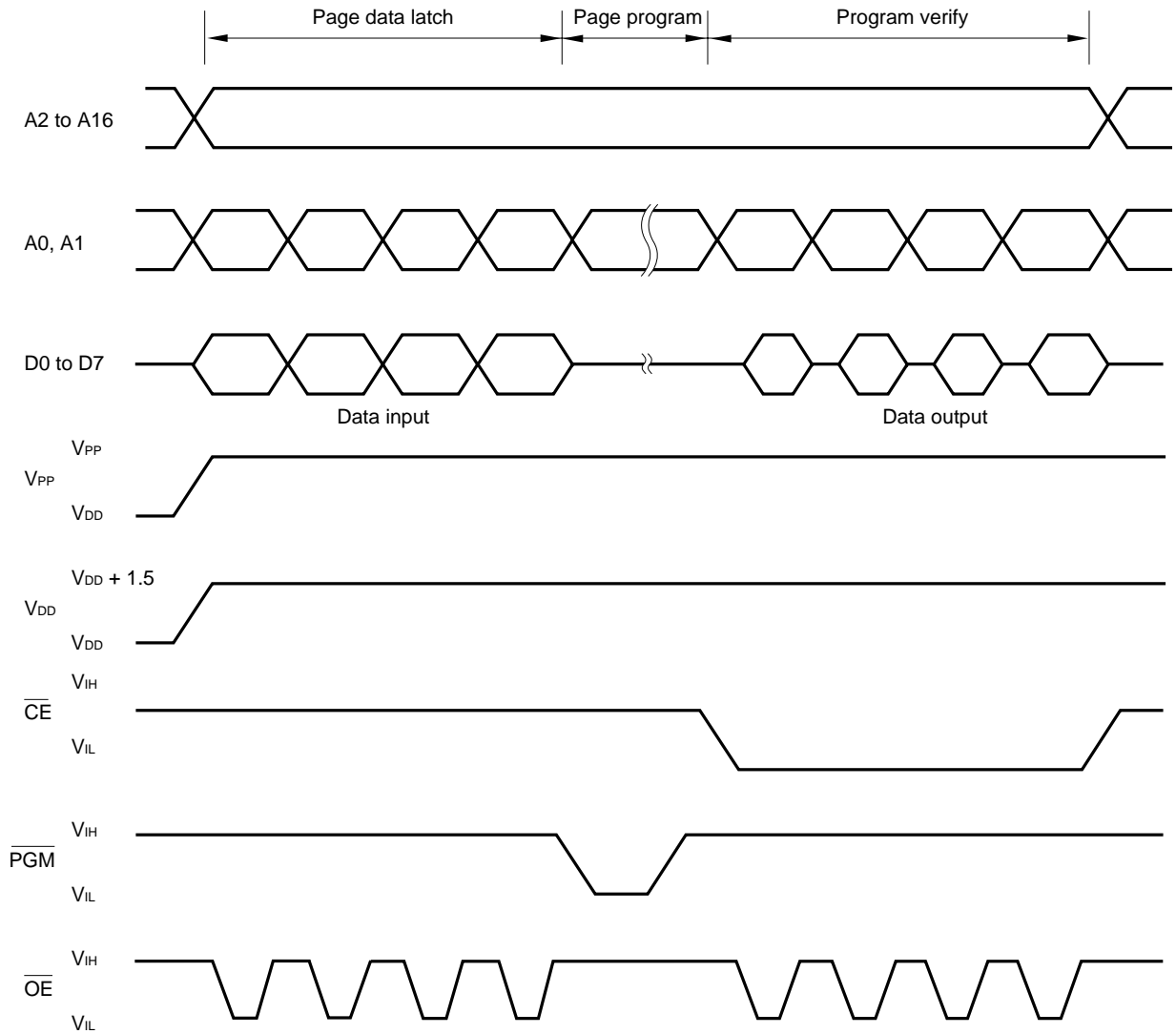
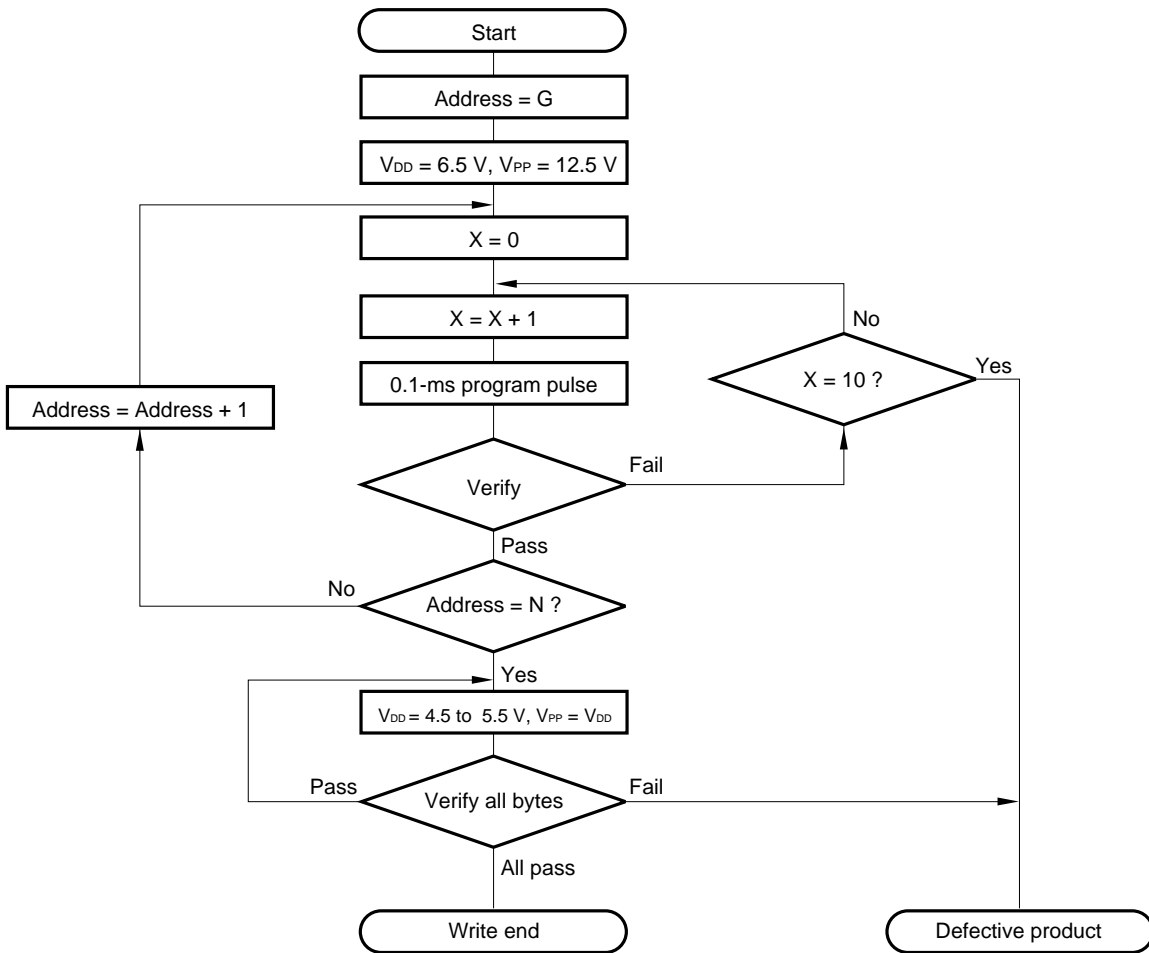
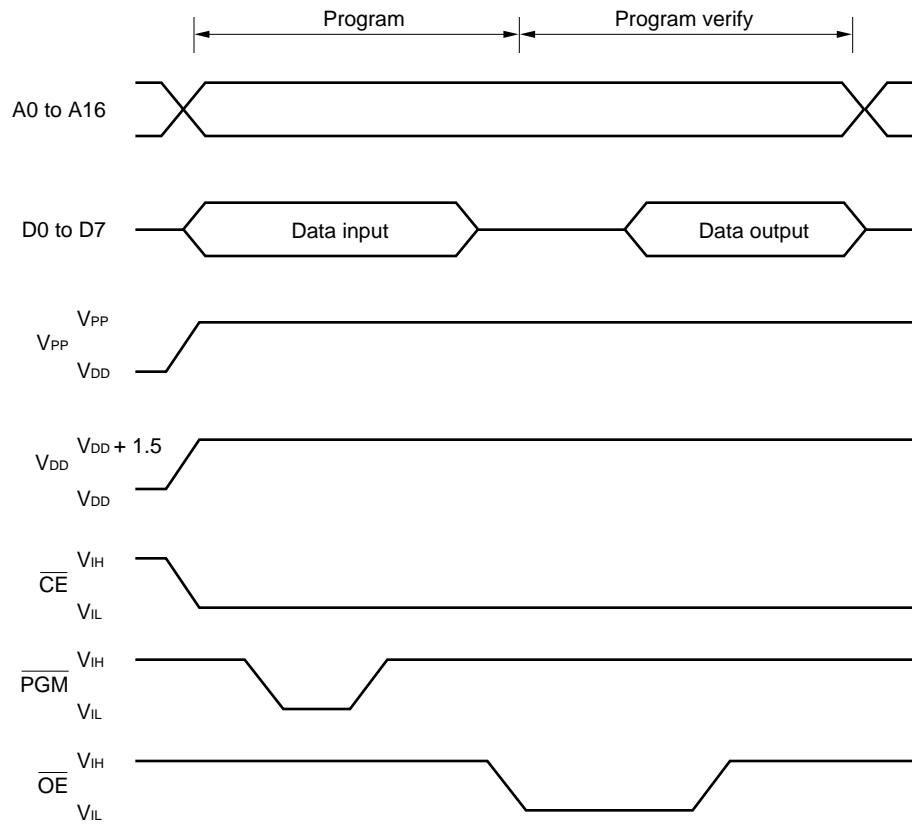


Figure 5-3. Byte Program Mode Flow Chart



G = Start address
 N = Program last address

Figure 5-4. Byte Program Mode Timing



- Cautions**
1. V_{DD} should be applied before V_{PP} and removed after V_{PP}.
 2. V_{PP} must not exceed +13.5 V including overshoot.
 3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

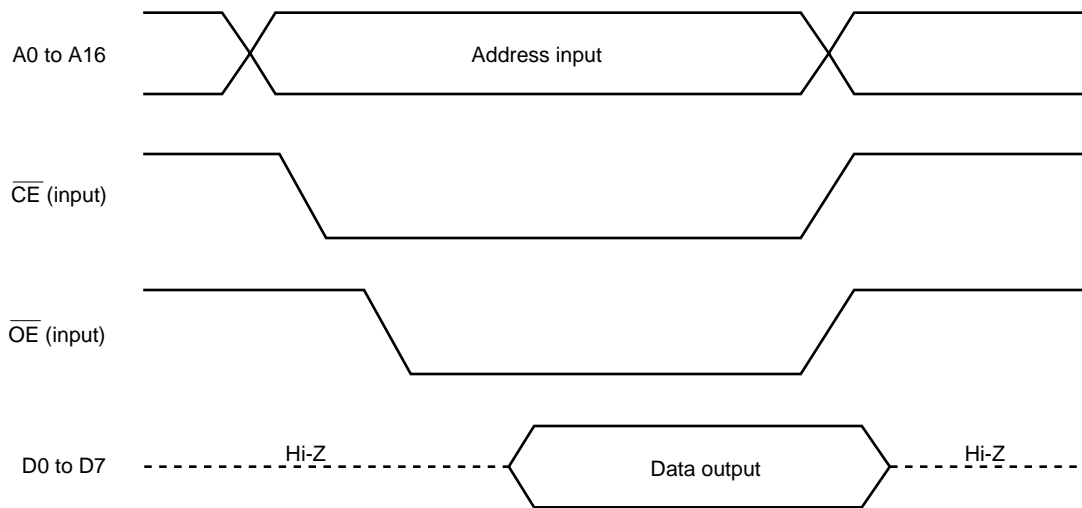
5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

- (1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in “PIN CONFIGURATIONS (2) PROM programming mode”.
- (2) Supply +5 V to the V_{DD} and V_{PP} pins.
- (3) Input address of read data into the A0 to A16 pins.
- (4) Read mode
- (5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

Figure 5-5. PROM Read Timings



6. PROGRAM ERASURE (μPD78P078KL-T ONLY)

The μPD78P078KL-T is capable of erasing (FFH) the data written in a program memory and rewriting.

To erase the programmed data, expose the erasure window to light having a wavelength shorter than about 400 nm. Normally, irradiate ultraviolet rays of 254-nm wavelength. The amount of exposure required to completely erase the programmed data is as follows:

- UV intensity × erasing time: 30 W•s/cm² or more
- Erasure time: 40 min. or more (When a UV lamp of 12 000 μW/cm² is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, soiled erasure window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasure window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

7. OPAQUE FILM ON ERASURE WINDOW (μPD78P078KL-T ONLY)

To protect from unintentional erasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, cover the erasure window with an opaque film when EPROM contents erasure is not performed.

8. ONE-TIME PROM VERSION SCREENING

The one-time PROM version (μPD78P078GC-7EA, 78P078GC-8EU, and 78P078GF-3BA) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125 °C	24 hours

NEC offers for an additional fee one-time PROM writing to marking, screening, and verify for products designated as “QTOP microcontroller”. Please contact an NEC sales representative for details.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V _{DD}			-0.3 to +7.0	V
	V _{PP}			-0.3 to +13.5	V
	AV _{DD}			-0.3 to V _{DD} + 0.3	V
	AV _{REF0}			-0.3 to V _{DD} + 0.3	V
	AV _{REF1}			-0.3 to V _{DD} + 0.3	V
Input voltage	AV _{SS}			-0.3 to +0.3	V
	V _{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		-0.3 to V _{DD} + 0.3	V
	V _{I2}	P60 to P63, P90 to 93	N-ch open-drain	-0.3 to +16	V
	V _{I3}	A9	PROM programming mode	-0.3 to +13.5	V
Output voltage	V _O			-0.3 to V _{DD} + 0.3	V
Analog input voltage	V _{AN}	P10 to P17	Analog input pins	AV _{SS} - 0.3 to AV _{REF0} + 0.3	V
Output current, high	I _{OH}	Per pin		-10	mA
		Total for P30 to P37, P56, P57, P60 to P67, P90 to P96, P100 to P103, P120 to P127		-15	mA
		Total for P01 to P06, P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P80 to P87, P130, P131		-15	mA
Output current, low	I _{OL} ^{Note}	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for P50 to P55	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P30 to P37, P64 to P67, P90 to P96, P100 to P103, P120 to P127	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P20 to P27, P40 to P47, P80 to P87	Peak value	50	mA
			r.m.s. value	20	mA
Total for P01 to P06, P10 to P17, P70 to P72, P130, P131	Peak value	50	mA		
	r.m.s. value	20	mA		
Operating ambient temperature	T _A			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × √Duty

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

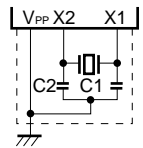
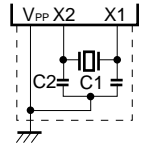
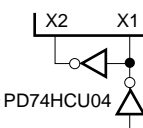
Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C _{IO}	f = 1 MHz, Unmeasured pins returned to 0 V.			15	pF
		P01 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131 P60 to P63, P90 to P93			20	

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}	V _{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	After V _{DD} reaches MIN. value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 4.5 to 5.5 V			10 30	ms
External clock		X1 input frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})		85		500	ns

- Notes 1.** Only the oscillator characteristics are shown. For the instruction execution time, refer to AC Characteristics.
2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Cautions 1. When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- Keep the wiring length as short as possible.
 - Do not cross the wiring over other signal lines.
 - Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
 - Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.
 - Do not connect the ground pattern through which a high current flows.
 - Do not extract signals from the oscillation circuit.
- 2.** When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f _{XT}) ^{Note 1}		32	32.768	35	kHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 4.5 to 5.5 V		1.2	2	s
External clock		XT1 input frequency (f _{XT}) ^{Note 1}		32		100	kHz
		XT1 input high-/low-level width (t _{XTH} , t _{XTL})		5		15	μs

- Notes**
1. Only the oscillator characteristics are shown. For the instruction execution time, refer to AC Characteristics.
 2. Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

Cautions 1. When using the oscillation circuit of the subsystem clock, wire the portion enclosed in broken lines in the figure as follows to avoid adverse influences on the wiring capacitance:

- Keep the wiring length as short as possible.
 - Do not cross the wiring over other signal lines.
 - Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
 - Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.
 - Do not connect the ground pattern through which a high current flows.
 - Do not extract signals from the oscillation circuit.
2. The amplification factor of the subsystem clock oscillator is designed to be low to reduce the current consumption and therefore, the subsystem clock oscillator is influenced by noise more easily than the main system clock oscillator. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

Recommended Oscillator Constant

Main System Clock: Ceramic Resonator (T_A = -40 to +85 °C)

Manufacturer	Part Number	Frequency	Recommended Circuit Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
TDK	CCR1000K2	1.00 MHz	150	150	0	2.0	5.5	On-chip capacitor
	CCR2.0MC3	2.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor surface mount type
	CCR4.0MC3	4.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor surface mount type
	FCR4.0MC5	4.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor insertion type
Murata Mfg. Co., Ltd.	CSB1000J	1.00 MHz	100	100	5.6	1.8	5.5	Insertion type
	CSA2.00MG040	2.00 MHz	100	100	0	1.8	5.5	Insertion type
	CST2.00MG040	2.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type
	CSA4.00MG	4.00 MHz	30	30	0	1.8	5.5	Insertion type
	CST4.00MGW	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type
	CSA4.00MGU	4.00 MHz	30	30	0	1.8	5.5	Insertion type
	CST4.00MGWU	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type

Main System Clock: Ceramic Resonator (T_A = -20 to +80 °C)

Manufacturer	Part Number	Frequency	Recommended Circuit Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Kyocera Corporation	KFR-1000F	1.00 MHz	220	220	0	1.8	5.5	Insertion type
	PBR-1000Y	1.00 MHz	220	220	0	1.8	5.5	Surface mount type
	KBR-2.0MS	2.00 MHz	82	82	0	1.8	5.5	Insertion type
	KBR-4.0MKC	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type
	KBR-4.0MSB	4.00 MHz	33	33	0	1.8	5.5	Insertion type
	PBRC4.00B	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor surface mount type
	PBRC4.00A	4.00 MHz	33	33	0	1.8	5.5	Surface mount type

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V _{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V _{DD} = 2.7 to 5.5 V	0.7 V _{DD}		V _{DD}	V
				0.8 V _{DD}		V _{DD}	V
	V _{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, RESET	V _{DD} = 2.7 to 5.5 V	0.8 V _{DD}		V _{DD}	V
				0.85 V _{DD}		V _{DD}	V
	V _{IH3}	P60 to P63, P90 to P93 (N-ch open-drain)	V _{DD} = 2.7 to 5.5 V	0.7 V _{DD}		15	V
				0.8 V _{DD}		15	V
	V _{IH4}	X1, X2	V _{DD} = 2.7 to 5.5 V	V _{DD} - 0.5		V _{DD}	V
				V _{DD} - 0.2		V _{DD}	V
	V _{IH5}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 5.5 V	0.8 V _{DD}		V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0.9 V _{DD}		V _{DD}	V
Note			0.9 V _{DD}		V _{DD}	V	
Input voltage, low	V _{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V _{DD} = 2.7 to 5.5 V	0		0.3 V _{DD}	V
				0		0.2 V _{DD}	V
	V _{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, RESET	V _{DD} = 2.7 to 5.5 V	0		0.2 V _{DD}	V
				0		0.15 V _{DD}	V
	V _{IL3}	P60 to P63, P90 to P93 (N-ch open-drain)	4.5 V ≤ V _{DD} ≤ 5.5 V	0		0.3 V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.2 V _{DD}	V
				0		0.1 V _{DD}	V
	V _{IL4}	X1, X2	V _{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V _{IL5}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 5.5 V	0		0.2 V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.1 V _{DD}	V
			Note	0		0.1 V _{DD}	V
	Output voltage, high	V _{OH}	V _{DD} = 4.5 to 5.5 V, I _{OH} = -1 mA	V _{DD} - 1.0			V
I _{OH} = -100 μA			V _{DD} - 0.5			V	

Note When used as P07, the inverted phase of P07 should be input to XT2 pin using an inverter.

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V _{OL1}	P50 to P57, P60 to P63, P90 to P93	V _{DD} = 4.5 to 5.5 V, I _{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	V _{DD} = 4.5 to 5.5 V, I _{OL} = 1.6 mA			0.4	V
	V _{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V _{DD} = 4.5 to 5.5 V, open-drain, pulled up (R = 1 kΩ)			0.2 V _{DD}	V
	V _{OL3}	I _{OL} = 400 μA				0.5	V
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I _{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I _{LIH3}	V _{IN} = 15 V	P60 to P63, P90 to P93			80	μA
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{\text{RESET}}$			-3	μA
	I _{LIL2}		X1, X2, XT1/P07, XT2			-20	μA
	I _{LIL3}		P60 to P63, P90 to P93			-3 ^{Note}	μA
Output leakage current, high	I _{LOH}	V _{OUT} = V _{DD}				3	μA
Output leakage current, low	I _{LOL}	V _{OUT} = 0 V				-3	μA

Note The value is -200 μA (MAX.) only for 1.5 clock cycles (no wait) when read-out instruction is executed to port 6 (P6), port mode register 6 (PM6), port 9 (P9) and port mode register 9 (PM9). For cases other than the 1.5 clock cycles of read-out instruction execution, the value is -3 μA (MAX.).

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Software pull-up resistor ^{Note 1}	R	V _{IN} = 0 V, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	4.5 V ≤ V _{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 V ≤ V _{DD} < 4.5 V	20		500	kΩ
Supply current ^{Note 2}	I _{DD1}	5.0-MHz crystal oscillation operating mode (f _{xx} = 2.5 MHz) ^{Note 3}	V _{DD} = 5.0 V ± 10% ^{Note 6}		5.4	16.2	mA
			V _{DD} = 3.0 V ± 10% ^{Note 7}		0.8	2.4	mA
			V _{DD} = 2.2 V ± 10% ^{Note 7}		0.45	1.35	mA
		5.0-MHz crystal oscillation operating mode (f _{xx} = 5.0 MHz) ^{Note 4}	V _{DD} = 5.0 V ± 10% ^{Note 6}		9.5	28.5	mA
			V _{DD} = 3.0 V ± 10% ^{Note 7}		1.0	3.0	mA
		I _{DD2}	5.0 MHz crystal oscillation HALT mode (f _{xx} = 2.5 MHz) ^{Note 3}	V _{DD} = 5.0 V ± 10%		1.4	4.2
	V _{DD} = 3.0 V ± 10%				0.5	1.5	mA
			V _{DD} = 2.2 V ± 10%		280	840	μA
	5.0 MHz crystal oscillation HALT mode (f _{xx} = 5.0 MHz) ^{Note 4}		V _{DD} = 5.0 V ± 10%		1.6	4.8	mA
		V _{DD} = 3.0 V ± 10%		0.65	1.95	mA	
	I _{DD3}	32.768-kHz crystal oscillation operating mode ^{Note 5}	V _{DD} = 5.0 V ± 10%		135	270	μA
			V _{DD} = 3.0 V ± 10%		95	190	μA
			V _{DD} = 2.2 V ± 10%		70	140	μA
	I _{DD4}	32.768-kHz crystal oscillation HALT mode ^{Note 5}	V _{DD} = 5.0 V ± 10%		25	55	μA
			V _{DD} = 3.0 V ± 10%		5	15	μA
			V _{DD} = 2.2 V ± 10%		2.5	12.5	μA
	I _{DD5}	XT1 = V _{DD} STOP mode Feedback resistor used	V _{DD} = 5.0 V ± 10%		1	30	μA
			V _{DD} = 3.0 V ± 10%		0.5	10	μA
V _{DD} = 2.2 V ± 10%				0.3	10	μA	
I _{DD6}	XT1 = V _{DD} STOP mode Feedback resistor not used	V _{DD} = 5.0 V ± 10%		0.1	30	μA	
		V _{DD} = 3.0 V ± 10%		0.05	10	μA	
		V _{DD} = 2.2 V ± 10%		0.05	10	μA	

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- Notes**
1. Software pull-up resistor can be used only within a range of V_{DD} = 2.7 to 5.5 V.
 2. Current flowing to V_{DD} pin. However, the current flowing to the A/D converter, D/A converter, and on-chip pull-up resistor is not included.
 3. f_{xx} = f_x/2 operation (when oscillation mode selection register (OSMS) is set to 00H).
 4. f_{xx} = f_x operation (when OSMS is set to 01H).
 5. When the main system clock is stopped.
 6. High-speed mode operation (when processor clock control register (PCC) is set to 00H).
 7. Low-speed mode operation (when PCC is set to 04H).

- Remarks**
1. Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.
 2. f_{xx}: Main system clock frequency (f_x or f_x/2)
 3. f_x: Main system clock oscillation frequency

AC Characteristics

(1) Basic Operation (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit	
Cycle time (minimum instruction execution time)	T _{CY}	Operating on main system clock	f _{XX} = f _X /2 ^{Note 1}	V _{DD} = 2.7 to 5.5 V	0.8		64	μS
					2.0		64	μS
			f _{XX} = f _X ^{Note 2}	3.5 V ≤ V _{DD} ≤ 5.5 V	0.4		32	μS
				2.7 V ≤ V _{DD} < 3.5 V	0.8		32	μS
		Operating on subsystem clock			40	122	125	μS
TI00 input high-/low- level width	t _{TIH00} ,	3.5 V ≤ V _{DD} ≤ 5.5 V		2f _{sam} + 0.1 ^{Note 3}			μS	
	t _{TIL00}	2.7 V ≤ V _{DD} < 3.5 V		2f _{sam} + 0.2 ^{Note 3}			μS	
				2f _{sam} + 0.5 ^{Note 3}			μS	
TI01 input high-/low- level width	t _{TIH01} ,	V _{DD} = 2.7 to 5.5 V		10			μS	
	t _{TIL01}			20			μS	
TI1, TI2, TI5, TI6 input frequency	f _{TI1}	V _{DD} = 4.5 to 5.5 V		0		4	MHz	
				0		275	kHz	
TI1, TI2, TI5, TI6 input high-/low-level width	t _{TIH1} ,	V _{DD} = 4.5 to 5.5 V		100			ns	
	t _{TIL1}			1.8			μS	
Interrupt input high-/ low-level width	t _{INTH} ,	INTP0	3.5 V ≤ V _{DD} ≤ 5.5 V	2f _{sam} + 0.1 ^{Note 3}			μS	
			2.7 V ≤ V _{DD} < 3.5 V	2f _{sam} + 0.2 ^{Note 3}			μS	
				2f _{sam} + 0.5 ^{Note 3}			μS	
	t _{INTL}	INTP1 to INTP6, P40 to P47	V _{DD} = 2.7 to 5.5 V	10			μS	
				20			μS	
RESET low-level width	t _{RSL}	V _{DD} = 2.7 to 5.5 V		10			μS	
				20			μS	

Notes 1. When oscillation mode selection register (OSMS) is set to 00H.

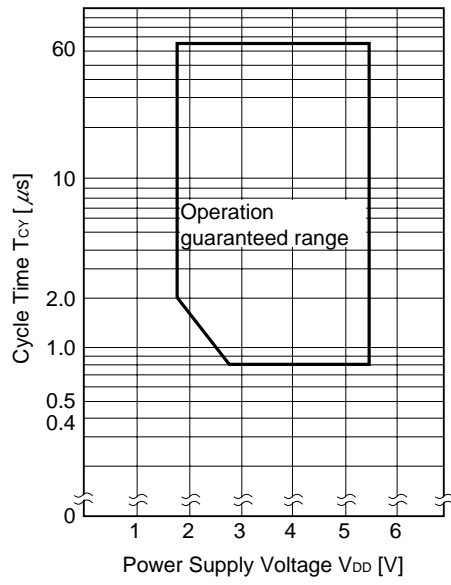
2. When OSMS is set to 01H.

3. f_{sam} can be selected as f_{XX}/2^N, f_{XX}/32, f_{XX}/64 or f_{XX}/128 (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of the sampling clock selection register (SCS).

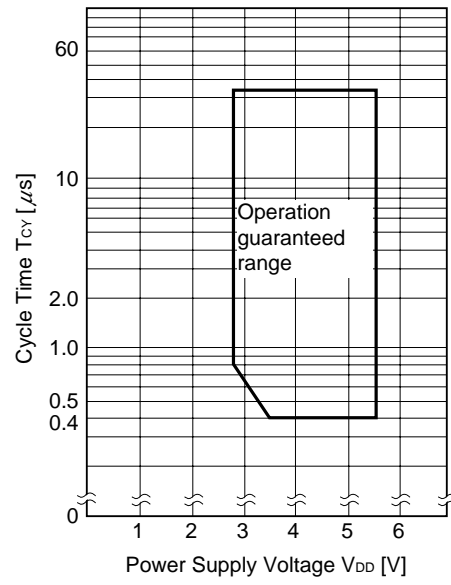
Remark f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

T_{CY} vs V_{DD}
(Main System Clock f_{XX} = f_X/2 Operation)



T_{CY} vs V_{DD}
(Main System Clock f_{XX} = f_X Operation)



(2) Read/Write Operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}		0.85t _{cy} - 50		ns
Address setup time	t _{ADS}		0.85t _{cy} - 50		ns
Address hold time	t _{ADH}		50		ns
Address → Data input time	t _{ADD1}			(2.85 + 2n)t _{cy} - 80	ns
	t _{ADD2}			(4 + 2n)t _{cy} - 100	ns
RD ↓ → Data input time	t _{RDD1}			(2 + 2n)t _{cy} - 100	ns
	t _{RDD2}			(2.85 + 2n)t _{cy} - 100	ns
Read data hold time	t _{RDH}		0		ns
RD low-level width	t _{RDL1}		(2 + 2n)t _{cy} - 60		ns
	t _{RDL2}		(2.85 + 2n)t _{cy} - 60		ns
RD ↓ → WAIT ↓ input time	t _{RDWT1}			0.85t _{cy} - 50	ns
	t _{RDWT2}			2t _{cy} - 60	ns
WR ↓ → WAIT ↓ input time	t _{WRWT}			2t _{cy} - 60	ns
WAIT low-level width	t _{WTL}		(1.15 + 2n)t _{cy}	(2 + 2n)t _{cy}	ns
Write data setup time	t _{WDS}		(2.85 + 2n)t _{cy} - 100		ns
Write data hold time	t _{WDH}	load resistance ≥ 5 kΩ	20		ns
WR low-level width	t _{WRL}		(2.85 + 2n)t _{cy} - 60		ns
ASTB ↓ → RD ↓ delay time	t _{ASTRD}		25		ns
ASTB ↓ → WR ↓ delay time	t _{ASTWR}		0.85t _{cy} + 20		ns
In external fetch RD ↑ → ASTB ↑ delay time	t _{RDAST}		0.85t _{cy} - 10	1.15t _{cy} + 20	ns
In external fetch RD ↑ → address hold time	t _{RDADH}		0.85t _{cy} - 50	1.15t _{cy} + 50	ns
RD ↑ → write data output time	t _{RDWD}		40		ns
WR ↓ → write data output time	t _{WRWD}		0	50	ns
WR ↑ → address hold time	t _{WRADH}		0.85t _{cy} - 20	1.15t _{cy} + 40	ns
WAIT ↑ → RD ↑ delay time	t _{WTRD}		1.15t _{cy} + 40	3.15t _{cy} + 40	ns
WAIT ↑ → WR ↑ delay time	t _{WTWR}		1.15t _{cy} + 30	3.15t _{cy} + 30	ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
 2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
 3. t_{cy} = T_{cy}/4
 4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}		t _{CY} - 80		ns
Address setup time	t _{ADS}		t _{CY} - 80		ns
Address hold time	t _{ADH}		0.4t _{CY} - 10		ns
Address → Data input time	t _{ADD1}			(3 + 2n)t _{CY} - 160	ns
	t _{ADD2}			(4 + 2n)t _{CY} - 200	ns
\overline{RD} ↓ → Data input time	t _{RDD1}			(1.4 + 2n)t _{CY} - 70	ns
	t _{RDD2}			(2.4 + 2n)t _{CY} - 70	ns
Read data hold time	t _{RDH}		0		ns
\overline{RD} low-level width	t _{RDL1}		(1.4 + 2n)t _{CY} - 20		ns
	t _{RDL2}		(2.4 + 2n)t _{CY} - 20		ns
\overline{RD} ↓ → \overline{WAIT} ↓ input time	t _{RDWT1}			t _{CY} - 100	ns
	t _{RDWT2}			2t _{CY} - 100	ns
\overline{WR} ↓ → \overline{WAIT} ↓ input time	t _{WRWT}			2t _{CY} - 100	ns
\overline{WAIT} low-level width	t _{WTL}		(1 + 2n)t _{CY}	(2 + 2n)t _{CY}	ns
Write data setup time	t _{WDS}		(2.4 + 2n)t _{CY} - 60		ns
Write data hold time	t _{WDH}	load resistance ≥ 5 kΩ	20		ns
\overline{WR} low-level width	t _{WRL}		(2.4 + 2n)t _{CY} - 20		ns
ASTB ↓ → \overline{RD} ↓ delay time	t _{ASTRD}		0.4t _{CY} - 30		ns
ASTB ↓ → \overline{WR} ↓ delay time	t _{ASTWR}		1.4t _{CY} - 30		ns
In external fetch \overline{RD} ↑ → ASTB ↑ delay time	t _{RDAST}		t _{CY} - 10	t _{CY} + 20	ns
In external fetch \overline{RD} ↑ → address hold time	t _{RDADH}		t _{CY} - 80	t _{CY} + 50	ns
\overline{RD} ↑ → write data output time	t _{RDWD}		0.4t _{CY} - 30		ns
\overline{WR} ↓ → write data output time	t _{WRWD}		0	60	ns
\overline{WR} ↑ → address hold time	t _{WRADH}		t _{CY} - 60	t _{CY} + 60	ns
\overline{WAIT} ↑ → \overline{RD} ↑ delay time	t _{WTRD}		0.6t _{CY} + 180	2.6t _{CY} + 180	ns
\overline{WAIT} ↑ → \overline{WR} ↑ delay time	t _{WTWR}		0.6t _{CY} + 120	2.6t _{CY} + 120	ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
 2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
 3. t_{CY} = T_{CY}/4
 4. n indicates the number of waits.

(3) Serial Interface (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY1}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1 600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3 200			ns
			4 800			ns
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH1} ,	V _{DD} = 4.5 to 5.5 V	t _{KCY1} /2 - 50			ns
	t _{KL1}		t _{KCY1} /2 - 100			ns
SIO setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK1}	4.5 V ≤ V _{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V _{DD} < 4.5 V	150			ns
		2.0 V ≤ V _{DD} < 2.7 V	300			ns
			400			ns
SIO hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KSI1}		400			ns
$\overline{\text{SCK0}}$ ↓ → SO0 output delay time	t _{KSO1}	C = 100 pF ^{Note}			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY2}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1 600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3 200			ns
			4 800			ns
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH2} ,	4.5 V ≤ V _{DD} ≤ 5.5 V	400			ns
	t _{KL2}		800			ns
			1 600			ns
			2 400			ns
SIO setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK2}	V _{DD} = 2.0 to 5.5 V	100			ns
			150			ns
SIO hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KSI2}		400			ns
$\overline{\text{SCK0}}$ ↓ → SO0 output delay time	t _{KSO2}	C = 100 pF ^{Note} V _{DD} = 2.0 to 5.5 V			300	ns
					500	ns
$\overline{\text{SCK0}}$ rise, fall time	t _{r2} ,	When using external device expansion function			160	ns
	t _{f2}		When not using external device expansion function		1 000	ns

Note C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{\text{SCK0}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK0 cycle time	t _{KCY3}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.0 V ≤ V _{DD} < 4.5 V	3 200			ns
			4 800			ns
SCK0 high-/low-level width	t _{KH3} ,	V _{DD} = 4.5 to 5.5 V	t _{KCY3} /2 – 50			ns
	t _{KL3}		t _{KCY3} /2 – 150			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK3}	4.5 V ≤ V _{DD} ≤ 5.5 V	100			ns
		2.0 V ≤ V _{DD} < 4.5 V	300			ns
			400			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KSI3}		t _{KCY3} /2			ns
SCK0 ↓ → SB0, SB1 output delay time	t _{KSO3}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 4.5 to 5.5 V	0	250	ns
				0	1 000	ns
SCK0 ↑ → SB0, SB1 ↓	t _{KSB}		t _{KCY3}			ns
SB0, SB1 ↓ → $\overline{\text{SCK0}}$ ↓	t _{SBK}		t _{KCY3}			ns
SB0, SB1 high-level width	t _{SBH}		t _{KCY3}			ns
SB0, SB1 low-level width	t _{SBL}		t _{KCY3}			ns

Note R and C are the SB0, SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{\text{SCK0}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	t _{KCY4}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns	
		2.0 V ≤ V _{DD} < 4.5 V	3 200			ns	
			4 800			ns	
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH4} ,	4.5 V ≤ V _{DD} ≤ 5.5 V	400			ns	
			t _{KL4}	2.0 V ≤ V _{DD} < 4.5 V	1 600		ns
					2 400		ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK4}	4.5 V ≤ V _{DD} ≤ 5.5 V	100			ns	
		2.0 V ≤ V _{DD} < 4.5 V	300			ns	
			400			ns	
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KSI4}		t _{KCY4} /2			ns	
$\overline{\text{SCK0}}$ ↓ → SB0, SB1 output delay time	t _{KSO4}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 4.5 to 5.5 V	0	300	ns	
				0	1 000	ns	
$\overline{\text{SCK0}}$ ↑ → SB0, SB1 ↓	t _{KSB}		t _{KCY4}			ns	
SB0, SB1 ↓ → $\overline{\text{SCK0}}$ ↓	t _{SBK}		t _{KCY4}			ns	
SB0, SB1 high-level width	t _{SBH}		t _{KCY4}			ns	
SB0, SB1 low-level width	t _{SBL}		t _{KCY4}			ns	
$\overline{\text{SCK0}}$ rise, fall time	t _{R4} , t _{F4}	When using external device expansion function			160	ns	
		When not using external device expansion function			1 000	ns	

Note R and C are the SB0, SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF ^{Note}	$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	1 600			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
				4 800			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH5}		$V_{\text{DD}} = 2.7 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY5}}/2 - 160$			ns
				$t_{\text{KCY5}}/2 - 190$			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL5}		$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY5}}/2 - 50$			ns
				$t_{\text{KCY5}}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	t_{SIK5}		$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	300			ns
			$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	350			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	400			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	t_{KS15}			500			ns
				600			ns
$\overline{\text{SCK0}}$ ↓ → SB0, SB1 output delay time	t_{KSO5}			0		300	ns

Note R and C are the $\overline{\text{SCK0}}$, SB0, SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY6}		$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	1 600			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
				4 800			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH6}		$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	650			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1 300			ns
				2 100			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL6}		$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1 600			ns
				2 400			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	t_{SIK6}		$V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$	100			ns
				150			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	t_{KS16}			$t_{\text{KCY6}}/2$			ns
$\overline{\text{SCK0}}$ ↓ → SB0, SB1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF ^{Note}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	0		300	ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	0		500	ns
						800	ns
$\overline{\text{SCK0}}$ rise, fall time	$t_{\text{r6}},$ t_{f6}		When using external device expansion function			160	ns
			When not using external device expansion function			1 000	ns

Note R and C are the SB0, SB1 output line load resistance and load capacitance.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1 600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
			4 800			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH7}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY7}}/2 - 50$			ns
	t_{KL7}		$t_{\text{KCY7}}/2 - 100$			ns
SI1 setup time (to $\overline{\text{SCK1}} \uparrow$)	t_{SIK7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	300			ns
			400			ns
SI1 hold time (from $\overline{\text{SCK1}} \uparrow$)	t_{KSI7}		400			ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ output delay time	t_{KSO7}	$C = 100 \text{ pF}$ ^{Note}			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1 600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
			4 800			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH8}},$ t_{KL8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1 600			ns
			2 400			ns
SI1 setup time (to $\overline{\text{SCK1}} \uparrow$)	t_{SIK8}	$V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI1 hold time (from $\overline{\text{SCK1}} \uparrow$)	t_{KSI8}		400			ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ output delay time	t_{KSO8}	$C = 100 \text{ pF}$ ^{Note} $V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$			300	ns
					500	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{R8}},$ t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1 000	ns

Note C is the SO1 output line load capacitance.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1 600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
			4 800			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH9}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY9}}/2 - 50$			ns
	t_{KL9}		$t_{\text{KCY9}}/2 - 100$			ns
S11 setup time (to $\overline{\text{SCK1}}$ ↑)	t_{SIK9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	300			ns
			400			ns
S11 hold time (from $\overline{\text{SCK1}}$ ↑)	t_{KS19}		400			ns
$\overline{\text{SCK1}}$ ↓ → SO1 output delay time	t_{KSO9}	$C = 100 \text{ pF}$ ^{Note}			300	ns
$\overline{\text{SCK1}}$ ↑ → STB ↑	t_{SBD}		$t_{\text{KCY9}}/2 - 100$		$t_{\text{KCY9}}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY9}} - 30$		$t_{\text{KCY9}} + 30$	ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	$t_{\text{KCY9}} - 60$		$t_{\text{KCY9}} + 60$	ns
			$t_{\text{KCY9}} - 90$		$t_{\text{KCY9}} + 90$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	200			ns
			300			ns
Busy inactive → $\overline{\text{SCK1}}$ ↓	t_{SPS}				$2t_{\text{KCY9}}$	ns

Note C is the SO1 output line load capacitance.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY10}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1 600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
			4 800			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH10}},$ t_{KL10}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1 600			ns
			2 400			ns
SI1 setup time (to $\overline{\text{SCK1}}$ ↑)	t_{SIK10}	$V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI1 hold time (from $\overline{\text{SCK1}}$ ↑)	t_{KSI10}		400			ns
$\overline{\text{SCK1}}$ ↓ → SO1 output delay time	t_{KSO10}	$C = 100 \text{ pF}$ ^{Note} $V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$			300	ns
					500	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{R10}},$ t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1 000	ns

Note C is the SO1 output line load capacitance.

(c) Serial Interface Channel 2

(i) 3-wire serial I/O mode ($\overline{\text{SCK2}}$... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY11}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1 600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
			4 800			ns
$\overline{\text{SCK2}}$ high-/low-level width	$t_{\text{KH11}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY11}}/2 - 50$			ns
	t_{KL11}		$t_{\text{KCY11}}/2 - 100$			ns
SI2 setup time (to $\overline{\text{SCK2}}$ ↑)	t_{SIK11}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	300			ns
			400			ns
SI2 hold time (from $\overline{\text{SCK2}}$ ↑)	t_{KSI11}		400			ns
$\overline{\text{SCK2}}$ ↓ → SO2 output delay time	t_{KSO11}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

Note C is the SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK2}}$... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY12}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1 600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3 200			ns
			4 800			ns
$\overline{\text{SCK2}}$ high-/low-level width	$t_{\text{KH12}},$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
	t_{KL12}	$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1 600			ns
			2 400			ns
SI2 setup time (to $\overline{\text{SCK2}}$ ↑)	t_{SIK12}	$V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI2 hold time (from $\overline{\text{SCK2}}$ ↑)	t_{KSI12}		400			ns
$\overline{\text{SCK2}}$ ↓ → SO2 output delay time	t_{KSO12}	$C = 100 \text{ pF}^{\text{Note}}$ $V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$			300	ns
					500	ns
$\overline{\text{SCK2}}$ rise, fall time	$t_{\text{R12}},$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$			1 000	ns
	t_{F12}	When not using external device expansion function			160	ns

Note C is the SO2 output line load capacitance.

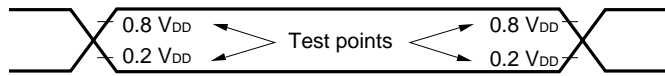
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			78 125	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			39 063	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			19 531	bps
					9 766	bps

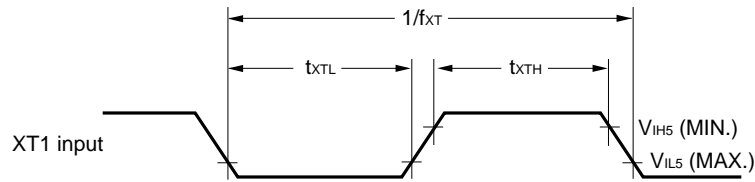
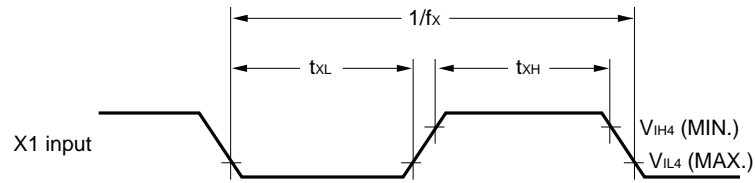
(iv) UART mode (external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t _{KCY13}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1 600			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	3 200			ns
			4 800			ns
ASCK high-/low-level width	t _{KH13} , t _{KL13}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	400			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	800			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1 600			ns
			2 400			ns
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			39 063	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			19 531	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			9 766	bps
					6 510	bps
ASCK rise, fall time	t _{R13} , t _{F13}	V _{DD} = 4.5 to 5.5 V When not using external device expansion function			1 000	ns
					160	ns

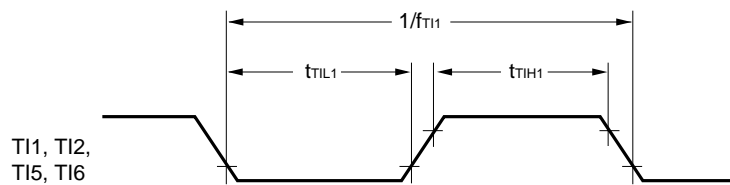
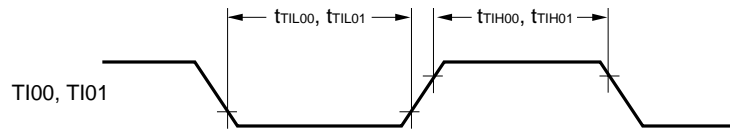
AC Timing Test Point (Excluding X1, XT1 Inputs)



Clock Timing

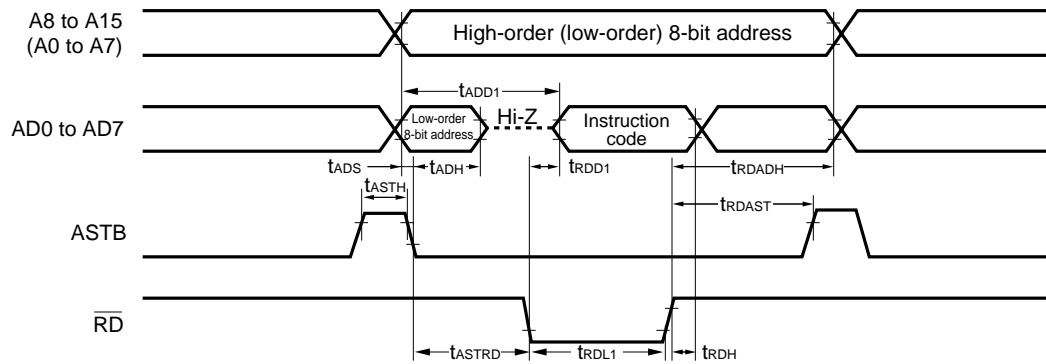


TI Timing



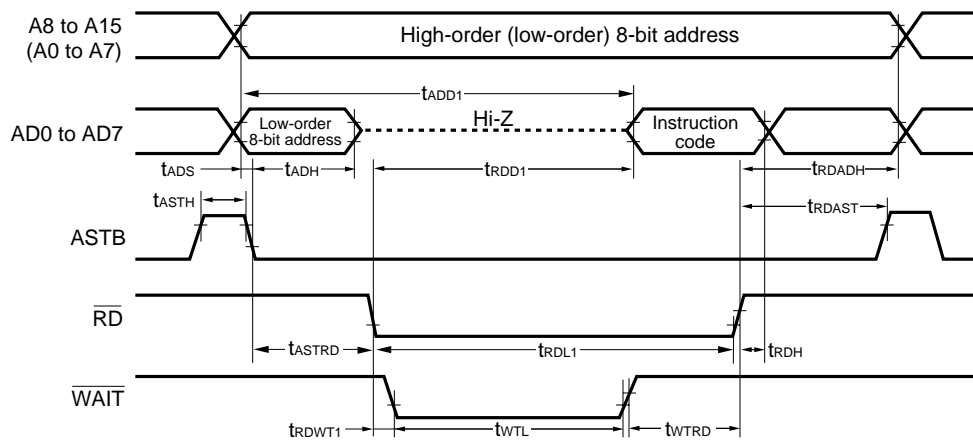
Read/Write Operation

External fetch (no wait):



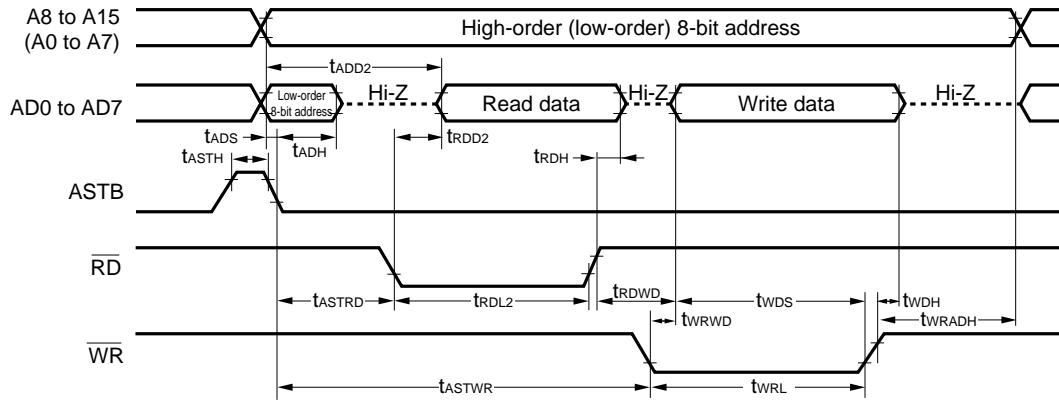
Remark () is effective only in separate bus mode.

External fetch (wait insertion):



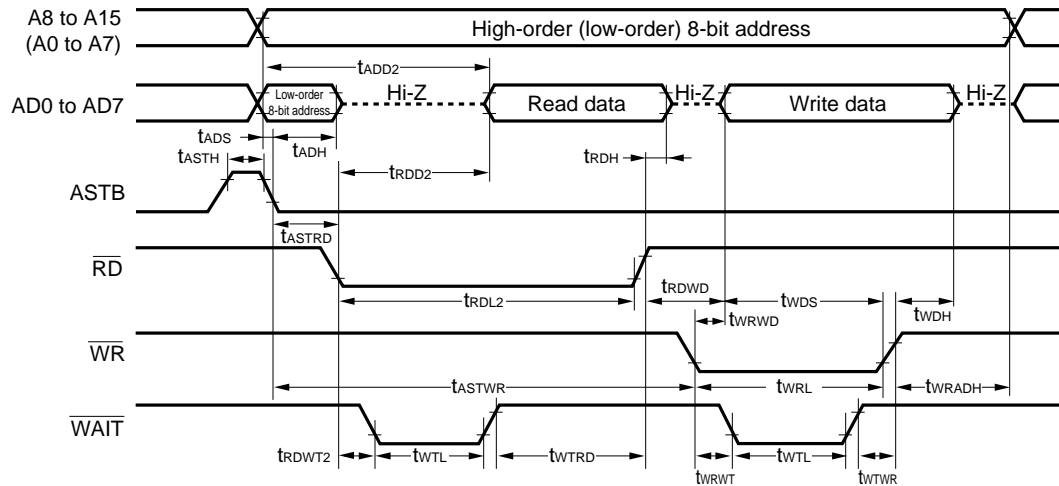
Remark () is effective only in separate bus mode.

External data access (no wait):



Remark () is effective only in separate bus mode.

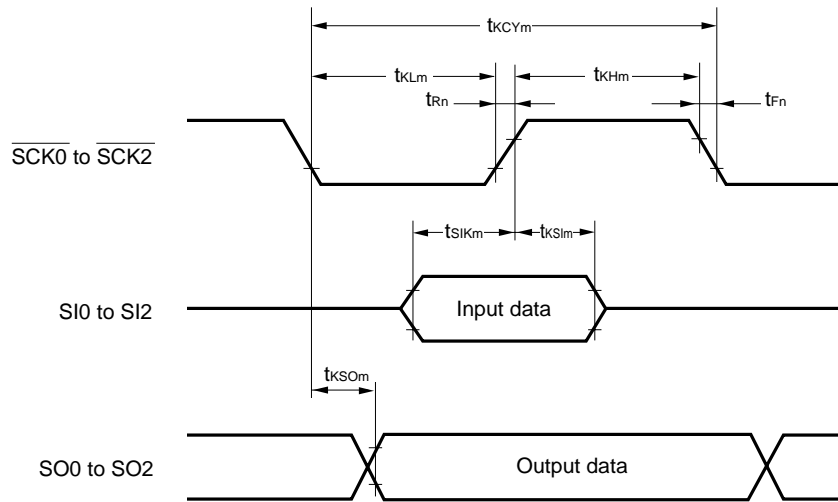
External data access (wait insertion):



Remark () is effective only in separate bus mode.

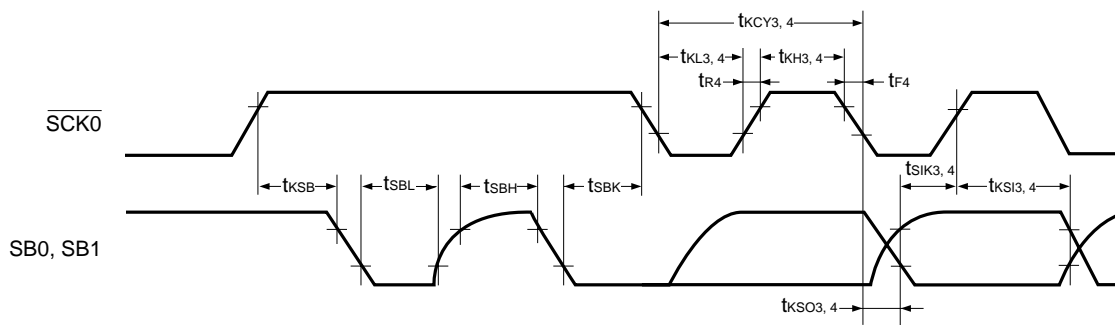
Serial Transfer Timing

3-wire serial I/O mode:

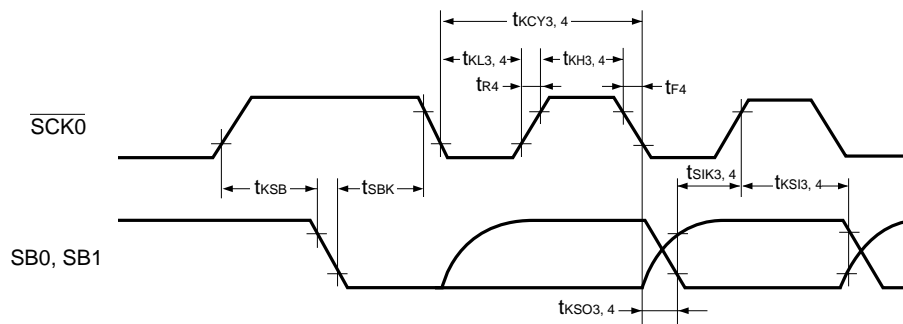


Remark $m = 1, 2, 7, 8, 11, 12$
 $n = 2, 8, 12$

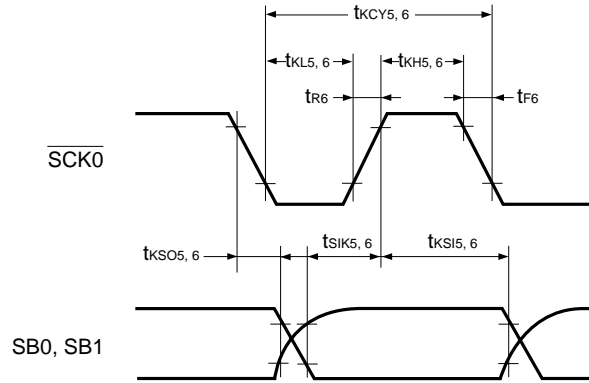
SBI mode (bus release signal transfer):



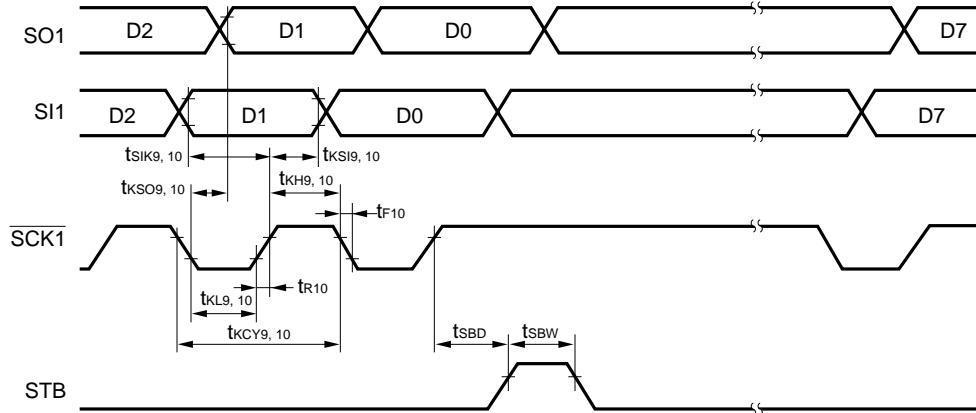
SBI mode (command signal transfer):



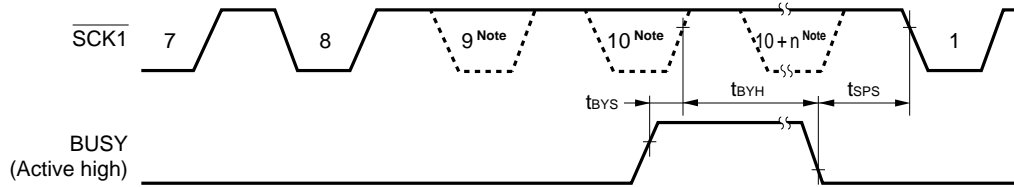
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:

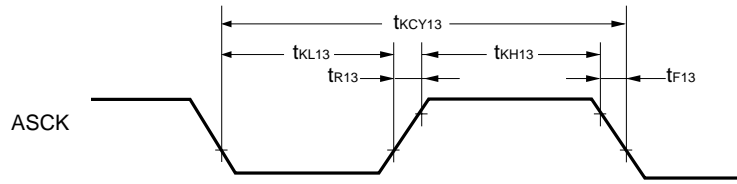


3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually low here, but is represented in this way to show the timing.

UART mode (external clock input):



A/D Converter Characteristics (T_A = -40 to +85 °C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error ^{Note}		2.7 V ≤ AV _{REF0} ≤ AV _{DD}			1.4	%
Conversion time	t _{CONV}		19.1		200	μs
Sampling time	t _{SAMP}		12/f _{xx}			μs
Analog input voltage	V _{IAN}		AV _{SS}		AV _{REF0}	V
Reference voltage	AV _{REF0}		2.7		AV _{DD}	V
AV _{REF0} to AV _{SS} resistance	RA _{IREF0}		4			kΩ

Note Excluding quantization error (±1/2LSB). Shown as a percentage of the full scale value.

Remark f_{xx}: Main system clock frequency (f_x or f_x/2)
 f_x: Main system clock oscillation frequency

D/A Converter Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Total error		R = 2 MΩ ^{Note 1}			1.2	%
		R = 4 MΩ ^{Note 1}			0.8	%
		R = 10 MΩ ^{Note 1}			0.6	%
Settling time		C = 30 pF ^{Note 1}	4.5 V ≤ AV _{REF1} ≤ 5.5 V		10	μs
			2.7 V ≤ AV _{REF1} < 4.5 V		15	μs
			1.8 V ≤ AV _{REF1} < 2.7 V		20	μs
Output resistance	R _o	Note 2		10		kΩ
Analog reference voltage	AV _{REF1}		1.8		V _{DD}	V
AV _{REF1} to AV _{SS} resistance	RA _{IREF1}	DACS0, DACS1 = 55H ^{Note 2}	4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance.
 2. Value for one D/A converter channel.

Remark DACS0, DACS1: D/A conversion value setting register 0, 1

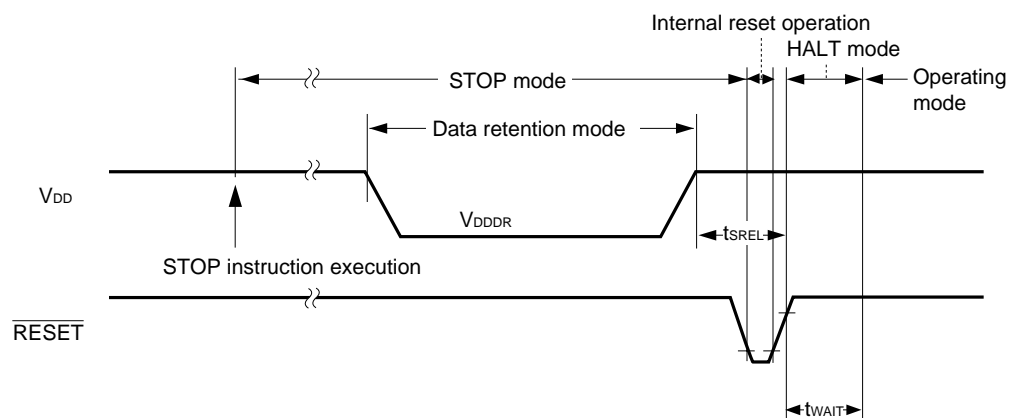
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.8		5.5	V
Data retention supply current	I _{DDDR}	V _{DDDR} = 1.8 V When subsystem clock stopped and feedback resistor disconnected		0.1	10	μA
Release signal setup time	t _{SREL}		0			μs
Oscillation stabilization wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _x		ms
		Release by interrupt		Note		ms

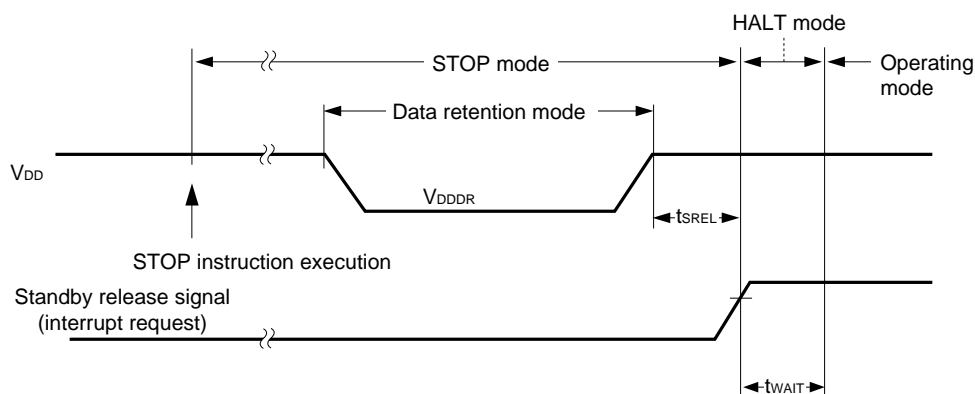
Note 2¹²/f_{xx} or 2¹⁴/f_{xx} to 2¹⁷/f_{xx} can be selected by bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time selection register.

Remark f_{xx}: Main system clock frequency (f_x or f_x/2)
f_x: Main system clock oscillation frequency

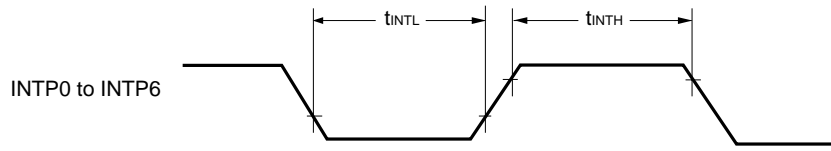
Data Retention Timing (STOP mode released by $\overline{\text{RESET}}$)



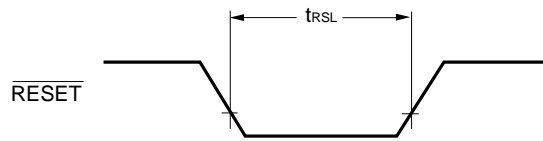
Data Retention Timing (Standby release signal: STOP mode released by interrupt signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM Programming Characteristics

DC Characteristics

(1) PROM Write Mode ($T_A = 25 \pm 5 \text{ }^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \pm 0.3 \text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7 V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3 V_{DD}$	V
Output voltage, high	V_{OH}	V_{OH}	$I_{OH} = -1 \text{ mA}$	$V_{DD} - 1.0$			V
Output voltage, low	V_{OL}	V_{OL}	$I_{OL} = 1.6 \text{ mA}$			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM} = V_{IL}$			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode ($T_A = 25 \pm 5 \text{ }^\circ\text{C}$, $V_{DD} = 5.0 \pm 0.5 \text{ V}$, $V_{PP} = V_{DD} \pm 0.6 \text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7 V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3 V_{DD}$	V
Output voltage, high	V_{OH1}	V_{OH1}	$I_{OH} = -1 \text{ mA}$	$V_{DD} - 1.0$			V
	V_{OH2}	V_{OH2}	$I_{OH} = -100 \text{ } \mu\text{A}$	$V_{DD} - 0.5$			V
Output voltage, low	V_{OL}	V_{OL}	$I_{OL} = 1.6 \text{ mA}$			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
Output leakage current	I_{LO}	I_{LO}	$0 \leq V_{OUT} \leq V_{DD}$, $\overline{OE} = V_{IH}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		$V_{DD} - 0.6$	V_{DD}	$V_{DD} + 0.6$	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	$V_{PP} = V_{DD}$			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$			50	mA

Note Corresponding μPD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode ($T_A = 25 \pm 5 \text{ }^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \pm 0.3 \text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE} \downarrow$)	t _{AS}	t _{AS}		2			μs
\overline{OE} setup time	to _{ES}	to _{ES}		2			μs
\overline{CE} setup time (to $\overline{OE} \downarrow$)	tc _{ES}	tc _{ES}		2			μs
Input data setup time (to $\overline{OE} \downarrow$)	td _S	td _S		2			μs
Address hold time (from $\overline{OE} \uparrow$)	t _{AH}	t _{AH}		2			μs
	t _{AHL}	t _{AHL}		2			μs
	t _{AHV}	t _{AHV}		0			μs
Input data hold time (from $\overline{OE} \uparrow$)	td _H	td _H		2			μs
$\overline{OE} \uparrow \rightarrow$ data output float delay time	td _F	td _F		0		250	ns
V _{PP} setup time (to $\overline{OE} \downarrow$)	tv _{PS}	tv _{PS}		1.0			ms
V _{DD} setup time (to $\overline{OE} \downarrow$)	tv _{DS}	tv _{CS}		1.0			ms
Program pulse width	tp _W	tp _W		0.095	0.1	0.105	ms
$\overline{OE} \downarrow \rightarrow$ valid data delay time	to _E	to _E				1	μs
\overline{OE} pulse width during data latching	tl _W	tl _W		1			μs
\overline{PGM} setup time	tp _{GM_S}	tp _{GM_S}		2			μs
\overline{CE} hold time	tc _{EH}	tc _{EH}		2			μs
\overline{OE} hold time	to _{EH}	to _{EH}		2			μs

(b) Byte program mode ($T_A = 25 \pm 5 \text{ }^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \pm 0.3 \text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM} \downarrow$)	t _{AS}	t _{AS}		2			μs
\overline{OE} setup time	to _{ES}	to _{ES}		2			μs
\overline{CE} setup time (to $\overline{PGM} \downarrow$)	tc _{ES}	tc _{ES}		2			μs
Input data setup time (to $\overline{PGM} \downarrow$)	td _S	td _S		2			μs
Address hold time (from $\overline{OE} \uparrow$)	t _{AH}	t _{AH}		2			μs
Input data hold time (from $\overline{PGM} \uparrow$)	td _H	td _H		2			μs
$\overline{OE} \uparrow \rightarrow$ data output float delay time	td _F	td _F		0		250	ns
V _{PP} setup time (to $\overline{PGM} \downarrow$)	tv _{PS}	tv _{PS}		1.0			ms
V _{DD} setup time (to $\overline{PGM} \downarrow$)	tv _{DS}	tv _{CS}		1.0			ms
Program pulse width	tp _W	tp _W		0.095	0.1	0.105	ms
$\overline{OE} \downarrow \rightarrow$ valid data delay time	to _E	to _E				1	μs
\overline{OE} hold time	to _{EH}	—		2			μs

Note Corresponding μPD27C1001A symbol.

(2) PROM Read Mode ($T_A = 25 \pm 5 \text{ }^\circ\text{C}$, $V_{DD} = 5.0 \pm 0.5 \text{ V}$, $V_{PP} = V_{DD} \pm 0.6 \text{ V}$)

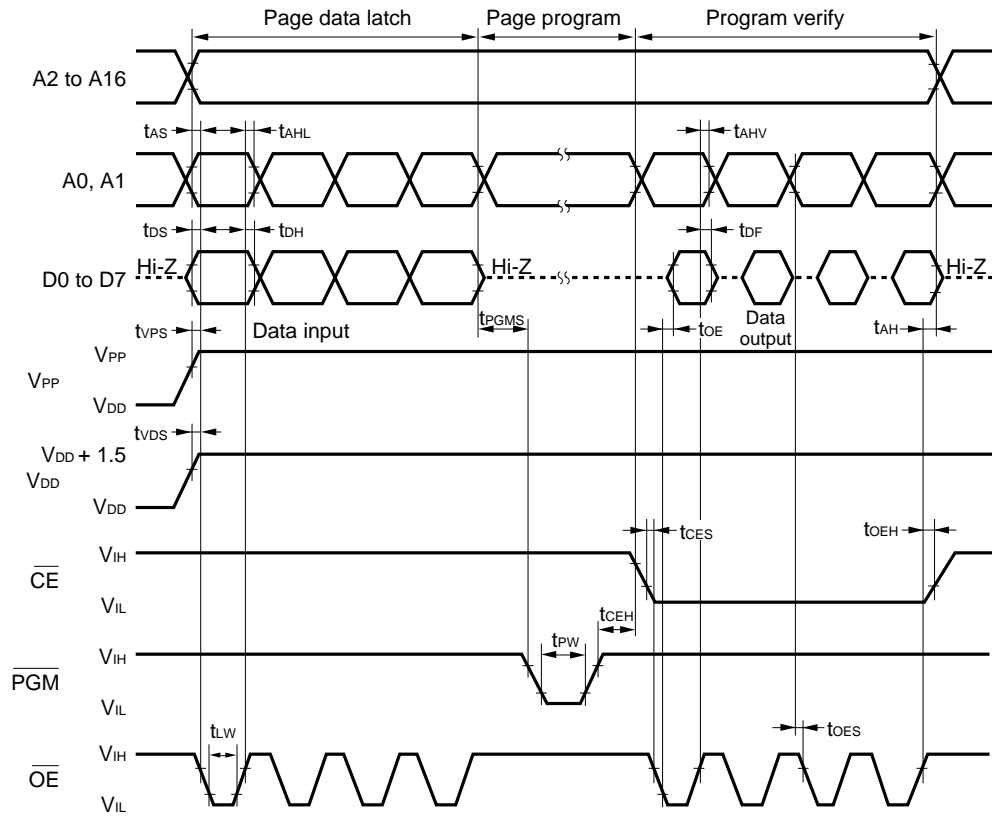
Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
Address → data output delay time	t _{ACC}	t _{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			800	ns
$\overline{CE} \downarrow \rightarrow$ data output delay time	t _{CE}	t _{CE}	$\overline{OE} = V_{IL}$			800	ns
$\overline{OE} \downarrow \rightarrow$ data output delay time	t _{OE}	t _{OE}	$\overline{CE} = V_{IL}$			200	ns
$\overline{OE} \uparrow \rightarrow$ data output float delay time	t _{DF}	t _{DF}	$\overline{CE} = V_{IL}$	0		60	ns
Address → data hold time	t _{OH}	t _{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note Corresponding μPD27C1001A symbol.

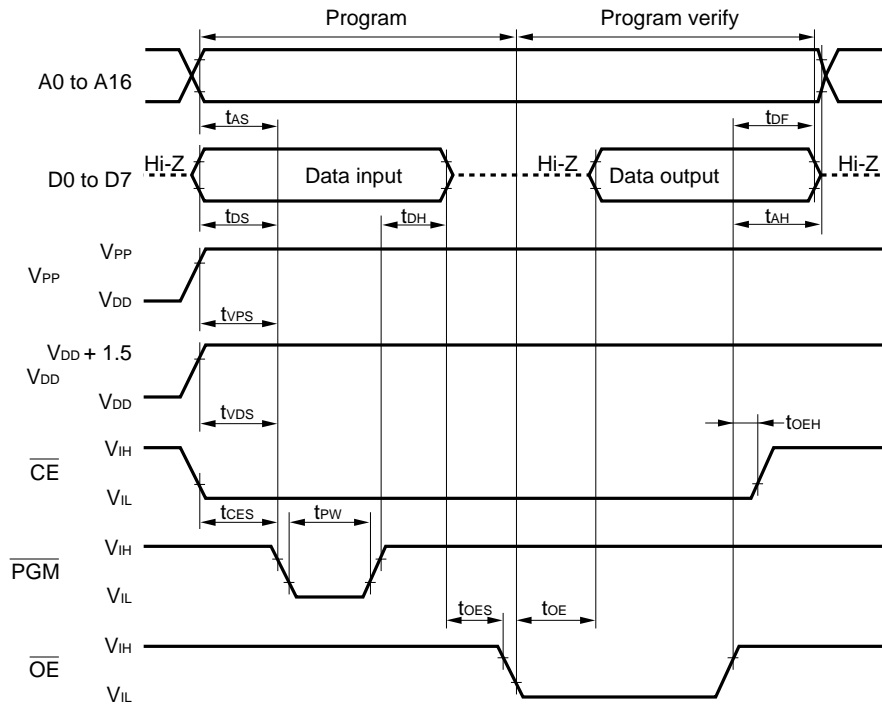
(3) PROM Programming Mode ($T_A = 25 \text{ }^\circ\text{C}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t _{SMA}			10			μs

PROM Write Mode Timing (page program mode)

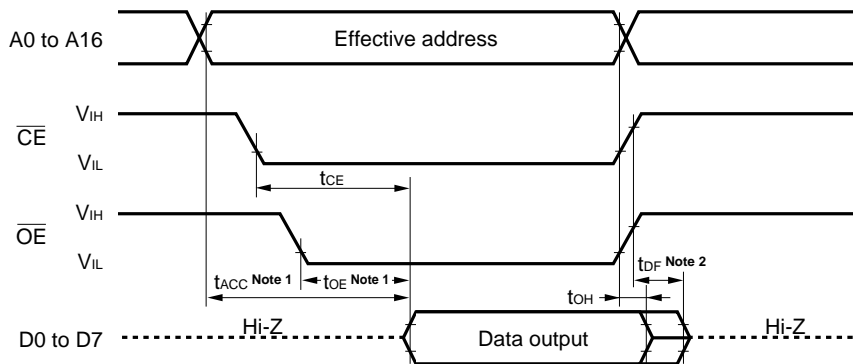


PROM Write Mode Timing (byte program mode)



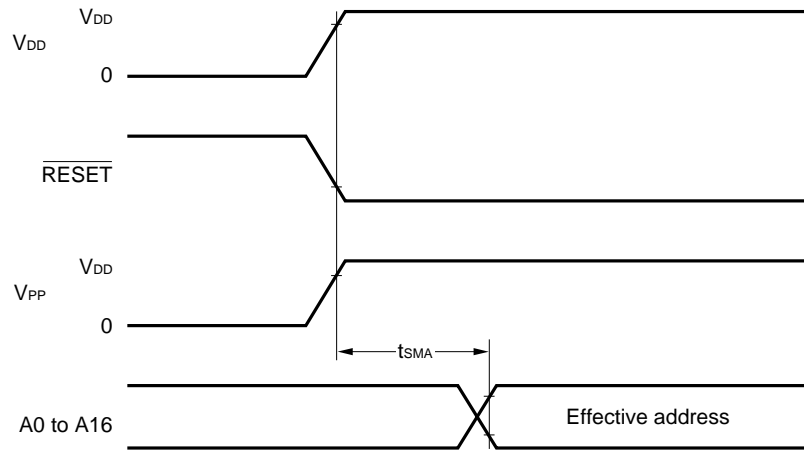
- Cautions**
1. V_{DD} should be applied before V_{PP}, and removed after V_{PP}.
 2. V_{PP} must not exceed +13.5 V including overshoot.
 3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

PROM Read Mode Timing



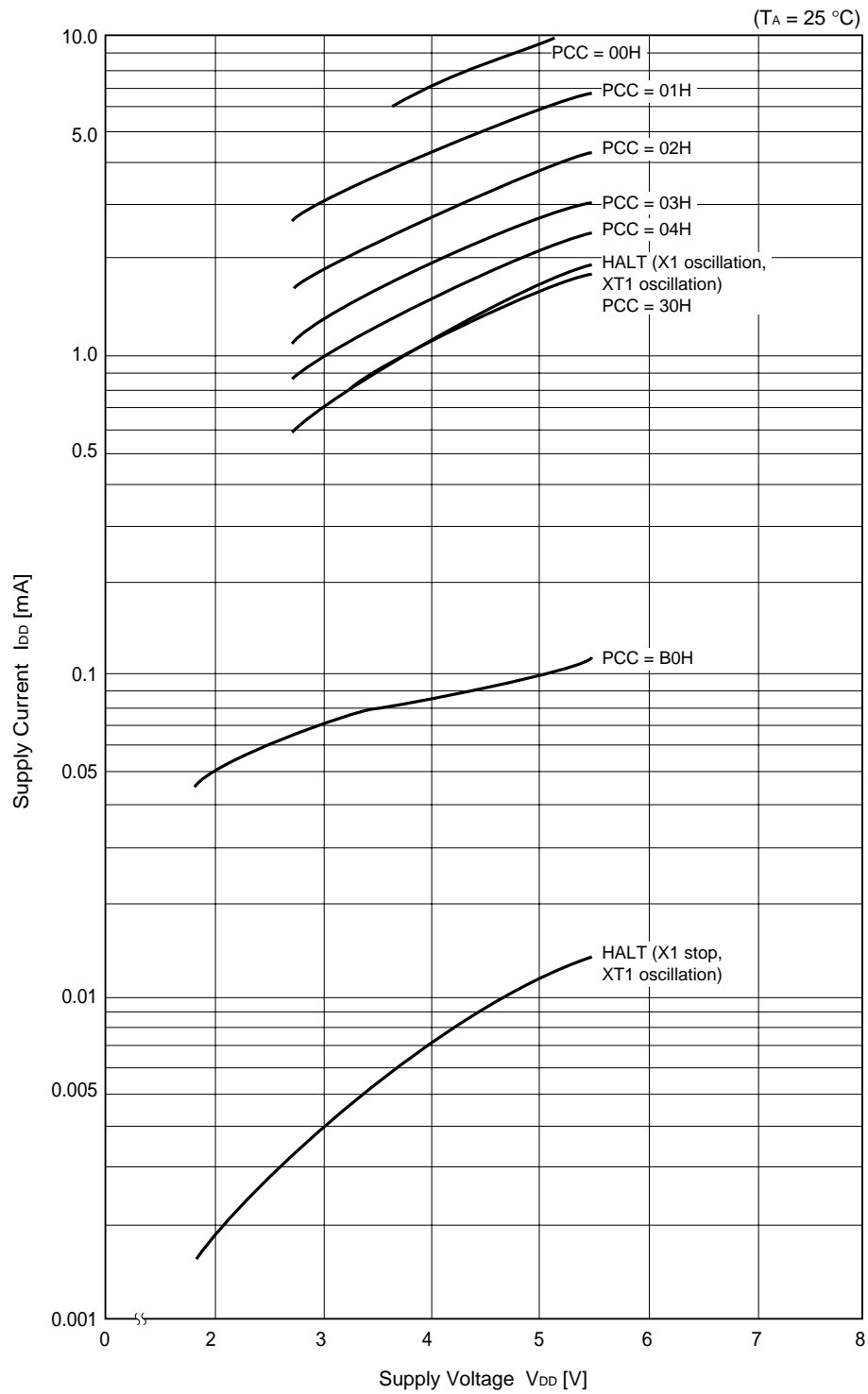
- Notes**
1. If you want to read within the range of t_{ACC}, make the OE input delay time from the fall of CE a maximum of t_{ACC} - t_{OE}.
 2. t_{DF} is the time from when either OE or CE first reaches V_{IH}.

PROM Programming Mode Setting Timing

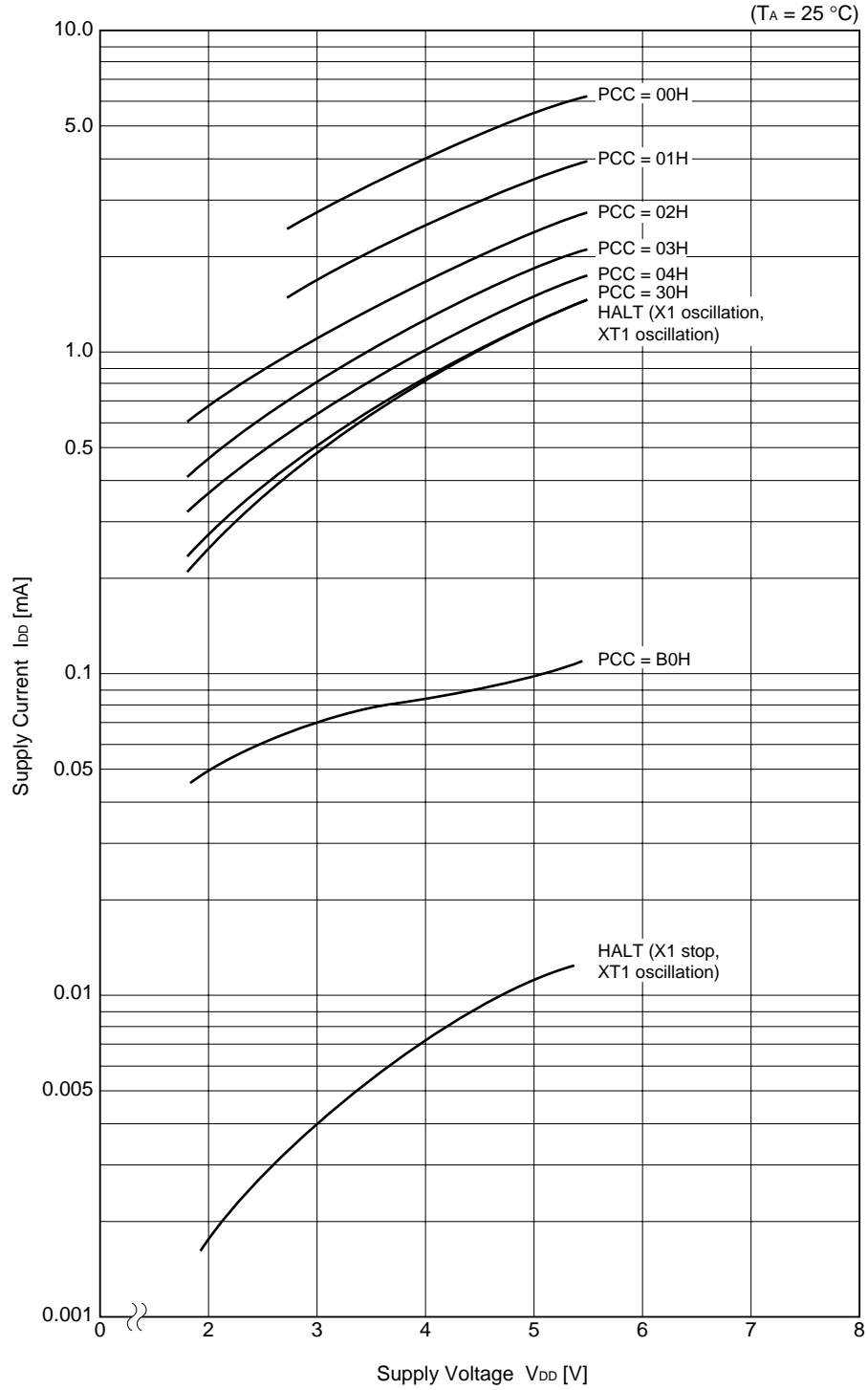


10. CHARACTERISTIC CURVES (REFERENCE VALUES)

I_{DD} VS V_{DD} (f_x = f_{XX} = 5.0 MHz)

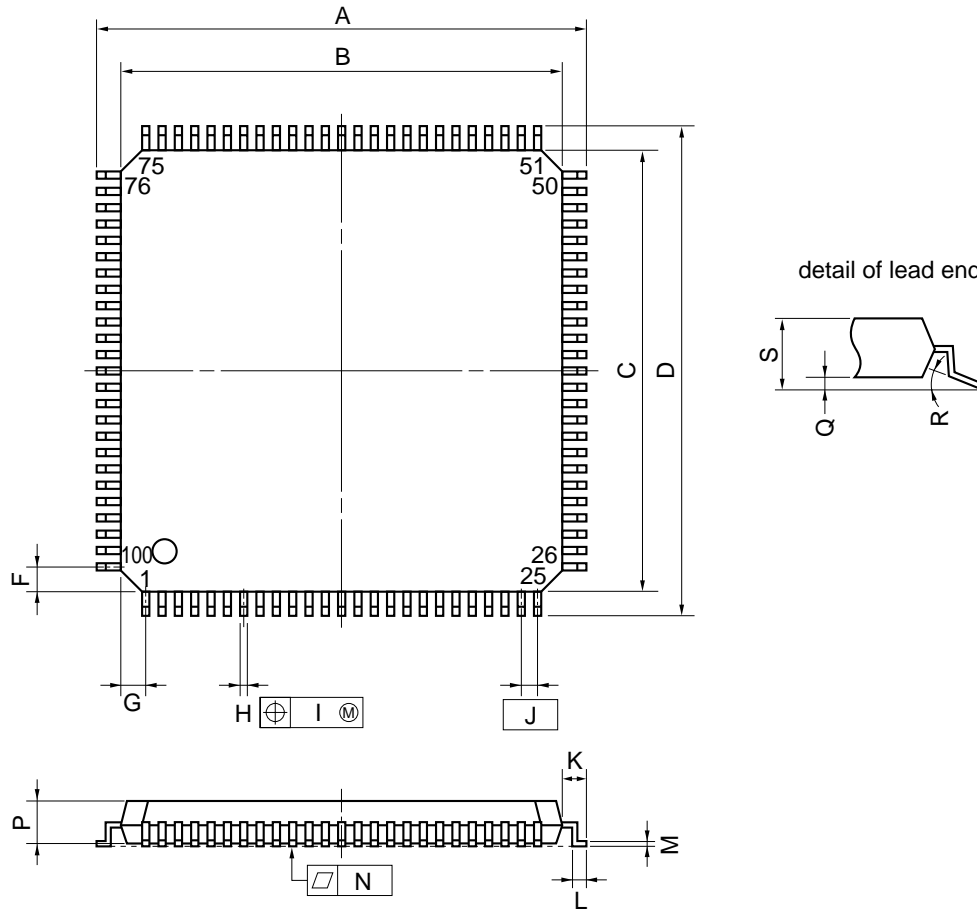


I_{DD} VS V_{DD} (f_x = 5.0 MHz, f_{xx} = 2.5 MHz)



11. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

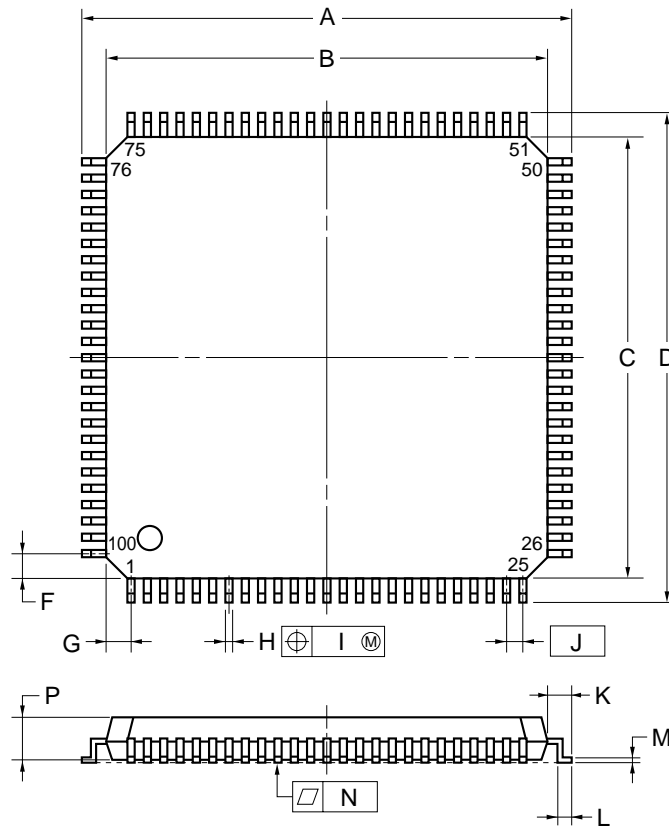
Remark

The shape and material of ES versions are the same as those of mass-produced versions.

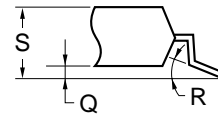
ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

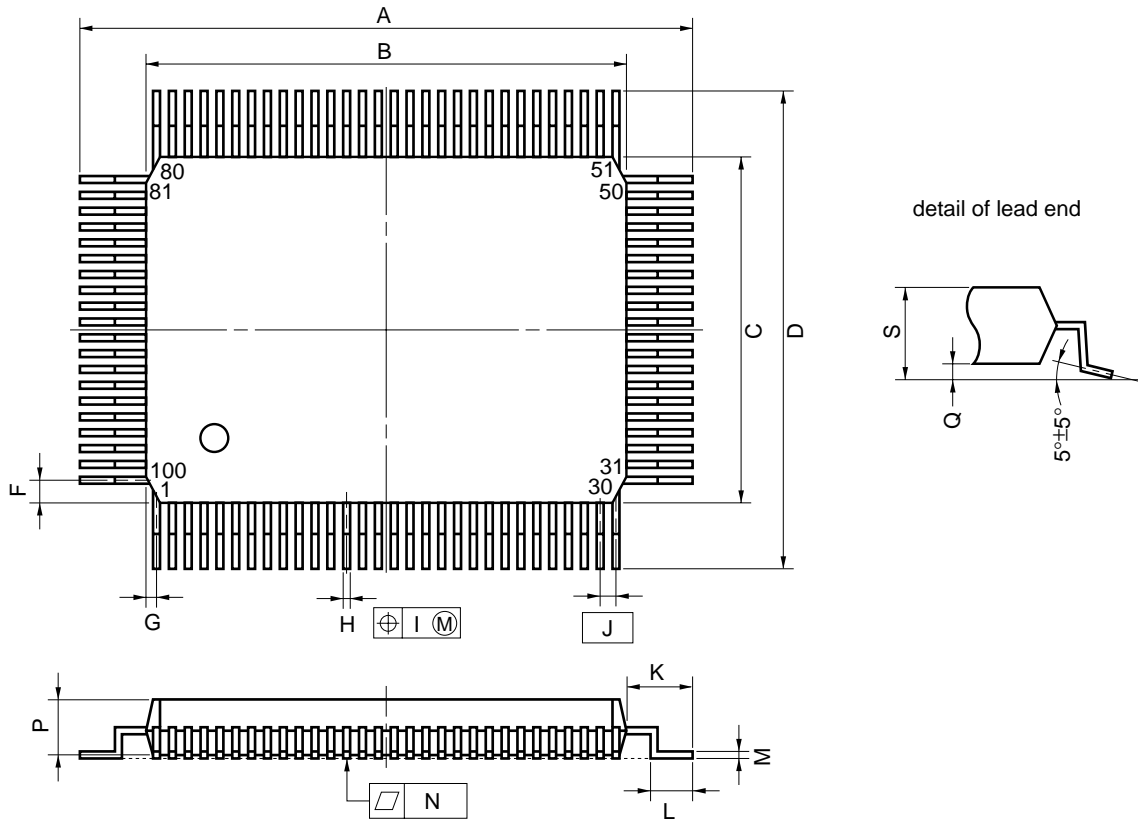
Remark

The shape and material of ES versions are the same as those of mass-produced versions.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	0.551 ^{+0.009} _{-0.008}
C	14.00±0.20	0.551 ^{+0.009} _{-0.008}
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	0.039 ^{+0.009} _{-0.008}
L	0.50±0.20	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

100 PIN PLASTIC QFP (14 × 20)



NOTE

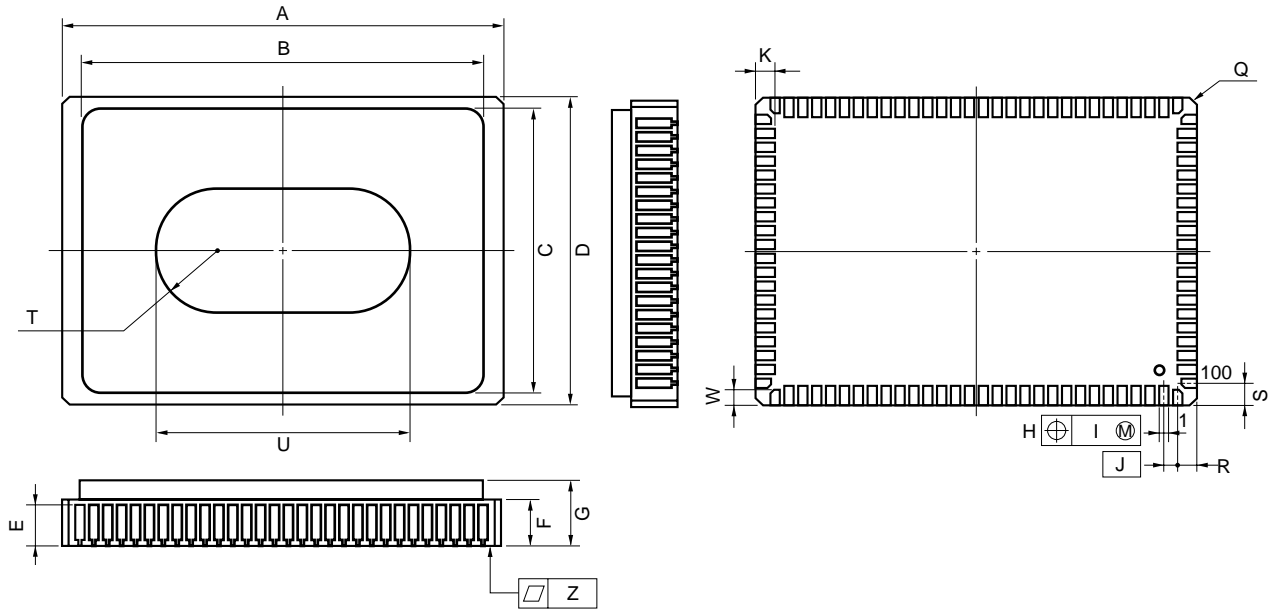
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

Remark The shape and material of ES versions are the same as those of mass-produced versions.

P100GF-65-3BA1-2

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

100 PIN CERAMIC WQFN



NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

X100KW-65A-1

ITEM	MILLIMETERS	INCHES
A	20.6±0.4	0.811±0.016
B	19.0	0.748
C	13.8	0.543
D	14.6±0.4	0.575±0.016
E	1.94	0.076
F	2.14	0.084
G	3.5 MAX,	0.138 MAX.
H	0.45±0.10	0.018 ^{+0.004} _{-0.005}
I	0.06	0.003
J	0.65	0.026
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
Q	C 0.3	C 0.012
R	0.875	0.034
S	1.125	0.044
T	R 3.17	R 0.125
U	12.0	0.472
W	0.75±0.2	0.030 ^{+0.008} _{-0.009}
Z	0.10	0.004

12. RECOMMENDED SOLDERING CONDITIONS

It is recommended that the μPD78P078 be soldered under the following conditions. For details on the recommended soldering conditions, refer to information document “**Semiconductor Device Mounting Technology Manual**” (C10535E).

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 12-1. Soldering Conditions for Surface Mount Devices (1/2)

(1) μPD78P078GC-7EA: 100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	IR35-107-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-2
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per pin row)	—

Note Exposure limit before soldering after the dry pack package is opened. Storage conditions: 25 °C and relative humidity at 65% or less.

Caution Do not use different soldering methods together (except for partial heating method).

Table 12-1. Soldering Conditions for Surface Mount Devices (2/2)

★ (2) μPD78P078GC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	IR35-107-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120 °C or below (package surface temperature), Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	WS60-107-1
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per pin row)	—

Note Exposure limit before soldering after the dry pack package is opened. Storage conditions: 25 °C and relative humidity at 65% or less.

(3) μPD78P078GF-3BA: 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: 3 or less	IR35-00-3
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow processes: 3 or less	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120 °C or below (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C or below, Flow time: 3 seconds or less (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating method).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available to support development of systems using the μPD78P078.

Language Processing Software

RA78K/0 <small>Note 1, 2, 3, 4</small>	Assembler package common to the 78K/0 Series
CC78K/0 <small>Note 1, 2, 3, 4</small>	C compiler package common to the 78K/0 Series
DF78078 <small>Note 1, 2, 3, 4</small>	Device file used for the μPD78078 Subseries
CC78K/0-L <small>Note 1, 2, 3, 4</small>	C compiler library source file common to the 78K/0 Series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P078GC PA-78P078GF PA-78P078KL-T	Programmer adapter connected to the PG-1500
PG-1500 Controller <small>Note 1, 2</small>	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 Series
★ IE-78000-R-A	In-circuit emulator common to the 78K/0 Series (for integrated debugger)
IE-78000-R-BK	Break board common to the 78K/0 Series
IE-78078-R-EM	Emulation board for evaluation of the μPD78078 Subseries
EP-78064GC-R EP-78064GF-R	Emulation probe common to the μPD78064
★ TGC-100SDW	Adapter mounted on board of target system created for 100-pin plastic QFP (GC-7EA, GC-8EU type). TGC-100SDW is a product of Tokyo Eletech Corporation (03-5295-1661). Contact an NEC dealer to purchase this product.
EV-9200GF-100	Socket mounted on board of target system created for 100-pin plastic QFP (GF-3BA type)
SM78K0 <small>Note 5, 6, 7</small>	System simulator common to the 78K/0 Series
ID78K0 <small>Note 4, 5, 6, 7</small>	Integrated debugger for the IE-78000-R-A
SD78K/0 <small>Note 1, 2</small>	Screen debugger for the IE-78000-R
DF78078 <small>Note 1, 2, 4, 5, 6, 7</small>	Device file used for the μPD78078 Subseries

Real-Time OS

RX78K/0 <small>Note 1, 2, 3, 4</small>	Real-time OS used for the 78K/0 Series
MX78K0 <small>Note 1, 2, 3, 4</small>	OS used for the 78K/0 Series

- Notes**
1. PC-9800 Series (MS-DOS™) based
 2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
 3. HP9000 Series 300™ (HP-UX™) based
 4. HP9000 Series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS4800 Series (EWS-UX/V) based
 5. PC-9800 Series (MS-DOS + Windows™) based
 6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
 7. NEWS™ (NEWS-OS™) based

Fuzzy Inference Development Support System

FE9000 <small>Note 1</small> /FE9200 <small>Note 3</small>	Fuzzy knowledge data input tool
FT9080 <small>Note 1</small> /FT9085 <small>Note 2</small>	Translator
FI78K0 <small>Note 1, 2</small>	Fuzzy inference module
FD78K0 <small>Note 1, 2</small>	Fuzzy inference debugger

Notes 1. PC-9800 Series (MS-DOS) based

2. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS) based

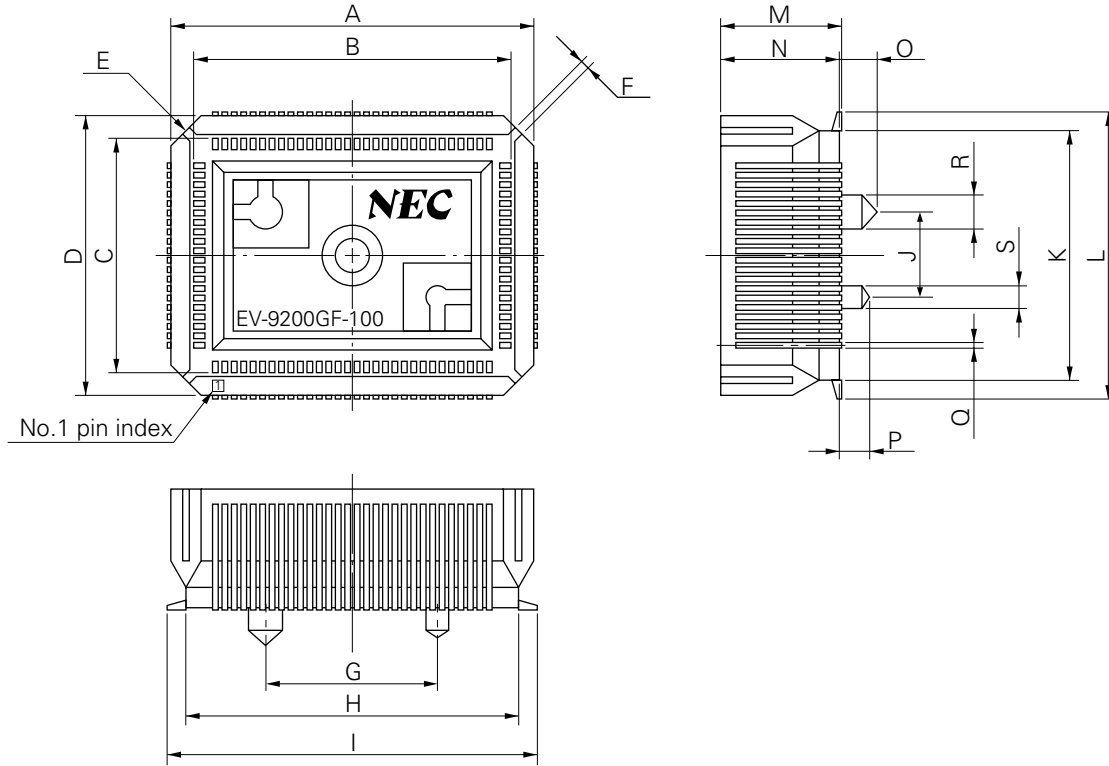
3. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

Remarks 1. Refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.

2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 in combination with the DF78078.

DRAWINGS OF CONVERSION SOCKET (EV-9200GF-100) AND RECOMMENDED FOOTPRINT

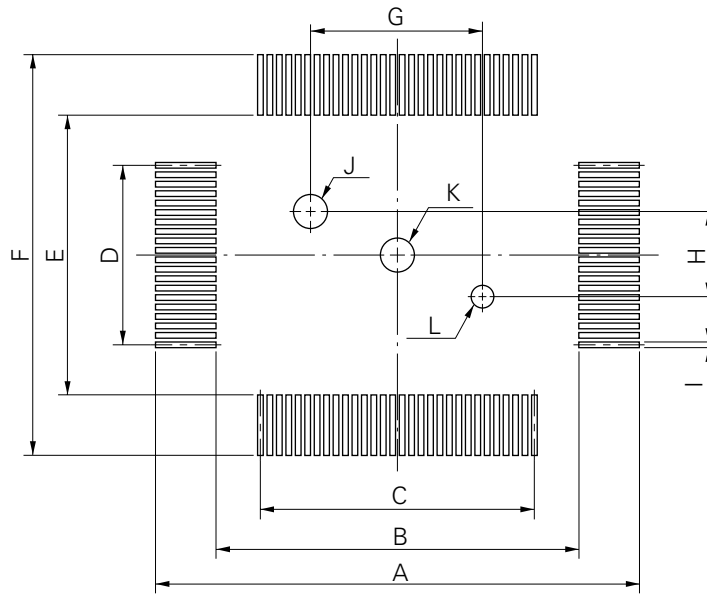
Figure A-1. Drawing of EV-9200GF-100 (for Reference only)



EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	0.76
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. Recommended Footprint of EV-9200GF-100 (for Reference only)



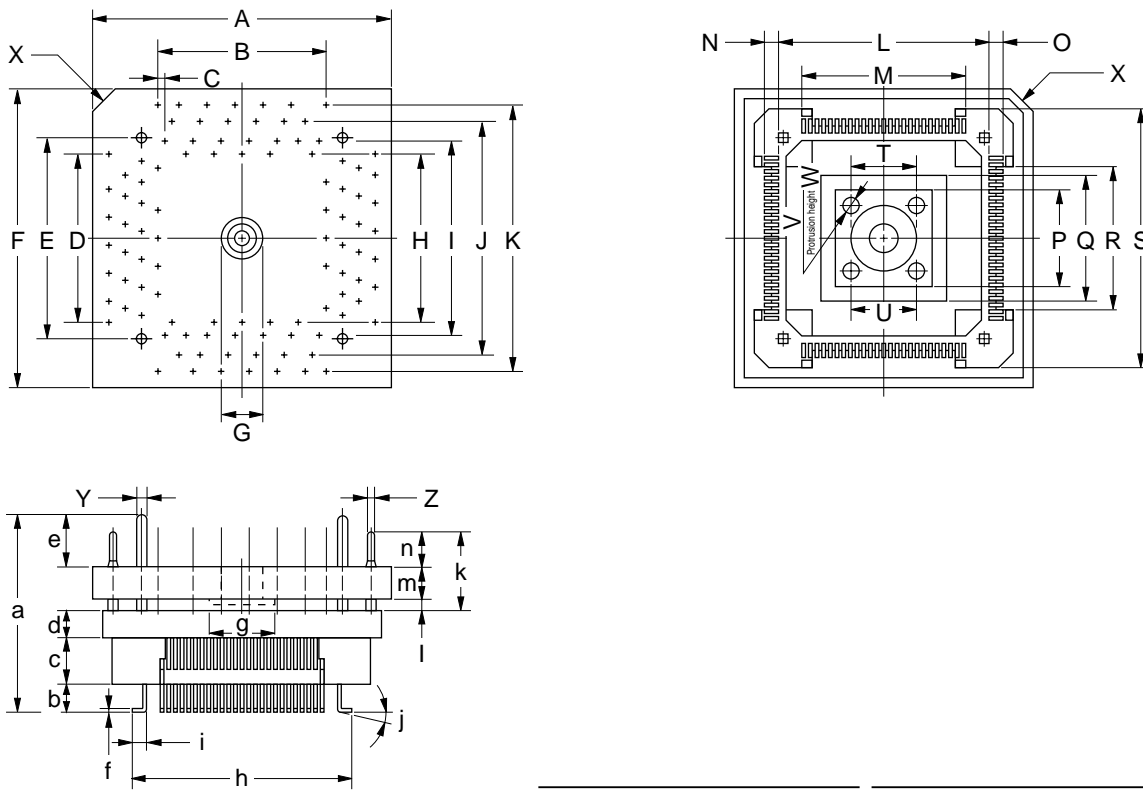
EV-9200GF-100-P1

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65 \pm 0.02 \times 29 = 18.85 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 1.142 = 0.742^{+0.002}_{-0.002}$
D	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.3$	$\phi 0.091$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

DRAWING OF CONVERSION ADAPTER (TGC-100SDW)

Figure A-3. Drawing of TGC-100SDW (for Reference only)



ITEM	MILLIMETERS	INCHES	ITEM	MILLIMETERS	INCHES
A	21.55	0.848	a	14.45	0.569
B	0.5x24=12	0.020x0.945=0.472	b	1.85±0.25	0.073±0.010
C	0.5	0.020	c	3.5	0.138
D	0.5x24=12	0.020x0.945=0.472	d	2.0	0.079
E	15.0	0.591	e	3.9	0.154
F	21.55	0.848	f	0.25	0.010
G	φ3.55	φ0.140	g	φ4.5	φ0.177
H	10.9	0.429	h	16.0	0.630
I	13.3	0.524	i	1.125±0.3	0.044±0.012
J	15.7	0.618	j	0-5°	0.000-0.197°
K	18.1	0.713	k	5.9	0.232
L	13.75	0.541	l	0.8	0.031
M	0.5x24=12.0	0.020x0.945=0.472	m	2.4	0.094
N	1.125±0.3	0.044±0.012	n	2.7	0.106
O	1.125±0.2	0.044±0.008			
P	7.5	0.295			
Q	10.0	0.394			
R	11.3	0.445			
S	18.1	0.713			
T	φ5.0	φ0.197			
U	5.0	0.197			
V	4-φ1.3	4-φ0.051			
W	1.8	0.071			
X	C 2.0	C 0.079			
Y	φ0.9	φ0.035			
Z	φ0.3	φ0.012			

TGC-100SDW-G1E

note: Product by TOKYO ELETECH CORPORATION.

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD78078, 78078Y Subseries User's Manual	U10641J	U10641E
μPD78076, 78078 Data Sheet	U10167J	U10167E
μPD78075B, 78075BY Subseries User's Manual	U12560J	Planned
μPD78074B, 78075B Data Sheet	U12017J	U12017E
μPD78P078 Data Sheet	U10168J	This document
78K/0 Series User's Manual—Instructions	U12326J	U12326E
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—
μPD78078 Subseries Special Function Register Table	IEM-5607	—
78K/0 Series Application Note—Basic (III)	IEU-767	U10182E

Documents Related to Development Tools (User's Manual) (1/2)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		EEU-810	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		U10775J	U10775E
EP-78064		EEU-934	EEU-1469
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E

Caution The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

Documents Related to Development Tools (User's Manual) (2/2)

Document Name		Document No.	
		Japanese	English
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basic	U11537J	—
	Installation	U11536J	—
78K/0 Series OS MX78K0	Basic	U12257J	—
Fuzzy Knowledge Data Input Tools		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Microcomputer Product Series Guide	U11416J	—

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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