SANYO

4M-Bit (512k × 8) Flash EEPROM

Features

CMOS Flash EEPROM Technology
Single 3.3-Volt Read and Write Operations
Sector Erase Capability: 256 Bytes per sector
Fast Access Time: 200 ns
Low Power Consumption
Active Current(Read): 10 mA (Max.)
Standby Current: 15 μA (Max.)
High Read/Write Reliability
Sector-write Endurance Cycles: 10^4
10 Years Data Retention
Latched Address and Data
Self-timed Erase and Programming
Byte Programming: 40μs (Max.)
End of Write Detection:Toggle Bit/ $\overline{\text{DATA}}$ Polling
Hardware/Software Data Protection
JEDEC Standard Byte-Wide EEPROM Pinouts
Packages Available
LE28FV4001CTS: 32-pin TSOP Normal(8×14mm)

Product Description

The LE28FV4001C is a 512K ×8 CMOS sector erase, byte program EEPROM. The LE28FV4001C is manufactured using SANYO's proprietary, high performance CMOS Flash EEPROM technology. Breakthroughs in EEPROM cell design and process architecture attain better reliability and manufacturability compared with conventional approaches. The LE28FV4001C erases and programs with a 3.3-volt only power supply. LE28FV4001C conforms to JEDEC standard pinouts for byte wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance programming, the LE28FV4001C typically byte programs in 30μs. The LE28FV4001C typically sector (256 bytes) erases in 2ms. Both program and erase times can be optimized using interface feature such as Toggle bit or $\overline{\text{DATA}}$ Polling to indicate the completion of the write cycle. To protect against an inadvertent write, the LE28FV4001C has on chip hardware and software date protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the LE28FV4001C is offered with a guaranteed sector write endurance of 10^4 cycles. Data retention is rated greater then 10 years.

The LE28FV4001C is best suited for applications that require reprogrammable nonvolatile mass storage of program or data memory. For all system applications, the LE28FV4001C significantly improves performance and reliability, while lowering power consumption when compared with floppy diskettes or EPROM approaches. EEPROM technology makes possible convenient and economical updating of codes and control programs on-line. The LE28FV4001C improves flexibility, while lowering the cost, of program and configuration storage applications.

Figure 1 shows the pin assignments for the 32 lead Plastic TSOP packages. Figure 2 shows the functional block diagram of the LE28FV4001C. Pin description and operation modes can be found in Tables 1 through 3.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting $\overline{\text{WE}}$ low while keeping $\overline{\text{CE}}$ low. The address bus is latched on the falling edge of $\overline{\text{WE}}$, $\overline{\text{CE}}$, whichever occurs last. The data bus is latched on the rising edge of $\overline{\text{WE}}$, $\overline{\text{CE}}$, whichever occurs first. However, during the software write protection sequence the address are latched on the rising edge of $\overline{\text{OE}}$ or $\overline{\text{CE}}$, whichever occurs first.

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This preliminary specification is subject to change without notice.

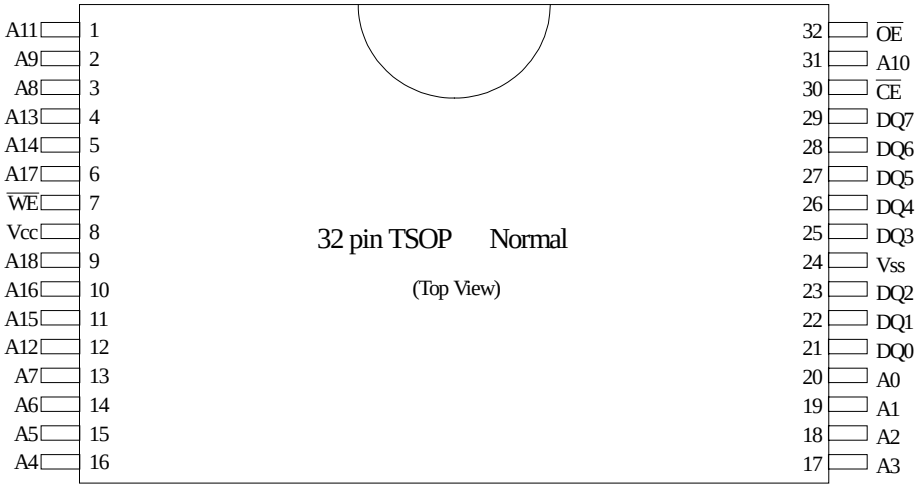


Figure 1: Pin Assignments for 32-pin Plastic TSOP

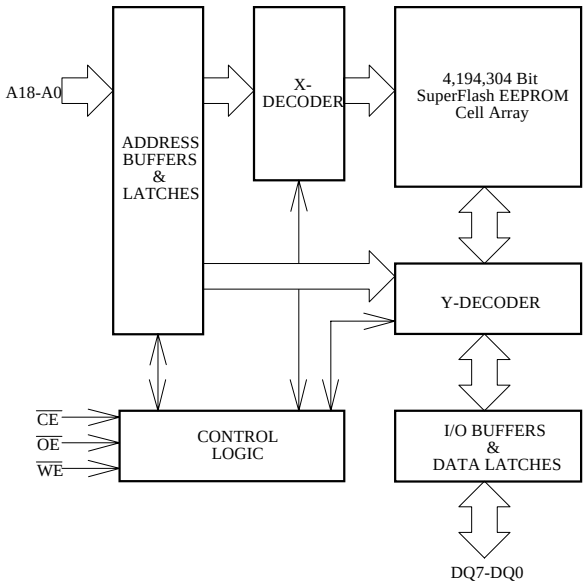


Figure 2: Functional Block Diagram of LE28FV4001C

Table 1: Pin Description

Symbol	Pin Name	Functions
A18-A0	Address Inputs	To provide memory address. Address are internally latched during write cycle.
DQ7-DQ0	Data Input/Output	To output data during read cycle and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when $\overline{OE}$ or $\overline{CE}$ is high.
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low. Deselects and puts the device to standby when $\overline{CE}$ is high.
$\overline{OE}$	Output Enable	To activate the data output buffers. $\overline{OE}$ is active low.
$\overline{WE}$	Write Enable	To activate the write operation. $\overline{WE}$ is active low.
V_{DD}	Power Supply	To provide 3.3V±0.3V supply.
V_{SS}	Ground	

Table 2: Operation Modes Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High-Z	X
Write Inhibit	X	V_{IL}	X	High-Z / D_{OUT}	X
	X	X	V_{IH}	High-Z / D_{OUT}	X
Product ID	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A18-A1=V_{IL}, A9=12V, A0=V_{IL}
				Device Code (04)	A18-A1=V_{IL}, A9=12V, A0=V_{IH}

Table 3: Command Summary

Command	Required Cycle	Setup Command Cycle			Execute Command Cycle			SDP
		Operation	Address	Data	Operation	Address	Data	
Sector_Erase	2	Write	X	20H	Write	SA	D0H	N
Byte_Program	2	Write	X	10H	Write	PA	PD	N
Reset	1	Write	X	FFH				Y
Read_ID	3	Write	X	90H	Read	(7)	(7)	Y
Software_Data_Unprotect (6)	7							
Software_Data_Protect (6)	7							

Definitions for Table 3:

1. Type definitions : X=high or low
2. Address definitions : SA=Sector Address=A18-A8 ; sector size=256byte ; A7-A0=X for this command
3. Address definitions : PA=Program Address=A18-A0
4. Data definition : PD=Program Data, H=number in hex.
5. SDP=Software Data Protect mode using 7-Read-Cycle-Sequence.
   Y=the operation can be executed with software data protect enabled. N=the operation cannot be executed with software data protect enabled.
6. Refer to Figure 11 and 12 for the 7-Read-Cycle-Sequence Software Data Protection.
7. Address 0000H retrieves the manufacturer code of BF(Hex), address 0001H retrieves the device code of 04(Hex).

Command Definition

Table 3 contains a command list and a brief summary of the commands.

The following is a detailed description of the options initiated by each command.

The LE28FV4001C has to have the Software Data Unprotect Sequence executed prior a Byte Program or Erase in order to perform those functions.

Sector_Erase Operation

The Sector_Erase operation is initiated by a setup command and an execute command. The setup command stages the device for electrical erasing of all bytes within a sector. A sector contains 256 bytes. This sector erasability enhances the flexibility and usefulness of the LE28FV4001C, since most applications only need to change a small number of bytes or sectors, not the entire chip. The setup command is performed by writing (20H) to the device. To execute the sector-erase operation, the execute command (D0H) must be written to the device. The erase operation begins with the rising edge of the $\overline{WE}$ pulse and terminated automatically by using an internal timer. See Figure 8 for timing waveforms.

The two-step sequence of a setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Sector_Erase Flowchart Description

Fast and Reliable erasing of the memory contents within a sector is accomplished by following the sector erase flowchart as shown in Figure 3. The entire procedure consists of the execution of two commands. The Sector_Erase operation will terminate after a maximum of 4ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 4ms time-out, the sector may not be completely erased. An erase command can be reissued as many times an necessary to complete the erase operation. The LE28FV4001C cannot be “overerased”.

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (10H).

Once the program setup is performed, programming is executed by the next $\overline{WE}$ pulse. See Figure 6 and 7 for timing waveforms. The address bus is latched on the falling edge of $\overline{WE}$, $\overline{CE}$, or the rising edge of $\overline{OE}$, whichever occurs first. The programming operation begins with either the rising edge of $\overline{WE}$, $\overline{CE}$, whichever occurs first. The programming operation is terminated automatically by an internal timer. See the programming characteristics and waveforms for details, Figures 4, 6 and 7.

The two-step sequence of a setup command followed by an execute command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flow Chart Description

Programming data into the device is accomplished by following the Byte_Program flowchart as shown in Figure 3. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of $\overline{WE}$, $\overline{CE}$, whichever occurs last. The data bus is latched on the rising edge of $\overline{WE}$, $\overline{CE}$, whichever occurs first, and begins the program operation. The end of write can be detected using either the $\overline{DATA}$ polling or Toggle bit.

Reset Operation

A Reset Command is provided as a means to safely abort the erase or program command sequences. Following either setup command (erase or program) with a write of (FFH) will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The reset command dose not enable write protect. See figure 10 for timing waveforms.

Read Operation

The read operation is initiated by setting $\overline{CE}$, $\overline{OE}$ and $\overline{WE}$ into the read mode. See Figure 5 for read memory timing waveforms and Table 2 for the read mode. Read cycles from the host retrieve data from the array. The device remains enabled for read until another operating mode is accessed.

During initial power-up, the device is in the read mode and is write protected. The device must be unprotected in order to execute a write operation

The read operation is controlled by $\overline{OE}$ and $\overline{CE}$ at logic low. When $\overline{CE}$ is high, the chip is deselected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate to the output pins. The data bus is in a high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high.

Read_ID Operation

The Read_ID operation is initiated by writing a single command (90H). A read of address 0000H will outputs the manufacturer's code (BFH). A read of address 0001H will outputs the device code (04H).Any other valid command will terminate this operation.

Data Protection from Inadvertent Writes

In order to protect the integrity of nonvolatile data storage, the LE28FV4001C provides hardware and software features to prevent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Write Protection

The LE28FV4001C is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibit the write operation.
2. Noise and Glitch Protection: Write operations are initiated when the $\overline{WE}$ pulse width is less than 15 ns.
3. After power-up the device is in the read mode and the device is in the write protect state.

Software Data Protection

Provisions have been made to further prevent inadvertent writes through software. In order to perform the write functions of erase or program, a two-step command sequence consisting of a setup command followed by an execute command avoids inadvertent erasing or programming of the device.

The LE28FV4001C will default to write protect after power-up. A sequence of seven consecutive reads at specified device addresses will unprotect the device. The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address has to be latched in the rising edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also, refer to Figure 11, 12 for the 7-read-sequence Software Write Protection. The DQ pins can be in any state (i.e., high, low, or High-Z).

End of Write Detection

Detection of where a write cycle ended is necessary to optimize system performance. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the $\overline{DATA}$ polling bit; 2) monitoring the Toggle bit; 3) by two successive reads of the same data. These three detection mechanisms are described below.

$\overline{DATA}$ Polling (DQ7)

The LE28FV4001C features $\overline{DATA}$ Polling to indicate the and of a write cycle. During a write cycle, any attempt to read the last byte loaded will result in the complement of the loaded data on DQ7. Once the write cycle is completed, DQ7 will show true data. See Figure 13 for timing waveforms. In order for $\overline{DATA}$ Polling to function correctly, the byte being polled must be erased prior to programming.

Toggle Bit (DQ6)

An alternate means for determining the end of a write cycle is by monitoring the Toggle Bit DQ6. During a write operation, successive attempts to read data from the device will result in DQ6 toggling between logic "1" (high) and "0" (low). Once the write cycle has completed, DQ6 will stop toggling and valid data will be read. The Toggle Bit may be monitored any time during the write cycle. See Figure 14 for timing waveforms.

Successive Reads

An alternate means for determining the end of a write cycle is by reading the same address for two consecutive data matches.

Product Identification

The Product Identification mode identifies the device and manufacturer as SANYO. This mode may be accessed by hardware or software operations. The hardware operation is typically used by an external programming to identify the correct algorithm for the SANYO LE28FV4001C. Users may wish to use the software operation to identify the device (i.e., using the device code). For details, see Table 2 for the hardware operation. The manufacturer and device codes are the same for both operations.

Notes for Operation

During power up, the device's state should be the write inhibition mode. (During power up, the device's state should be $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IL}$ or $\overline{WE}=V_{IH}$)

If $\overline{CE}=\overline{WE}=V_{IL}$ and $\overline{OE}=V_{IH}$ during power up, RESET command should be asserted before operation.

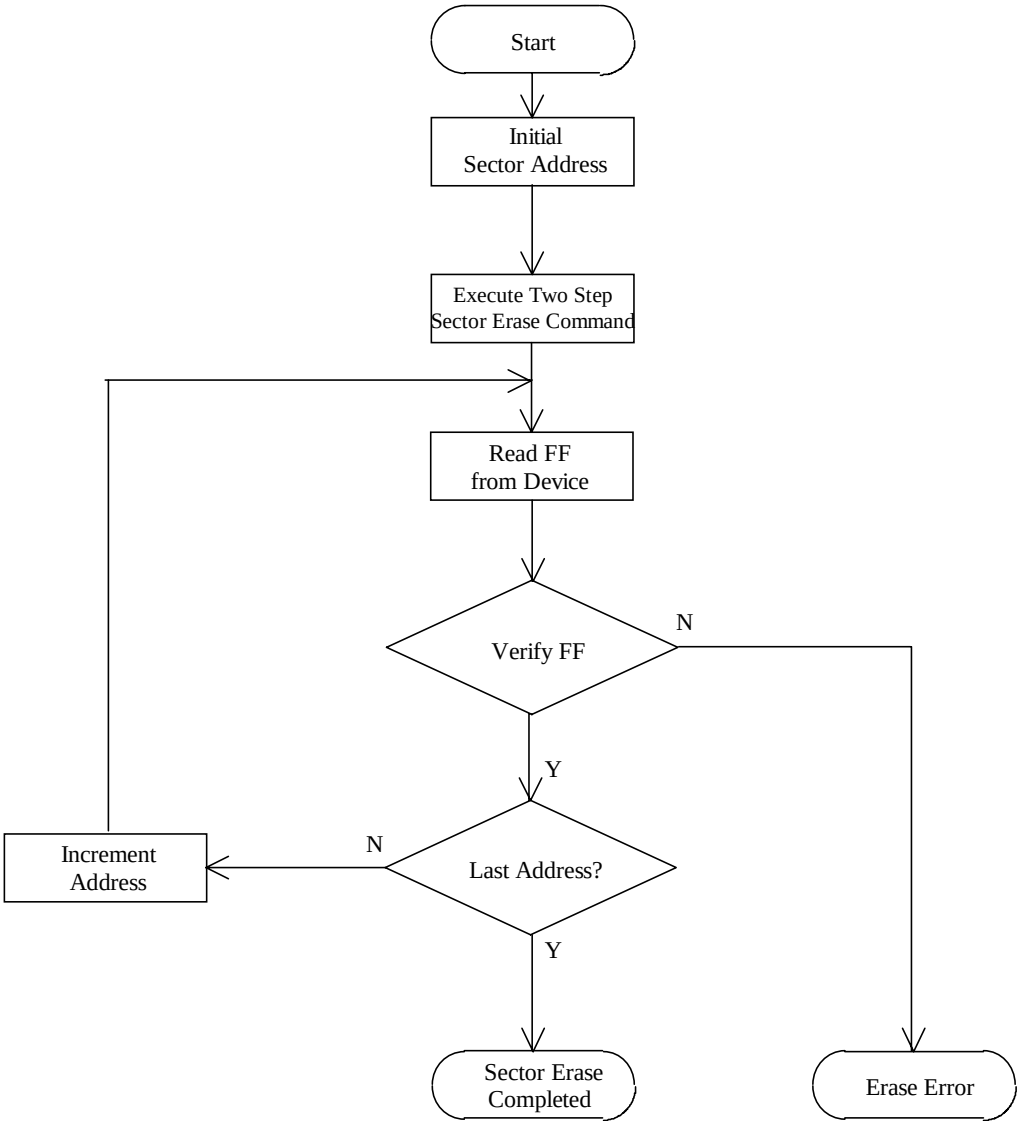


Figure 3: Sector_Erase Flowchart

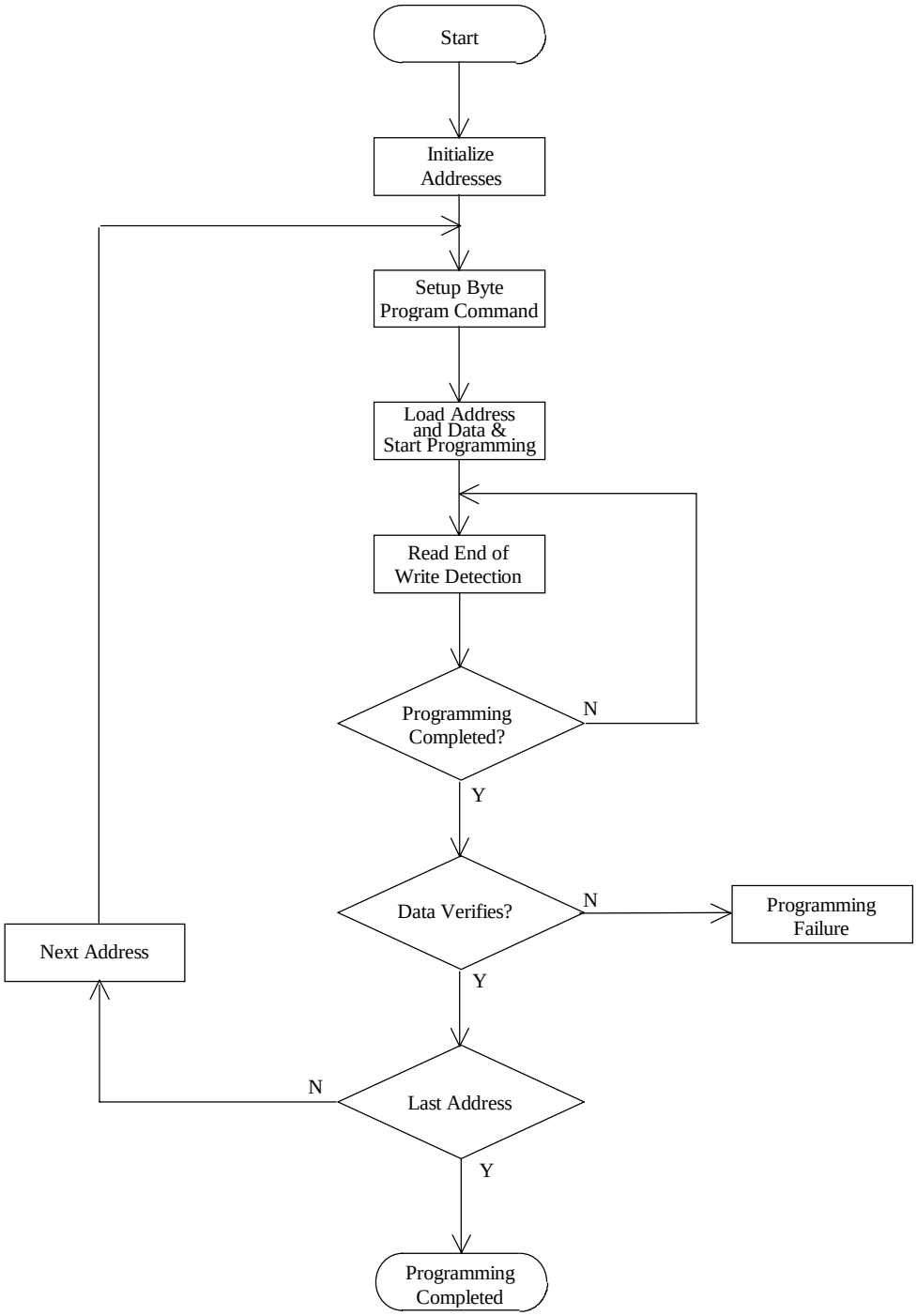


Figure 4: Byte_Program Flowchart

Absolute Maximum Stress Ratings

Temperature Under Bias.....-55 °C ~ 125 °C
Storage Temperature.....-65 °C ~ 150 °C
D.C. Voltage on Any Pin to Grand Potential.....-0.5V ~ V_{CC}+0.5V
Transient Voltage (<20ns) on any Pin to Grand Potential .....-1.0V ~ V_{CC}+1.0V
Voltage on A9 to Grand Potential.....-0.5V ~ 14.0V

Operating Range

Ambient Temperature.....0 °C ~ 70 °C
Supply Voltage (V_{DD}) .....3.0V ~ 3.6V

DC Operating Characteristics

Symbol	Parameter	Limit			Units	Test Condition
		Min.	Typ.	Max.		
I_{CCR}	Power Supply Current (Read)			10	mA	$\overline{CE}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ =V_{IH}, all DQs open Address inputs=V_{IH} / V_{IL}, at f=1/tRC, V_{DD}=V_{DD} max.
I_{CCW}	Power Supply Current (Write)			25	mA	$\overline{CE}$ = $\overline{WE}$ =V_{IL}, $\overline{OE}$ =V_{IH}, V_{DD}=V_{DD} max.
I_{SB2}	Standby V_{DD} Current (CMOS input)			15	µA	$\overline{CE}$ =V_{DD}-0.3V, V_{DD}=V_{DD} max.
I_{LI}	Input Leakage Current			10	µA	V_{IN}=V_{SS}~V_{DD}, V_{DD}=V_{DD} max.
I_{LO}	Output Leakage Current			10	µA	V_{OUT}=Vss~V_{DD}, V_{DD}=V_{DD} max.
V_{IL}	Input Low Voltage	-0.3		0.6	V	V_{DD}=V_{DD} max.
V_{IH}	Input High Voltage	2.0		Vcc+0.3	V	V_{DD}=V_{DD} max.
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=100µA, V_{DD}=V_{DD} min.
V_{OH}	Output High Voltage	2.4			V	I_{OH}= -100µA, V_{DD}=V_{DD} min.

Power-up Timing

Symbol	Parameter	Minimum	Units
tPU_READ	Power-up to Read Operation	10	ms
tPU_WRITE	Power-up to Write Operation	10	ms

Capacitance (Ta=25°C, f=1MHz)

Symbol	Descriptions	Maximum	Units	Test Condition
C_{DQ}	DQ Pin Capacitance	12	pF	V_{DQ} = 0V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V

AC Characteristics

Read Cycle Timing Parameters

Symbol	Parameter	-20		Units
		Min.	Max.	
tRC	Read Cycle Time	200		ns
tCE	Chip Enable Access Time		200	ns
tAA	Address Access Time		200	ns
tOE	Output Enable Access Time		100	ns
tCLZ	$\overline{CE}$ Low to Active Output	0		ns
tOLZ	$\overline{OE}$ Low to Active Output	0		ns
tCHZ	$\overline{CE}$ High to High-Z Output		60	ns
tOHZ	$\overline{OE}$ High to High-Z Output		60	ns
tOH	Output Hold Time	0		ns

Erase/Program Cycle Timing Parameters

Symbol	Parameter	-20		Units
		Min.	Max.	
tSE	Sector Erase Cycle Time		4	ms
tBP	Byte Program Cycle Time		40	µs
tAS	Address Setup Time	10		ns
tAH	Address Hold Time	50		ns
tCS	Chip Enable Setup Time	0		ns
tCH	Chip Enable Hold Time	0		ns
tOES	Output Enable Setup Time from $\overline{WE}$	10		ns
tOEH	Output Enable Hold Time from $\overline{WE}$	10		ns
tCP	Write Pulse Width ($\overline{CE}$)	100		ns
tWP	Write Pulse Width	100		ns
tCPH	$\overline{CE}$ High Pulse Width	50		ns
tWPH	$\overline{WE}$ High Pulse Width	50		ns
tDS	Data Setup Time	50		ns
tDH	Data Hold Time	10		ns
tRST	Reset Command Recovery Time		4	µs
tPCP	Protect Chip Enable Pulse Width	100		ns
tPCH	Protect Chip Enable High Time	150		ns
tPAS	Protect Address Setup Time	40		ns
tPAH	Protect Address Hold Time	100		ns

Note: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Test Conditions

Input Load Levels .....1TTL Gate and CL=30pF
Input Rise/Fall Time 10ns

Figure 5: Read Cycle Diagram

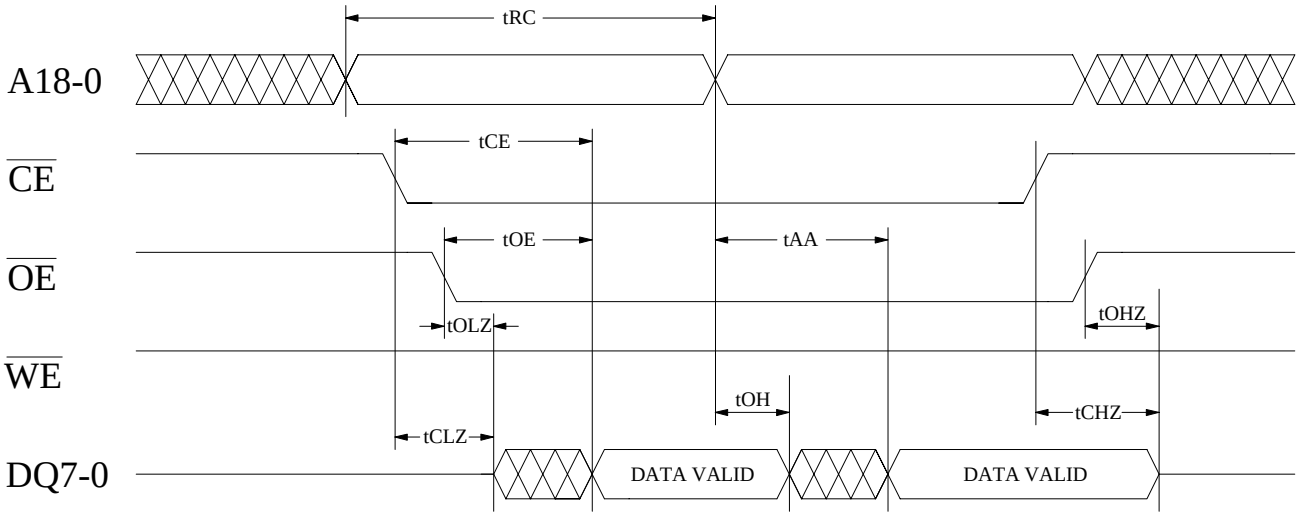


Figure 6: $\overline{WE}$ Controlled Write Cycle Timing Diagram

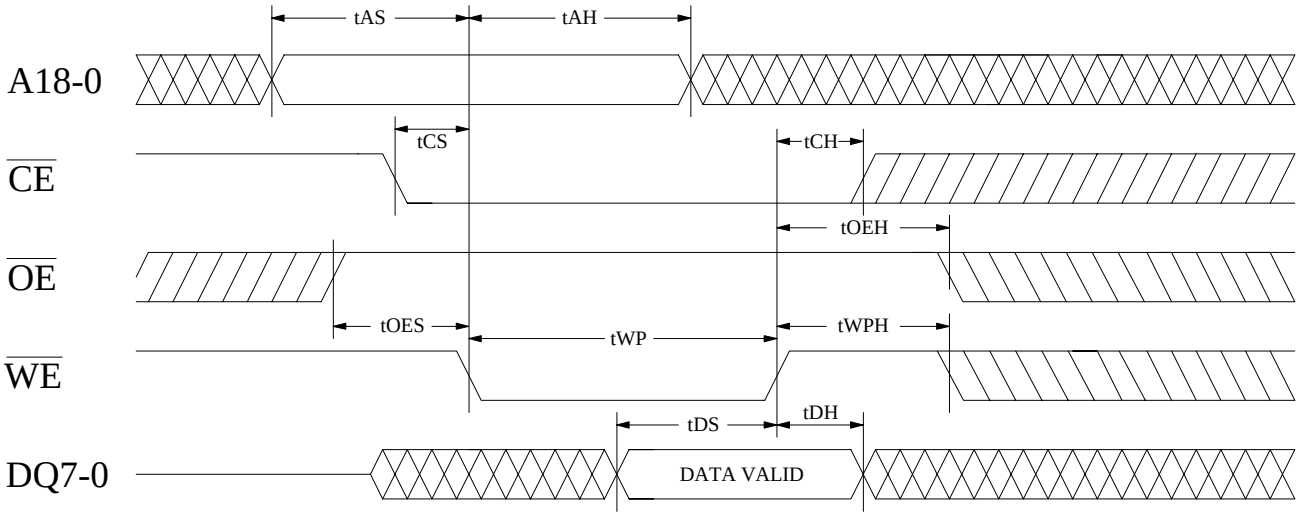


Figure 7: $\overline{CE}$ Controlled Write Cycle Timing Diagram

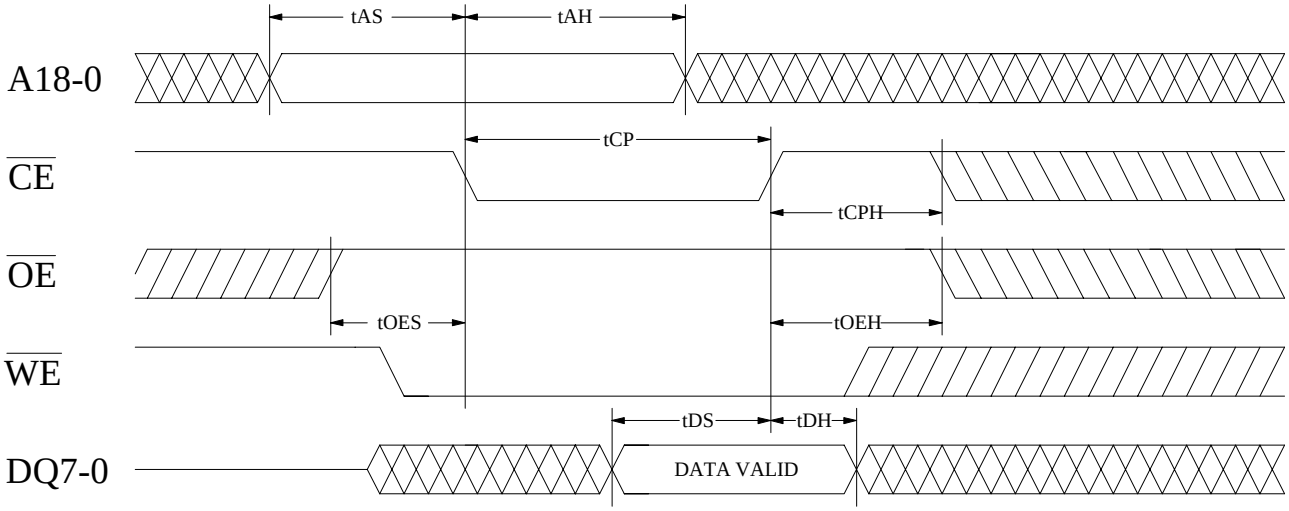


Figure 8: Sector Erase Timing Diagram

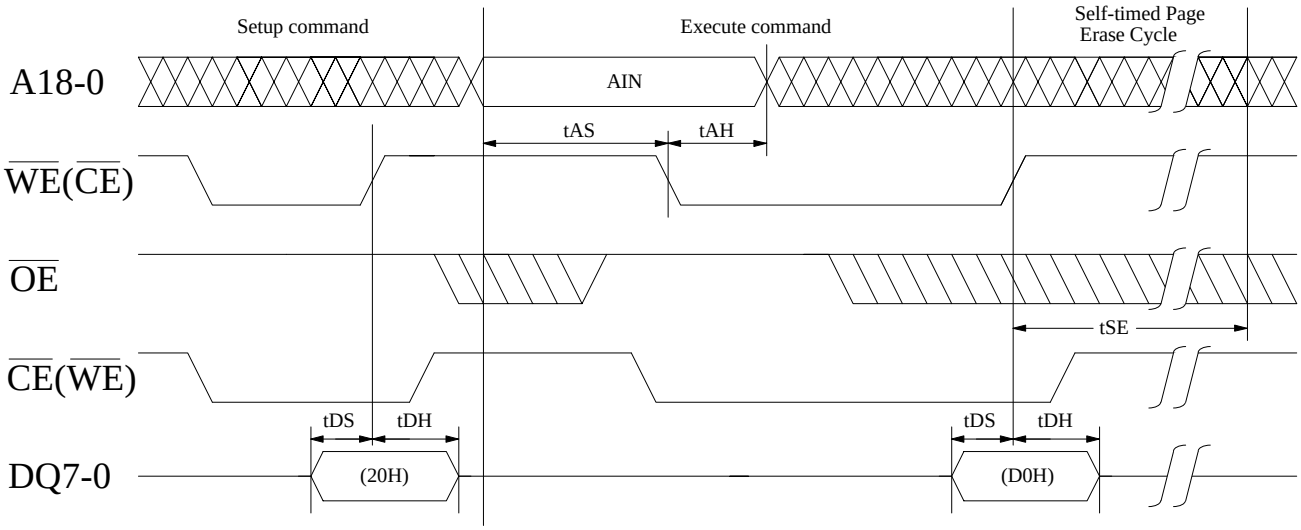


Figure 9: Byte Program Timing Diagram

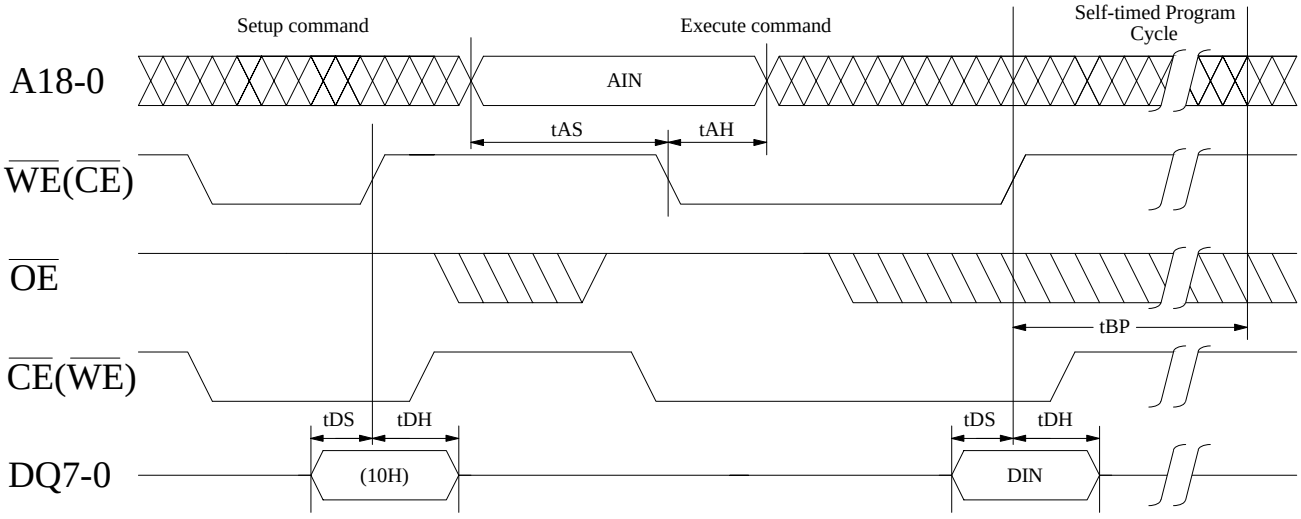


Figure 10: Reset Command Timing Diagram

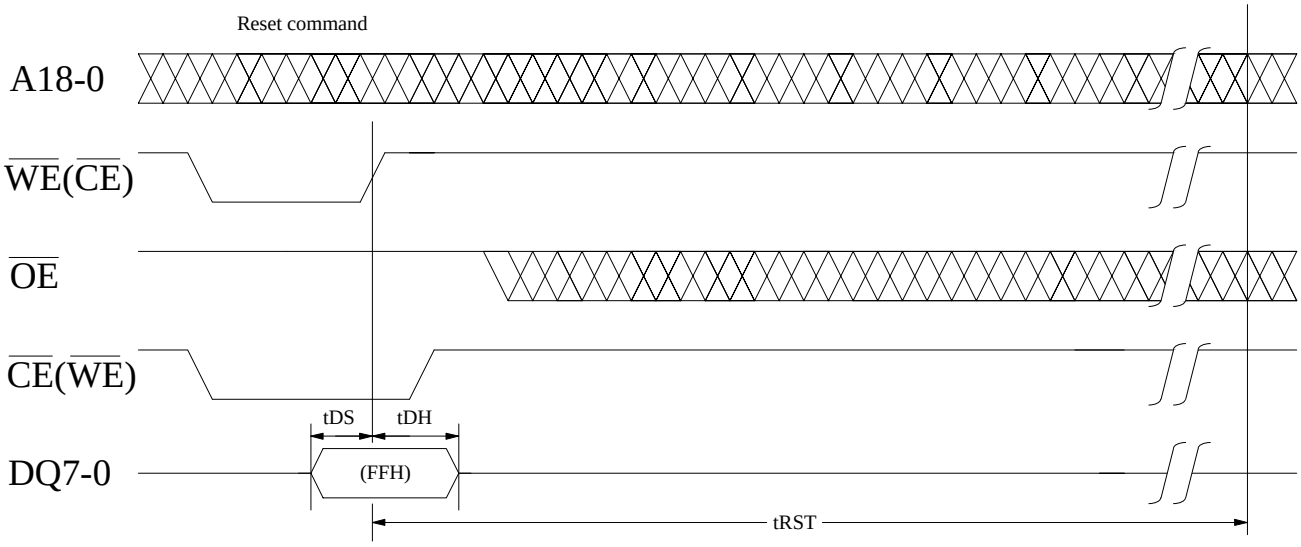
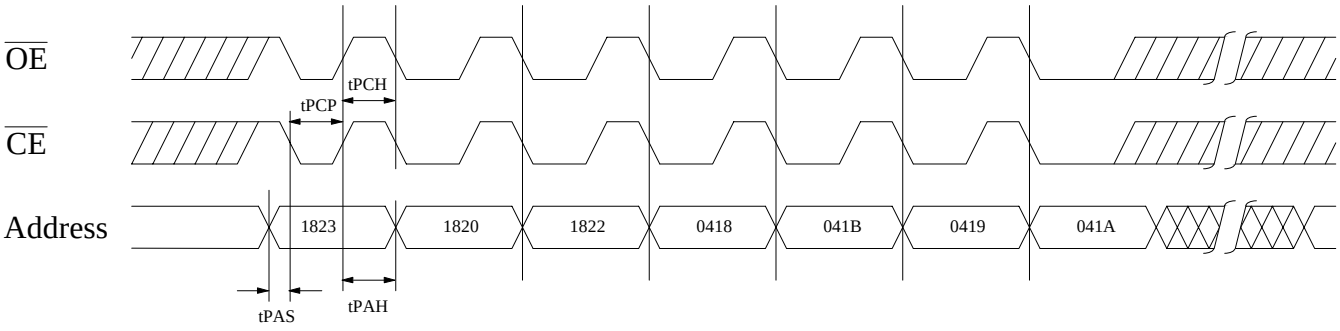


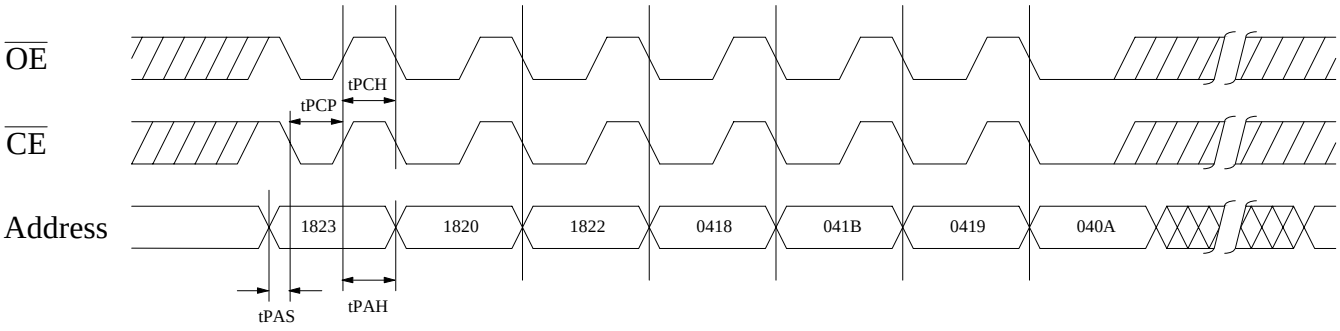
Figure 11: Software Data Unprotect Sequence



Notes on Figure 11

1. The address is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is earlier.
2. Pins A16 to A18 should be at either V_{IL} or V_{IH}

Figure 12: Software Data Protect Sequence



Notes on Figure 12

1. The address is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is earlier.
2. Pins A16 to A18 should be at either V_{IL} or V_{IH}

Figure 13: $\overline{\text{DATA}}$ Polling Timing Diagram (DQ7)

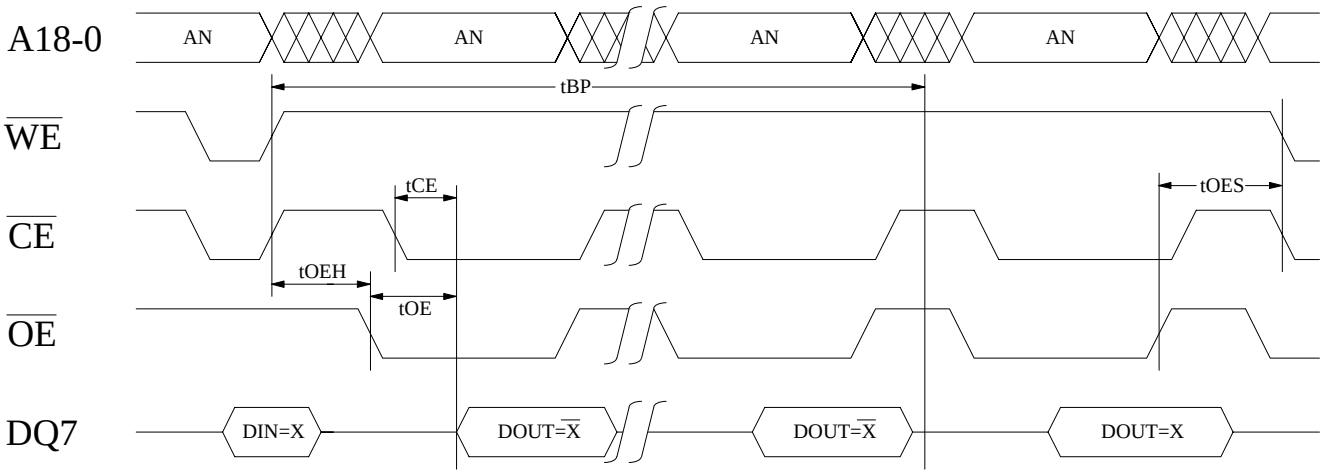
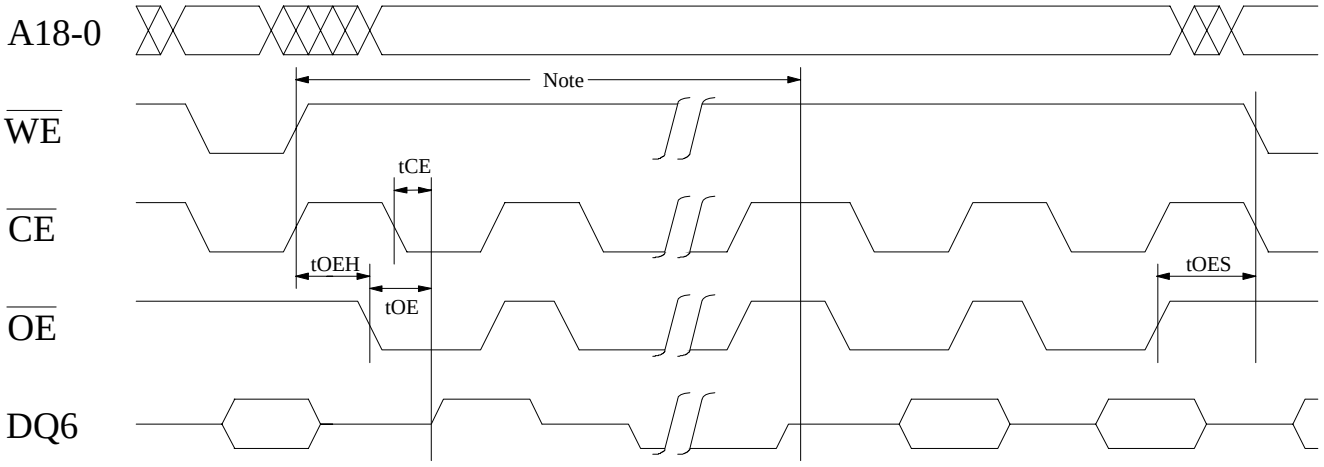


Figure 14: Toggle Bit Timing Diagram (DQ6)

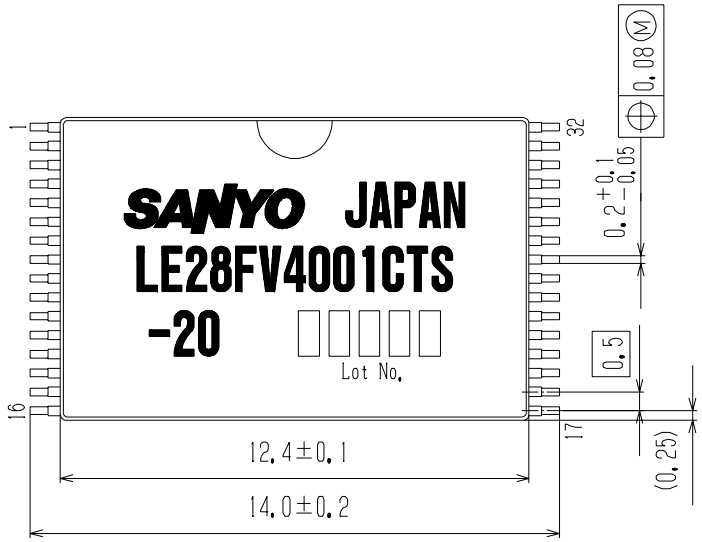


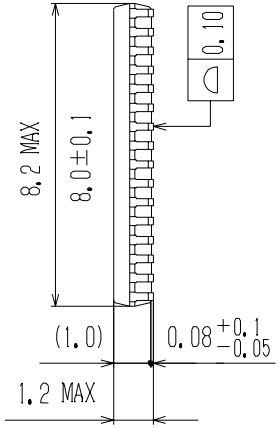
Note: This time interval signal can be tSE or tBP, depending upon the selected operation mode.

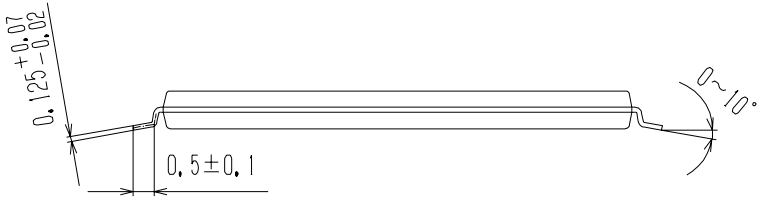
OUTLINE DRAWING

SANYO

SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass(g)	Measure	Unit
TSOP32DA(8×14)	———	———	LE28FV4001CTS-20	S−041	0.25	5/1	mm







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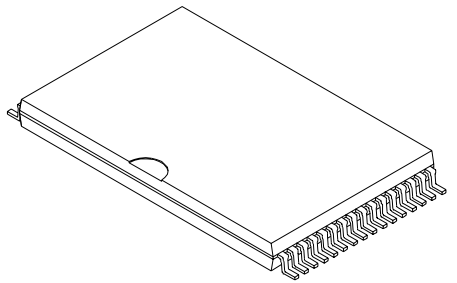
Appearance



TSOP32DA(8×14)

REVISION : 2

SANYO : Thin Small Outline Package 32Pin Plastic