1M-BIT, 2M-BIT, 4M-BIT AND 8M-BIT 2.5V SERIAL FLASH MEMORY WITH 4KB SECTORS AND DUAL OUTPUT SPI

Table of Contents

1. GENERAL DESCRIPTION

The W25X10L (1M-bit), W25X20L (2M-bit), W25X40L (4M-bit) and W25X80L (8M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25X series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code download applications as well as storing voice, text and data. The devices operate on a single 2.5V (a range of 2.3V to 3.3V) power supply with current consumption as low as 5mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25X10L/20L/40L/80L array is organized into 512/1024/2048/4096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instruction. Pages can be erased in groups of 16 (sector erase), groups of 256 (block erase) or the entire chip (chip erase). The W25X10L/20L/40L/80L has 32/64/128/256 erasable sectors and 2/4/8/16 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25X10L/20L/40L/80L supports the standard Serial Peripheral Interface (SPI), and a high performance dual output SPI and low voltage operation using four pins: Serial Clock, Chip Select, Serial Data I/O and Serial Data Out. SPI clock frequencies of up to 40MHz are supported allowing equivalent clock rates of 80MHz when using the Fast Read Dual Output instruction. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protect, with top or bottom array control features, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification.

2. FEATURES

- **Family of Serial Flash Memories**
  - W25X10L: 1M-bit / 128K-byte (131,072)
  - W25X20L: 2M-bit / 256K-byte (262,144)
  - W25X40L: 4M-bit / 512K-byte (524,288)
  - W25X80L: 8M-bit / 1M-byte (1,048,576)
  - 256-bytes per programmable page
  - Uniform 4K-byte Sectors / 64K-byte Blocks
- **SPI with Single or Dual Outputs**
  - Clock, Chip Select, Data I/O, Data Out
  - Optional Hold function for SPI flexibility
- **Data Transfer up to 80M-bits / second**
  - Clock operation to 40MHz
  - Fast Read Dual Output instruction
  - Auto-increment Read capability
- **Flexible Architecture with 4KB sectors**
  - Sector Erase (4K-byte)
  - Block Erase (64K-byte)
  - Page program up to 256 bytes <2ms
  - Minimum 100,000 erase/write cycles
  - 20-year retention
- **Low Power Consumption, Wide Temperature Range**
  - Single 2.3 to 3.3V supply
  - 5mA active current, 1µA Power-down (typ)
  - 0° to +85°C operating range
- **Software and Hardware Write Protection**
  - Write-Protect all or portion of memory
  - Enable/Disable protection with /WP pin
  - Top or bottom array protection
- **Space Efficient Packaging**
  - 8-pin SOIC 150-mil (W25X10L/20L/40L)
  - 8-pin SOIC 208-mil (W25X40L/80L)
  - 8-pin WSON 6x5-mm (W25X10L/20L/40L/80L)

3. PIN CONFIGURATION SOIC 150-MIL

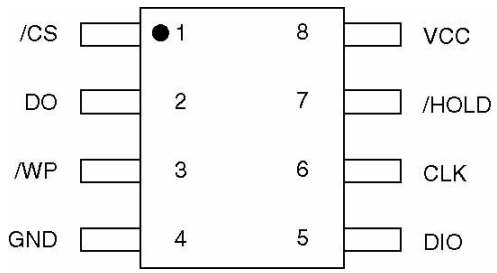


Figure 1a. W25X10L, W25X20L and W25X40L Pin Assignments, 8-pin SOIC (Package Code SN)

4. PIN CONFIGURATION SOIC 208-MIL

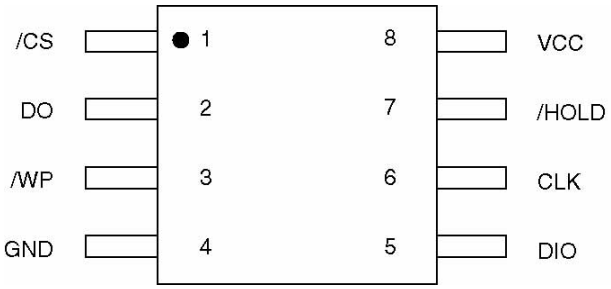


Figure 1b. W25X40L and W25X80L Pin Assignments, 8-pin SOIC (Package Code SS)

5. PIN CONFIGURATION WSON 6X5-MM

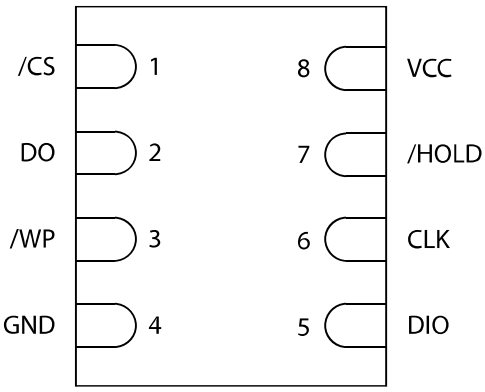


Figure 1c. W25X10L, W25X20L, W25X40L and W25X80L Pin Assignments, 8-pin WSON (Package Code ZP)

6. PIN DESCRIPTION

SOIC 150-mil, SOIC 208-mil, and WSON 6x5-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO	O	Data Output
3	/WP	I	Write Protect Input
4	GND		Ground
5	DIO	I/O	Data Input / Output
6	CLK	I	Serial Clock Input
7	/HOLD	I	Hold Input
8	VCC		Power Supply

6.1 Package Types

At the time this data sheet was published not all package types had been finalized. Contact Winbond to confirm availability of these packages before designing to this specification. The W25X10L, W25X20L and W25X40L are offered in an 8-pin plastic 150-mil width SOIC (package code SN) as shown in figure 1a. The W25X40L and W25X80L is offered in an 8-pin plastic 208-mil width SOIC (package code SS) as shown in figure 1b. All parts will be offered in 6x5-mm WSON (package code ZP) Package diagrams and dimensions are illustrated at the end of this data sheet.

6.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 20). If needed a pull-up resister on /CS can be used to accomplish this.

6.3 Serial Data Output (DO)

The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

6.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (BP2, BP1, and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low.

6.5 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DIO and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. (“See Hold function”)

6.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. (“See SPI Operations”)

6.7 Serial Data Input / Output (DIO)

The SPI Serial Data Input/Output (DIO) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin. The DIO pin is also used as an output when the Fast Read Dual Output instruction is executed.

7. BLOCK DIAGRAM

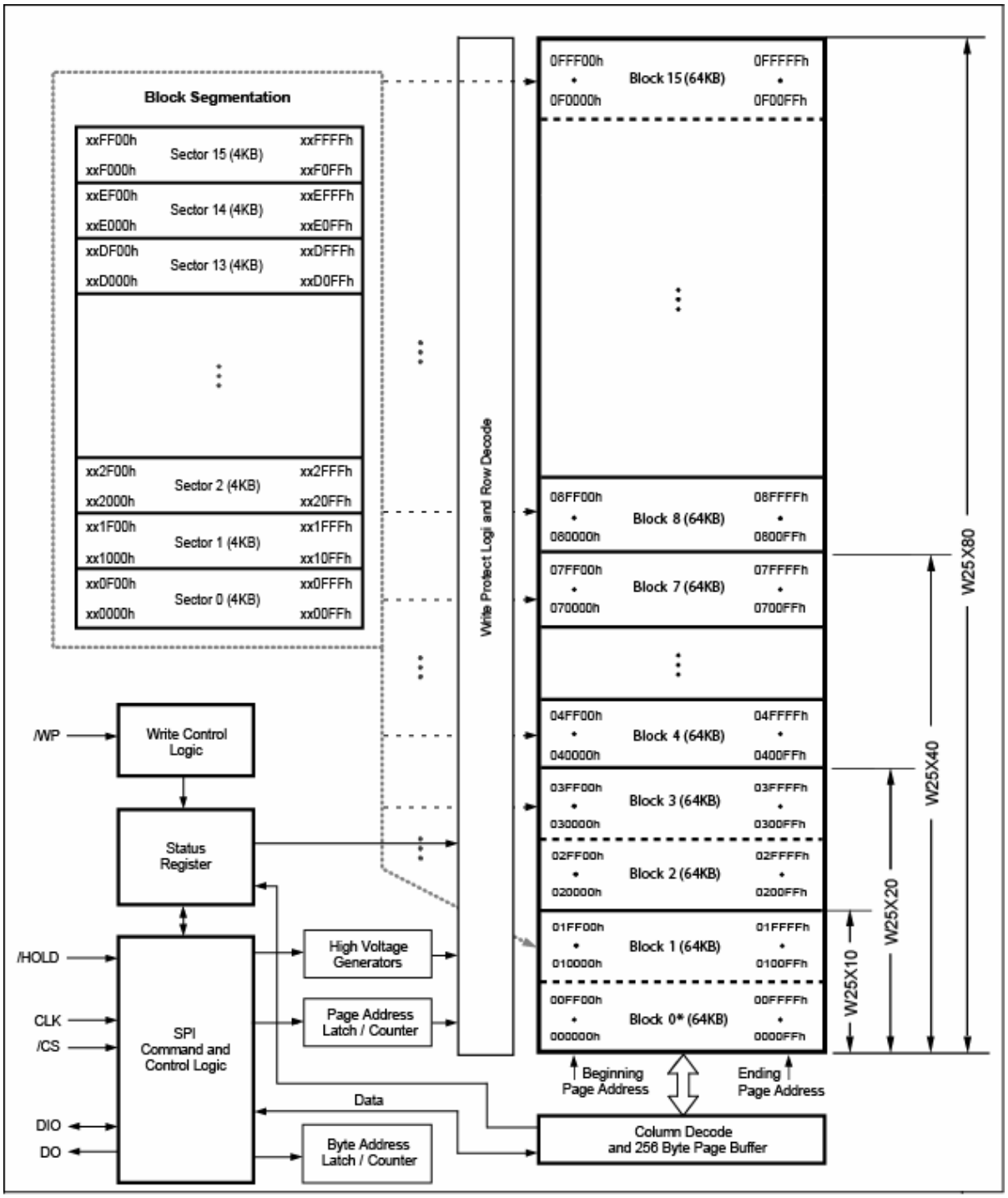


Figure 2. W25X10L, W25X20L, W25X40L and W25X80L Block Diagram

8. FUNCTIONAL DESCRIPTION

8.1 SPI OPERATIONS

8.1.1 SPI Modes

The W25X10L/20L/40L/80L is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input/Output (DIO) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DIO pin is sampled on the rising edge of the CLK. Data on the DO and DIO pins are clocked out on the falling edge of CLK.

8.1.2 Dual Output SPI

The W25X10L/20L/40L/80L supports Dual output operation when using the “Fast Read with Dual Output” (3B hex) instruction. This feature allows data to be transferred from the Serial Flash memory at twice the rate possible with the standard SPI. This instruction is ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for applications that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. All other operations use the standard SPI interface with single output signal.

8.1.3 Hold Function

The /HOLD signal allows the W25X10L/20L/40L/80L operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK.

During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input/Output (DIO) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

8.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the W25X10L/20L/40L/80L provides several means to protect data from inadvertent writes.

8.2.1 Write Protect Features

- Device resets when VCC is below threshold.
- Time delay write disable after Power-up.
- Write enable/disable instructions.
- Automatic write disable after program and erase.
- Software write protection using Status Register.
- Hardware write protection using Status Register and /WP pin.
- Write Protection using Power-down instruction.

Upon power-up or at power-down the W25X10L/20L/40L/80L will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 20). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (TB, BP2, BP1, and BP0) bits. These Status Register bits allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information.

Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

9. CONTROL AND STATUS REGISTERS

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, and the state of write protection. The Write Status Register instruction can be used to configure the devices write protection features. See Figure 3.

9.1 STATUS REGISTER

9.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

9.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

9.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, and BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

9.1.4 Top/Bottom Block Protect (TB)

The Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The TB bit is non-volatile and the factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction provided that the Write Enable instruction has been issued. The TB bit can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

9.1.5 Reserved Bits

Status register bit location S6 is reserved for future use. Current devices will read 0 for this bit location. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

9.1.6 Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a non-volatile read/write bit in status register (S7) that can be used in conjunction with the Write Protect (/WP) pin to disable writes to status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

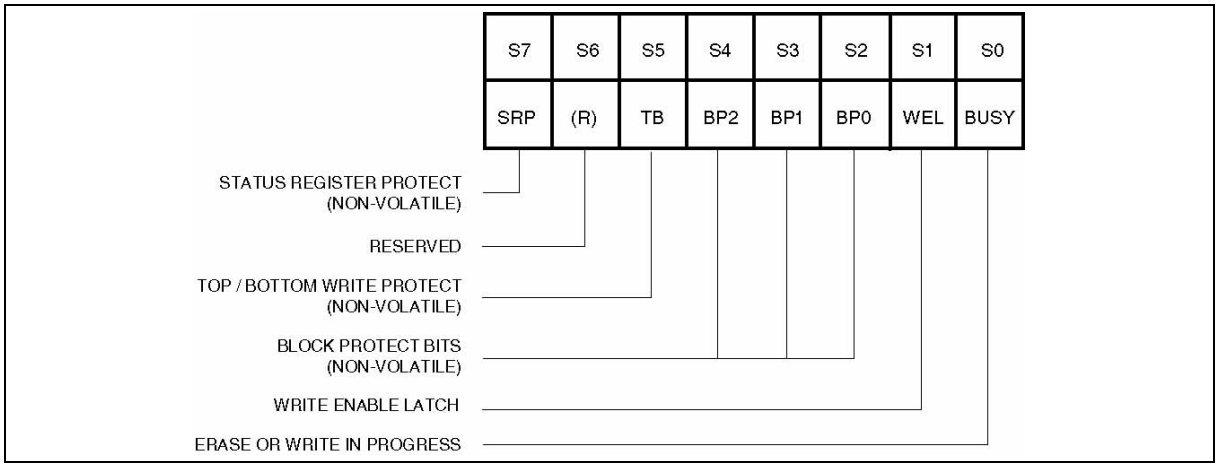


Figure 3. Status Register Bit Locations

9.1.7 Status Register Memory Protection

STATUS REGISTER(1)				W25X80L (8M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	1	15	0F0000h - 0FFFFFh	64KB	Upper 1/16
0	0	1	0	14 and 15	0E0000h - 0FFFFFh	128KB	Upper 1/8
0	0	1	1	12 thru 15	0C0000h - 0FFFFFh	256KB	Upper 1/4
0	1	0	0	8 thru 15	080000h - 0FFFFFh	512KB	Upper 1/2
1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/16
1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/8
1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/4
1	1	0	0	0 thru 7	000000h - 07FFFFh	512KB	Lower 1/2
x	1	0	1	0 thru 15	000000h - 0FFFFFh	1MB	ALL
x	1	1	x	0 thru 15	000000h - 0FFFFFh	1MB	ALL

STATUS REGISTER(1)				W25X40L (4M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	1	7	070000h - 07FFFFh	64KB	Upper 1/8
0	0	1	0	6 and 7	060000h - 07FFFFh	128KB	Upper 1/4
0	0	1	1	4 thru 7	040000h - 07FFFFh	256KB	Upper 1/2
1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/8
1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/4
1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/2
x	1	x	x	0 thru 7	000000h - 07FFFFh	512KB	ALL

STATUS REGISTER(1)				W25X20L (2M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	x	0	0	NONE	NONE	NONE	NONE
0	x	0	1	3	030000h - 03FFFFh	64KB	Upper 1/4
0	x	1	0	2 and 3	020000h - 03FFFFh	128KB	Upper 1/2
1	x	0	1	0	000000h - 00FFFFh	64KB	Lower 1/4
1	x	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/2
x	x	1	1	0 thru 3	000000h - 03FFFFh	256KB	ALL

STATUS REGISTER(1)				W25X10L (1M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	x	0	0	NONE	NONE	NONE	NONE
0	x	0	1	1	010000h - 01FFFFh	64KB	Upper 1/2
1	x	0	1	0	000000h - 00FFFFh	64KB	Lower 1/2
x	x	1	x	0 and 1	000000h - 01FFFFh	128KB	ALL

Note:
1. x = don't care

9.2 INSTRUCTIONS

The instruction set of the W25X10L/20L/40L/80L consists of fifteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DIO input provides the instruction code. Data on the DIO input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 19. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

9.2.1 Manufacturer and Device Identification

MANUFACTURER ID	**(M7-M0)**	
Winbond Serial Flash	EFH	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h**	**9Fh**
W25X10L	10h	3011h
W25X20L	11h	3012h
W25X40L	12h	3013h
W25X80L	13h	3014h

9.2.2 Instruction Set [1]

INSTRUCTION NAME	BYTE 1 CODE	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	N-BYTES
Write Enable	06h						
Write Disable	04h						
Read Status Register	05h	(S7–S0)[1]					[2]
Write Status Register	01h	S7–S0					
Read Data	03h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	continuous
Fast Read	0Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0)	(Next Byte) continuous
Fast Read Dual Output	3Bh	A23–A16	A15–A8	A7–A0	dummy	I/O = (D6,D4,D2,D0) O = (D7,D5,D3,D1)	(one byte per 4 clocks, continuous)
Page Program	02h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	Up to 256 bytes
Block Erase (64KB)	D8h	A23–A16	A15–A8	A7–A0			
Sector Erase (4KB)	20h	A23–A16	A15–A8	A7–A0			
Chip Erase	C7h						
Power-down	B9h						
Release Power-down / Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)[4]		
Manufacturer/ Device ID [3]	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	
JEDEC ID	9Fh	(M7-M0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity			

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until /CS terminates the instruction.
3. See Manufacturer and Device Identification table for Device ID information.
4. The Device ID will repeat continuously until /CS terminates the instruction.

9.2.3 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

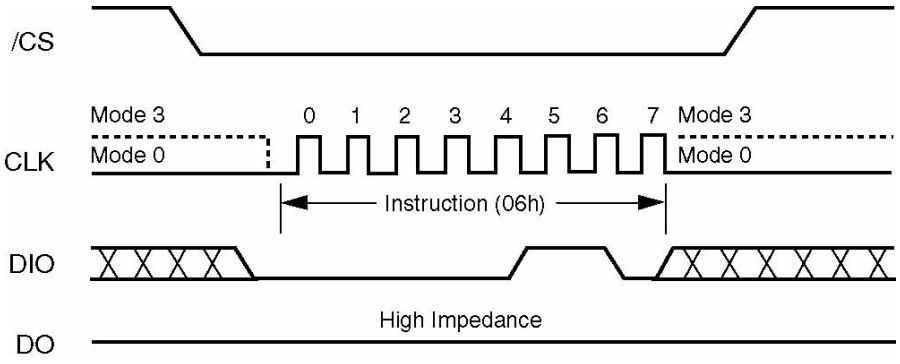


Figure 4. Write Enable Instruction Sequence Diagram

9.2.4 Write Disable (04h)

The Write Disable instruction (Figure 5) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DIO pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

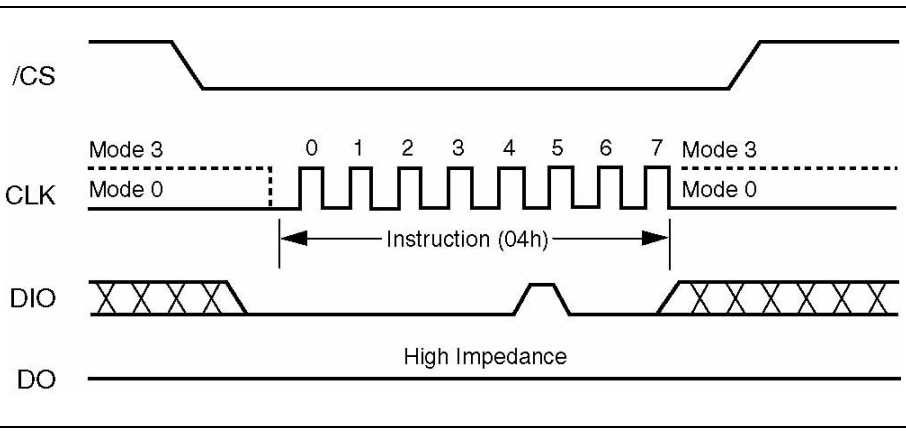


Figure 5. Write Disable Instruction Sequence Diagram

9.2.5 Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” into the DIO pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3 and include the BUSY, WEL, BP2-BP0, TB and SRP bits (see description of the Status Register earlier in this data sheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 6. The instruction is completed by driving /CS high.

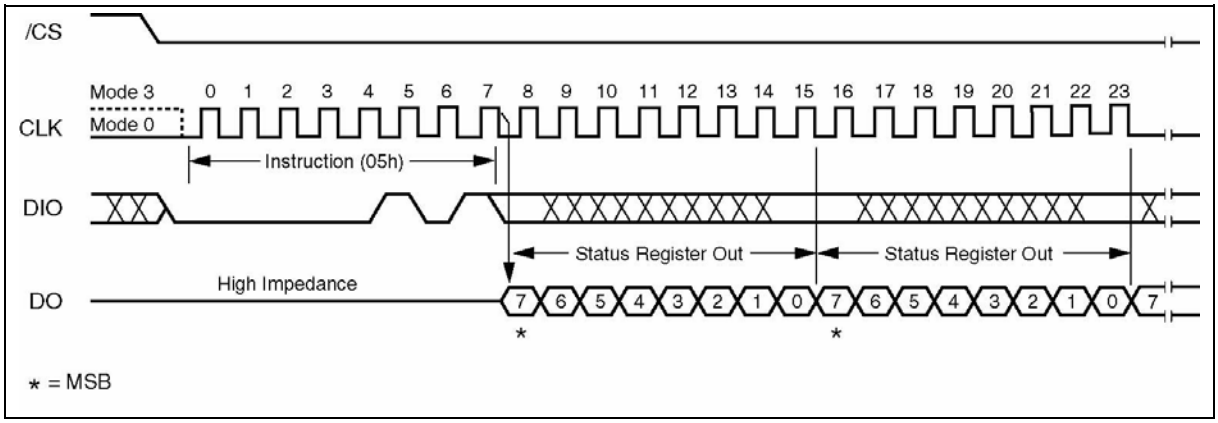


Figure 6. Read Status Register Instruction Sequence Diagram

9.2.6 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this data sheet.

Only non-volatile Status Register bits SRP, TB, BP2, BP1 and BP0 (bits 7, 5, 4, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (TB, BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

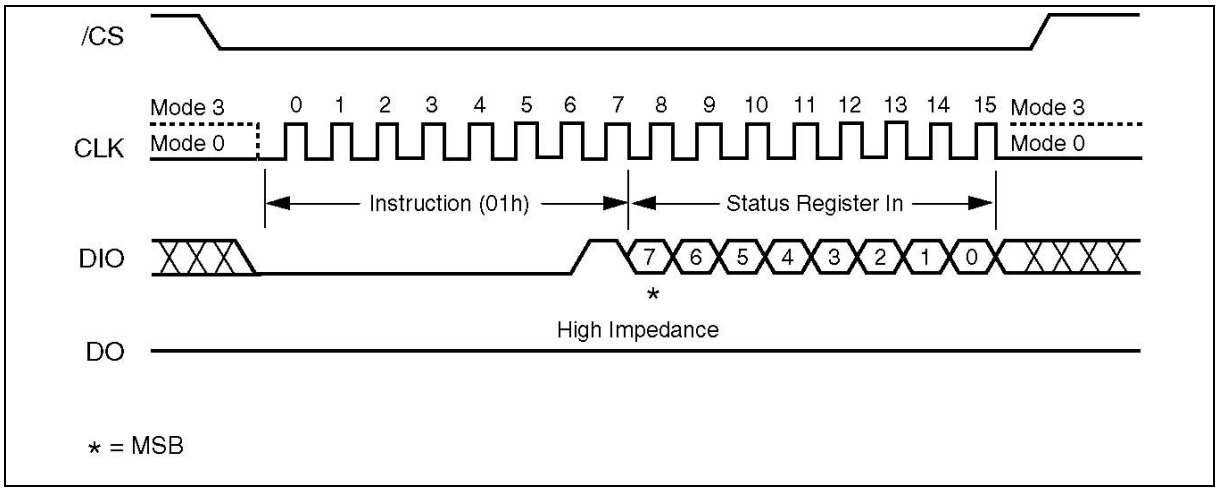


Figure 7. Write Status Register Instruction Sequence Diagram

9.2.7 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DIO pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

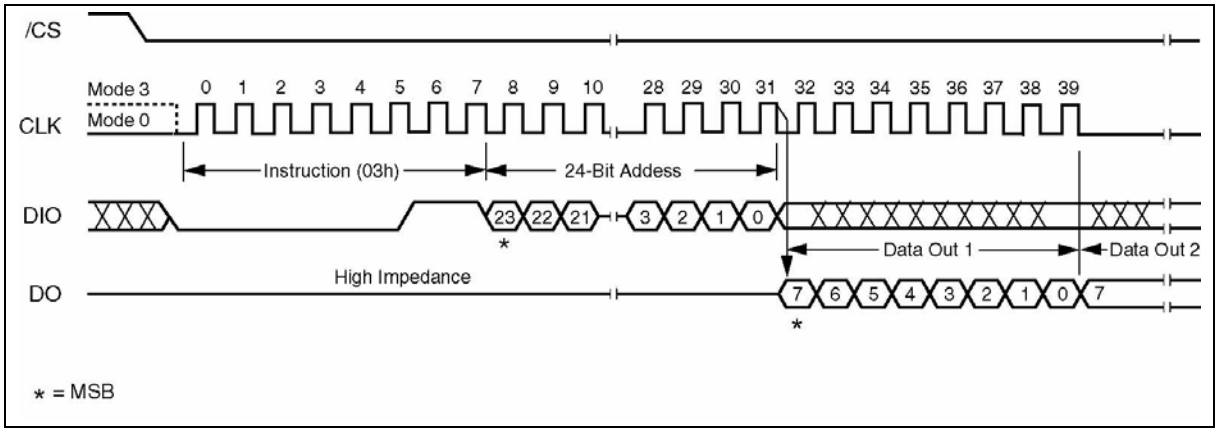


Figure 8. Read Data Instruction Sequence Diagram

9.2.8 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 9. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DIO pin is a “don’t care”.

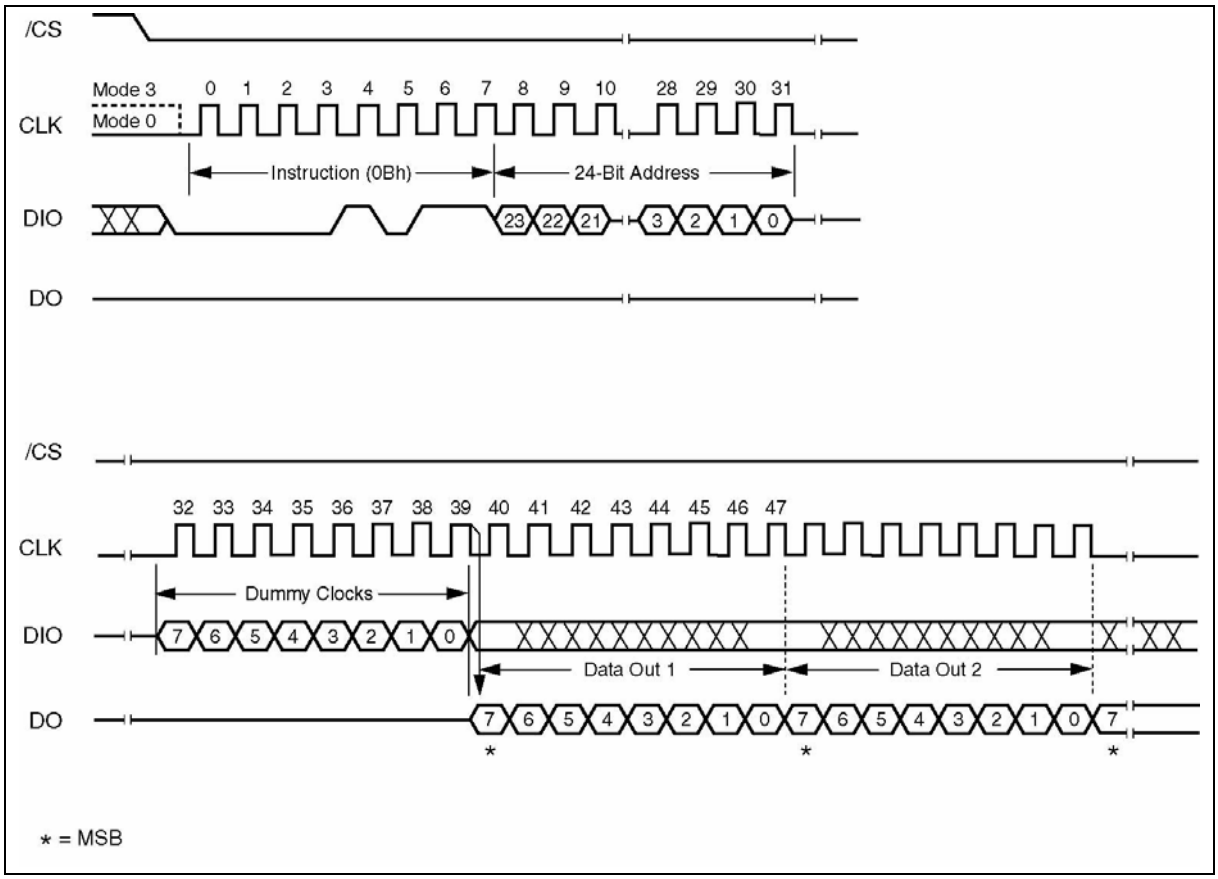


Figure 9. Fast Read Instruction Sequence Diagram

9.2.9 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DO and DIO, instead of just DO. This allows data to be transferred from the W25X10L/20L/40L/80L at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DIO pin should be high-impedance prior to the falling edge of the first data out clock.

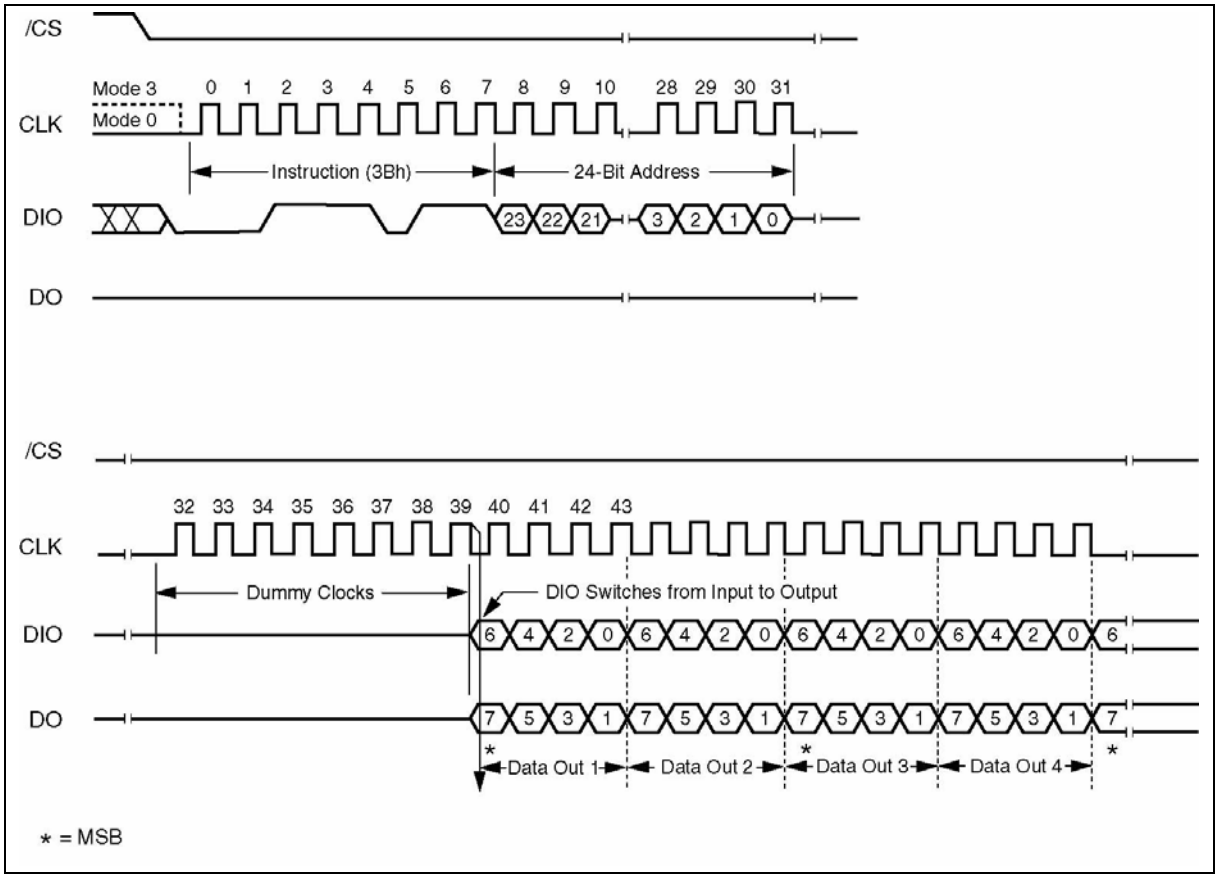


Figure 10. Fast Read Dual Output Instruction Sequence Diagram

9.2.10 Page Program (02h)

The Page Program instruction allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The Page Program instruction sequence is shown in figure 11. The instruction is initiated by driving the /CS pin low then shifting the instruction code "02h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DIO pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

The W25X10/20/40/80L program address must start on a page boundary (A7-A0 = 00h). If it is necessary to program an address within a page (A7-A0 = /00h), use the following procedure: read all 256 bytes from a page into working RAM, append the new data (only 1's can be changed to 0's) and then program 256-bytes starting at the page boundary address (A7-A0 = 00h).

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of t_{PP} (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. **It is recommended to wait for a duration of t_{BP1} (~100uS typ.) before reading the status register to check the BUSY bit.** The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

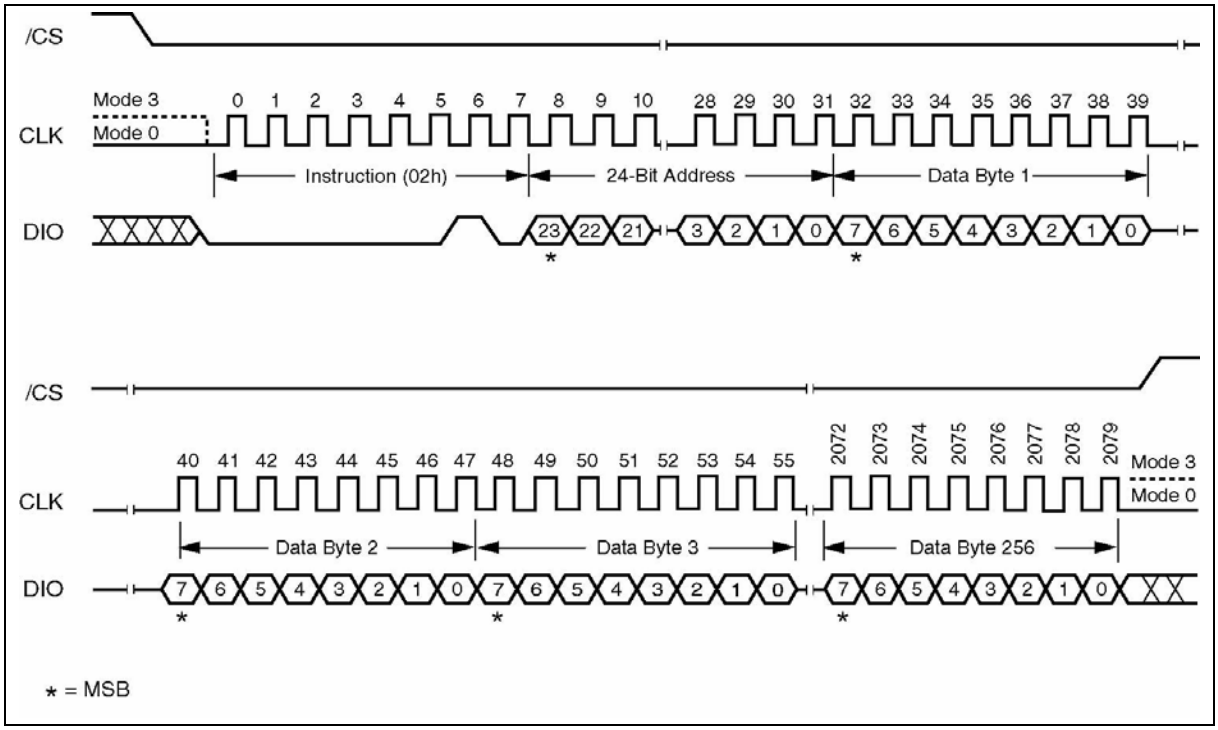


Figure 11. Page Program Instruction Sequence Diagram

9.2.11 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 12.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

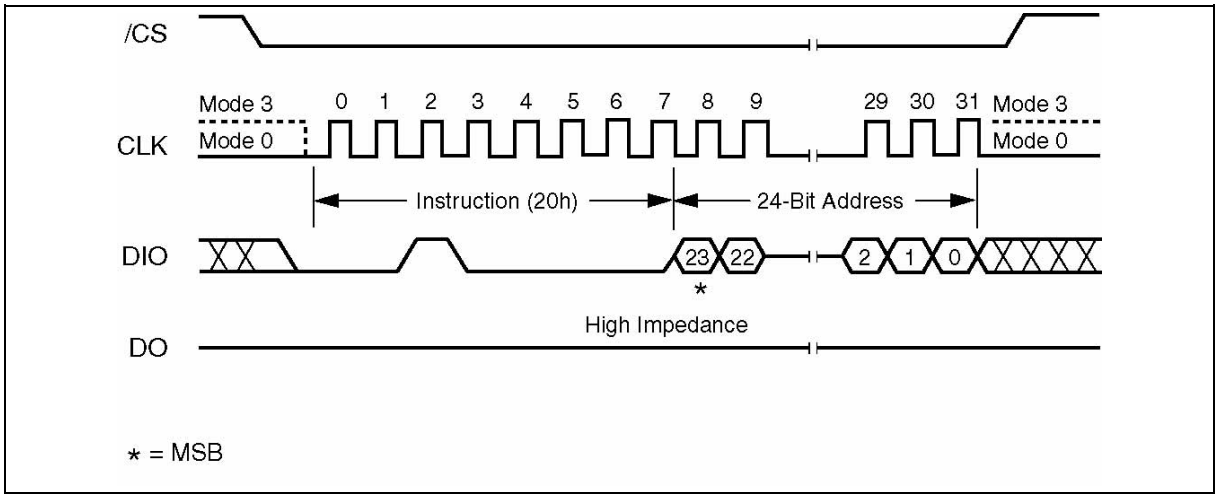


Figure 12. Sector Erase Instruction Sequence Diagram

9.2.12 Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 13.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

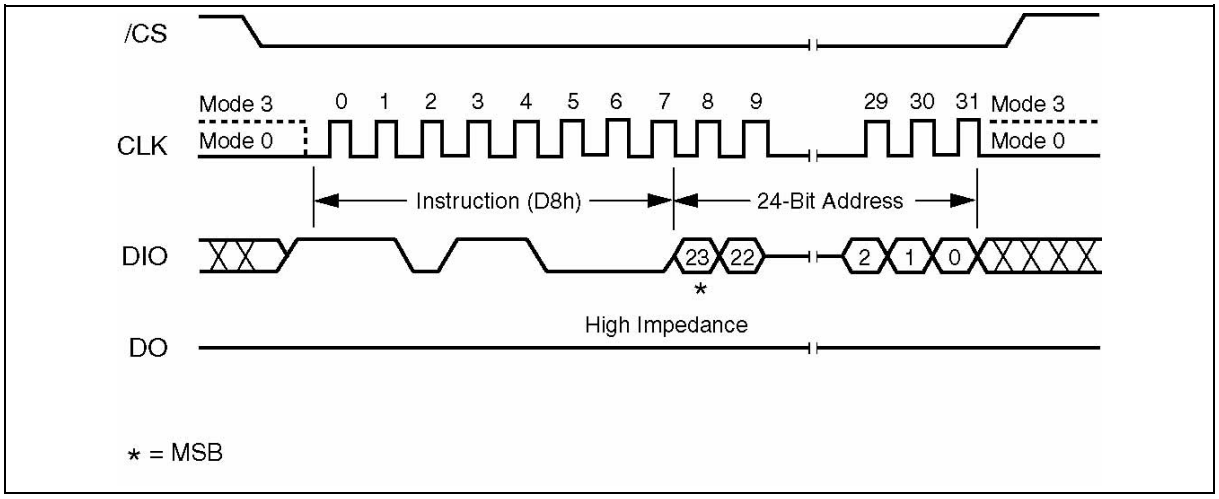


Figure 13. Block Erase Instruction Sequence Diagram

9.2.13 Chip Erase (C7h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h”. The Chip Erase instruction sequence is shown in figure 14.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

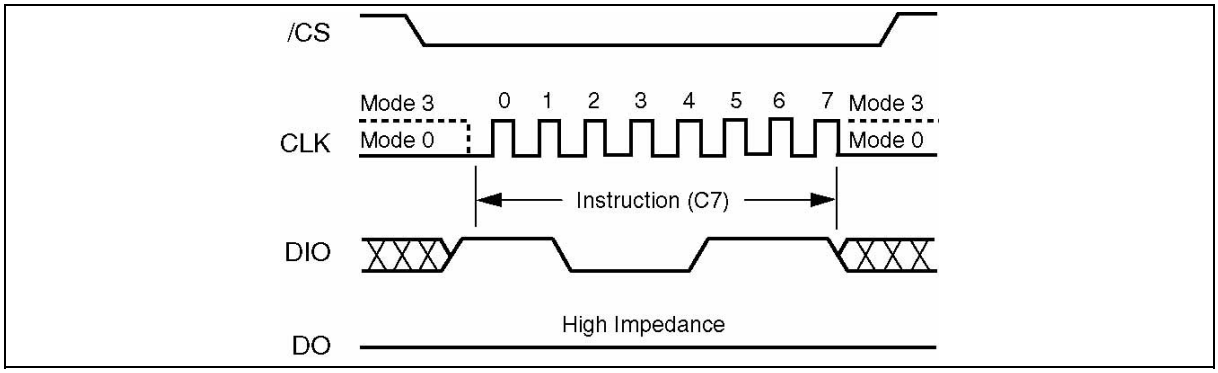


Figure 14. Chip Erase Instruction Sequence Diagram

9.2.14 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in figure 15.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

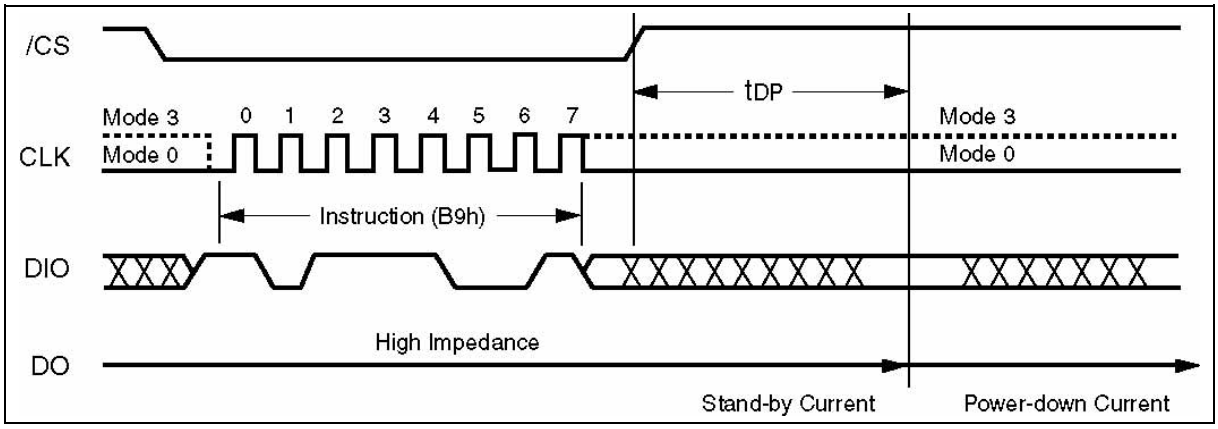


Figure 15. Deep Power-down Instruction Sequence Diagram

9.2.15 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or do both.

When used only to release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in figure 16. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 17. The Device ID values for the W25X10L, W25X20L , W25X40L and W25X80L are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 17, except that after /CS is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted.

If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

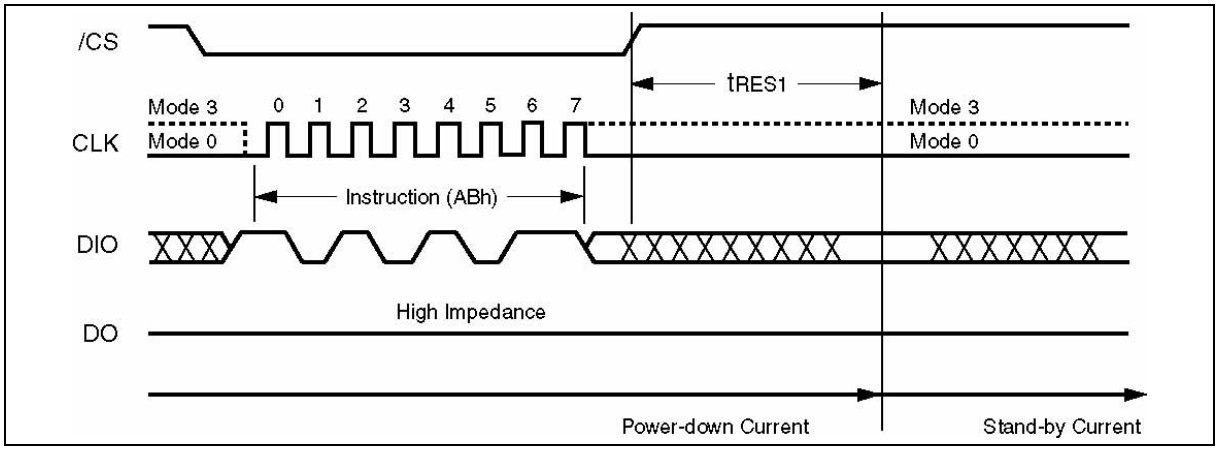


Figure 16. Release Power-down Instruction Sequence

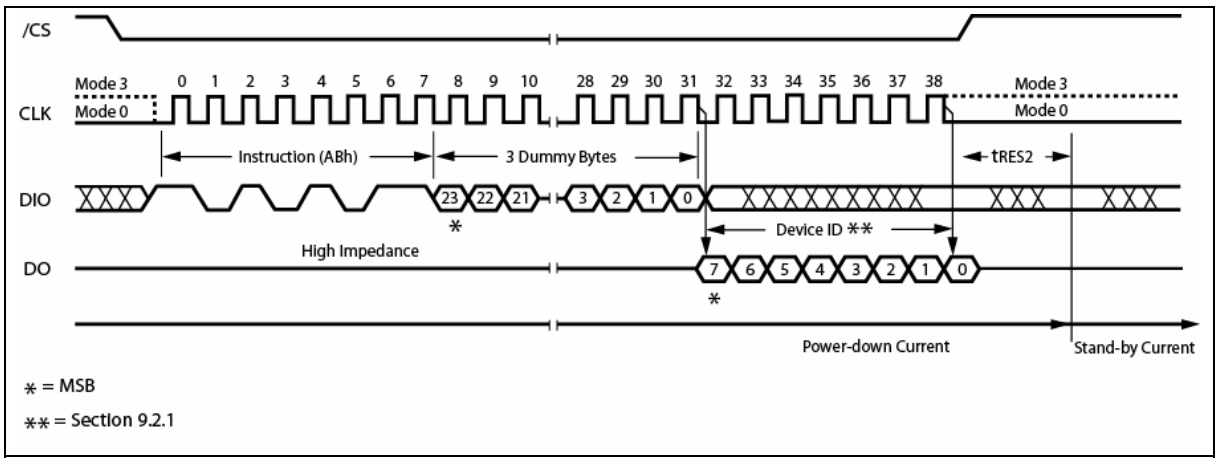


Figure 17. Release Power-down / Device ID Instruction Sequence Diagram

9.2.16 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 18. The Device ID values for the W25X10L, W25X20L, W25X40L and W25X80L are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

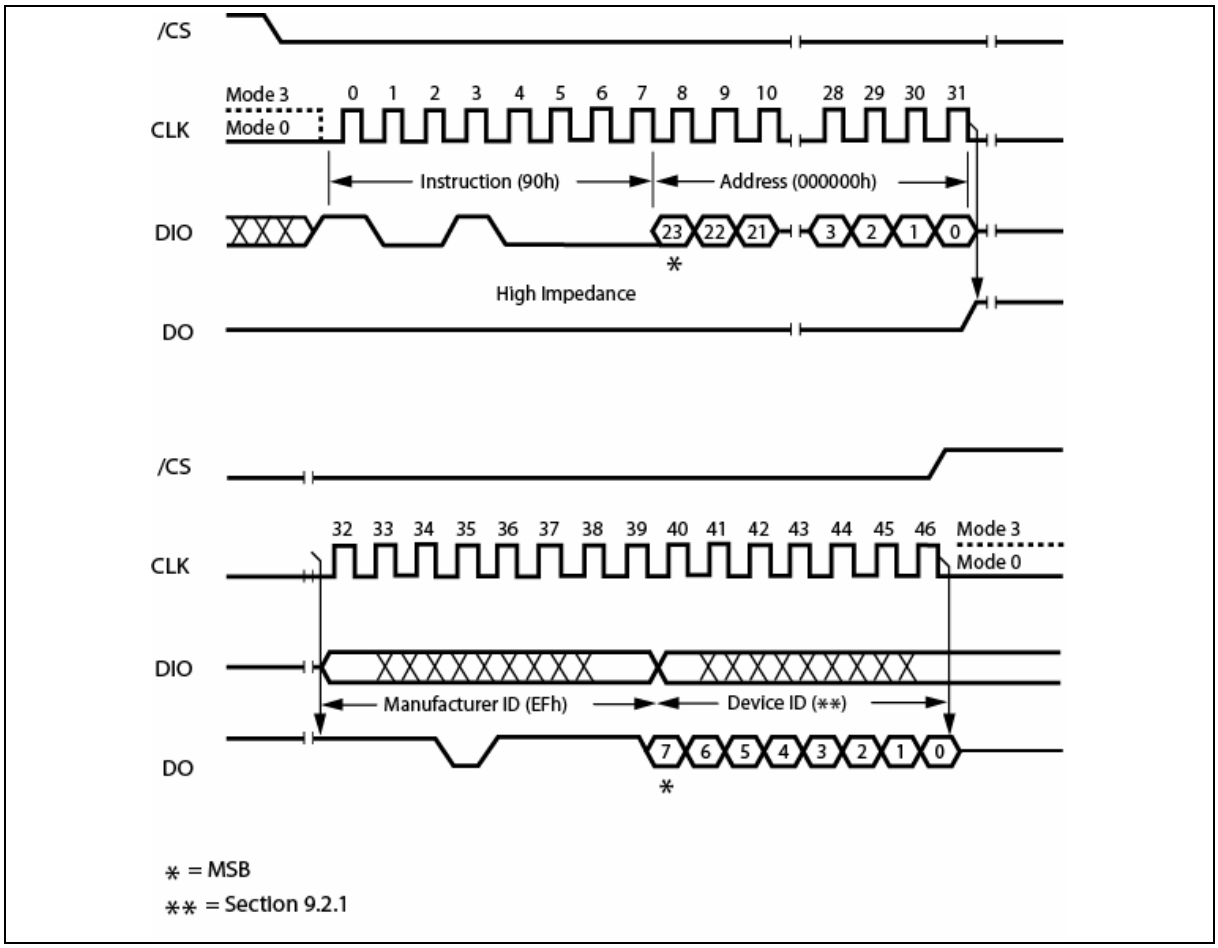


Figure 18. Read Manufacturer / Device ID Diagram

9.2.17 JEDEC ID (9Fh)

For compatibility reasons, the W25X10L/20L/40L/80L provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 19. For memory type and capacity values refer to Manufacturer and Device Identification table.

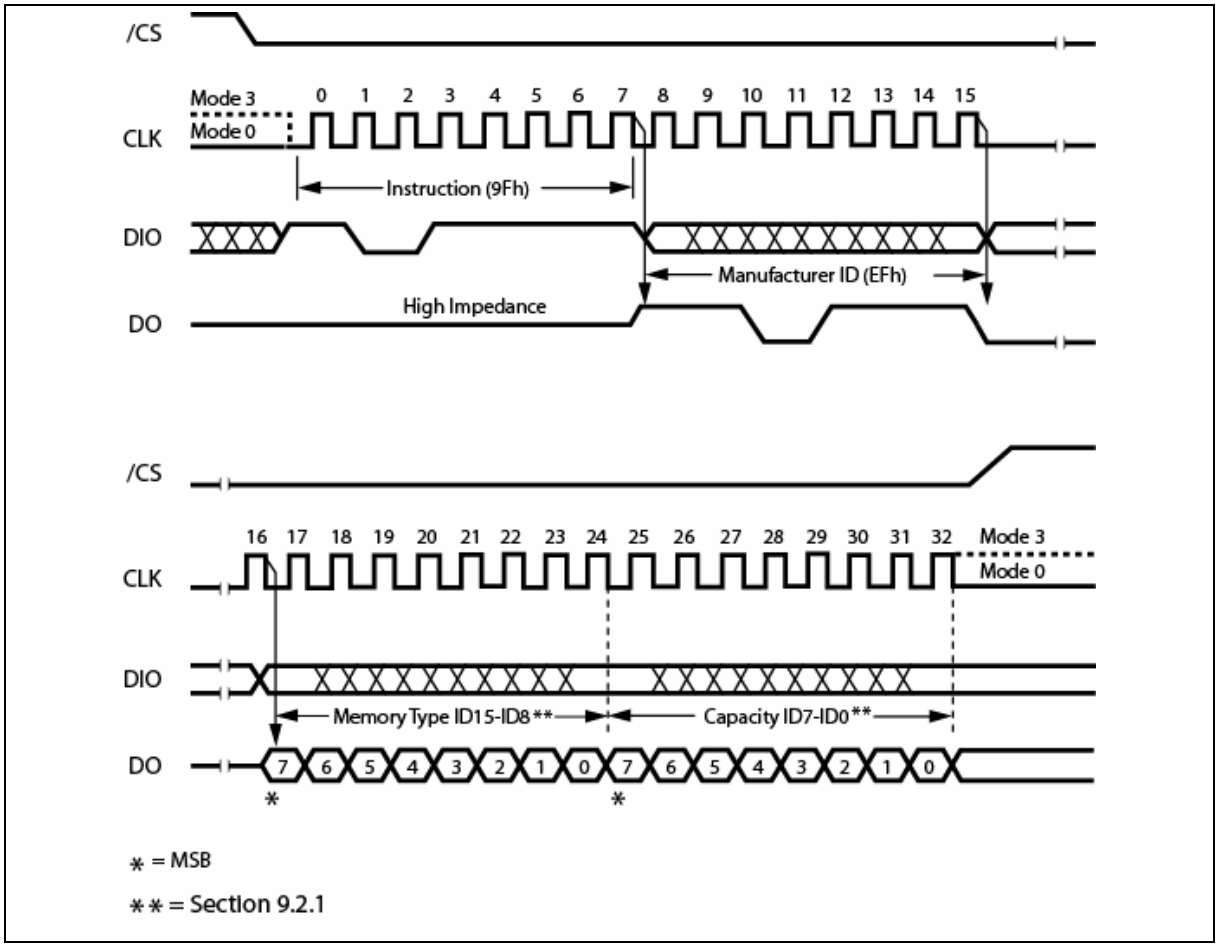


Figure 19. Read JEDEC ID

10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.0	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0 to VCC+2.0	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

10.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	FR = 40MHz, fR = 20MHz	2.3	3.3	V
Ambient Temperature	TA	Extended	0	+85	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±5% of the programming (erase/write) voltage.

10.3 Endurance and Data Retention

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Erase/Program Cycles	4KB sector, 64KB block or full chip.	100,000		cycles
Data Retention	55°C		20	years

10.4 Power-up Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}[1]	10		µs
Time Delay Before Write Instruction	t_{PUW}[1]	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}[1]	1	2	V

Note:

1. These parameters are characterized only.

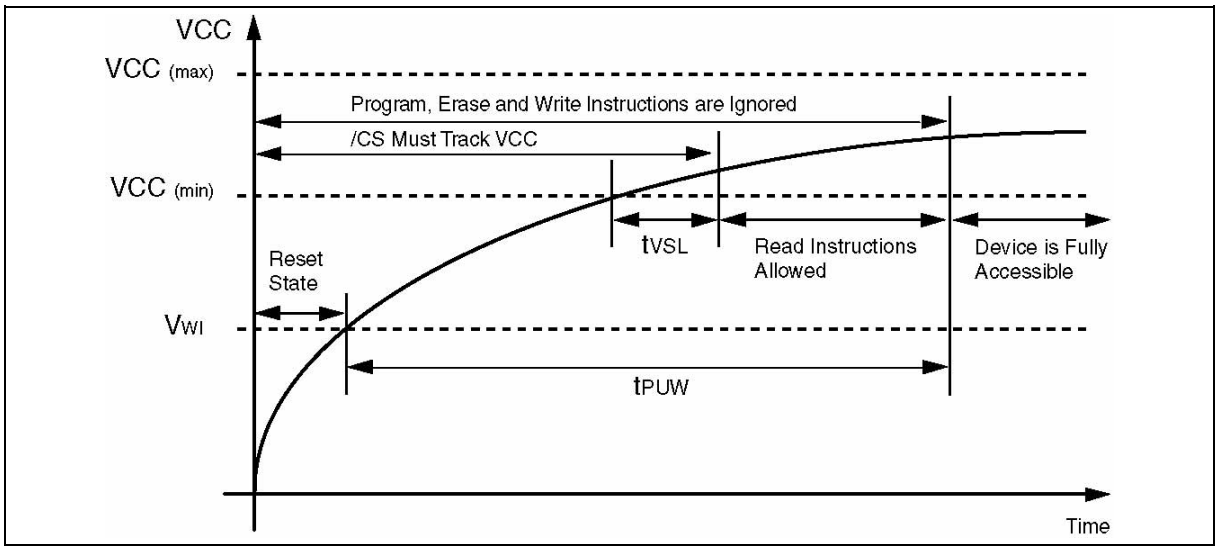


Figure 20. Power-up Timing and Voltage Levels

10.5 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}[1]	V_{IN} = 0V[2]			6	pF
Output Capacitance	Cout[1]	V_{OUT} = 0V[2]			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		25	50	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		<1	10	µA
Current Read Data / Dual Output Read 1MHz[2]	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		4/5	10/12	mA
Current Read Data / Dual Output Read 25MHz[2]	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		7/8	12/15	mA
Current Read Data / Dual Output Read 40MHz[2]	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		8/10	15/18	mA
Current Page Program	I_{CC4}	/CS = VCC		12	20	mA
Current Write Status Register	I_{CC5}	/CS = VCC		4	8	mA
Current Sector/Block Erase	I_{CC6}	/CS = VCC		12	20	mA
Current Chip Erase	I_{CC7}	/CS = VCC		12	20	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x0.7		VCC +0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC –0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA=25° C, VCC 2.5V.
2. Checker Board Pattern.

10.6 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L	30	30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

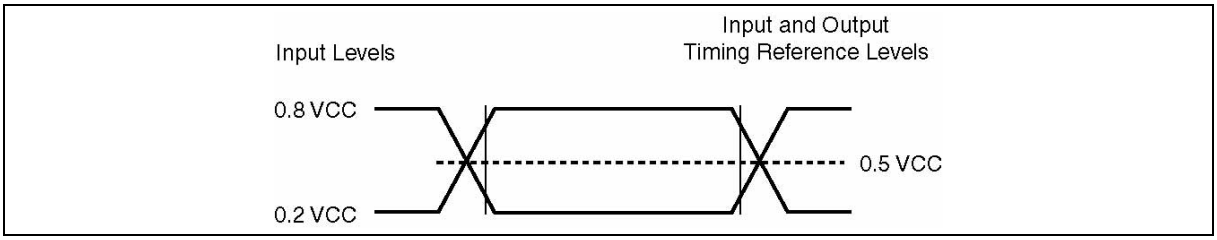


Figure 21. AC Measurement I/O Waveform

10.7 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency, for Fast Read (0Bh, 3Bh) and all other instructions except Read Data (03h)	F_R	f_C	D.C.		40	MHz
Clock freq. Read Data instruction 03h	f_R		D.C.		20	MHz
Clock High, Low Time, for Fast Read (0Bh, 3Bh) and other instructions except Read Data (03h)	t_{CLH}, t_{CLL}(1)		9			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL}(1)		14			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	5			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		10			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		0			ns
/CS Deselect Time	t_{SHSL}	t_{CSH}	100			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			9	ns
Clock Low to Output Valid	t_{CLQV}	t_V			10	ns
Output Hold Time	t_{CLQX}	t_{HO}	0			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	$t_{HHQX(2)}$	t_{LZ}			7	ns
/HOLD to Output High-Z	$t_{HLQZ(2)}$	t_{HZ}			13	ns

Continued – next page

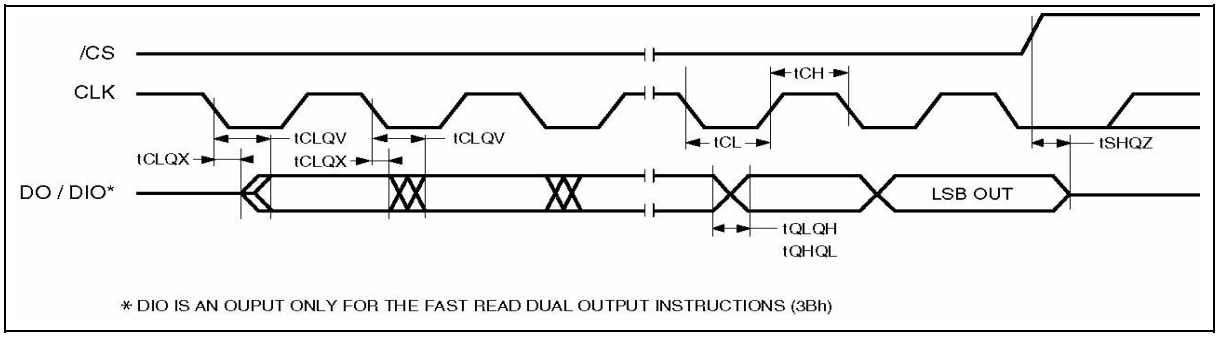
10.8 AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Write Protect Setup Time Before /CS Low	t_{WHSL} (3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL} (3)		100			ns
/CS High to Power-down Mode	t_{DP} (2)				3	µs
/CS High to Standby Mode without Electronic Signature Read	t_{RES1} (2)				3	µs
/CS High to Standby Mode with Electronic Signature Read	t_{RES2} (2)				1.8	µs
Write Status Register Time	t_W			5	15	ms
Byte Program Time (First Byte) (4)	t_{BP1}			100	150	µs
Additional Byte Program Time (After First Byte) (4)	t_{BP2}			6	12	µs
Page Program Time	t_{PP}			1.5	5	ms
Sector Erase Time (4KB)	t_{SE}			170	300	ms
Block Erase Time (64KB)	t_{BE}			1	2	s
Chip Erase Time W25X10L / W25X20L Chip Erase Time W25X40L Chip Erase Time W25X80L	t_{CE}			4 6 12	6 10 20	s s s

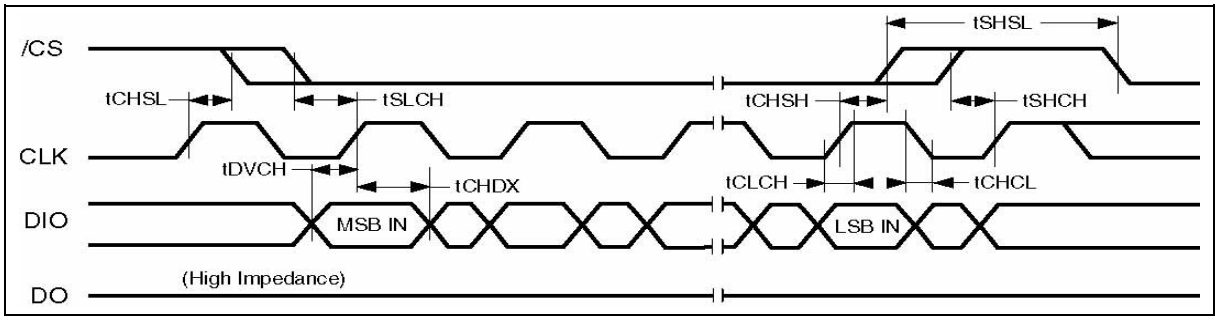
Notes:

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.
4. For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed. The program address for the 25X L-Series must start on a page boundary (A7-A0 = 00h). tBP1 (typical) is also the recommended delay time before reading the status register after issuing a program page instruction.

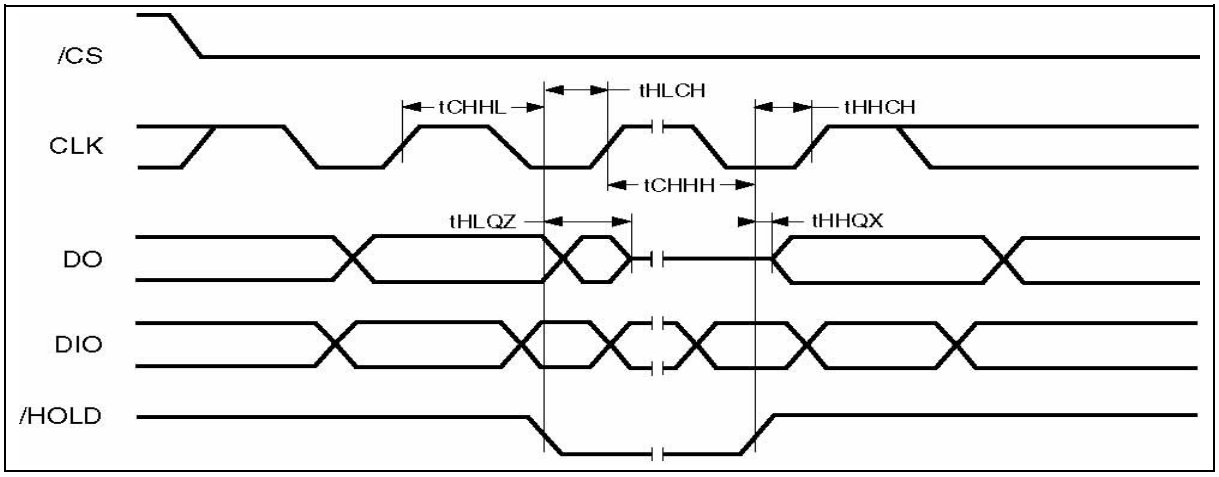
10.9 Serial Output Timing



10.10 Input Timing

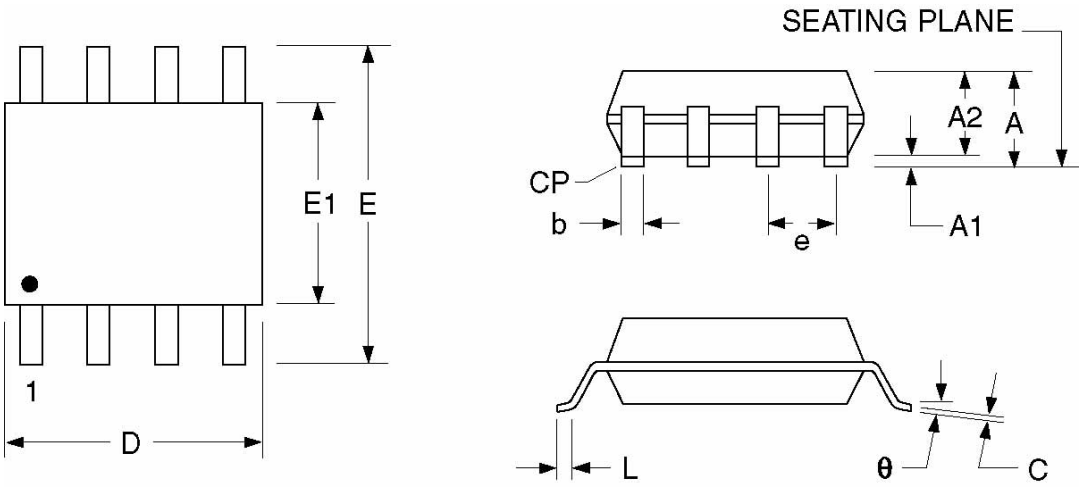


10.11 Hold Timing



11. PACKAGE SPECIFICATION

11.1 8-Pin SOIC 150-mil (Package Code SN)

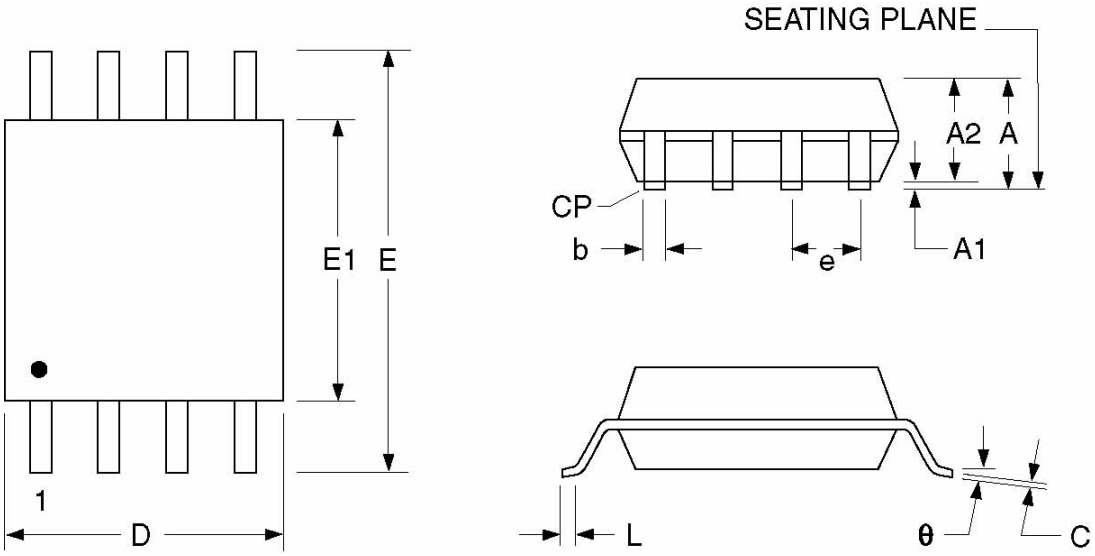


SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	1.47	1.60	1.72	0.058	0.063	0.068
A1	0.10	---	0.24	0.004	---	0.009
A2	---	1.45	---	---	0.057	---
b	0.33	0.41	0.50	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D(3)	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.19	0.228	0.236	0.244
E1(3)	3.80	3.90	4.00	0.150	0.154	0.157
e(2)		1.27 BSC			0.050 BSC	
L	0.40	0.71	1.27	0.015	0.028	0.050
θ	0°	---	8°	0°	---	8°
CP	---	---	0.10	---	---	0.004

Notes:

1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within .0004 inches at the seating plane.

11.2 8-Pin SOIC 208-mil (Package Code SS)

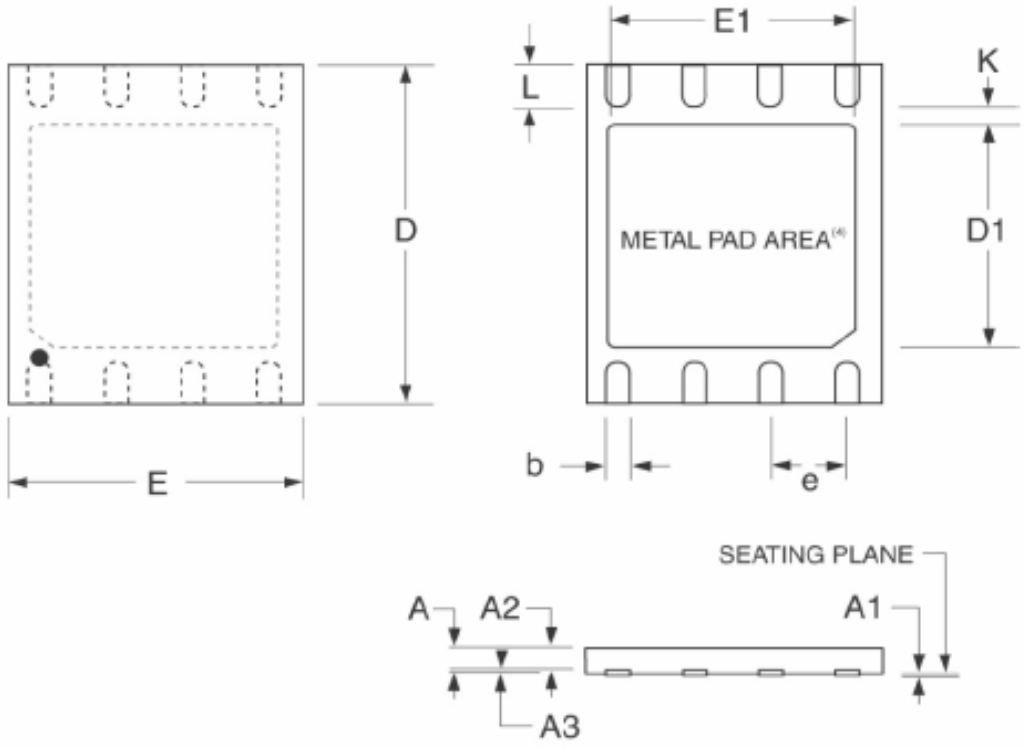


SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1	5.18	5.38	0.204	0.212
e	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	---	0.10	---	0.004

Notes:

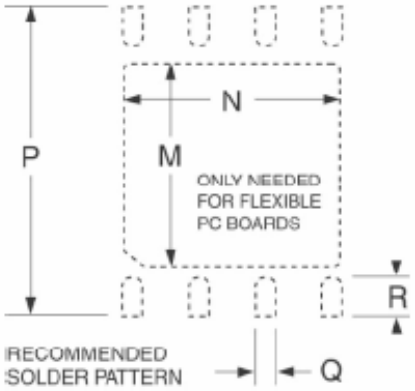
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within .0004 inches at the seating plane.

11.3 8-contact 6x5 WSON (Package Code ZP)



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	.0.20	0.25	0.0075	0.0080	0.0098
b	0.36	0.40	0.48	0.0138	0.0157	0.0190
D(3)	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3)	4.20	4.30	4.40	0.1653	0.1692	0.1732
e(2)	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

11.4 8-contact 6x5 WSON Cont'd. (Package Code ZP)

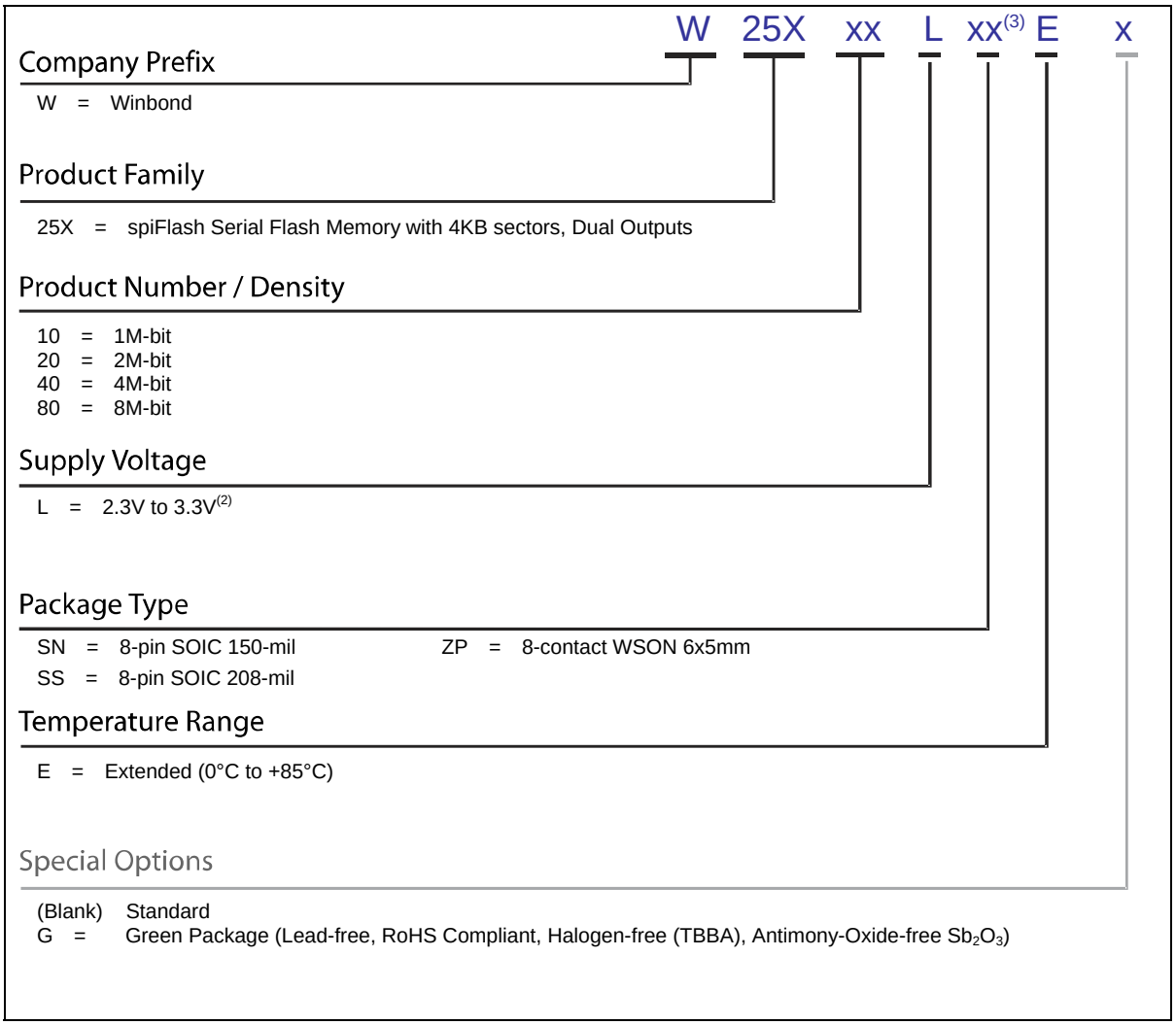


SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
SOLDER PATTERN						
M		3.40			0.1338	
N		4.30			0.1692	
P		6.00			0.2360	
Q		0.50			0.0196	
R		0.75			0.0255	

Notes:

1. Advanced Packaging Information; please contact Winbond for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. The metal pad area on the bottom center of the package is connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

12. ORDERING INFORMATION [1]



Notes:

1. The Winbond W25X20, W25X40 and W25X80 are fully compatible with the previous Nexflash NX25X20, NX25X40 and NX25X80 Serial Flash Memories.

1a. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T), when placing orders.

1b. The "W" prefix is not included on the part marking.

2. Not all densities are available, please check with Winbond for the availability.

3. Only the 2nd letter is used for the part marking; WSON package type ZP is not used for the part marking.

Valid Part Numbers and Top Side Marking:

The following table provides the valid part numbers for the 25X10/20/40/80L SpiFlash Memories. Please contact *Winbond* for specific availability by density and package type. *Winbond* SpiFlash memories use an 11-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages use an abbreviated 9-digit number.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150mil	1M-bit	W25X10LSNEG	25X10LNEG
	2M-bit	W25X20LSNEG	25X20LNEG
	4M-bit	W25X40LSNEG	25X40LNEG
SS SOIC-8 208mil	4M-bit	W25X40LSSEG	25X40LSEG
	8M-bit	W25X80LSSEG	25X80LSEG
ZP WSON-8 6x5mm	1M-bit	W25X10LZPEG	25X10LEG
	2M-bit	W25X20LZPEG	25X20LEG
	4M-bit	W25X40LZPEG	25X40LEG
	8M-bit	W25X80LZPEG	25X80LEG

Note:

1. For WSON packages, the package type ZP is not used in the top side marking.

13. W25X10/20/40/80V AND W25X10/20/40/80L SPEC. COMPARISON

Winbond's W25X family of SpiFlash® memories support 3V (V-series) and 2.5V (L-series) supply voltage operation. Both versions are based on the same silicon design but tested to different specifications. The L series SpiFlash® memory has the same features and functionality as the original W25X family except for the differences highlighted in the following table. Please see DC and AC Electrical Characteristics for further details.

	W25XxxV	W25XxxL
Supply Voltage	2.7V ~ 3.6V	2.3V ~ 3.3V
Ambient Temperature	-40 ~ +85°C	0 ~ +85°C
Clock Frequency	Up to 75MHz	Up to 40MHz
Page Program Address	Any Address	A7-A0 must = 00h

14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	05/04/06		New Create
B	06/30/06	4, 31, 35-36	Changed minimum Vcc from 2.37V to 2.3V. Added byte program parameters t_{PB1}, $t_{PB2.}$ Reduced t_{SHCH} from 5ns to 0ns.
C	11/08/06	16, 42	Corrected Write Enable/Disable text in (10.2). Added footnotes in ordering information table.
D	12/1/06	4, 31, 42	Added Extended Temp. range 0°C ~ +85°C
E	1/30/07	33	ICC2 max changed from 5uA to 10uA
F	3/2/07	31 & 42	Added transient voltage specification.
G	3/21/07	31, 42 & 43	Updated table 10.3. Added Valid Part Number and Top Side Marking table.
H	5/17/07	22, 36 & 44	Updated Page Program description and footnote for tBP1. Added comparison of 2.5V (L-series) and 3V (V-series).
I	2/27/08	42 & 43	Added note for WSON top side marking. Removed Priliminary designation.

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