STL24NM60N

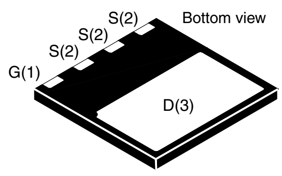
N-channel 600 V, 0.200 Ω, 16 A PowerFLAT™ 8x8 HV MDmesh™ II Power MOSFET

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STL24NM60N	650 V	< 0.215 Ω	16 A (1)

1. The value is rated according to $R_{thj\text{-}case}$

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

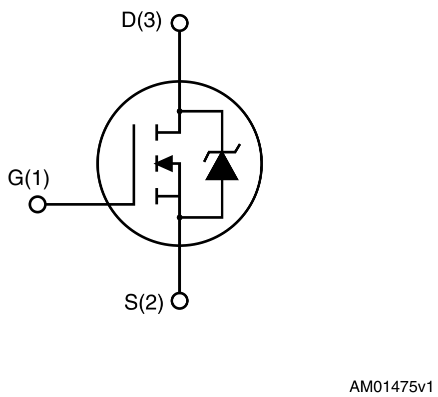


Table 1. Device summary

Order code	Marking	Package	Packaging
STL24NM60N	24NM60N	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	16	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	10	A
I_D (2)	Drain current (continuous) at T_{amb} = 25 °C	3.3	A
I_D (2)	Drain current (continuous) at T_{amb} = 100 °C	1.5	A
I_{DM} (2),(3)	Drain current (pulsed)	13.2	A
P_{TOT} (2)	Total dissipation at T_{amb} = 25 °C	3	W
P_{TOT} (1)	Total dissipation at T_C = 25 °C	125	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj\text{-}case}$
2. When mounted on FR-4 board of inch², 2oz Cu
3. Pulse width limited by safe operating area
4. I_{SD} ≤ 16 A, di/dt ≤ 400 A/µs, $V_{DSpeak} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-amb max	45	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8 A		0.2	0.215	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1400 44 7.4	-	pF pF pF
$C_{oss\ eq.}$ (1)	Output equivalent capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	190	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 16 A, V_{GS} = 10 V (see *Figure 3*)	-	46 7 23	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(off)}$ t_r t_c t_f	Turn-off delay time Rise time Cross time Fall time	V_{DD} = 300 V, I_D = 8 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 4*)	-	11.5 16.5 73 37	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		16 64	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 16 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 16 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 4*)	-	340 4.6 27		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 16 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 4*)	-	4.4 5.7 28		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

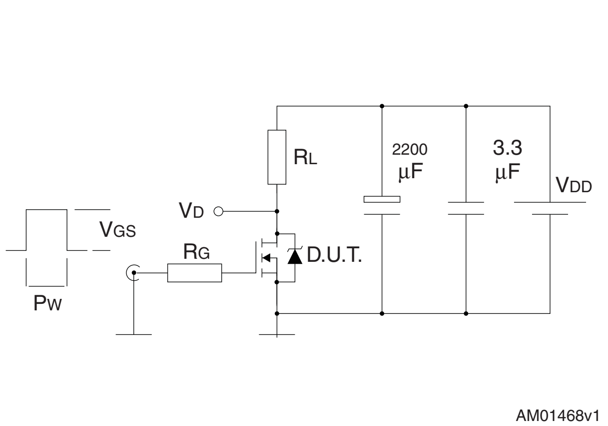


Figure 3. Gate charge test circuit

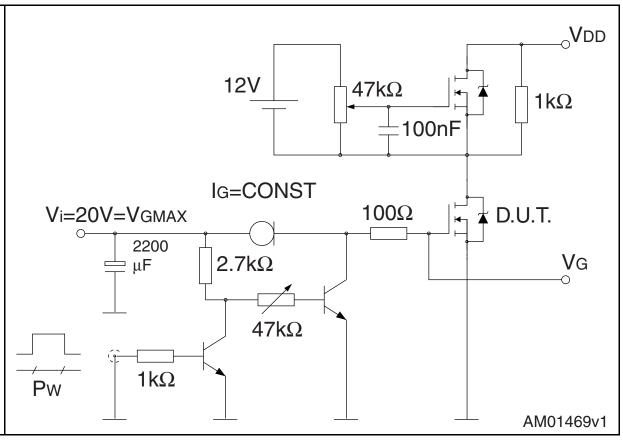


Figure 4. Test circuit for inductive load switching and diode recovery times

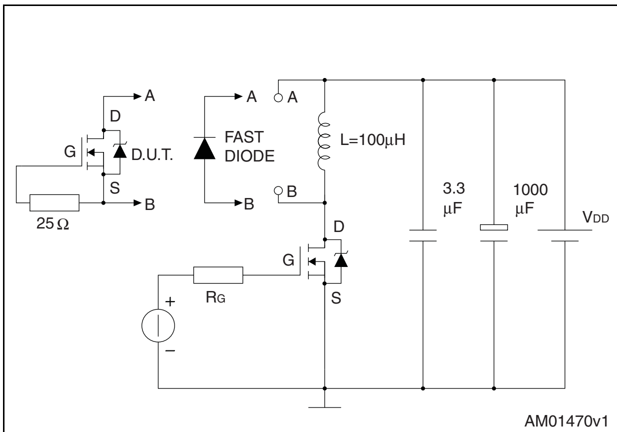


Figure 5. Unclamped inductive load test circuit

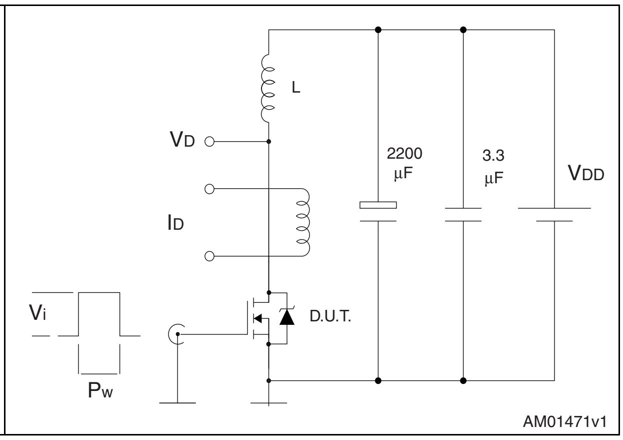


Figure 6. Unclamped inductive waveform

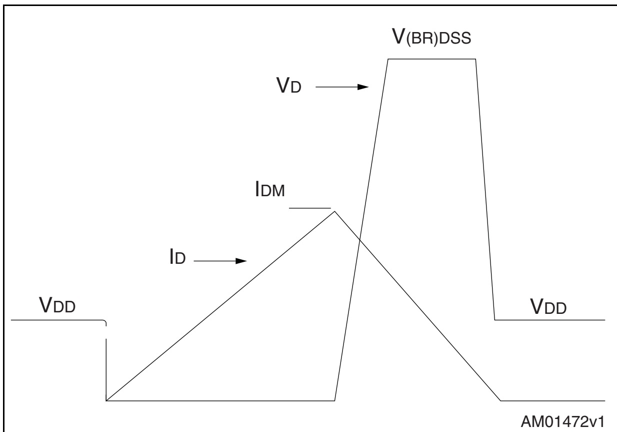
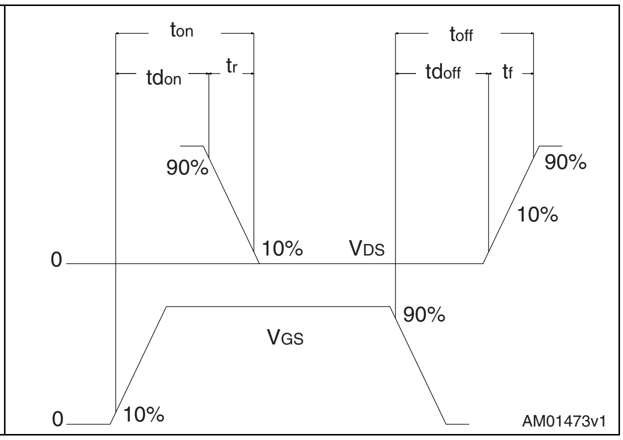


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

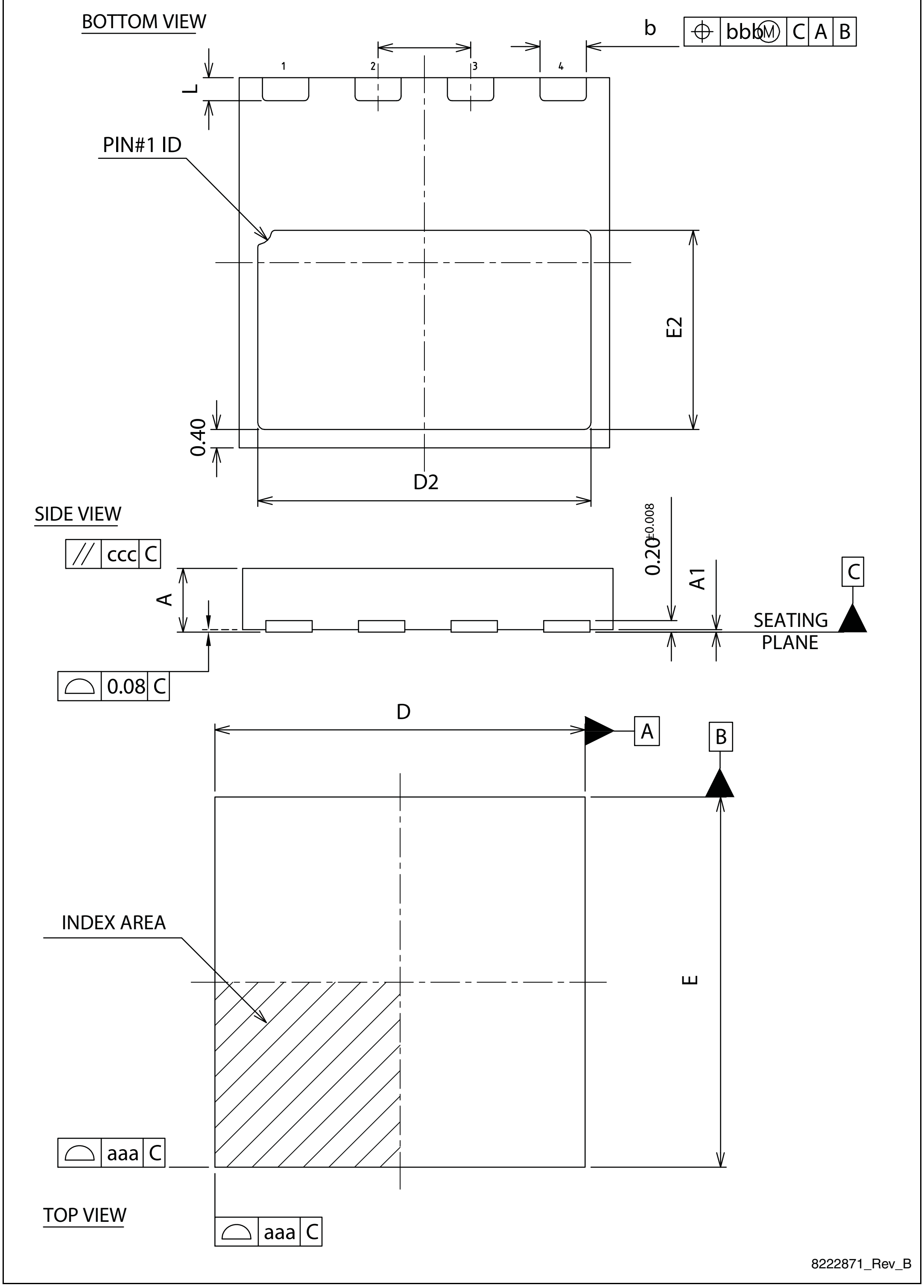
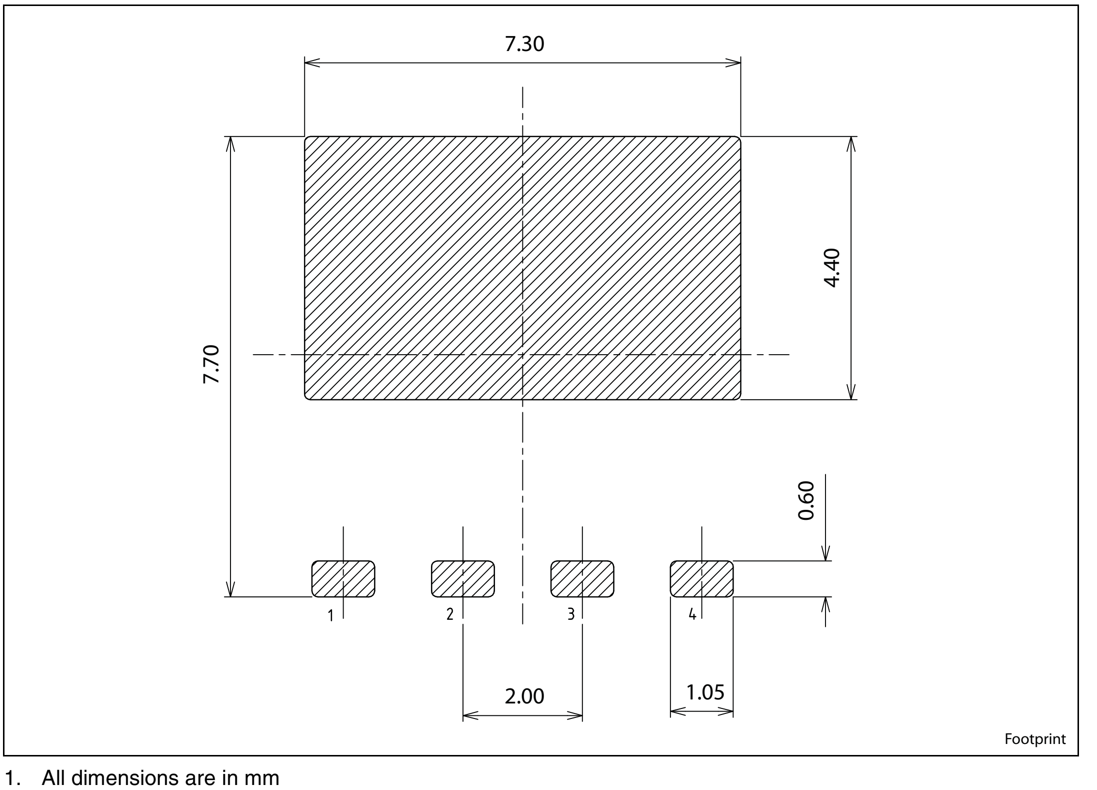


Figure 9. PowerFLAT™ 8x8 HV recommended footprint (1)



1. All dimensions are in mm

5 Packaging mechanical data

Figure 10. PowerFLAT™ 8x8 HV tape

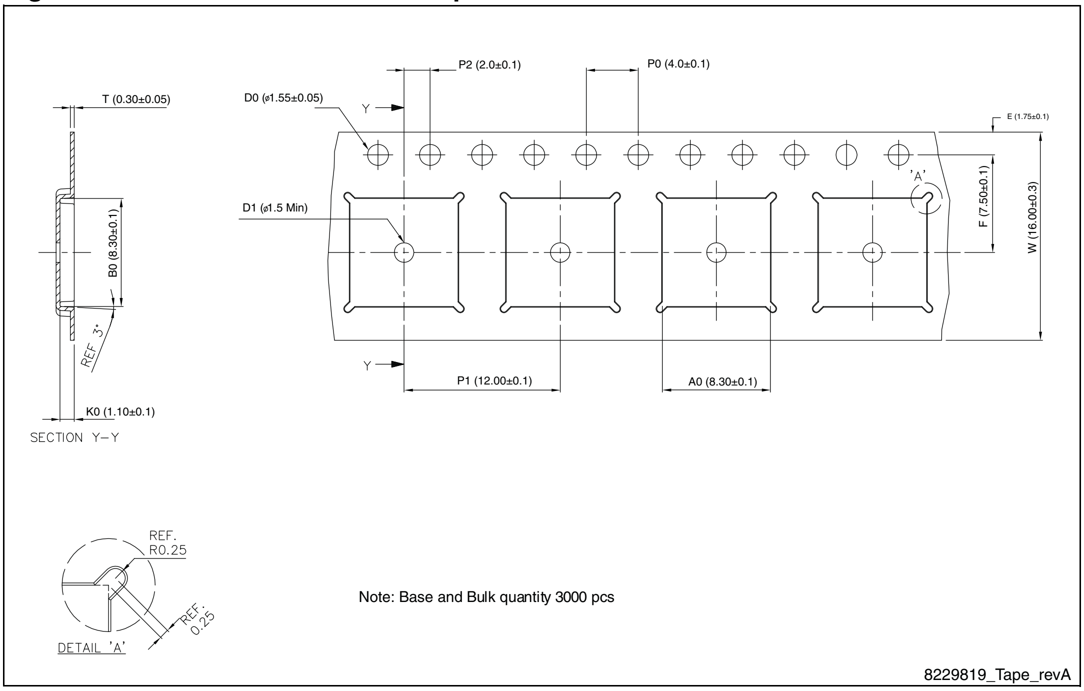


Figure 11. PowerFLAT™ 8x8 HV package orientation in carrier tape

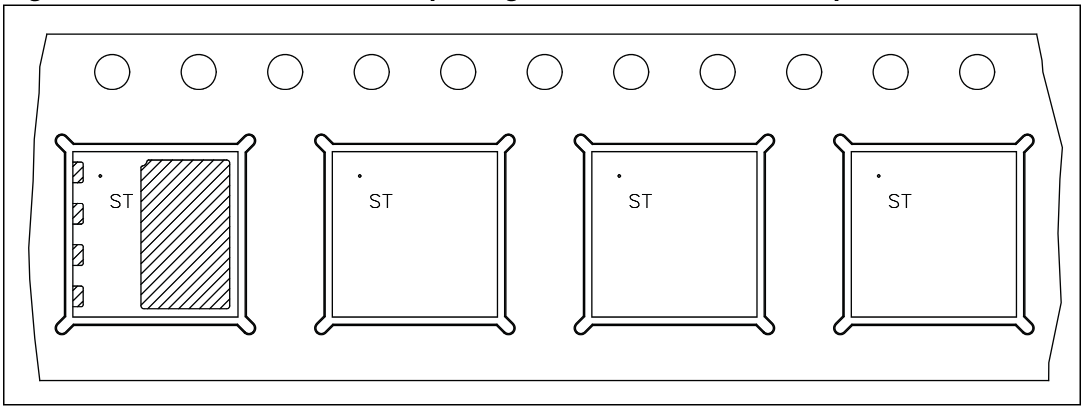
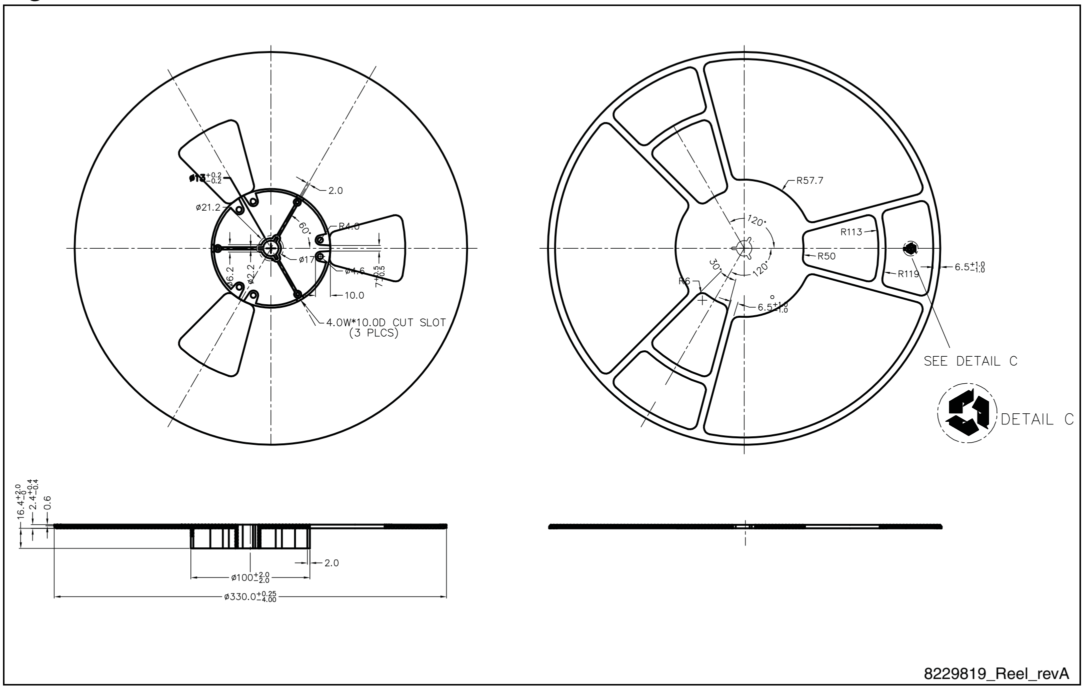


Figure 12. PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
05-Jan-2011	1	First release.
10-Nov-2011	2	*Section 4: Package mechanical data* has been updated. Minor text changes.