MCP6401/1R/1U

1 MHz, 45 µA Op Amps

Features

- Low Quiescent Current: 45 µA (typical)
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input and Output
- Supply Voltage Range: 1.8V to 6.0V
- Unity Gain Stable
- Extended Temperature Range: -40°C to +125°C
- No Phase Reversal

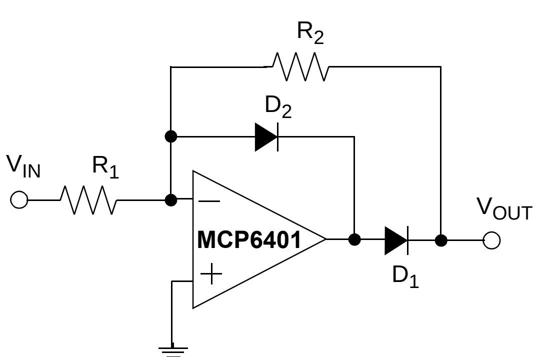
Applications

- Portable Equipment
- Battery Powered System
- Medical Instrumentation
- Data Acquisition Equipment
- Sensor Conditioning
- Supply Current Sensing
- Analog Active Filters

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



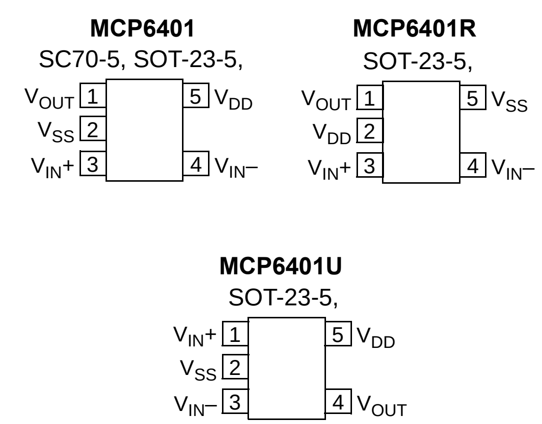
Precision Half-Wave Rectifier

Description

The Microchip Technology Inc. MCP6401/1R/1U family of operational amplifiers (op amps) has low quiescent current (45 µA, typical) and rail-to-rail input and output operation. This family is unity gain stable and has a gain bandwidth product of 1 MHz (typical). These devices operate with a single supply voltage as low as 1.8V. These features make the family of op amps well suited for single-supply, battery-powered applications.

The MCP6401/1R/1U family is designed with Microchip's advanced CMOS process and offered in single packages. All devices are available in the extended temperature range, with a power supply range of 1.8V to 6.0V.

Package Types



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 7.0V
Current at Input Pins ....±2 mA
Analog Inputs (V_{IN}+, V_{IN}-)†† .... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage .... $|V_{DD} – V_{SS}|$
Output Short-Circuit Current ....continuous
Current at Output and Supply Pins ....±30 mA
Storage Temperature ....-65°C to +150°C
Maximum Junction Temperature (T_J)..........................+150°C
ESD protection on all pins (HBM; MM) .... ≥ 4 kV; 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage And Current Limits"**

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +6.0V, V_{SS}= GND, T_A= +25°C, $V_{CM} = V_{DD}/2$, V_{OUT} » $V_{DD}/2$, $V_L = V_{DD}/2$ and R_L = 100 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV	$V_{CM} = V_{SS}$
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A= -40°C to +125°C, $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	63	78	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1.0	100	pA	
		—	30	—	pA	T_A = +85°C
		—	800	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS}-0.2	—	V_{DD}+0.2	V	V_{DD} = 1.8V, **Note 1**
		V_{SS}-0.3	—	V_{DD}+0.3	V	V_{DD} = 6.0V, **Note 1**
Common Mode Rejection Ratio	CMRR	56	71	—	dB	V_{CM} = -0.2V to 2.0V, V_{DD} = 1.8V
		63	78	—	dB	V_{CM} = -0.3V to 6.3V, V_{DD} = 6.0V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	90	110	—	dB	V_{OUT} = 0.3V to V_{DD}-0.3V $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS}+20	—	V_{DD}–20	mV	V_{DD} = 6.0V, R_L = 10 kΩ 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±5	—	mA	V_{DD} = 1.8V
		—	±15	—	mA	V_{DD} = 6.0V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	6.0	V	
Quiescent Current per Amplifier	I_Q	20	45	70	µA	I_O = 0, V_{DD} = 5.0V $V_{CM} = 0.2V_{DD}$

Note 1: Figure 2-11 shows how V_{CMR} changes across temperature.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	0.5	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	3.6	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +6.0V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, SOT-23-5	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, SC70-5	θ_{JA}	—	331	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.3 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

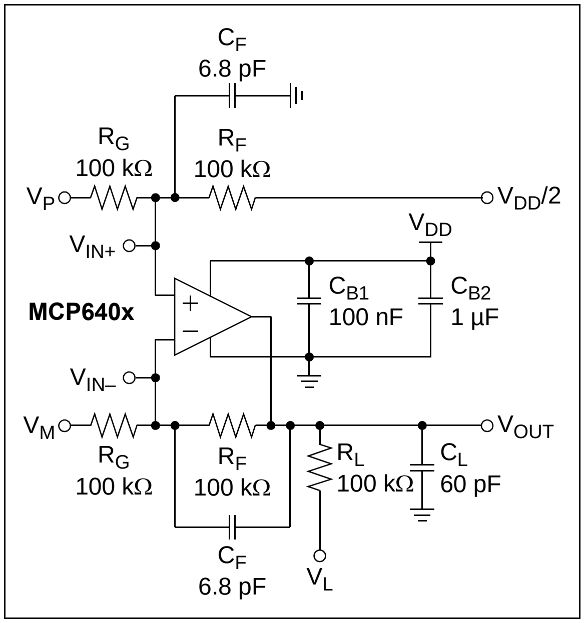


FIGURE 1-1: AC and DC Test Circuit for Most Specifications.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 100 kΩ to V_L and C_L = 60 pF.

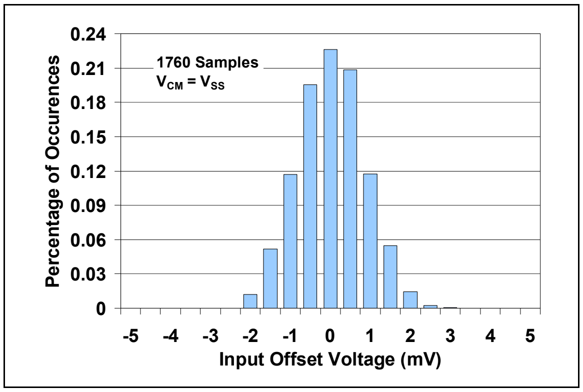


FIGURE 2-1: *Input Offset Voltage.*

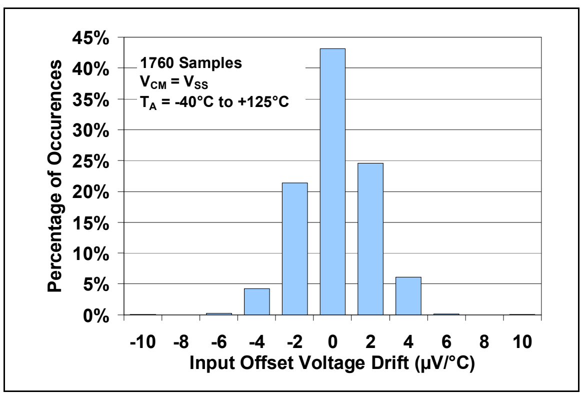


FIGURE 2-2: *Input Offset Voltage Drift.*

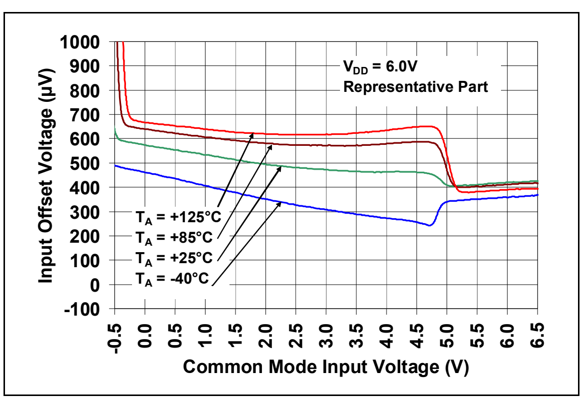


FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage with* V_{DD} *= 6.0V.*

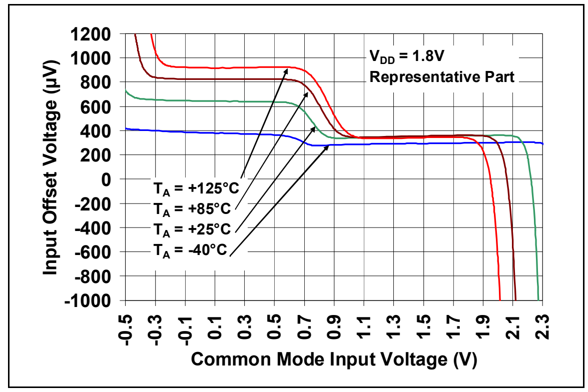


FIGURE 2-4: *Input Offset Voltage vs. Common Mode Input Voltage with* V_{DD} *= 1.8V.*

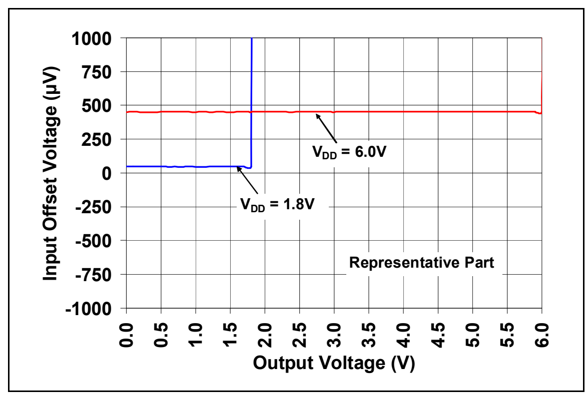


FIGURE 2-5: *Input Offset Voltage vs. Output Voltage.*

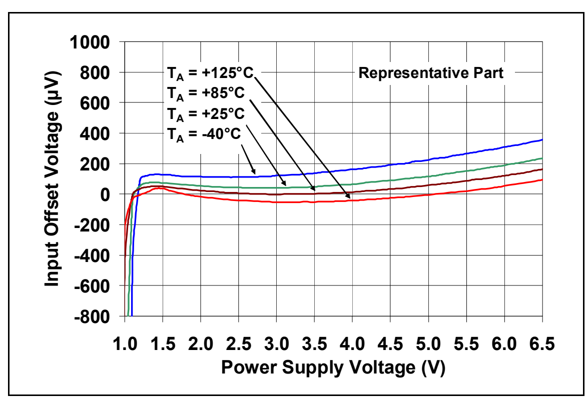


FIGURE 2-6: *Input Offset Voltage vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 100 kΩ to V_L and C_L = 60 pF.

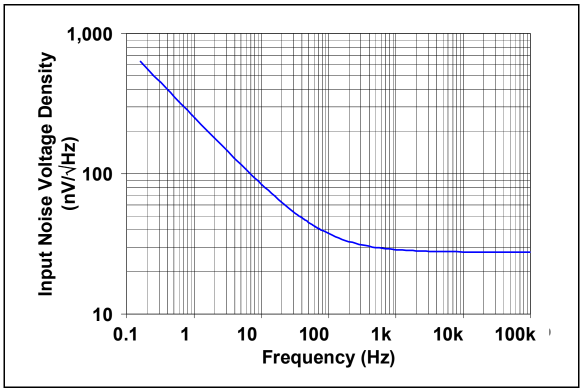


FIGURE 2-7: *Input Noise Voltage Density vs. Frequency.*

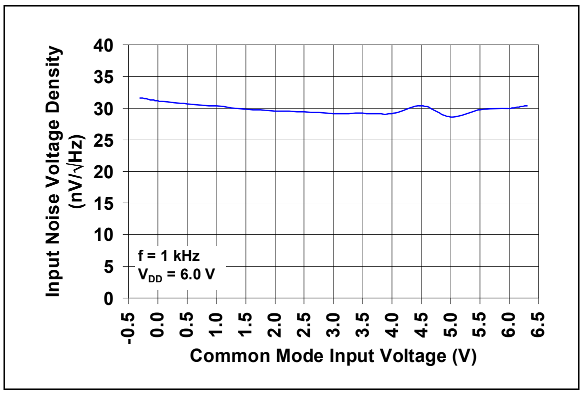


FIGURE 2-8: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

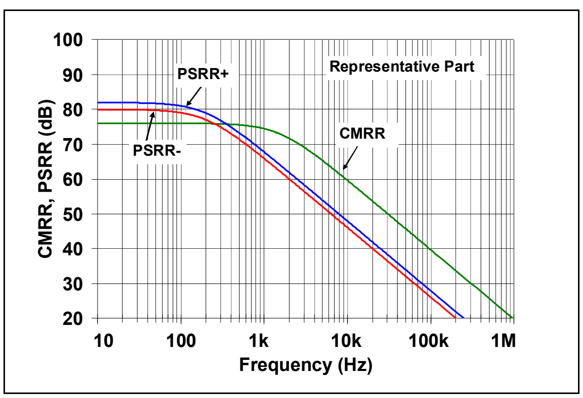


FIGURE 2-9: *CMRR, PSRR vs. Frequency.*

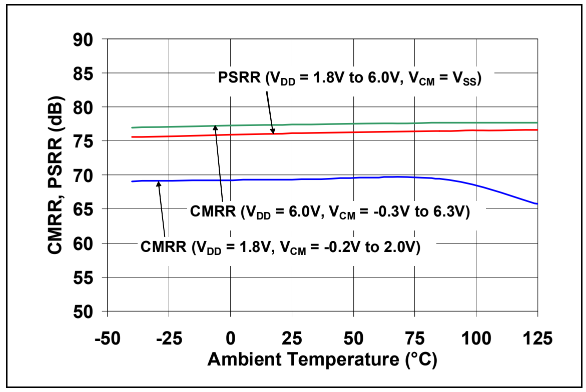


FIGURE 2-10: *CMRR, PSRR vs. Ambient Temperature.*

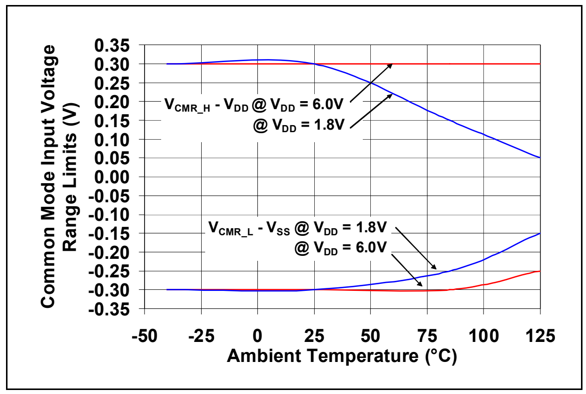


FIGURE 2-11: *Common Mode Input Voltage Range Limits vs. Ambient Temperature.*

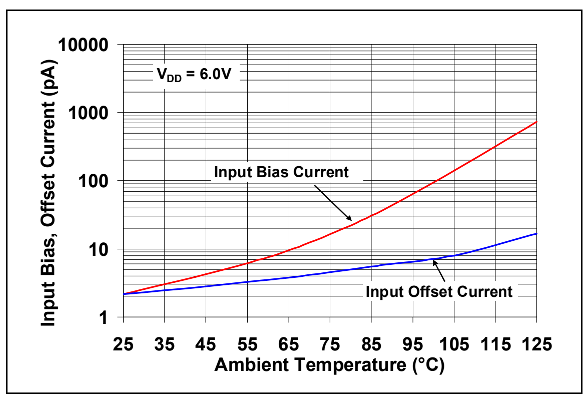


FIGURE 2-12: *Input Bias, Offset Current vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 100 kΩ to V_L and C_L = 60 pF.

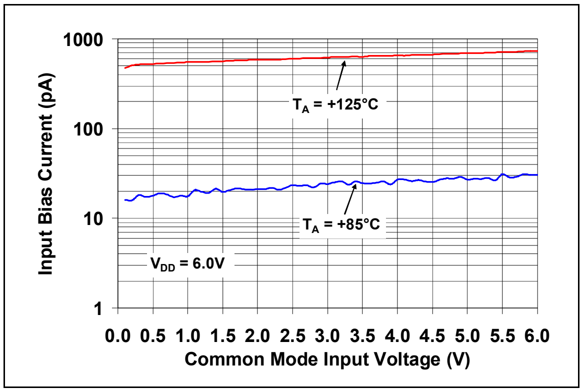


FIGURE 2-13: *Input Bias Current vs. Common Mode Input Voltage.*

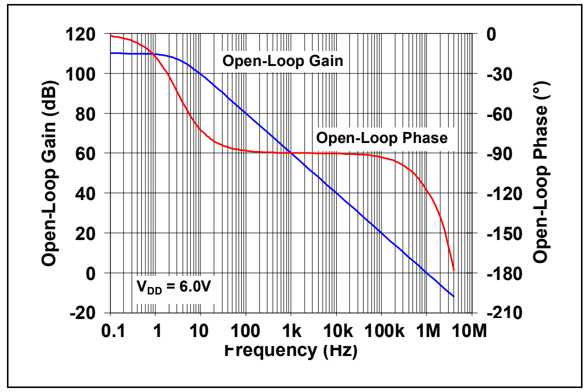


FIGURE 2-16: *Open-Loop Gain, Phase vs. Frequency.*

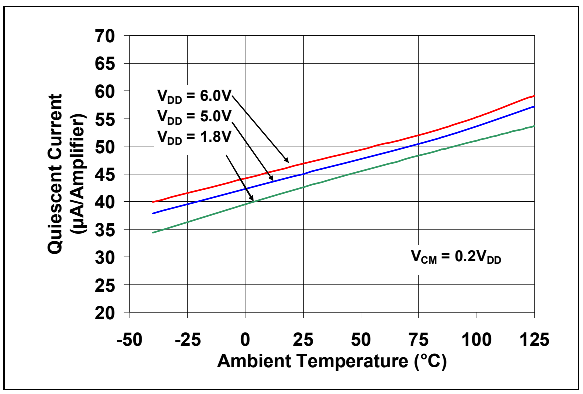


FIGURE 2-14: *Quiescent Current vs Ambient Temperature.*

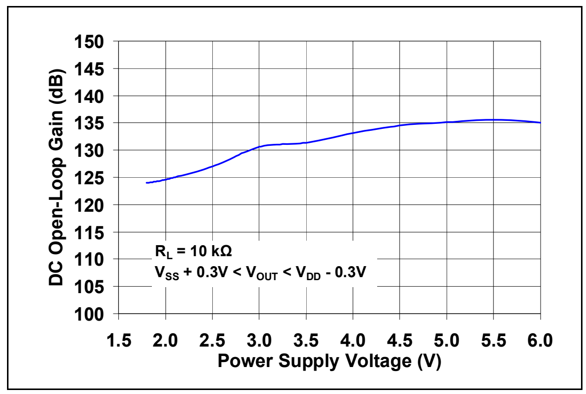


FIGURE 2-17: *DC Open-Loop Gain vs. Power Supply Voltage.*

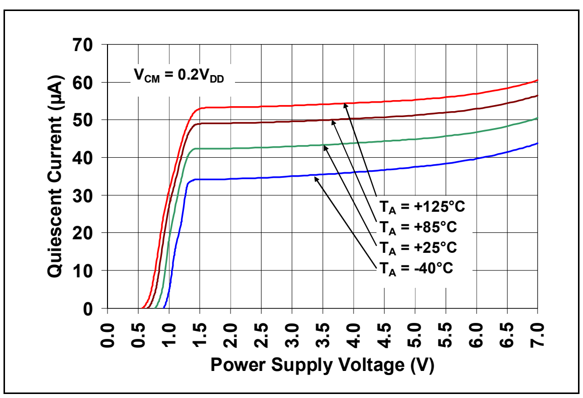


FIGURE 2-15: *Quiescent Current vs. Power Supply Voltage.*

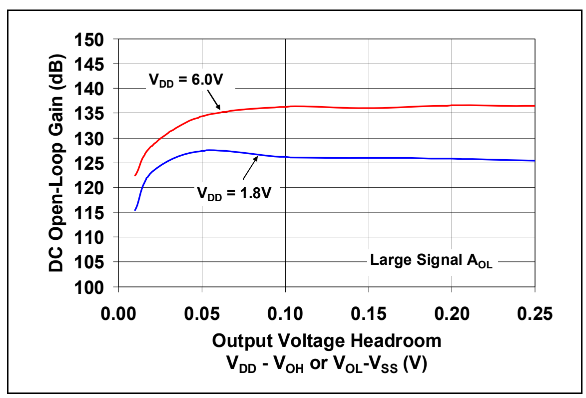


FIGURE 2-18: *DC Open-Loop Gain vs. Output Voltage Headroom.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

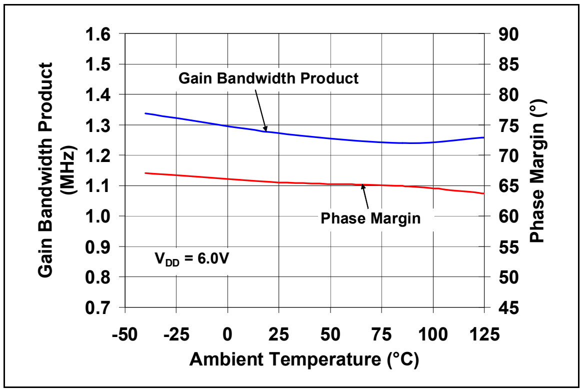


FIGURE 2-19: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

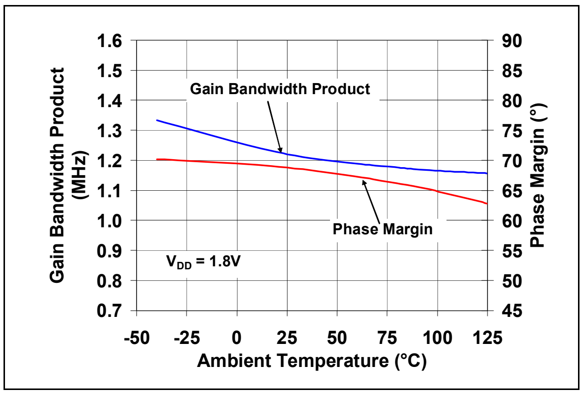


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

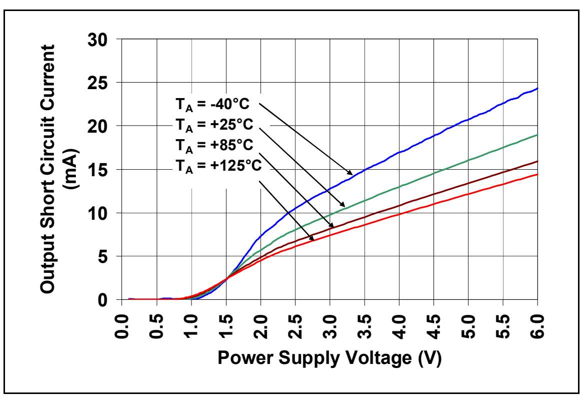


FIGURE 2-21: *Output Short Circuit Current vs. Power Supply Voltage.*

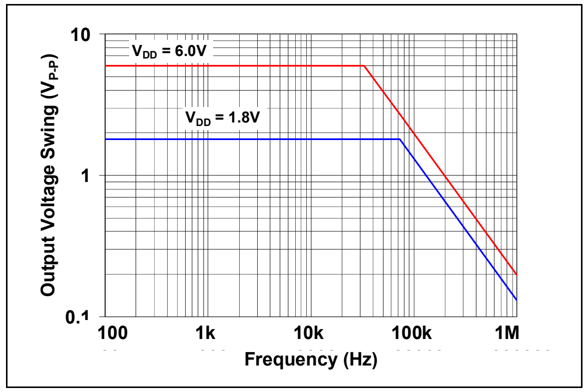


FIGURE 2-22: *Output Voltage Swing vs. Frequency.*

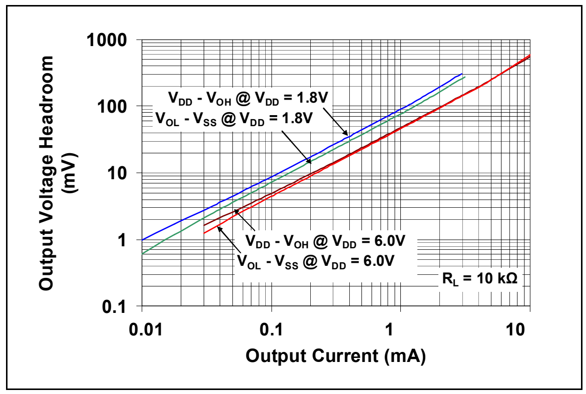


FIGURE 2-23: *Output Voltage Headroom vs. Output Current.*

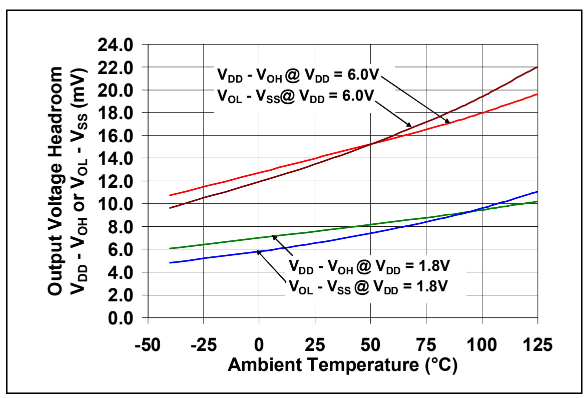


FIGURE 2-24: *Output Voltage Headroom vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

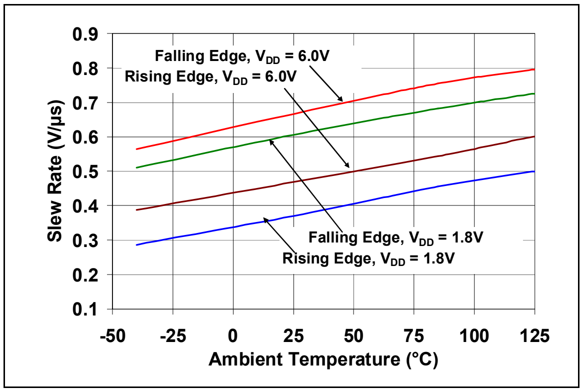


FIGURE 2-25: *Slew Rate vs. Ambient Temperature.*

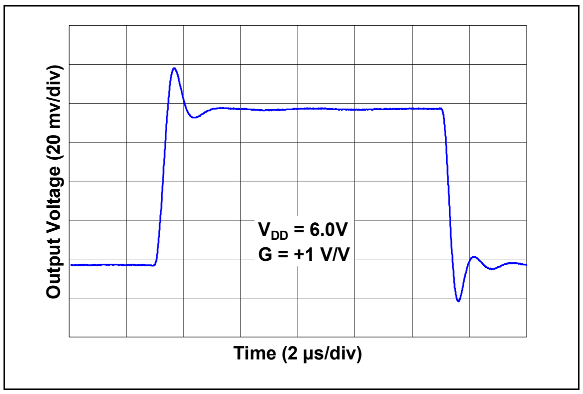


FIGURE 2-26: *Small Signal Non-Inverting Pulse Response.*

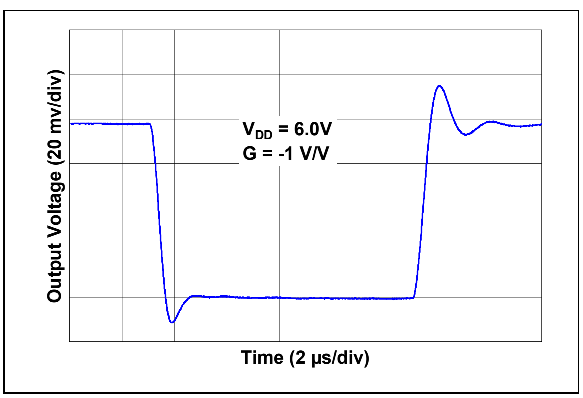


FIGURE 2-27: *Small Signal Inverting Pulse Response.*

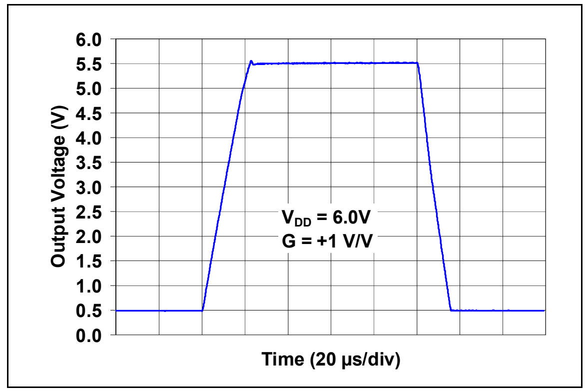


FIGURE 2-28: *Large Signal Non-Inverting Pulse Response.*

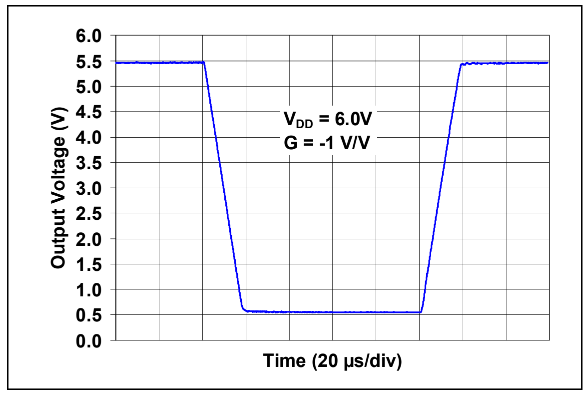


FIGURE 2-29: *Large Signal Inverting Pulse Response.*

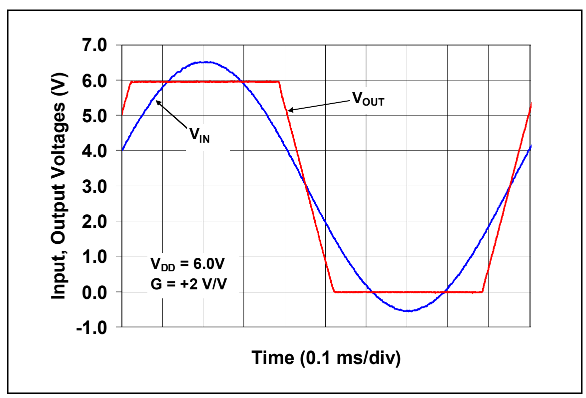


FIGURE 2-30: *The MCP6401/1R/1U Shows No Phase Reversal.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 100 kΩ to V_L and C_L = 60 pF.

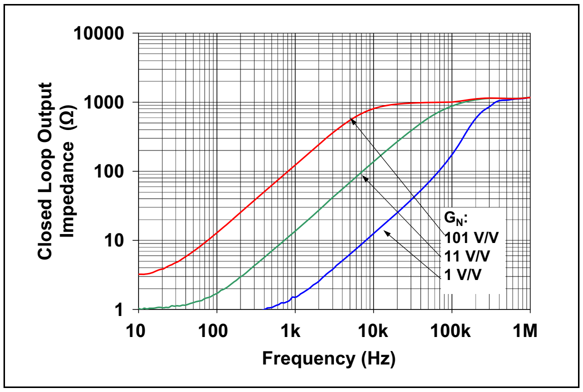


FIGURE 2-31: *Closed Loop Output Impedance vs. Frequency.*

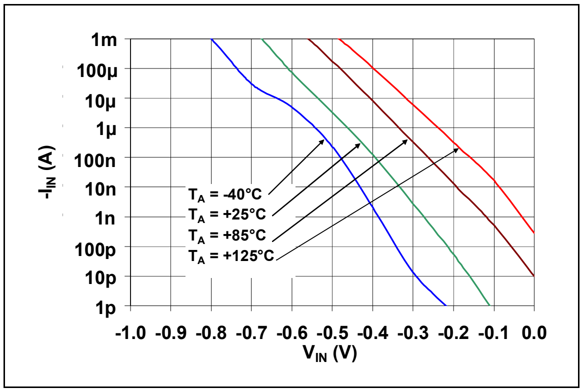


FIGURE 2-32: *Measured Input Current vs. Input Voltage (below V_{SS}).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6401	MCP6401R	MCP6401U	Symbol	Description
SC70-5, SOT-23-5	SOT-23-5	SOT-23-5		
1	1	4	V_{OUT}	Analog Output
2	5	2	V_{SS}	Negative Power Supply
3	3	1	$V_{IN}+$	Non-inverting Input
4	4	3	$V_{IN}-$	Inverting Input
5	2	5	V_{DD}	Positive Power Supply

3.1 Analog Output (V_{OUT})

The output pin is low-impedance voltage source.

3.2 Analog Inputs ($V_{IN}+$, $V_{IN}-$)

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pin (V_{DD}, V_{SS})

The positive power supply (V_{DD}) is 1.8V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

NOTES:

4.0 APPLICATION INFORMATION

The MCP6401/1R/1U family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-power, high precision applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The MCP6401/1R/1U op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-30 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltage that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation and low enough to bypass ESD events within the specified limits.

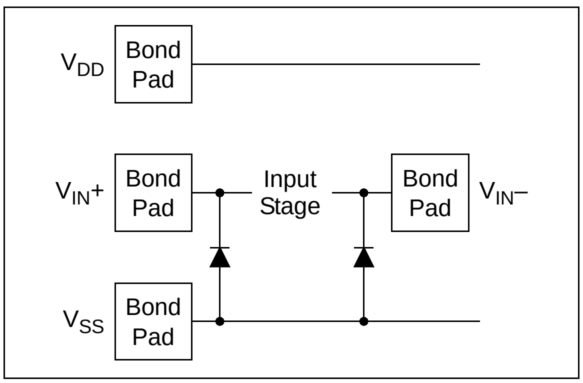
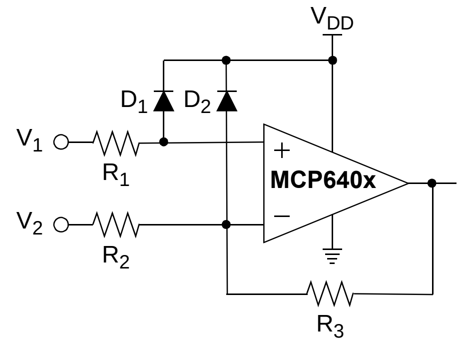


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the voltages and currents at the V_{IN+} and V_{IN-} pins (see **Absolute Maximum Ratings †** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN+} and V_{IN-}) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN+} and V_{IN-}) from going too far above V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistors R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC currents into the input pins (V_{IN+} and V_{IN-}) should be very small. A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}). (See Figure 2-32).

4.1.3 NORMAL OPERATION

The input stage of the MCP6401/1R/1U op amps uses two differential input stages in parallel. One operates at a low common mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. (See Figure 2-11). The input offset voltage is measured at $V_{CM} = V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

The transition between the input stages occurs when V_{CM} is near $V_{DD} - 1.1V$ (See Figures 2-3 and 2-4). For the best distortion performance and gain linearity, with non-inverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6401/1R/1U op amps is V_{SS} + 20 mV (minimum) and V_{DD} – 20 mV (maximum) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 6.0V. Refer to Figures 2-23 and 2-24 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1 V/V) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

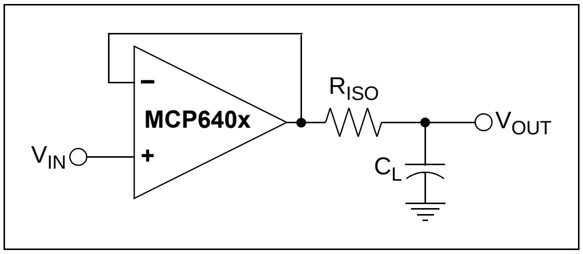


FIGURE 4-3: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

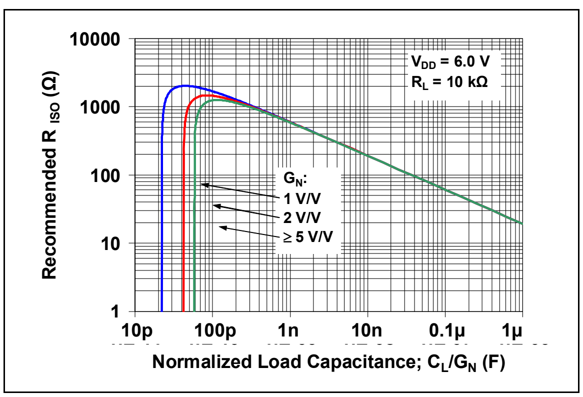


FIGURE 4-4: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6401/1R/1U SPICE macro model are very helpful.

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6401/1R/1U family's bias current at +25°C (±1.0 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-5.

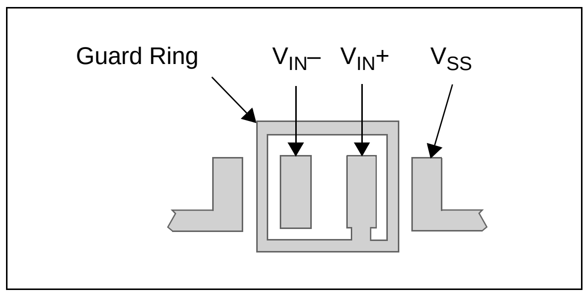


FIGURE 4-5: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.6 Application Circuits

4.6.1 PRECISION HALF-WAVE RECTIFIER

The precision half-wave rectifier, which is also known as a super diode, is a configuration obtained with an operational amplifier in order to have a circuit behaving like an ideal diode and rectifier. It effectively cancels the forward voltage drop of the diode so that very low level signals can still be rectified with minimal error. This can be useful for high-precision signal processing. The MCP6401/1R/1U op amps have high input impedance, low input bias current and rail-to-rail input/output, which makes this device suitable for precision rectifier applications.

Figure 4-6 shows a precision half-wave rectifier and its transfer characteristic. The rectifier's input impedance is determined by the input resistor R_1. To avoid loading effect, it must be driven from a low impedance source.

When V_{IN} is greater than zero, D_1 is OFF and D_2 is ON, V_{OUT} is zero. When V_{IN} is less than zero, D_1 is ON and D_2 is OFF, and V_{OUT} is the V_{IN} with an amplification of $-R_2/R_1$.

The rectifier circuit shown in Figure 4-6 has the benefit that the op amp never goes in saturation, so the only thing affecting its frequency response is the amplification and the gain bandwidth product.

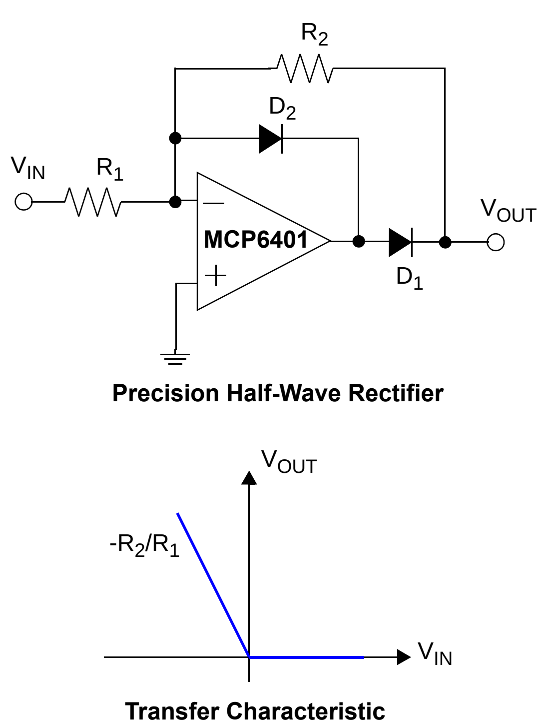
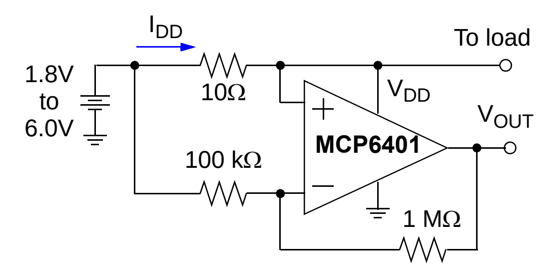


FIGURE 4-6: Precision Half-Wave Rectifier.

4.6.2 BATTERY CURRENT SENSING

The MCP6401/1R/1U op amps' Common Mode Input Range, which goes 0.3V beyond both supply rails, supports their use in high side and low side battery current sensing applications. The low quiescent current (45 µA, typical) helps prolong battery life, and the rail-to-rail output supports detection of low currents.

Figure 4-7 shows a high side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the common mode input voltage of the op amp below V_{DD}, which is within its allowed range. The output of the op amp will also be below V_{DD}, which is within its Maximum Output Voltage Swing specification.

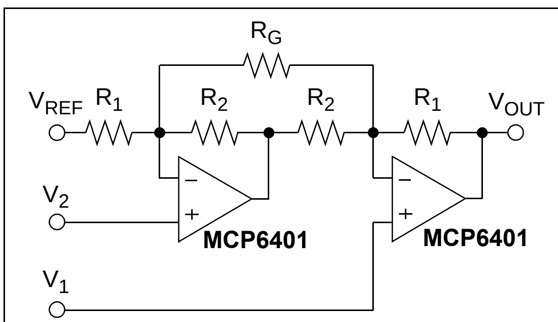


$$I_{DD} = \frac{V_{DD} - V_{OUT}}{(10\ V/V) \cdot (10\Omega)}$$

FIGURE 4-7: Supply Current Sensing.

4.6.3 INSTRUMENTATION AMPLIFIER

The MCP6401/1R/1U op amps are well suited for conditioning sensor signals in battery-powered applications. Figure 4-8 shows a two op amp instrumentation amplifier, using the MCP6401, that works well for applications requiring rejection of common mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low impedance source. In single supply applications, V_{REF} is typically $V_{DD}/2$.



$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

FIGURE 4-8: Two Op Amp Instrumentation Amplifier.

NOTES:

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6401/1R/1U family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6401/1R/1U op amp is available on the Microchip web site at www.microchip.com. The model was written and tested in official Orcad (Cadence) owned PSPICE. For the other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot be guaranteed that it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Datasheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV

5.6 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1297:** *"Microchip's Op Amp SPICE Macro Models",* DS01297

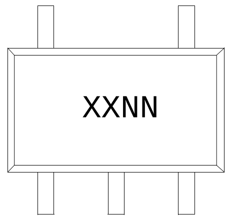
These application notes and others are listed in the design guide:

- *"Signal Chain Design Guide",* DS21825

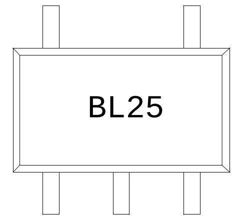
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

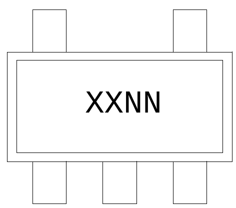
5-Lead SC70 **(MCP6401 only)**



Example:

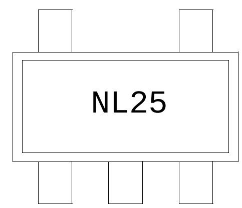


5-Lead SOT-23



Part Number	Code
MCP6401T-E/OT	NLNN
MCP6401RT-E/OT	NMNN
MCP6401UT-E/OT	NPNN

Example:



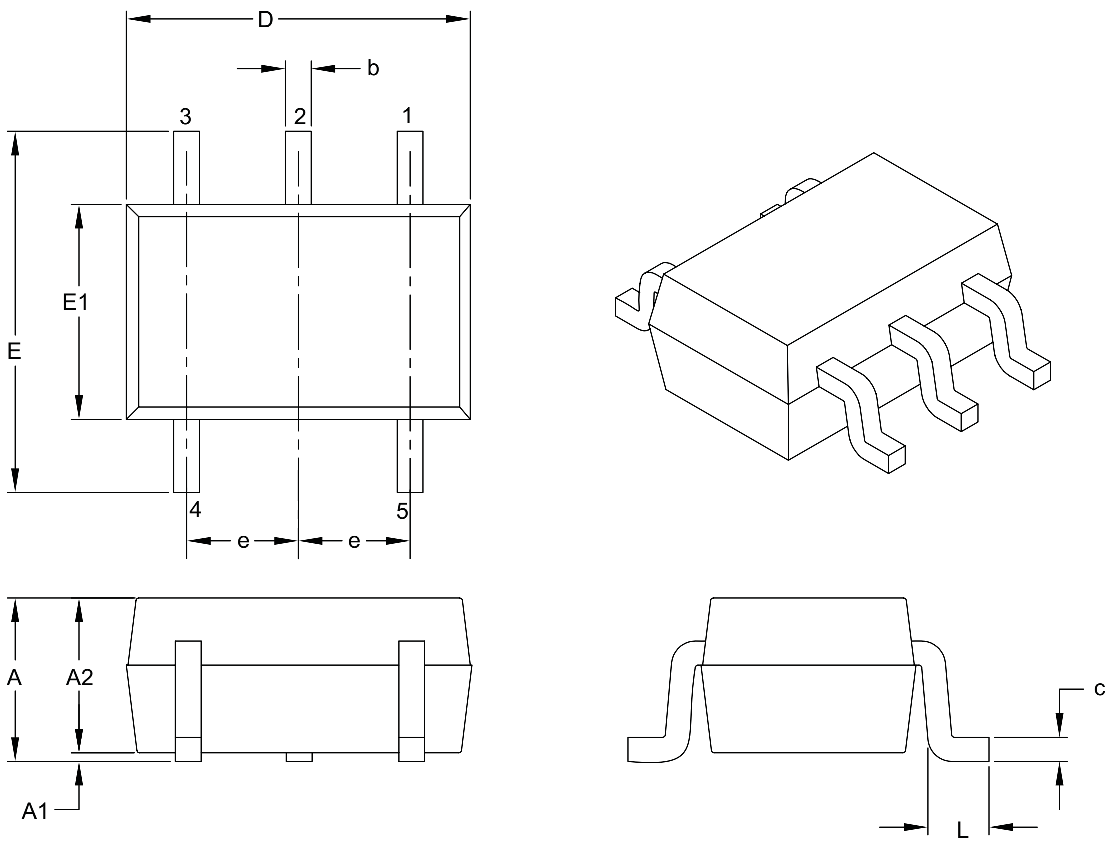
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

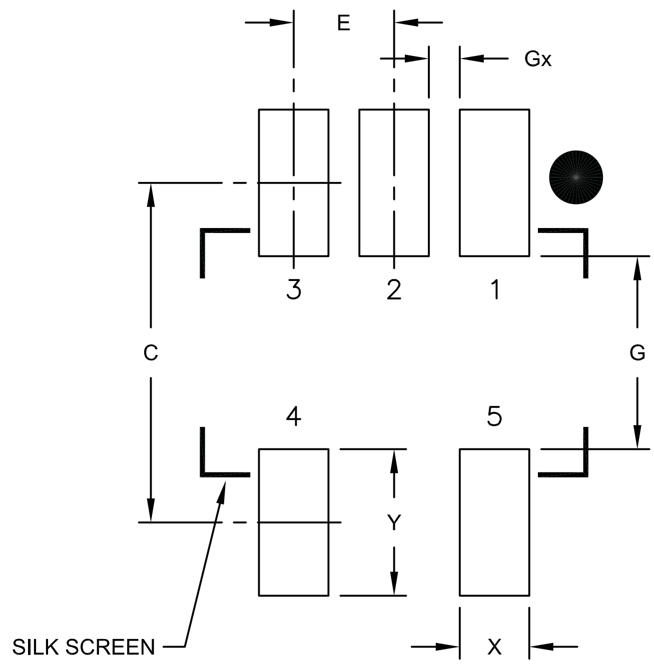
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

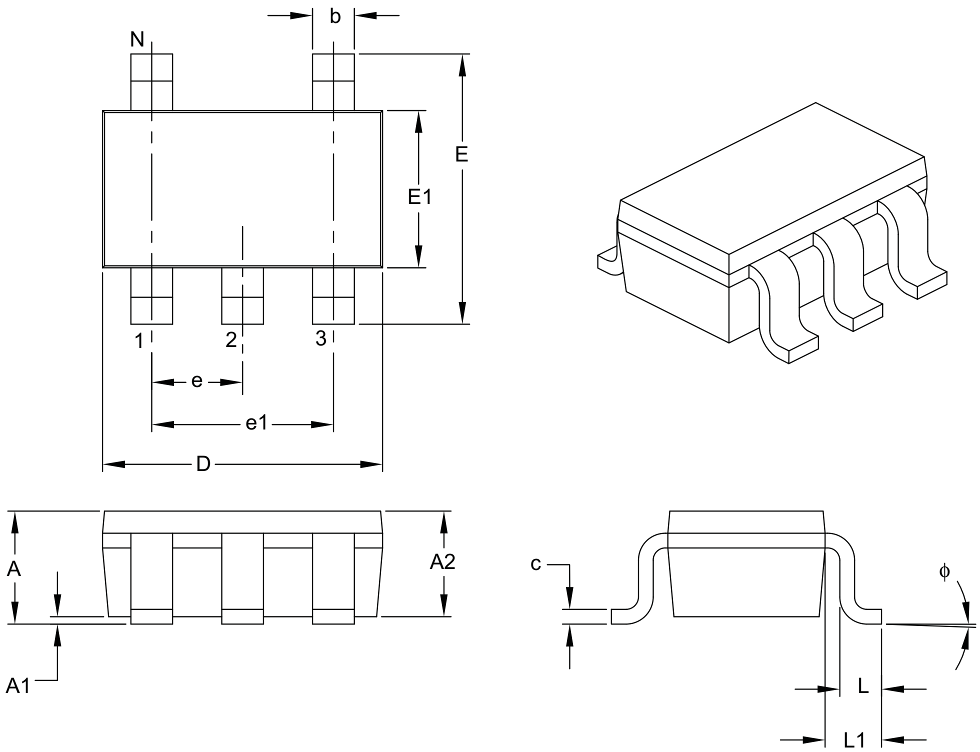
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

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Microchip Technology Drawing C04-091B

APPENDIX A: REVISION HISTORY

Revision A (December 2009)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6401T:	Single Op Amp (Tape and Reel) (SC70-5, SOT-23-5)
	MCP6401RT:	Single Op Amp (Tape and Reel) (SOT-23-5)
	MCP6401UT:	Single Op Amp (Tape and Reel) (SOT-23-5)
Temperature Range:	E	= -40°C to +125°C
Package:	LT	= Plastic Package (SC70), 5-lead
	OT	= Plastic Small Outline Transistor (SOT-23), 5-lead

Examples:

a) MCP6401T-E/LT: Tape and Reel, 5LD SC70 pkg
b) MCP6401T-E/OT: Tape and Reel, 5LD SOT-23 pkg
c) MCP6401RT-E/OT: Tape and Reel, 5LD SOT-23 pkg
d) MCP6401UT-E/OT: Tape and Reel, 5LD SOT-23 pkg

NOTES:

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- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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