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ITE Tech. Inc.

IT8780F

ServerWork I/O
(Code Name: SWIO)

Preliminary Specification V0.3

INTEGRATED TECHNOLOGY EXPRESS, INC.

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1. Features

- **Low Pin Count Interface**
  - Compliant with Intel Low Pin Count Interface Specification Rev. 1.0 (Sept. 29, 1997)
  - Supports LDRQ#, SERIRQ protocols
- **Two 16C550 UARTs**
  - Supports two standard Serial Ports
  - Maximum data rate up to 1.5 Mbps
  - Supports Smart Card Reader protocols
- **Smart Card Reader**
  - Compliant with Personal Computer Smart Card (PC/SC) Working Group standard
  - Compliant with smart card (ISO 7816) protocols
  - Supports card present detect
  - Supports one programmable clock frequency, 7.1 MHz, and 3.5 MHz (default) card clocks
- **IEEE 1284 Parallel Port**
  - Standard mode -- Bi-directional SPP compliant
  - Enhanced mode -- EPP V. 1.7 and V. 1.9 compliant
  - High speed mode -- ECP, IEEE 1284 compliant
  - Back-drive current reduction
  - Printer power-on damage reduction
  - Supports POST (Power-On Self Test) Data Port
- **Floppy Disk Controller**
  - Supports two 360K/720K/1.2M/1.44M/2.88M floppy disk drives
  - Enhanced digital data separator
  - 3-Mode drives supported
  - Supports write protection via software
- **Keyboard Controller**
  - 8042 compatible for PS/2 keyboard and mouse
  - 2KB of programmable ROM and 256-byte data RAM
  - GateA20 and Keyboard reset output
  - Supports Keyboard and Mouse I/F hardware auto-swap
- **Extended I/F**
  - Provides Flash ROM I/F and User-defined Memory extension
  - Provides 2 Programmable Chip Selects for the I/O devices.
- **43 General Purpose I/O Pins**
  - GPIO pins can be individually enabled or disabled via software configuration registers
  - GPIO pins can be individually set as input or output via software configuration registers
  - Supports 16 programmable De-bouncing inputs and two Blinking outputs
  - Some GPIO pins are powered by VSB and can be used as power-up events
- **External IRQ Input Routing Capability**
  - Provides IRQ input routing through GPIO input mode
- **Real Time Clock (RTC)**
  - 146818 Compatible with 242-byte CMOS RAM
  - Binary or BCD data format for time, alarm and calendar
  - Time of Century Wake-Up Alarm
  - 12/24 hour format for hour register and alarm hour register
- **ACPI**
  - ACPI 1.0b compliant
  - Power up events: IRQ, KBD, Mouse, RING Indicator, GPIO, Power Button, …
  - Generation of SIOSMI#
  - Individual function enable/disable control bits
- **SM Bus Slave**
  - Accessing internal registers
- **Clocks**
  - 33 MHz LPC Clock Input
  - 48 MHz System Clock Input
  - 32.768 KHz oscillator circuit for RTC
  - 40 MHz and 1 Hz outputs
- **Power Supply**
  - +3.3V pad with 5V tolerance; +3.3V core
  - V_Battery (VBAT) for RTC
  - V_Standby (VSB) supported
- **Package: 128-pin QFP**

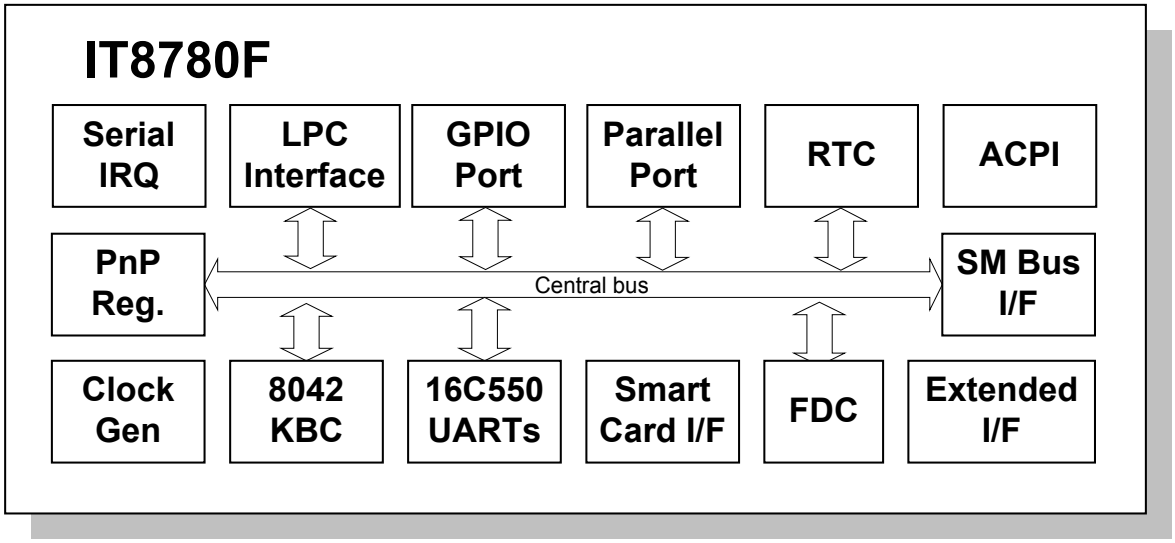
2. General Description

The IT8780F is a Low Pin Count Interface-based highly integrated Super I/O. The IT8780F provides the most commonly used legacy Super I/O functionality plus the Real Time Clock (RTC) and Smart Card Reader Interface. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.0". The IT8780F meets the "Microsoft® PC98 & PC99 System Design Guide" requirements.

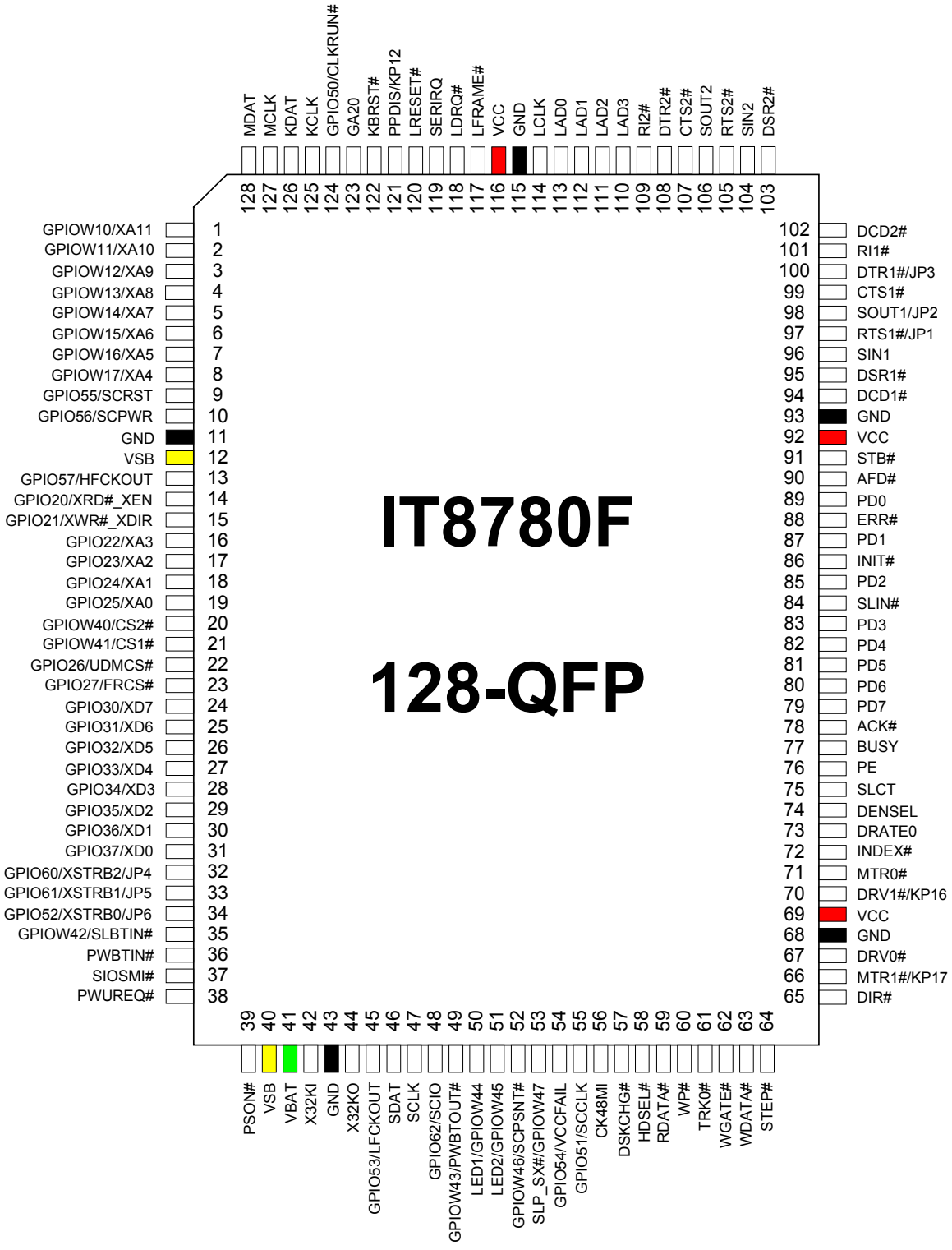
The IT8780F has integrated 8 logical devices. One high-performance 2.88MB floppy disk controller, with digital data separator, supports two 360K/720K/1.2M/1.44M/2.88M floppy disk drives. One multi-mode high-performance parallel port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9 are supported), and the IEEE 1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication. The IT8780F also has an integrated 8042 compatible Keyboard Controller with 2KB of programmable ROM for customer application and a 146818-compatible Real Time Clock with 242-byte CMOS RAM. IT8780F provides an extended I/F to LPC bus to enable the ISA-like external 8-bit peripherals, including the Flash ROM I/F. It also provides 43 General Purpose I/O pins (multi-function pins) and SM bus slave mode to access the chip configuration registers.

These 8 logical devices can be individually enabled or disabled via software configuration registers. The IT8780F utilizes power-saving circuitry to reduce power consumption, and once a logical device is disabled, the inputs are gated inhibit, the outputs are tri-state, and the input clock is disabled. The device requires a single 24/48 MHz clock input and operates with +3.3V power supply but +5V tolerance. The IT8780F is available in 128-pin QFP (Quad Flat Package).

3. Block Diagram



4. Pin Configuration



Top View

Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GPIOW10/XA11	33	GPIO61/XSTRB1/ JP5	65	DIR#	97	RTS1#/JP1
2	GPIOW11/XA10	34	GPIO52/XSTRB0/ JP6	66	MTR1#/KP17	98	SOUT1/JP2
3	GPIOW12/XA9	35	GPIOW42/SLBTI N#	67	DRV0#	99	CTS1#
4	GPIOW13/XA8	36	PWBTIN#	68	GND	100	DTR1#/JP3
5	GPIOW14/XA7	37	SIOSMI#	69	VCC	101	RI1#
6	GPIOW15/XA6	38	PWUREQ#	70	DRV1#/KP16	102	DCD2#
7	GPIOW16/XA5	39	PSON#	71	MTR0#	103	DSR2#
8	GPIOW17/XA4	40	VSB	72	INDEX#	104	SIN2
9	GPIO55/SCRST	41	VBAT	73	DRATE0	105	RTS2#
10	GPIO56/SCPWR	42	X32KI	74	DENSEL	106	SOUT2
11	GND	43	GND	75	SLCT	107	CTS2#
12	VSB	44	X32KO	76	PE	108	DTR2#
13	GPIO57/HFCKOU T	45	GPIO53/LFCKOU T	77	BUSY	109	RI2#
14	GPIO20/XRD#_X EN	46	SDAT	78	ACK#	110	LAD3
15	GPIO21/ XWR#_XDIR	47	SCLK	79	PD7	111	LAD2
16	GPIO22/XA3	48	GPIO62/SCIO	80	PD6	112	LAD1
17	GPIO23/XA2	49	GPIOW43/ PWBTOUT#	81	PD5	113	LAD0
18	GPIO24/XA1	50	LED1/GPIOW44	82	PD4	114	LCLK
19	GPIO25/XA0	51	LED2/GPIOW45	83	PD3	115	GND
20	GPIOW40/CS2#	52	GPIOW46/SCPS NT#	84	SLIN#	116	VCC
21	GPIOW41/CS1#	53	SLP_SX#/GPIOW 47	85	PD2	117	LFRAME#
22	GPIO26/UDMCS#	54	GPIO54/VCCFAIL	86	INIT#	118	LDRQ#
23	GPIO27/FRCS#	55	GPIO51/SCCLK	87	PD1	119	SERIRQ
24	GPIO30/XD7	56	CK48MI	88	ERR#	120	LRESET#
25	GPIO31/XD6	57	DSKCHG#	89	PD0	121	PPDIS/KP12
26	GPIO32/XD5	58	HDSEL#	90	AFD#	122	KBRST#
27	GPIO33/XD4	59	RDATA#	91	STB#	123	GA20
28	GPIO34/XD3	60	WP#	92	VCC	124	GPIO50/CLKRUN #
29	GPIO35/XD2	61	TRK0#	93	GND	125	KCLK
30	GPIO36/XD1	62	WGATE#	94	DCD1#	126	KDAT
31	GPIO37/XD0	63	WDATA#	95	DSR1#	127	MCLK
32	GPIO60/XSTRB2/ JP4	64	STEP#	96	SIN1	128	MDAT

Table 4-2. Pins Listed in Alphabetical Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
78	ACK#	23	GPIO27/FRCS#	52	GPIOW46/SCPSNT#	36	PWBTIN#
90	AFD#	24	GPIO30/XD7	58	HDSEL#	38	PWUREQ#
77	BUSY	25	GPIO31/XD6	72	INDEX#	59	RDATA#
56	CK48MI	26	GPIO32/XD5	86	INIT#	101	RI1#
99	CTS1#	27	GPIO33/XD4	122	KBRST#	109	RI2#
107	CTS2#	28	GPIO34/XD3	125	KCLK	97	RTS1#/JP1
94	DCD1#	29	GPIO35/XD2	126	KDAT	105	RTS2#
102	DCD2#	30	GPIO36/XD1	113	LAD0	47	SCLK
74	DENSEL	31	GPIO37/XD0	112	LAD1	46	SDAT
65	DIR#	124	GPIO50/CLKRUN#	111	LAD2	119	SERIRQ
73	DRATE0	55	GPIO51/SCCLK	110	LAD3	96	SIN1
67	DRV0#	34	GPIO52/XSTRB0/JP6	114	LCLK	104	SIN2
70	DRV1#/KP16	45	GPIO53/LFCKOUT	118	LDRQ#	37	SIOSMI#
57	DSKCHG#	54	GPIO54/VCCFAIL	50	LED1/GPIOW44	75	SLCT
95	DSR1#	9	GPIO55/SCRST	51	LED2/GPIOW45	84	SLIN#
103	DSR2#	10	GPIO56/SCPWR	117	LFRAME#	53	SLP_SX#/GPIOW47
100	DTR1#/JP3	13	GPIO57/HFCKOUT	120	LRESET#	98	SOUT1/JP2
108	DTR2#	32	GPIO60/XSTRB2/JP4	127	MCLK	106	SOUT2
88	ERR#	33	GPIO61/XSTRB1/JP5	128	MDAT	91	STB#
123	GA20	48	GPIO62/SCIO	71	MTR0#	64	STEP#
11	GND	1	GPIOW10/XA11	66	MTR1#/KP17	61	TRK0#
43	GND	2	GPIOW11/XA10	89	PD0	41	VBAT
68	GND	3	GPIOW12/XA9	87	PD1	69	VCC
93	GND	4	GPIOW13/XA8	85	PD2	92	VCC
115	GND	5	GPIOW14/XA7	83	PD3	116	VCC
14	GPIO20/XRD#_XEN	6	GPIOW15/XA6	82	PD4	12	VSB
15	GPIO21/XWR#_XDIR	7	GPIOW16/XA5	81	PD5	40	VSB
16	GPIO22/XA3	8	GPIOW17/XA4	80	PD6	63	WDATA#
17	GPIO23/XA2	20	GPIOW40/CS2#	79	PD7	62	WGATE#
18	GPIO24/XA1	21	GPIOW41/CS1#	76	PE	60	WP#
19	GPIO25/XA0	35	GPIOW42/SLBTIN#	121	PPDIS/KP12	42	X32KI
22	GPIO26/UDMCS#	49	GPIOW43/PWBTOUT#	39	PSON#	44	X32KO

5. IT8780F Pin Descriptions

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
69, 92, 116	**VCC**	PWR	-	***+3.3V Power Supply.***
12, 40	**VSB**	PWR	-	***+3.3V Standby Power Supply.***
41	**VBAT**	PWR	-	***+3.3V Battery Supply.***
11, 43, 68, 93, 115	**GND**	GND	-	***Ground.***

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
120	**LRESET#**	DI	VCC	***LPC RESET #.***
118	**LDRQ#**	DO16	VCC	***LPC DMA Request #.*** An encoded signal for DMA channel select.
119	**SERIRQ**	DIO16	VCC	***Serial IRQ.***
117	**LFRAME#**	DI	VCC	***LPC Frame #.*** This signal indicates the start of LPC cycle.
110 – 113	**LAD[3:0]**	DIO8	VCC	***LPC Address/Data 3 - 0.*** 4-bit LPC address/bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
114	**LCLK**	DI	VCC	***LPC Clock.*** 33 MHz LPC clock input.
124	**CLKRUN#/ GPIO50**	DIOD8/ DIOD8	VSB	***Clock Run # / General Purpose I/O 50.*** • The first function of this pin is the clock run #. This is an open-drain output and input. The IT8780F uses this signal to request starting (or speed up) the clock. CLKRUN# also indicates the clock status. • The second function of this pin is the General Purpose I/O 50. • The function configuration of this pin is decided by the software configuration registers.

Table 5-3. Pin Description of SM Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
46	**SDAT**	DIOD8	VSB	***Serial Bus Bi-directional Data.*** The function of this pin is SM bus bi-directional data.
47	**SCLK**	DI	VSB	***Serial Bus Clock.*** The function of this pin is SM Bus clock.

Table 5-4. Pin Description of Serial Port 1 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
96	**SIN1**	DI	VCC	***Serial Data In 1.*** This input receives serial data from the communications link.
98	**SOUT1/JP2**	DO8/ DI	VCC	***Serial Data Out 1.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. *During LRESET#, this pin is input for JP2 power-on strapping option.*
95	**DSR1#**	DI	VCC	***Data Set Ready 1 #.*** When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR1# signal is a MODEM status input whose condition can be tested by reading the MSR register.
97	**RTS1#/JP1**	DO8/DI	VCC	***Request to Send 1 #.*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS1# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS1# is set to its inactive state. *During LRESET#, this pin is input for JP1 power-on strapping option.*
100	**DTR1#/JP3**	DO8/DI	VCC	***Data Terminal Ready 1 #.*** DTR1# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR1# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR1# is set to its inactive state. *During LRESET#, this pin is input for JP3 power-on strapping option.*
99	**CTS1#**	DI	VCC	***Clear to Send 1 #.*** When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS1# signal is a MODEM status input whose condition can be tested by reading the MSR register.
101	**RI1#**	DI	VCC	***Ring Indicator 1 #.*** When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI1# signal is a MODEM status input whose condition can be tested by reading the MSR register.
94	**DCD1#**	DI	VCC	***Data Carrier Detect 1 #.*** When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD1# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-6. Pin Description of Serial Port 2 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
104	**SIN2**	DI	VCC	***Serial Data In 2.*** This input receives serial data from the communications link.
106	**SOUT2**	DO8	VCC	***Serial Data Out 2.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
103	**DSR2#**	DI	VCC	***Data Set Ready 2 #.*** When low, indicates that the MODEM or data set is ready to establish a communications link. The DSR2# signal is a MODEM status input whose condition can be tested by reading the MSR register.
105	**RTS2#**	DO8	VCC	***Request to Send 2 #.*** When low, this output indicates to the MODEM or data set that the device is ready to send data. RTS2# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS2# is set to its inactive state.
108	**DTR2#**	DO8	VCC	***Data Terminal Ready 2 #.*** DTR2# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR2# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR2# is set to its inactive state.
107	**CTS2#**	DI	VCC	***Clear to Send 2 #.*** When low, indicates that the MODEM or data set is ready to accept data. The CTS2# signal is a MODEM status input whose condition can be tested by reading the MSR register.
109	**RI2#**	DI	VCC	***Ring Indicator 2 #.*** When low, indicates that a telephone ring signal has been received by the MODEM. The RI2# signal is a MODEM status input whose condition can be tested by reading the MSR register.
102	**DCD2#**	DI	VCC	***Data Carrier Detect 2 #.*** When low, indicates that the MODEM or data set has detected a carrier. The DCD2# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-7. Pin Description of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
75	**SLCT**	DI	VCC	***Printer Select.*** This signal goes high when the line printer has been selected.
76	**PE**	DI	VCC	***Printer Paper End.*** This signal is set high by the printer when it runs out of paper.
77	**BUSY**	DI	VCC	***Printer Busy.*** This signal goes high when the line printer has a local operation in progress and cannot accept data.
78	**ACK#**	DI	VCC	***Printer Acknowledge #.*** This signal goes low to indicate that the printer has already received a character and is ready to accept another.
84	**SLIN#**	$DO_{16/24}$	VCC	***Printer Select Input #.*** When low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register.
86	**INIT#**	$DO_{16/24}$	VCC	***Printer Initialize #.*** Active low. This signal is derived from bit 2 of the printer control register, and is used to initialize the printer.
88	**ERR#**	DI	VCC	***Printer Error #.*** When low, it indicates that the printer has encountered an error. The error message can be read from bit 3 of the printer status register.
90	**AFD#**	$DO_{16/24}$	VCC	***Printer Auto Line Feed #.*** Active low. This signal is derived from the complement of bit 1 of the printer control register, and is used to advance one line after each line is printed.
91	**STB#**	$DO_{16/24}$	VCC	***Printer Strobe #.*** Active low. This signal is the complement of bit 0 of the printer control register, and is used to strobe the printing data into the printer.
79–83, 85, 87, 89	**PD[7:0]**	$DIO_{16/24}$	VCC	***Parallel Port Data Bus.*** This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
121	**PPDIS/ KP12**	DI/ DIOD8	VCC	***Parallel Port Disable/ KBC I/O Port 12.*** • The first function of this pin is Parallel Port Disable. When high, this input disables all the output signals of the Parallel Port. • The second function of this pin is the KBC I/O Port 12. • The function configuration of this pin is decided by the software configuration registers.

Table 5-8. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
74	**DENSEL**	$DO_{4/24}$	VCC	***FDD Density Select.*** DENSEL is high for high data rates (500 Kbps, 1 Mbps). DENSEL is low for low data rates (250 Kbps, 300 Kbps).
73	**DRATE0**	$DO_{4/24}$	VCC	***Data Rate 0.*** DRATE0 reflects the currently selected FDC data rate, or the Data Rate Select Register (DSR).
71	**MTR0#**	$DO_{4/24}$	VCC	***FDD Motor 0 Enable #.*** Active low. MTR0# is controlled by the Digital Output Register (DOR).
66	**MTR1#/ KP17**	$DO_{4/24}$/ $DIOD_{4/24}$	VCC	***FDD Motor 1 Enable #/ KBC I/O Port 17.*** • The first function of this pin is the motor enable line for FDD drive 1. This is an active low signal, and is controlled by the Digital Output Register (DOR). • The second function of this pin is the KBC I/O Port 17. • The function configuration of this pin is decided by the software configuration registers.
70	**DRV1#/ KP16**	$DO_{4/24}$/ $DIOD_{4/24}$	VCC	***FDD Drive 1 Enable #/ KBC I/O Port 16.*** • The first function of this pin is the decoded drive select output for FDD drive 1. This is an active low signal, and is controlled by the Digital Output Register (DOR). • The second function of this pin is the KBC I/O Port 16. • The function configuration of this pin is decided by the software configuration registers.
67	**DRV0#**	$DO_{4/24}$	VCC	***FDD Drive 0 Enable #.*** Active low. DRV0# is controlled by the Digital Output Register (DOR).
63	**WDATA#**	$DO_{4/24}$	VCC	***FDD Write Serial Data to the drive #.*** active low.
65	**DIR#**	$DO_{4/24}$	VCC	***FDD Head Direction #.*** Step in when low and step out when high during a SEEK operation.
64	**STEP#**	$DO_{4/24}$	VCC	***FDD Step Pulse #.*** Active low.
58	**HDSEL#**	$DO_{4/24}$	VCC	***FDD Head Select #.*** Active low.
62	**WGATE#**	$DO_{4/24}$	VCC	***FDD Write Gate Enable #*** Active low.
59	**RDATA#**	DI	VCC	***FDD Read Disk Data #.*** Active low, serial data input from FDD.
61	**TRK0#**	DI	VCC	***FDD Track 0 #.*** Active low. Indicates that the head of the selected drive is on track 0.
72	**INDEX#**	DI	VCC	***FDD Index #.*** Active low. Indicates the beginning of a disk track.
60	**WP#**	DI	VCC	***FDD Write Protect #.*** Active low. Indicates that the disk of the selected drive is write-protected.
57	**DSKCHG#**	DI	VCC	***Floppy Disk Change #.*** Active low. This input pin senses whether the drive door has been opened or a diskette has been changed.

Table 5-10. Pin Description of Smart Card Reader Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
9	**GPIO55/ SCRST**	DIOD8/ DOD8	VSB	***General Purpose I/O 55 / Smart Card Reset.*** • The first function of this pin is the General Purpose I/O 55. • The second function of this pin is Smart Card Reset. • The function configuration of this pin is decided by the software configuration registers.
10	**GPIO56/ SCPWR**	DIOD8/ DOD8	VSB	***General Purpose I/O 56 / Smart Card Power FET Control Output.*** • The first function of this pin is the General Purpose I/O 56. • The second function of this pin is Smart Card Power FET Control Output #. The Smart Card Reader interface requires this pin to drive an external Power FET to supply the current for the Smart Card (65 mA typical, 100 mA short to ground). • The function configuration of this pin is decided by the software configuration registers.
48	**GPIO62/ SCIO**	DIOD8/ DIOD8	VSB	***General Purpose I/O 62 / Smart Card Serial Data I/O.*** • The first function of this pin is the General Purpose I/O 62. • The second function of this pin is Smart Card Serial Data I/O. • The function configuration of this pin is decided by the software configuration registers.
52	**GPIOW46/ SCPSNT#**	DIOD8/ DI	VSB	***General Purpose I/O/Wake-up Event 46 / Smart Card Present Detect #.*** • The first function of this pin is the General Purpose I/O and Wake-up event input 46. • The second function of this pin is Smart Card Present Detect #. This pin provides the Smart Card insertion detection for the Smart Card Reader interface. Upon detecting the insertion of the Smart Card, this pin will trigger the power-on event. • The function configuration of this pin is decided by the software configuration registers.
55	**GPIO51/ SCCLK**	DIOD8/ DOD8	VSB	***General Purpose I/O 51 / Smart Card Clock.*** • The first function of this pin is the General Purpose I/O 51. • The second function of this pin is Smart Card Clock. Three different card clocks are selectable from this pin: high speed (7.1 MHz), low speed (Default: 3.5 MHz) and a programmable card clock. • The function configuration of this pin is decided by the software configuration registers.

Table 5-11. Pin Description of Keyboard Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
126	**KDAT**	DIOD16	VSB	***Keyboard Data.***
125	**KCLK**	DIOD16	VSB	***Keyboard Clock.***
128	**MDAT**	DIOD16	VSB	***PS/2 Mouse Data.***
127	**MCLK**	DIOD16	VSB	***PS/2 Mouse Clock.***
122	**KRST#**	DO8	VCC	***Keyboard Reset #.***
123	**GA20**	DO8	VCC	***Gate Address 20.***

Table 5-12. Pin Description of Real Time Clock Signals

Pin(s) No.	Symbol	Attribute	Power	Description
42	**X32KI**	OSCI	VPP	***Crystal Input.*** Input signal to the RTC crystal oscillator.
44	**X32KO**	OSCO	VPP	***Crystal Output.*** Output signal from the RTC crystal oscillator.

Table 5-13. System Wake-up and ACPI Signals

Pin(s) No.	Symbol	Attribute	Power	Description
36	**PWBTIN#**	DI	VSB	***Main Power Switch Button Input #.*** Active low.
35	**SLBTIN#/ GPIOW42**	DI/ DIOD8	VSB	***Sleep Button Input #/ General Purpose I/O/Wake-up Event 42.*** • The first function of this pin is Sleep Button Input #. • The second function of this pin is the General Purpose I/O and Wake-up event input 42. • The function configuration of this pin is decided by the software configuration registers.
37	**SIOSMI#**	DOD8	VSB	***System Management Interrupt #.*** Active low.
38	**PWUREQ#**	DOD8	VSB	***Power-Up Request Output #.*** Active (low) level indicates that a wake-up event has occurred, and the system should exit its current sleep state.
39	**PSON#**	DOD8	VSB	***Power Supply On/Off Control #.*** Active (low) level indicates that the power should be turned on.
50–51	**LED[1:2]/ GPIOW 4[4:5]**	DOD8/ DIOD8	VSB	***LED Control [1:2]/ General Purpose I/O/Wake-up Event 4[4:5].*** • The first functions of these pins are LED Control [1:2]. • The second functions of these pins are the General Purpose I/O and Wake-up event input 4[4:5]. • The function configuration of this pin is decided by the software configuration registers.
53	**SLP_SX#/ GPIOW47**	DI/ DIOD8	VSB	***Chipset Sleep State Input #/ General Purpose I/O/Wake-up Event 47.*** • The first function of this pin is Chipset Sleep State Input #. • The second function of this pin is the General Purpose I/O and Wake-up event input 47. • The function configuration of this pin is decided by the software configuration registers.
54	**VCCFAIL/ GPIO54**	DO8/ DIOD8	VSB	***VCC Failing / General Purpose I/O 54.*** • The first function of this pin is VCC Failing. • The second function of this pin is the General Purpose I/O 54. • The function configuration of this pin is decided by the software configuration registers.

Table 5-14. Pin Description of Flash ROM I/F and Programmable Chip Select Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1–8	**GPIOW1[0:7]/ XA[11:4]**	DIOD8/ DO8	VSB	***General Purpose I/O/Wake-up Event 1[0:7] / X Addresses [11:4].*** • The first functions of these pins are the General Purpose I/O and Wake-up event input 1[0:7]. • The second functions of these pins are X Addresses [11:4]. • The function configuration of this pin is decided by the software configuration registers.
14	**GPIO20/ XRD#_XEN**	DIOD8/ DO8	VSB	***General Purpose I/O 20 / X Read #/Data Enable.*** • The first function of this pin is the General Purpose I/O 20. • The second function of this pin is X Read Strobe # or X-Data Enable. An active low level of XRD# indicates a read cycle. An active high level of XEN indicates valid data on the XD bus. • The function configuration of this pin is decided by the software configuration registers.
15	**GPIO21/ XWR#_XDIR**	DIOD8/ DO8	VSB	***General Purpose I/O 21 / X Write #/Data Direction.*** • The first function of this pin is General Purpose I/O 21. • The second function of this pin is X Write Strobe # or X-Data Direction. An active low level of XWR# indicates a write cycle. A high level of XDIR indicates a read cycle on the XD bus; a low level of XDIR indicates a write cycle on the XD bus. • The function configuration of this pin is decided by the software configuration registers.
16–19	**GPIO2[2:5]/ XA[3:0]**	DIOD8/ DO8	VSB	***General Purpose I/O 2[2:5] / X Addresses [3:0].*** • The first functions of these pins are General Purpose I/O 2[2:5]. • The second functions of these pins are X Addresses [3:0]. • The function configuration of this pin is decided by the software configuration registers.
20–21	**GPIOW4[0:1]/ CS[2:1]#**	DIOD8/ DO8	VSB	***General Purpose I/O/Wake-up Event 4[0:1] / Programmable Chip Select [2:1] #.*** • The first functions of these pins are General Purpose I/O and Wake-up event input 4[0:1]. • The second functions of these pins are Programmable Chip Select [2:1]#. • The function configuration of this pin is decided by the software configuration registers.
22	**GPIO26/ UDMCS#**	DIOD8/ DO8	VSB	***General Purpose I/O 26 / User-Defined Memory Chip Select #.*** • The first function of this pin is General Purpose I/O 26. • The second function of this pin is User-Defined Memory Chip Select #. • The function configuration of this pin is decided by the software configuration registers.

Pin Description of Flash ROM I/F and Programmable Chip Select Signals [cont'd]

Pin(s) No.	Symbol	Attribute	Power	Description
23	**GPIO27/ FRCS#**	DIOD8/ DO8	VSB	***General Purpose I/O 27 / Flash ROM I/F Chip Select #.*** • The first function of this pin is the General Purpose I/O 27. • The second function of this pin is Flash ROM I/F Chip Select #. • The function configuration of this pin is decided by the software configuration registers.
24–31	**GPIO3[0:7]/ XD[7:0]**	DIOD8/ DIOD8	VSB	***General Purpose I/O 3[0:7] / X Data [7:0].*** • The first functions of these pins are General Purpose I/O 3[0:7]. • The second functions of these pins are X Data [7:0]. • The function configuration of this pin is decided by the software configuration registers.
32–33	**GPIO6[0:1]/ XSTRB[2:1]/ JP[4:5]**	DIOD8/ DO8/ DI	VSB	***General Purpose I/O 6[0:1] / X Address Strobes [2:1] / JP [4:5].*** • The first functions of these pins are General Purpose I/O 6[0:1]. • The second functions of these pins are X Data [2:1]. • The function configuration of this pin is decided by the software configuration registers. *During VSB Power-on and LRESET# activation, these pins are inputs for JP[4:5] power-on strapping option. A weak internal pull-down will be active during the same moment.*
34	**GPIO52/ XSTRB0/ JP6**	DIOD8/ DO8/ DI	VSB	***General Purpose I/O 52 / X Address Strobe 0 / JP6.*** • The first function of this pin is the General Purpose I/O 52. • The second function of this pin is X Address Strobe 0. • The function configuration of this pin is decided by the software configuration registers. *During VSB Power-on and LRESET# activation, these pins are inputs for JP6 power-on strapping option. A weak internal pull-down will be active during the same moment.*

Table 5-15. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
13	**GPIO57/ HFCKOUT**	DIOD8/ DO8	VSB	***General Purpose I/O 57 / High Frequency Clock Output.*** • The first function of this pin is the General Purpose I/O 57. • The second function of this pin is High Frequency Clock Output. • The function configuration of this pin is decided by the software configuration registers.
45	**GPIO53/ LFCKOUT**	DIOD8/ DO8	VSB	***General Purpose I/O 53 / Low Frequency Clock Output.*** • The first function of this pin is the General Purpose I/O 53. • The second function of this pin is Low Frequency Clock Output. • The function configuration of this pin is decided by the software configuration registers.
49	**GPIOW43/ PWBTOUT#**	DIOD8/ DOD8	VSB	***General Purpose I/O/Wake-up Event 43 / Power Button Output.*** • The first function of this pin is the General Purpose I/O and Wake-up event input 43. • The second function of this pin is Power Button Output. • The function configuration of this pin is decided by the software configuration registers.
56	**CK48MI**	DI	VSB	***Clock Input.*** 48 MHz clock Input.

IO Cell:
DO8: Sourcing/Sinking 8mA Digital Output buffer
DOD8: Sinking 8mA Digital Open-Drain Output buffer
DO16: Souring/Sinking 16mA Digital Output buffer
$DO_{4/24}$: Sourcing 4mA/Sinking 24mA Digital Output buffer
$DO_{16/24}$: Sourcing 16mA/Sinking 24mA Digital Output buffer

DIO8: Sourcing/Sinking 8mA Digital input/output buffer
DIOD8: Sinking 8mA Digital Open-Drain input/output buffer
DIO16: Sourcing/Sinking 16mA Digital input/output buffer
DIOD16: Sinking16mA Digital Open-Drain input/output buffer
$DIO_{4/24}$: Sourcing 4mA/Sinking 24mA Digital input/output buffer
$DIO_{16/24}$: Sourcing 16mA/Sinking 24mA Digital input/output buffer
OSCO: Crystal Oscillator output buffer

DI: Digital Input
OSCI: Crystal Oscillator input buffer

6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1 (Set 1)

Signal	Pin #	Attribute	Description
GPIOW10/XA11	1	DIOD8/DO8	General Purpose I/O/Wake-up Event 10 / X Address 11.
GPIOW11/XA10	2	DIOD8/DO8	General Purpose I/O/Wake-up Event 11 / X Address 10.
GPIOW12/XA9	3	DIOD8/DO8	General Purpose I/O/Wake-up Event 12 / X Address 9.
GPIOW13/XA8	4	DIOD8/DO8	General Purpose I/O/Wake-up Event 13 / X Address 8.
GPIOW14/XA7	5	DIOD8/DO8	General Purpose I/O/Wake-up Event 14 / X Address 7.
GPIOW15/XA6	6	DIOD8/DO8	General Purpose I/O/Wake-up Event 15 / X Address 6.
GPIOW16/XA5	7	DIOD8/DO8	General Purpose I/O/Wake-up Event 16 / X Address 5.
GPIOW17/XA4	8	DIOD8/DO8	General Purpose I/O/Wake-up Event 17 / X Address 4.

Table 6-2. General Purpose I/O Group 2 (Set 2)

Signal	Pin #	Attribute	Description
GPIO20/XRD#_XEN	14	DIOD8/DO8	General Purpose I/O 20 / X Read #/Data Enable.
GPIO21/XWR#_XDIR	15	DIOD8/DO8	General Purpose I/O 21 / X Write #/Data Direction.
GPIO22/XA3	16	DIOD8/DO8	General Purpose I/O 22 / X Address 3.
GPIO23/XA2	17	DIOD8/DO8	General Purpose I/O 23 / X Address 2.
GPIO24/XA1	18	DIOD8/DO8	General Purpose I/O 24 / X Address 1.
GPIO25/XA0	19	DIOD8/DO8	General Purpose I/O 25 / X Address 0.
GPIO26/UDMCS#	22	DIOD8/DO8	General Purpose I/O 26 / User-Defined Memory Chip Select #.
GPIO27/FRCS#	23	DIOD8/DO8	General Purpose I/O 27 / Flash ROM I/F Chip Select #.

Table 6-3. General Purpose I/O Group 3 (Set 3)

Signal	Pin #	Attribute	Description
GPIO30/XD7	24	DIOD8/DIOD8	General Purpose I/O 30 / X Data 7.
GPIO31/XD6	25	DIOD8/DIOD8	General Purpose I/O 31 / X Data 6.
GPIO32/XD5	26	DIOD8/DIOD8	General Purpose I/O 32 / X Data 5.
GPIO33/XD4	27	DIOD8/DIOD8	General Purpose I/O 33 / X Data 4.
GPIO34/XD3	28	DIOD8/DIOD8	General Purpose I/O 34 / X Data 3.
GPIO35/XD2	29	DIOD8/DIOD8	General Purpose I/O 35 / X Data 2.
GPIO36/XD1	30	DIOD8/DIOD8	General Purpose I/O 36 / X Data 1.
GPIO37/XD0	31	DIOD8/DIOD8	General Purpose I/O 37 / X Data 0.

Table 6-4. General Purpose I/O Group 4 (Set 4)

Signal	Pin #	Attribute	Description
GPIOW40/CS2#	20	DIOD8/DO8	General Purpose I/O/Wake-up Event 40 / Programmable Chip Select 2 #.
GPIOW41/CS1#	21	DIOD8/DO8	General Purpose I/O/Wake-up Event 41 / Programmable Chip Select 1 #.
GPIOW42/SLBTIN#	35	DIOD8/DI	General Purpose I/O/Wake-up Event 42 / Sleep Button Input #.
GPIOW43/ PWBTOUT#	49	DIOD8/DOD8	General Purpose I/O/Wake-up Event 43 / Power Button Output #.
GPIOW44/LED1	50	DIOD8/DOD8	General Purpose I/O/Wake-up Event 44 / LED Control 1.
GPIOW45/LED2	51	DIOD8/DOD8	General Purpose I/O/Wake-up Event 45 / LED Control 2.
GPIOW46/ SCPSNT#	52	DIOD8/DI	General Purpose I/O/Wake-up Event 46/ Smart Card Present Detect #..
GPIOW47/SLP_SX#	53	DIOD8/DI	General Purpose I/O/Wake-up Event 47 / Chipset Sleep State Input #.

Table 6-5. General Purpose I/O Group 5 (Set 5)

Signal	Pin #	Attribute	Description
GPIO50/CLKRUN#	124	DIOD8/DIOD8	General Purpose I/O 50 / Clock Run #.
GPIO51/SCCLK	55	DIOD8/DOD8	General Purpose I/O 51 / Smart Card Clock.
GPIO52/XSTRB0/ JP6	34	DIOD8/DO8	General Purpose I/O 52 / X Address Strobe 0 / JP6.
GPIO53/LFCKOUT	45	DIOD8/DO8	General Purpose I/O 53 / Low Frequency Clock Output.
GPIO54/VCCFAIL	54	DIOD8/DO8	General Purpose I/O 54 / VCC Failing.
GPIO55/SCRST	9	DIOD8/DOD8	General Purpose I/O 55 / Smart Card Reset.
GPIO56/SCPWR	10	DIOD8/DOD8	General Purpose I/O 56 / Smart Card Power FET Control Output #.
GPIO57/HFCKOUT	13	DIOD8/DO8	General Purpose I/O 57 / High Frequency Clock Output.

Table 6-6. General Purpose I/O Group 6 (Set 6)

Signal	Pin #	Attribute	Description
GPIO60/XSRTB2/ JP4	32	DIOD8/DO8	General Purpose I/O 60 / X Address Strobe 2 / JP4.
GPIO61/XSRTB1/ JP5	33	DIOD8/DO8	General Purpose I/O 61 / X Address Strobe 1 / JP5.
GPIO62/SCIO	48	DIOD8/DIOD8	General Purpose I/O 62 / Smart Card Serial Data I/O.

7. Power On Strapping Options

Signal	Pin #	Description
JP1	97	**KBC_RTC_EN (KBC and RTC Enable)** Sampled at LRESET# to determine the default values of **KBC_EN** and **RTC_EN** (bit0 of activation register, Index 30h, of Logical Device 5 and 8). During LRESET#, a week pull-up resistor will be turned on. 0: Default values of **KBC_EN** and **RTC_EN** are 0. 1: Default values of **KBC_EN** and **RTC_EN** are 1.
JP2	98	**Reserved.** During LRESET#, **DO NOT** be pulled to 0.
JP3	100	**CONF_SEL** (Configuration Register Base Address Select). Sampled at LRESET# to determine the base address of the configuration Index/Data register pair. During LRESET#, a week pull-up resistor will be turned on. 0: 4Eh/4Fh. 1: 2Eh/2Fh.
JP4	32	**Flash_ROM_EN (Flash ROM I/F Enable)** Sampled at VSB power-on or LRESET# to determine the default values of **FLASH_SEG1**, **FLASH_SEG2** and **GPIO2_3_SEL**. During LRESET#, a week pull-down resistor will be turned on. 0: Default values of **FLASH_SEG1** and **FLASH_SEG2** are 1. **GPIO2_3_SEL** is 0. 1: Default values of **FLASH_SEG1** and **FLASH_SEG2** are 0. **GPIO2_3_SEL** is 1.
JP5	33	**ADD_MOD_SEL (X Address 11-4 Mode Select)** Sampled at VSB power-on or LRESET# to determine the default values of **GPIO1_SEL** and **PIN34_SEL**. During LRESET#, a week pull-down resistor will be turned on. 0: Default value of **GPIO1_SEL** is 1; Default value of **PIN34_SEL** is 0. 1: Default value of **GPIO1_SEL** is 0; Default value of **PIN34_SEL** is 1.
JP6	34	**SB_ADD_SEL (Serial Bus Address Select)** Sampled at VSB power-on or LRESET# to determine the Serial Bus Address. During LRESET#, a week pull-down resistor will be turned on. 0: Serial Bus Address is 0100111b. 1: Serial Bus Address is 1010111b.

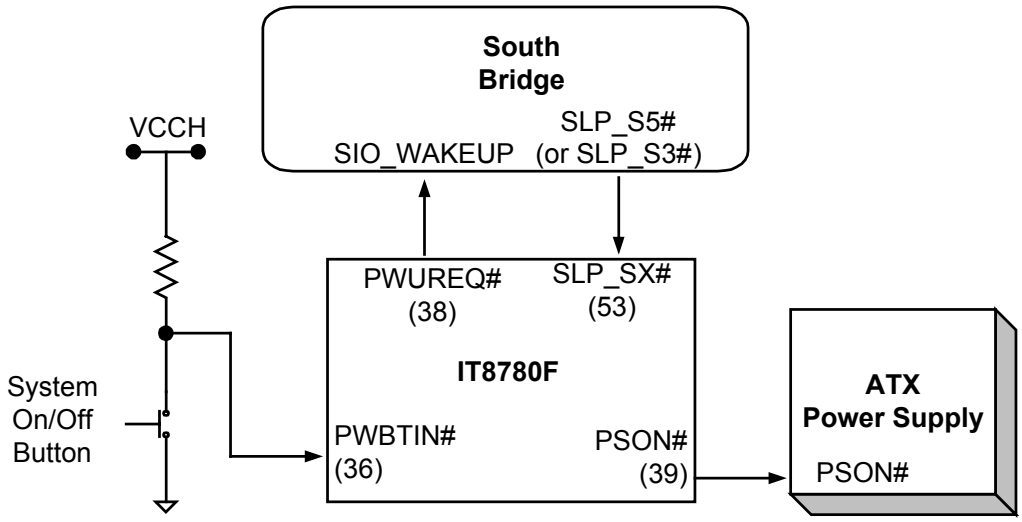


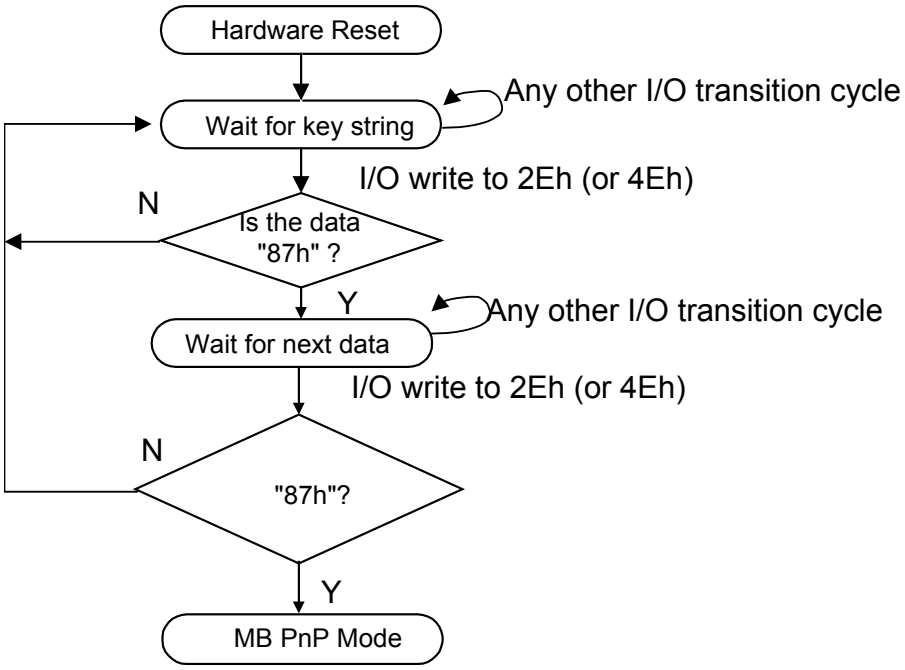
Figure 7-1. IT8780F Power Control Suggestion Applications Circuitry

8. Configuration

8.1 Configuring Sequence Description

Following the hardware reset or power-on reset, the IT8780F enters the normal mode with all logical devices disabled except KBC and RTC. The initial states (enable bits) of the logical devices (KBC and RTC) are determined by the state of pin 97 (JP1) at the raising edge of LRESET# during power-on reset.

There are three steps to completing the Motherboard mode of configuration. Step 1 is to enter the MB PnP mode. Step 2 is to modify the data of configuration registers. Step 3 is to exit the MB PnP mode. These three steps are explained below. Please note that step three must be followed or an undefined state will occur.



(1) Enter the MB PnP Mode

To enter the MB PnP Mode, 2 specific I/O write operations (87h) must be performed during the “Wait for key” state. The addresses of the configuration Index/Data register pair are determined by the power-on strapping of pin 100 (JP3). 2Eh/2Fh is selected when the power-on strapping value of this pin is low (without pull-up resistor); 4Eh/4Fh is selected when the power-on strapping value of this pin is high (with 10-Kohm pull-up resistor).

(2) Modifying the Data of the Registers

All configuration registers can be accessed after the MB PnP Mode is accessed. Before a selected register is accessed, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exiting the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to "1" to exit the MB PnP Mode.

8.2 Description of the Configuration Registers

All the registers except APC/PME registers will be reset to the default state when RESET is activated.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
All	02h	WO	NA	Configure Control
All	07h	R/W	NA	Logical Device Number (LDN)
All	20h	RO	87h	Chip ID Byte 1
All	21h	RO	80h	Chip ID Byte 2
All	22h	RO	00h	Chip Version
All	23h	R/W	ss0000s0b	Clock Selection and Flash ROM I/F control Register
All	24h	R/W	s1000000b	Function Fast Disable Register
All	25h	R/W	03h	GPIO Set 4 Multi-Function Pin Selection Register
All	26h	R/W	01100s00b	GPIO Set 5 Multi-Function Pin Selection Register
All	27h	R/W	s00000ssb	GPIO Set 6 and Misc. Multi-Function Pin Selection Register
F4h Note	2Ah	R/W	12h	Reserved Register
F4h Note	2Bh	RO	--	Reserved Register
F4h Note	2Ch	RO	--	Reserved Register
F4h Note	2Eh	R/W	00h	Test 1 Register
F4h Note	2Fh	R/W	00h	Test 2 Register

Note: All these registers can be read from all LDNs.

Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	00h	Serial Port 2 Special Configuration Register 2
02h	F2h	R/W	7Fh	Serial Port 2 Special Configuration Register 3

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	64h	R/W	00h	POST Data Port Base Address MSB Register
03h	65h	R/W	80h	POST Data Port Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select [Note1]
03h	F0h	R/W	03h [Note2]	Parallel Port Special Configuration Register

Note 1: When the ECP mode is not enabled, this register is **read only** as "04h", and cannot be written.
Note 2: When bit 2 of the Primary Base Address LSB Register of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

Table 8-7. SWC and ACPI Configuration Registers

LDN	Index	R/W	Power-Well	Default	Configuration Register or Action
04h	30h	R/W	VSB	00h	SWC Activate
04h	60h	R/W	VSB	00h	PM1b_EVT_BLK Base Address MSB Register
04h	61h	R/W	VSB	00h	PM1b_EVT_BLK Base Address LSB Register
04h	62h	R/W	VSB	00h	PM1b_CNT_BLK Base Address MSB Register
04h	63h	R/W	VSB	00h	PM1b_CNT_BLK Base Address LSB Register
04h	64h	R/W	VSB	00h	GPE1_BLK Base Address MSB Register
04h	65h	R/W	VSB	00h	GPE1_BLK Base Address LSB Register
04h	70h	R/W	VSB	00h	SWC Interrupt Level Select Register
04h	E0h	R/W	VSB	00h	GPE1_STS_0 to IRQ Enable Register
04h	E1h	R/W	VSB	00h	GPE1_STS_1 to IRQ Enable Register
04h	E2h	R/W	VSB	00h	GPE1_STS_2 to IRQ Enable Register
04h	E3h	R/W	VSB	00h	GPE1_STS_3 to IRQ Enable Register
04h	E4h	R/W	VSB	00h	GPE1_STS_0 to SMI# Enable Register
04h	E5h	R/W	VSB	00h	GPE1_STS_1 to SMI# Enable Register
04h	E6h	R/W	VSB	00h	GPE1_STS_2 to SMI# Enable Register
04h	E7h	R/W	VSB	00h	GPE1_STS_3 to SMI# Enable Register
04h	E8h	RO	VSB	--	Power ON Status Register
04h	F0h	R/W	VPP Note	00h	SWC Miscellaneous Control Register
04h	F1h	R/W	VPP Note	00h	Power ON Control Register
04h	F2h	R/W	VPP Note	00h	Keyboard Wake-up Control Register
04h	F3h	R/W	VPP Note	00h	GPE1_STS_0 to PSON# Enable Register
04h	F4h	R/W	VPP Note	00h	GPE1_STS_1 to PSON# Enable Register
04h	F5h	R/W	VPP Note	00h	GPE1_STS_2 to PSON# Enable Register
04h	F6h	R/W	VPP Note	00h	GPE1_STS_3 to PSON# Enable Register
04h	F7h	R/W	VPP Note	00h	LED Control Register
04h	F8h	R/W	VPP Note	--	Keyboard Code Data 0 Register
04h	F9h	R/W	VPP Note	--	Keyboard Code Data 1 Register
04h	FAh	R/W	VPP Note	--	Keyboard Code Data 2 Register
04h	FBh	R/W	VPP Note	--	Keyboard Code Data 3 Register
04h	FCh	R/W	VPP Note	--	Keyboard Code Data 4 Register

Table 8-8. SWC and ACPI Configuration Registers [cont'd]

LDN	Index	R/W	Power-Well	Default	Configuration Register or Action
04h	FDh	R/W	VPP Note	--	Keyboard Code Data 5 Register
04h	FEh	R/W	VPP Note	--	Keyboard Code Data 6 Register
04h	FFh	R/W	VPP Note	--	Keyboard Code Data 7 Register

Note: VPP will be supported by VSB when VSB is present, and is supported by VBAT when VSB is not present. Its power well is the same as the RTC.

Table 8-9. Keyboard Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
05h	30h	R/W	00h or 01h	Keyboard Activate
05h	60h	R/W	00h	KBC Data Base Address MSB Register
05h	61h	R/W	60h	KBC Data Base Address LSB Register
05h	62h	R/W	00h	KBC Command Base Address MSB Register
05h	63h	R/W	64h	KBC Command Base Address LSB Register
05h	70h	R/W	01h	Keyboard Interrupt Level Select
05h	71h	RO-R/W	02h	Keyboard Interrupt Type Note
05h	F0h	R/W	00h	KBC Special Configuration Register

Note: The register is **read only** unless the write enable bit (Index=F0h) is asserted.

Table 8-10. Mouse Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
06h	30h	R/W	00h	Mouse Activate
06h	70h	R/W	0Ch	Mouse Interrupt Level Select
06h	71h	RO-R/W	02h	Mouse Interrupt Type Note
06h	F0h	R/W	00h	Mouse Special Configuration Register

Note: The register is **read only** unless the write enable bit (Index=F0h) is asserted.

Table 8-12. GPIO Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
07h	60h	R/W	00h	Programmable Chip Select 1 Base Address MSB Register
07h	61h	R/W	00h	Programmable Chip Select 1 Base Address LSB Register
07h	62h	R/W	00h	Programmable Chip Select 2 Base Address MSB Register
07h	63h	R/W	00h	Programmable Chip Select 2 Base Address LSB Register
07h	B0h	R/W	00h	GPIOW Set 1 Pin Polarity Register
07h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
07h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
07h	B3h	R/W	00h	GPIOW Set 4 Pin Polarity Register
07h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
07h	B5h	R/W	00h	GPIO Set 6 Pin Polarity Register
07h	B8h	R/W	00h	GPIOW Set 1 Pin Internal Pull-up Enable Register
07h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
07h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
07h	BBh	R/W	00h	GPIOW Set 4 Pin Internal Pull-up Enable Register
07h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
07h	BDh	R/W	00h	GPIO Set 6 Pin Internal Pull-up Enable Register
07h	C0h	R/W	00h	Simple I/O Set 1 Data Register
07h	C1h	R/W	00h	Simple I/O Set 2 Data Register
07h	C2h	R/W	00h	Simple I/O Set 3 Data Register
07h	C3h	R/W	00h	Simple I/O Set 4 Data Register
07h	C4h	R/W	00h	Simple I/O Set 5 Data Register
07h	C5h	R/W	00h	Simple I/O Set 6 Data Register
07h	C8h	R/W	00h	Simple I/O Set 1 Input/Output Selection Register
07h	C9h	R/W	00h	Simple I/O Set 2 Input/Output Selection Register
07h	CAh	R/W	00h	Simple I/O Set 3 Input/Output Selection Register
07h	CBh	R/W	00h	Simple I/O Set 4 Input/Output Selection Register
07h	CCh	R/W	00h	Simple I/O Set 5 Input/Output Selection Register
07h	CDh	R/W	00h	Simple I/O Set 6 Input/Output Selection Register
07h	E3h	R/W	00h	IRQ3 External Routing Input Pin Mapping Register
07h	E4h	R/W	00h	IRQ4 External Routing Input Pin Mapping Register
07h	E5h	R/W	00h	IRQ5 External Routing Input Pin Mapping Register
07h	E6h	R/W	00h	IRQ6 External Routing Input Pin Mapping Register

GPIO Configuration Registers [cont'd]

LDN	Index	R/W	Default	Configuration Register or Action
07h	E7h	R/W	00h	IRQ7 External Routing Input Pin Mapping Register
07h	E9h	R/W	00h	IRQ9 External Routing Input Pin Mapping Register
07h	EAh	R/W	00h	IRQ10 External Routing Input Pin Mapping Register
07h	EBh	R/W	00h	IRQ11 External Routing Input Pin Mapping Register
07h	ECh	R/W	00h	IRQ12 External Routing Input Pin Mapping Register
07h	EEh	R/W	00h	IRQ14 External Routing Input Pin Mapping Register
07h	EFh	R/W	00h	IRQ15 External Routing Input Pin Mapping Register
07h	F0h	R/W	00h	Programmable Chip Select Configuration Register
07h	F1h	R/W	00h	User-defined Memory Base Address High Byte Register
07h	F2h	R/W	00h	User-defined Memory Base Address Low Byte Register
07h	F3h	R/W	00h	User-defined Memory Size High Byte Register
07h	F4h	R/W	00h	User-defined Memory Size Low Byte Register

Table 8-13. RTC Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
08h	30h	R/W	00h or 01h	RTC Activate
08h	60h	R/W	00h	RTC Primary Base Address MSB Register
08h	61h	R/W	70h	RTC Primary Base Address LSB Register
08h	62h	R/W	00h	RTC Secondary Base Address MSB Register
08h	63h	R/W	72h	RTC Secondary Base Address LSB Register
08h	70h	R/W	08h	RTC Interrupt Level Select
08h	71h	RO-R/W	02h	Keyboard Interrupt Type [Note]
08h	F0h	R/W	00h	RTC Special Configuration Register

Note: The register is **read only** unless the write enable bit (Index=F0h) is asserted.

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	**Reserved**
1	Returns to the "Wait for Key" state. This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices. This register is **read/write**.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This register is the Chip ID Byte 1 and is **read only**. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=80h)

This register is the Chip ID Byte 2 and is **read only**. Bits [7:0]=80h when read.

8.3.5 Chip Version (Index=22h, Default=00h)

This register is the Chip Version and is **read only**.

8.3.6 Clock Selection and Flash ROM I/F Control Register (Index=23h, Default=ss0000s0b, VSB)

Bit	Description
7	**FLASH_SEG1 (Flash ROM Interface Address Segment 1 Enable)** This bit enables the Flash ROM Interface Address Segment 1 (FFFE_0000h-FFFF_FFFFh). The initial value of this bit depends on the VSB power-on strapping of pin 32 (JP4) (The initial value will be 1 if the strapping value of pin 32 is low). 0: Disabled. 1: Enable the Flash ROM Interface Address Segment 1 (FFFE_0000h-FFFF_FFFFh).
6	**FLASH_SEG2 (Flash ROM Interface Address Segment 2 Enable)** This bit enables the Flash ROM Interface Address Segment 2 (000F_0000h-000F_FFFFh). The initial value of this bit depends on the VSB power-on strapping of pin 32 (JP4) (The initial value will be 1 if the strapping value of pin 32 is low). 0: Disabled. 1: Enable the Flash ROM Interface Address Segment 2 (000F_0000h-000F_FFFFh).
5	**FLASH_SEG3 (Flash ROM Interface Address Segment 3 Enable** This bit enables the Flash ROM Interface Address Segment 3 (000E_0000h-000E_FFFFh). 0: Disabled (default). 1: Enable the Flash ROM Interface Address Segment 3 (000E_0000h-000E_FFFFh).
4	**FLASH_SEG4 (Flash ROM Interface Address Segment 4 Enable)** This bit enables the Flash ROM Interface Address Segment 4 (FFC0_0000h-FFF7_FFFFh). 0: Disabled (default). 1: Enable the Flash ROM Interface Address Segment 4 (FFC0_0000h-FFF7_FFFFh).
3	**FLASH_SEG5 (Flash ROM Interface Address Segment 5 Enable)** This bit enables the Flash ROM Interface Address Segment 5 (FFF8_0000h-FFFD_FFFFh). 0: Disabled (default). 1: Enable the Flash ROM Interface Address Segment 5 (FFF8_0000h-FFFD_FFFFh).
2	**FLASH_WE (Flash ROM Interface Write Enable)** This bit enables the Flash ROM Interface WRITE operation. 0: Disabled (default). 1: Enable the Flash ROM I/F WRITE operation.
1	**GPIO1_SEL (GPIO Set 1 Multi-function Pin Selection)** This bit selects the function of pin 1 ~ pin 8. The initial value of this bit depends on the VSB power-on strapping of pin 33 (JP5). 0: XA11~XA4. 1: GPIOW10~GPIOW17.
0	**CLKIN_FREQ (CLKIN Frequency)** This bit determines the frequency of CLKIN pin. 0: 48 MHz (default). 1: 24 MHz.

8.3.7 Function Fast Disable Register (Index=24h, Default=s1000000b, VSB)

Bit	Description
7	**GPIO2_3_SEL (GPIO Set 2 and 3 Multi-function Pin Selection)** This bit selects the function of pins 14 ~ 19 and pins 23 ~ 31. The initial value of this bit depends on the VSB power-on strapping of pin 32. **Pin 14, Pin 15, Pins 16 ~ 19, Pin 23, Pins 24 ~31** 0: XRD#, XWR#, XA3 ~ XA0, FRCS#, XD7 ~ XD0 1: GPIO20, GPIO21, GPIO22~GPIO25, GPIO27, GPIO30~GPIO37
6	**PIN22_SEL (Pin 22 Multi-function Selection).** This bit selects the function of pin 22. 0: UDMCS#. 1: GPIO26 (default).
5	**Reserved**
4	**KBMSDIS (Keyboard and Mouse Controller Disable)** When set, this bit will force the Keyboard and Mouse Controller function of IT8780F to be disabled regardless of the settings of their Activation bits (bit 0 of LDN5 and LDN6 index 30h). 0: Keyboard and Mouse Enable or Disable, according to Keyboard and Mouse Activation bits (default). 1: Keyboard and Mouse Disable.
3	**PPDIS (Parallel Port Disable)** When set, this bit will force the Parallel Port function of IT8780F to be disabled regardless of the setting of its Activation bit (bit 0 of LDN3 index 30h). 0: Parallel Port Enable or Disable, according to Parallel Port Activation bit (default). 1: Parallel Port Disable.
2	**S2DIS (Serial Port 2 Disable)** When set, this bit will force the Serial Port 2 function of IT8780F to be disabled regardless of the setting of its Activation bit (bit 0 of LDN2 index 30h). 0: Serial Port 2 Enable or Disable, according to S2 Activation bit (default). 1: Serial Port 2 Disable.
1	**S1DIS (Serial Port 1 Disable)** When set, this bit will force the Serial Port 1 function of IT8780F to be disabled regardless of the setting of its Activation bit (bit 0 of LDN1 index 30h). 0: Serial Port 1 Enable or Disable, according to S1 Activation bit (default). 1: Serial Port 1 Disable.
0	**FDCDIS (Floppy Disk Controller Disable)** When set, this bit will force the Floppy Disk Controller function of IT8780F to be disabled regardless of the setting of its Activation bit (bit 0 of LDN0 index 30h). 0: FDC Enable or Disable, according to FDC Activation bit (default). 1: FDC Disable.

8.3.8 GPIO Set 4 Multi-Function Pin Selection Register (Index=25h, Default=03h, VSB)

Bit	Description
7	**PIN53_SEL (Pin 53 Multi-function Selection)** This bit selects the function of pin 53. 0: SLP_SX# (default). 1: GPIOW47.
6	**PIN52_SEL (Pin 52 Multi-function Selection)** This bit selects the function of pin 49. 0: SCPSNT# (default). **1: GPIOW46.**
5	**PIN51_SEL (Pin 51 Multi-function Selection)** This bit selects the function of pin 51. 0: LED2 (default). 1: GPIOW45.
4	**PIN50_SEL (Pin 50 Multi-function Selection)** This bit selects the function of pin 50. 0: LED1 (default) 1: GPIOW44
3	**PIN49_SEL (Pin 49 Multi-function Selection)** This bit selects the function of pin 49. 0: PWBTOUT (default). 1: GPIOW43.
2	**PIN35_SEL (Pin 35 Multi-function Selection)** This bit selects the function of pin 35. 0: SLBTIN# (default). 1: GPIOW42.
1	**PIN21_SEL (Pin 21 Multi-function Selection)** This bit selects the function of pin 21. 0: CS1#. 1: GPIOW41 (default).
0	**PIN20_SEL (Pin 20 Multi-function Selection)** This bit selects the function of pin 20. 0: CS2#. 1: GPIOW40 (default).

8.3.9 GPIO Set 5 Multi-Function Pin Selection Register (Index=26h, Default= 01100s00b, VSB)

Bit	Description
7	**PIN13_SEL (Pin 13 Multi-function Selection)** This bit selects the function of pin 13. 0: HFCKOUT (default). 1: GPIO57.
6	**PIN10_SEL (Pin 10 Multi-function Selection)** This bit selects the function of pin 10. 0: SCPWR. 1: GPIO56 (default).
5	**PIN9_SEL (Pin 9 Multi-function Selection)** This bit selects the function of pin 9. 0: SCRST. 1: GPIO55 (default).
4	**PIN54_SEL (Pin 54 Multi-function Selection)** This bit selects the function of pin 54. 0: VCCFAIL (default). 1: GPIO54.
3	**PIN45_SEL (Pin 45 Multi-function Selection)** This bit selects the function of pin 45. 0: LFCKOUT (default). 1: GPIO53.
2	**PIN34_SEL (Pin 34 Multi-function Selection)** This bit selects the function of pin 34. The initial value of this bit depends on the VSB power-on strapping of pin 33. 0: XSTRB0. 1: GPIO52.
1	**PIN55_SEL (Pin 55 Multi-function Selection)** This bit selects the function of pin 55. 0: SCCLK. (default). 1: GPIO51.
0	**PIN124_SEL (Pin 124 Multi-function Selection)** This bit selects the function of pin 124. 0: CLKRUN# (default). 1: GPIO50.

8.3.10 GPIO Set 6 and Misc. Multi-Function Pin Selection Register (Index=27h, Default= s00000ssb, VSB)

Bit	Description
7	**SB_ADD (Serial Bus Address)** This bit selects the Serial Bus Address. The initial value of this bit depends on the VSB power-on strapping of pin 34. 0: Serial Bus Address is 0100111b. 1: Serial Bus Address is 1010111b.
6	**Reserved**
5	**PIN121_SEL (Pin 121 Multi-function Selection)** This bit selects the function of pin 121. 0: PPDIS (default). 1: KP12.
4	**PIN70_SEL (Pin 70 Multi-function Selection)** This bit selects the function of pin 70. 0: DRV1# (default). 1: KP16.
3	**PIN66_SEL (Pin 66 Multi-function Selection)** This bit selects the function of pin 66. 0: MTR1# (default). 1: KP17.
2	**PIN48_SEL (Pin 48 Multi-function Selection)** This bit selects the function of pin 48. 0: SCIO (default). 1: GPIO62.
1	**PIN33_SEL (Pin 33 Multi-function Selection)** This bit selects the function of pin 33. The initial value of this bit depends on the VSB power-on strapping of pin 32. 0: XSTRB1. 1: GPIO61.
0	**PIN32_SEL (Pin 32 Multi-function Selection)** This bit selects the function of pin 32. The initial value of this bit depends on the VSB power-on strapping of pin 32. 0: XSTRB2. 1: GPIO60.

8.3.11 Reserved Registers (Index=2Ah, 2Bh and 2Ch, Default=00h, --, --)

This is a protection register for ITE test use.

8.3.12 Test 1 Register (Index=2Eh, Default=00h)

This register is the Test 1 Register and reserved for ITE. It should not be set.

8.3.13 Test 2 Register (Index=2Fh, Default=00h)

This register is the Test 2 Register and reserved for ITE. It should not be set.

8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**FDC_EN (FDC Activation)** When FDCDIS (bit 0 of the Function Fast Disable Register) is cleared and this bit is set, the FDC function is enabled. 0: Disabled (default). 1: FDC enabled, if FDCDIS=0.

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only**, with "0h" for Base Addresses [15:12].
3-0	Mapped as Base Addresses [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	**Read/write**, mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-3	Reserved with default "0h."
4	**WK_EN (Wake-Up Enable)** 0: Disabled (default). 1: Enable to set MOD_IRQ_STS of GPE1_STS_3 by an activation of FDC IRQ.
3-0	Select the interrupt level [Note1] for FDC.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	Reserved with default "00h."
2-0	Select the DMA channel [Note2] for FDC.

8.4.6 FDC Special Configuration Register 1 (Index=F0h, D7efault=00h)

Bit	Description
7-6	Reserved with default “00b”.
5	**DRVB_MOD (Floppy Drive B Operation Mode).** 0: Drive B is PC-AT mode (default). 1: Drive B is 3-Mode.
4	**DRVA_MOD (Floppy Drive A Operation Mode).** 0: Drive A is PC-AT mode (default). 1: Drive A is 3-Mode.
3	**FDC_IRQ_SHR (FDC Interrupt Request Sharing).** 0: Normal (default). 1: Enable FDC IRQ sharing.
2	**DRV_SWAP (Swap Floppy Drives).** 0: Normal (default). 1: Swap Floppy Drives A, B.
1	**Reserved**
0	**SOFT_WP (Software Write Protect).** 0: Normal (default). 1: Software Write Protect.

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-6	**FDD B Drive Type Select (DT1-0).**
5-4	**FDD A Drive Type Select (DT1-0).**
3-2	**FDD B Data Rate Table Select (DRT1-0).**
1-0	**FDD A Data Rate Table Select (DRT1-0).**

8.5 Serial Port 1 Configuration Registers (LDN=01h)

8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**S1_EN (Serial Port 1 Activation)** When S1DIS (bit 1 of the Function Fast Disable Register) is cleared and this bit is set, the Serial Port 1 function is enabled. 0: Disabled (default). 1: Serial Port 1 enabled, if S1DIS=0.

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as “0h” for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-5	Reserved with default "0h."
4	**WK_EN (Wake-Up Enable)** 0: Disable (default). 1: Enable to set MOD_IRQ_STS of GPE1_STS_3 by an activation of Serial Port 1 IRQ.
3-0	Select the interrupt level [Note1] for Serial Port 1.

8.5.5 Serial Port 1 Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	**Reserved**
1	**S1_CLK (Serial Port 1 Clock Source)** 0: 24MHz/13 (default). 1: 24MHz.
0	**S1_IRQ_SHR (Serial Port 1 Interrupt Request Sharing)** 0: Normal (default). 1: Enable S1 IRQ sharing.

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**S2_EN (Serial Port 2 Activation)** When S2DIS (bit 2 of the Function Fast Disable Register) is cleared and this bit is set, the Serial Port 2 function is enabled. 0: Disabled (default). 1: Serial Port 2 enabled, if S2DIS=0.

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-5	Reserved with default "0h."
4	**WK_EN (Wake-Up Enable)** 0: Disabled (default). 1: Enable to set MOD_IRQ_STS of GPE1_STS_3 by an activation of Serial Port 2 IRQ.
3-0	Select the interrupt level [Note1] for Serial Port 2.

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-6	**S2_MOD (Serial Port 2 Mode)** 00: Standard (default) 01: Smart Card Reader (SCR) else: Reserved
5-2	Reserved with default "0.h"
1	**S2_CLK (Serial Port 2 Clock Source)** 0: 24MHz/13 (default). 1: 24MHz.
0	**S2_IRQ_SHR (Serial Port 2 Interrupt Request Sharing)** 0: Normal (default). 1: Enable S2 IRQ sharing.

8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=00h)

This register is valid only when Serial Port 2's Mode is Smart Card Reader.

Bit	Description
7-3	**Reserved**
2	**SCPWR_POR (SCPWR Polarity)** 0: Active low (default). 1: Active high.
1-0	**SCCLK_SEL1-0 (SCCLK Frequency Selection)** 00: Stop (default) 01: 3.5 MHz 10: 7.1 MHz 11: Special Frequency (96 MHz/SCDIV)

8.6.7 Serial Port 2 Special Configuration Register 3 (Index=F2h, Default=7Fh)

This register is valid only when Serial Port 2's Mode is Smart Card Reader.

Bit	Description
7	**Reserved**
6-0	**SCDIV6-0** (SCCLK Special Divisor).

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**PP_EN (Parallel Port Activation)** When PPDIS (bit 3 of the Function Fast Disable Register) is cleared and this bit is set, the Parallel Port function is enabled. 0: Disabled (default). 1: Parallel Port enabled, if PPDIS=0.

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If the bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	**Read/write**, mapped as Base Addresses [7:2].
1-0	**Read only** as "00b."

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	**Read/write**, mapped as Base Addresses [7:2].
1-0	**Read only** as "00b."

8.7.6 POST Data Port Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.7.7 POST Data Port Base Address LSB Register (Index=65h, Default=80h)

Bit	Description
7-2	**Read/write**, mapped as Base Addresses [7:2].
1-0	**Read only** as "00b."

8.7.8 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-5	Reserved with default "0h."
4	**WK_EN (Wake-Up Enable)** 0: Disabled (default). 1: Enable to set MOD_IRQ_STS of GPE1_STS_3 by an activation of Parallel Port IRQ.
3-0	Select the interrupt level [Note1] for Parallel Port.

8.7.9 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	Reserved with default "00h."
2-0	Select the DMA channel [Note2] for Parallel Port.

8.7.10 Parallel Port Special Configuration Register (Index=F0h, Default=03h)

Bit	Description
7-4	**Reserved**
3	**POSTDIS (Post Data Port Disable)** When this bit is set, the Post Data Port is disabled. It is better to disable the Post Data Port after the system is boot up. 0: POST Data Port Enable (default). 1: POST Data Port Disable.
2	**PP_IRQ_SHR (Parallel Port Interrupt Request Sharing)** 0: Normal (default). 1: Enable Parallel Port IRQ sharing.
1-0	**Parallel Port Modes** 00: Standard Parallel Port mode (SPP) 01: EPP mode 10: ECP mode 11: EPP mode & ECP mode (default)

If bit 1 is set, ECP mode is enabled. If bit 0 is set, EPP mode is enabled. These two bits are independent. However, according to the EPP spec., when Parallel Port Primary Base Address LSB Register bit 2 is set to 1, the EPP mode cannot be enabled.

8.8 SWC and ACPI Configuration Registers (LDN=04h)

8.8.1 SWC Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**SWC_EN (SWC Module Activation)** 0: Disabled (default). 1: SWC enabled.

8.8.2 PM1b_EVT_BLK Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.8.3 PM1b_EVT_BLK Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-2	**Read/write**, mapped as Base Addresses [7:2].
1-0	**Read only** as "00b."

8.8.4 PM1b_CNT_BLK Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.8.5 PM1b_CNT_BLK Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-1	**Read/write**, mapped as Base Addresses [7:1].
0	**Read only** as "0b."

8.8.6 GPE1_BLK Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.8.7 GPE1_BLK Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-3	**Read/write**, mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

8.8.8 SWC Interrupt Level Select (Index=70h, Default=00h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for SWC.

8.8.9 GPE1_STS_0 to IRQ Enable Register (GE0_2IRQ) (Index=E0h, Default=00h)

Bit	Description
7	**GE0_2IRQ7** Enable the activation of the IRQ by an active event of GPIOW17_STS. The event affects the output regardless of the setting of the GPE1_EN_0 register. 0: Disabled (default). 1: Enabled.
6-0	**GE0_2PON6-0.** These bits are the same as above for GPIOW16_STS to GPIOW10_STS.

8.8.10 GPE1_STS_1 to IRQ Enable Register (GE1_2IRQ) (Index=E1h, Default=00h)

Bit	Description
7	**GE1_2IRQ7** Enable the activation of the IRQ by an active event of GPIOW47_STS. The event affects the output regardless of the setting of the GPE1_EN_1 register. 0: Disabled (default). 1: Enabled.
6-0	**GE1_2IRQ6-0.** These bits are the same as above for GPIOW46_STS to GPIOW40_STS.

8.8.11 GPE1_STS_2 to IRQ Enable Register (GE2_2IRQ) (Index=E2h, Default=00h)

Bit	Description
7	**GE2_2IRQ7** Enable the activation of the IRQ by an active event of PBT_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
6	**GE2_2IRQ6** Enable the activation of the IRQ by an active event of SBT_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
5	**GE2_2IRQ5** Enable the activation of the IRQ by an active event of KBD_EVT3_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
4	**GE2_2IRQ4** Enable the activation of the IRQ by an active event of KBD_EVT2_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
3	**GE2_2IRQ3** Enable the activation of the IRQ by an active event of KBD_EVT1_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
2	**GE2_2IRQ2** Enable the activation of the IRQ by an active event of MS_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
1	**GE2_2IRQ1** Enable the activation of the IRQ by an active event of RI2_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
0	**GE2_2IRQ0** Enable the activation of the IRQ by an active event of RI1_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.

8.8.12 GPE1_STS_3 to IRQ Enable Register (GE3_2IRQ) (Index=E3h, Default=00h)

Bit	Description
7	**GE3_2IRQ7** Enable the de-activation of the IRQ by an active event of SW_OFF_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
6	**GE3_2IRQ6** Enable the activation of the IRQ by an active event of SW_ON_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
5	**Reserved**
4	**GE3_2IRQ4** Enable the activation of the IRQ by an active event of MOD_IRQ_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
3	**GE3_2IRQ3** Enable the activation of the IRQ by an active event of MS_IRQ_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enable.
2	**GE3_2IRQ2** Enable the activation of the IRQ by an active event of KBD_IRQ_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disable (default). 1: Enabled.
1	**GE3_2IRQ1** Enable the activation of the IRQ by an active event of P12_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
0	**GE3_2IRQ0** Enable the activation of the IRQ by an active event of RTC_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.

8.8.13 GPE1_STS_0 to SMI# Enable Register (GE0_2SMI) (Index=E4h, Default=00h)

Bit	Description
7	**GE0_2SMI7** Enable the activation of the SMI# by an active event of GPIOW17_STS. The event affects the output regardless of the setting of the GPE1_EN_0 register. 0: Disabled (default). 1: Enabled.
6-0	**GE0_2PON6-0** These bits are the same as above for GPIOW16_STS to GPIOW10_STS.

8.8.14 GPE1_STS_1 to SMI# Enable Register (GE1_2SMI) (Index=E5h, Default=00h)

Bit	Description
7	**GE1_2SMI7** Enable the activation of the SMI# by an active event of GPIOW47_STS. The event affects the output regardless of the setting of the GPE1_EN_1 register. 0: Disabled (default). 1: Enabled.
6-0	**GE1_2SMI6-0** These bits are the same as above for GPIOW46_STS to GPIOW40_STS.

8.8.15 GPE1_STS_2 to SMI# Enable Register (GE1_2SMI) (Index=E6h, Default=00h)

Bit	Description
7	**GE2_2SMI7** Enable the activation of the SMI# by an active event of PBT_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
6	**GE2_2SMI6** Enable the activation of the SMI# by an active event of SBT_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disable (default). 1: Enable.
5	**GE2_2SMI5** Enable the activation of the SMI# by an active event of KBD_EVT3_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disable (default). 1: Enable.
4	**GE2_2SMI4** Enable the activation of the SMI# by an active event of KBD_EVT2_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
3	**GE2_2SMI3** Enable the activation of the SMI# by an active event of KBD_EVT1_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
2	**GE2_2SMI2** Enable the activation of the SMI# by an active event of MS_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
1	**GE2_2SMI1** Enable the activation of the SMI# by an active event of RI2_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
0	**GE2_2SMI0** Enable the activation of the SMI# by an active event of RI1_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.

8.8.16 GPE1_STS_3 to SMI# Enable Register (GE3_2SMI) (Index=E7h, Default=00h)

Bit	Description
7	**GE3_2SMI7** Enable the de-activation of the SMI# by an active event of SW_OFF_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
6	**GE3_2SMI6** Enable the activation of the SMI# by an active event of SW_ON_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
5	**Reserved**
4	**GE3_2SMI4** Enable the activation of the SMI# by an active event of MOD_IRQ_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
3	**GE3_2SMI3** Enable the activation of the SMI# by an active event of MS_IRQ_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
2	**GE3_2SMI2** Enable the activation of the SMI# by an active event of KBD_IRQ_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
1	**GE3_2SMI1** Enable the activation of the SMI# by an active event of P12_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
0	**GE3_2SMI0** Enable the activation of the SMI# by an active event of RTC_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.

8.8.17 Power ON Status Register (PONSTS) (Index=E8h, Default=--)

Bit	R/W	Description
7	R/W1C	**PWR_FAIL (Power Fail Status)** Indicate that IT8780F has been waken-up from a Power Fail condition (both VCC and VSB off). This bit is set by the VSB power-on reset. Writing "1" will clear it; writing "0" will be ignored. 0: Inactive. 1: Waken-up from Power Fail.
6	RO	**LAST_PSON (Last Value of PSON)** This bit reflects the last value of the PSON# pin when the last previous Power Fail condition (both VCC and VSB off) occurred. Writing to this bit is ignored. 0: PSON# Inactive -- VCC power off (default). 1: PSON# active – VCC power on.
5-0	R/W	**Reserved**

8.8.18 SWC Miscellaneous Control Register (SWC_CTL) (Index=F0h, Default=00h)

Bit	R/W	Description
7	R/W	**SW_OFF_CTL (Software OFF Control)** Write "1" to set the SW_OFF_STS bit in the GPE1_STS_3 register, which triggers a VCC power off sequence. This bit clears itself. 0: Inactive (default). 1: Trigger a VCC power off sequence.
6	R/W	**SW_ON_CTL (Software ON Control)** Write "1" to set the SW_ON_STS bit in the GPE1_STS_3 register, which triggers a VCC power on sequence. This bit clears itself. When the VCC power is off, this bit can be written only through the SM bus. 0: Inactive (default). 1: Trigger a VCC power on sequence.
5	R/W1C	**PBT_OVR_STS (Power Button Override Status)** Indicate that the Power Button Override event has occurred (Power button pressed for more than 4 seconds). In this condition, the VCC power is unconditionally turned off. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive (default). 1: Power Button Override event has occurred.
4	R/W	**DIS_ASW_KBMS (Disable Auto-Swap Keyboard and Mouse Inputs)** Disable the hardware auto-swapping Keyboard (KCLK, KDAT) and Mouse (MCLK, MDAT) signals. The Auto-Swap function is only enabled in both **DIS_ASW_KBMS** and **SWAP_KBMS** being cleared. 0: Enable hardware Auto-Swapping Keyboard and Mouse Inputs (default). 1: Disable hardware Auto-Swapping Keyboard and Mouse Inputs.
3	R/W	**SWAP_KBMS (Swap Keyboard and Mouse Inputs)** When this bit set, the keyboard signals (KCLK, KDAT) will be swapped by mouse signals (MCLK, MDAT), and the Auto-Swap function is disabled regardless of the setting of **DIS_ASW_KBMS.** 0: No forced swapping (default). 1: Swaps the Keyboard and mouse signals.
2	R/W	**EN_RTC_EVT (Enable RTC alarm Event)** Enable the RTC alarm event to the PM1b_STS_HIGH and to the PM1b_EN_HIGH registers. However, the RTC_EVT_STS bit in the GPE1_STS_3 register and the RTC_EVT_EN bit in the GPE1_EN_3 register are not affected. 0: Disable the RTC alarm event (default). 1: Enable the RTC alarm event.

[cont'd]

Bit	R/W	Description
1	R/W	**EN_SLPBTN_EVT (Enable Sleep Button Event)** Enable the Sleep Button pressing event to the PM1b_STS_HIGH and to the PM1b_EN_HIGH registers. However, the SLPT_EVT_STS bit in the GPE1_STS_2 register and the SLBT_EVT_EN bit in the GPE1_EN_2 register are not affected. 0: Disable the Sleep Button pressing event (default). 1: Enable the Sleep Button pressing event.
0	R/W	**EN_PWRBTN_EVT (Enable Power Button Event)** Enable the Power Button pressing event to the PM1b_STS_HIGH and to the PM1b_EN_HIGH registers. However, the PWRT_EVT_STS bit in the GPE1_STS_2 register and the PWRT_EVT_EN bit in the GPE1_EN_2 register are not affected. 0: Disable the Power Button pressing event (default). 1: Enable the Power Button pressing event.

8.8.19 Power ON Control Register (PONCTL) (Index=F1h, Default=00h, VPP)

Bit	R/W	Description
7	R/W	**GPIOW1_DEB (GPIOW1 De-bounce Control)** This bit controls the de-bounced mode of GPIOW17-10. If the fast mode is selected, the GPIOW17_STS-GPIOW10_STS will not be active unless the related inputs have been active for at least 800ns. If the slow mode is selected, the GPIOW17_STS-GPIOW10_STS will not be active unless the related inputs have been active for at least 8ms. 0: Fast mode (default). 1: Slow mode.
6	R/W	**GPIOW4_DEB (GPIOW4 De-bounce Control)** This bit controls the de-bounced mode of GPIOW47-40. If the fast mode is selected, the GPIOW47_STS-GPIOW40_STS will not be active unless the related inputs have been active for at least 800ns. If the slow mode is selected, the GPIOW47_STS-GPIOW40_STS will not be active unless the related inputs have been active for at least 8ms. 0: Fast mode (default). 1: Slow mode.
5-4	R/W	**RSU_MOD1-0 (Resume Mode Control)** These bits control the behavior of the PSON# and PWUREQ# signals after waking-up from a Power Fail condition (both VCC and VSB are off). shows the details.
3	R/W	**SLP_SX_2PSON (SLP_SX# Signal to PSON#)** Enable SLP_SX# signal as a source to activate PSON#. 0: Disabled (default). 1: Enable PSON# from SLP_SX# signal.
2-0	R/W	**MSEVCFG2-0 (Mouse Event Configuration)** These bits configure the mouse data sequence for the Mouse event. Before setting them to a new value, these bits should be cleared by writing a value of 000b. 000: Disable mouse wake-up detection (default) 001: Wake-up on any mouse movement or button click 010: Wake-up on left button click 011: Wake-up on left button double-click 100: Wake-up on right button click 101: Wake-up on right button double-click 110: Wake-up on any button single-click 111: Wake-up on any button double-click

Table 8-15. PSON# and PWUREQ# as a Function of the Resume Mode.

RSU_MOD1-0	SLP_SX#[1]	LAST_PSON	RTC Alarm in Power Fail	PSON#	PWUREQ#
00	0	X	X	Inactive	--
	1	X	X	Active	Pulse
01	0	X	0	Inactive	--
	1	X	X	Active	Pulse
	X	X	1	Active	Pulse
10	X	0	X	Inactive	--
	X	1	X	Active	Pulse
11	X	0	0	Inactive	--
	X	1	X	Active	Pulse
	X	X	1	Active	Pulse

1. SLP_SX_2PSON should be set or SLP_SX# will not affect PSON#.

8.8.20 Keyboard Wake-up Control Register (KBD_CTL) (Index=F2h, Default=00h, VPP)

Bit	Description
7	**KBD_MOD (Keyboard Wake-up Mode Control)** This bit selects the keyboard wake-up modes for the Keyboard Wake-up Detector. 0: "Power Management Keys" mode (default). 1: "Password" mode.
6-5	**EVT3CFG1-0 (Keyboard Event 3 Configuration)** These bits configure the keyboard data sequence for Keyboard Event 3, which indicates that "PM Key 3" was pressed on the Keyboard. They are relevant only if KBD_MOD=0. The Keyboard data sequence used to detect Keyboard Event 3 is stored in registers KEYCD0-2, starting with KEYCD0. 00: 0 byte – Keyboard Event 3 disabled (default) 01: 1 byte (KEYCD0) 10: 2 bytes (KEYCD0, KEYCD1) 11: 3 bytes (KEYCD0, KEYCD1, KEYCD2)
4-3	**EVT2CFG1-0 (Keyboard Event 2 Configuration)** These bits configure the keyboard data sequence for Keyboard Event 2, which indicates that "PM Key 2" was pressed on the Keyboard. They are relevant only if KBD_MOD=0. The Keyboard data sequence used to detect Keyboard Event 2 is stored in registers KEYCD3-5, starting with KEYCD3. 00: 0 byte – Keyboard Event 2 disabled (default) 01: 1 byte (KEYCD3) 10: 2 bytes (KEYCD3, KEYCD4) 11: 3 bytes (KEYCD3, KEYCD4, KEYCD5)

Keyboard Wake-up Control Register [cont'd]

Bit	Description
2-0	**EVT1CFG2-0 (Keyboard Event Configuration)** These bits configure the keyboard data sequence for Keyboard Event 1, which indicates that "PM Key 1" or "Password" was pressed on the Keyboard. If KBD_MOD=1 ("Password" mode). EVT1CFG2-0 bits determine the keys' number. The keyboard data sequence used to detect a Keyboard Event is stored in registers KEYCD0-7, starting with KEYCD0. If KBD_MOD=0 ("Power Management Keys" mode), EVT1CFG2-0 determine the byte number. The Keyboard data sequence used to detect Keyboard Event 2 is stored in registers KEYCD6-7, starting with KEYCD6. KBD_MOD=0: 000: 0 byte – Keyboard Event 1 disabled (default) 001: 1 byte (KEYCD6) 010: 2 bytes (KEYCD6, KEYCD7) 100: Any Key mode others: Reserved KBD_MOD=1: 000~111: "Password" mode with 1~8 keys "Make" code (excluding Shift, Enter, Back Space, and ALT keys)

8.8.21 GPE1_STS_0 to PSON# Enable Register (GE0_2PON) (Index=F3h, Default=00h, VPP)

Bit	Description
7	**GE0_2PON7** Enable the activation (turn VCC ON) of the PSON# by an active event of GPIOW17_STS. The event affects the output regardless of the setting of the GPE1_EN_0 register. 0: Disabled (default). 1: Enabled.
6-0	**GE0_2PON6-0** These bits are the same as above for GPIOW16_STS to GPIOW10_STS.

8.8.22 GPE1_STS_1 to PSON# Enable Register (GE1_2PON) (Index=F4h, Default=00h, VPP)

Bit	Description
7	**GE1_2PON7** Enable the activation (turn VCC ON) of the PSON# by an active event of GPIOW47_STS. The event affects the output regardless of the setting of the GPE1_EN_1 register. 0: Disabled (default). 1: Enabled.
6-0	**GE1_2PON6-0** These bits are the same as above for GPIOW46_STS to GPIOW40_STS.

8.8.23 GPE1_STS_2 to PSON# Enable Register (GE1_2PON) (Index=F5h, Default=00h, VPP)

Bit	Description
7	**Reserved** Pressing Power Button will always cause the activation (turn VCC on) of the PSON# signal.
6	**GE2_2PON6** Enable the activation (turn VCC ON) of the PSON# by an active event of SBT_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
5	**GE2_2PON5** Enable the activation (turn VCC ON) of the PSON# by an active event of KBD_EVT3_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
4	**GE2_2PON4** Enable the activation (turn VCC ON) of the PSON# by an active event of KBD_EVT2_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
3	**GE2_2PON3** Enable the activation (turn VCC ON) of the PSON# by an active event of KBD_EVT1_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disable (default). 1: Enable.
2	**GE2_2PON2** Enable the activation (turn VCC ON) of the PSON# by an active event of MS_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
1	**GE2_2PON1** Enable the activation (turn VCC ON) of the PSON# by an active event of RI2_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.
0	**GE2_2PON0** Enable the activation (turn VCC ON) of the PSON# by an active event of RI1_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_2 register. 0: Disabled (default). 1: Enabled.

8.8.24 GPE1_STS_3 to PSON# Enable Register (GE3_2PON) (Index=F6h, Default=00h, VPP)

Bit	Description
7	**GE3_2PON7** Enable the de-activation (turn VCC **OFF**) of the PSON# by an active event of SW_OFF_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
6	**GE3_2PON6** Enable the activation (turn VCC ON) of the PSON# by an active event of SW_ON_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.
5	**Reserved**
4	**Reserved**
3	**Reserved**
2	**Reserved**
1	**Reserved**
0	**GE3_2PON0** Enable the activation (turn VCC ON) of the PSON# by an active event of RTC_EVT_STS. The event affects the output regardless of the setting of the GPE1_EN_3 register. 0: Disabled (default). 1: Enabled.

8.8.25 LED Control Register (LED_CTL) (Index=F7h, Default=00h, VPP)

Bit	Description
7	**Reserved**
6	**LEDPOL (Polarity of LEDs)** This bit determines the polarity of LED1 and LED2 outputs. When this bit is set to 0, the LED1 and LED2 is active low to turn on the LED. When this bit is set to 1, the LED1 and LED2 are active high to turn on the LED. 0: Active low (default). 1: Active high.
5	**LED2_ONVSB (LED2 Operation mode when VSB only)** This bit determines the operation mode of LED2 when VSB is on and VCC is off. 0: OFF (default). 1: Blinking on 1/4 Hz with 12.25% duty cycle.
4-3	**LED2BLK1-0 (LED1 Blink Rate)** These bits control the blinking rate of LED2 output when power is ON. **Bits1-0 Rate(Hz) Duty Cycle** 00 OFF Always inactive (default) 01 0.25 12.25% 10 1 50% 11 ON Always active
2	**LED1_ONVSB (LED1 Operation mode when VSB only)** This bit determines the operation mode of LED1 when VSB is on and VCC is off. 0: OFF (default). 1: Blinking on 1/4 Hz with 12.25% duty cycle.

LED Control Register [cont'd]

Bit	Description
1-0	**LED1BLK1-0 (LED1 Blink Rate)** These bits control the blinking rate of LED1 output when power is ON. **Bits1-0 Rate (Hz) Duty Cycle** 00 OFF Always inactive (default) 01 0.25 12.25% 10 1 50% 11 ON Always active

8.8.26 Keyboard Code Data 0-7 Registers (KEYCD0-7) (Index=F8h-FFh, Default = -- ,VPP)

Bit	Description
7-0	**Keyboard Scan Code Data 7-0.**

8.9 Keyboard Configuration Registers (LDN=05h)

8.9.1 Keyboard Activate (Index=30h, Default=01h or 00h)

Bit	Description
7-1	**Reserved**
0	**KBD_EN (Keyboard Activation)** When KBCDIS (bit 4 of the Function Fast Disable Register) is cleared and this bit is set, the Keyboard function is enabled. The default value depends on the state of the RTS1# when LRESET# is activated. The default value is 1b for the high state of RTS1# when LRESET# is activated. It is 0b for the low state of RTS1# when LRESET# is activated. 0: Disabled. 1: Keyboard enabled, if KBCDIS=0.

8.9.2 KBC Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write,** mapped as Base Addresses [11:8].

8.9.3 KBC Data Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-0	**Read/write**, mapped as Base Addresses [7:0].

8.9.4 KBC Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.9.5 KBC Command Base Address LSB Register (Index=63h, Default=64h)

Bit	Description
7-0	**Read/write**, mapped as Base Addresses [7:0].

8.9.6 Keyboard Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-5	Reserved with default "0h."
4	**WK_EN (Wake-Up Enable)** 0: Disabled (default). 1: Enable to set KBD_IRQ_STS of GPE_STS_3 by an activation of KBD_IRQ.
3-0	Select the interrupt level [Note1] for Keyboard.

8.9.7 keyboard Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt set for Keyboard and is **read only** as "02h" when bit 0 of the Keyboard Special Configuration Register is cleared. When bit 0 is set, this type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	**ACT_LEVEL (Active Level)** 0: Low Level. 1: High Level (default).
0	**ACT_TYPE (Active Type)** 0: Edge Type. 1: Level Type.

8.9.8 KBC Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**KBD_IRQ_SHR (Keyboard Interrupt Request Sharing)** 0: Normal (default). 1: Enable Keyboard IRQ sharing.
3	**KBC_CLK (KBC Clock Frequency Selection)** 0: KBC's clock frequency is 12 MHz (default). 1: KBC's clock frequency is 8 MHz.
2	**Reserved**
1	**IRQ_TYPE_WR (Interrupt Type Register Write Enable)** 0: Type of interrupt of Keyboard is fixed (default). 1: Type of interrupt of Keyboard can be changed.
0	**EXT_ROM (External ROM for Microprocessor)** 0: Internal built-in ROM is used (default). 1: Enable the External Access ROM of 8042.

8.10 Mouse Configuration Registers (LDN=06h)

8.10.1 Mouse Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**MS_EN (Mouse Activation)** When the Keyboard function is enabled, setting this bit will enable the Mouse function. 0: Disabled (default). 1: Mouse enabled, if Keyboard is enabled.

8.10.2 Mouse Interrupt Level Select (Index=70h, Default=0Ch)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for Mouse.

8.10.3 Mouse Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt used for Mouse and is **read only** as "02h" when bit 0 of the Mouse Special Configuration Register is cleared. When bit 0 is set, the type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	**ACT_LEVEL (Active Level)** 0: Low Level. 1: High Level (default).
0	**ACT_TYPE (Active Type)** 0: Edge Type. 1: Level Type.

8.10.4 Mouse Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	**Reserved with default "00h."**
1	**MS_IRQ_SHR (Keyboard Interrupt Request Sharing)** 0: Normal (default). 1: Enable Keyboard IRQ sharing.
0	**IRQ_TYPE_WR (Interrupt Type Register Write Enable)** 0: Type of interrupt of Mouse is fixed (default). 1: Type of interrupt of Mouse can be changed.

8.11 GPIO Configuration Registers (LDN=07h)

8.11.1 Programmable Chip Select 1 Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.11.2 Programmable Chip Select 1 Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Addresses [7:0].

8.11.3 Programmable Chip Select 2 Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.11.4 Programmable Chip Select 2 Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Addresses [7:0].

8.11.5 GPIO(W) Set 1, 2, 3, 4, 5, and 6 Pin Polarity Registers (Index=B0h, B1h, B2h, B3h, B4h, and B5h, Default=00h)

Bit	Description
7-0	**PIN_POR7-0 (Pin Polarity)** These bits program the GPIO pins' polarity. 0: Non-inverting (default). 1: Inverting.

8.11.6 GPIO(W) Set 1, 2, 3, 4, 5, and 6 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, BCh, and BDh, Default=00h)

Bit	Description
7-0	**PIN_PU7-0 (Pin Pull-up)** These bits are used to enable the GPIO pin internal pull-up. 0: No Pull-up (default). 1: With pull-up resistor.

8.11.7 Simple I/O Set 1, 2, 3, 4, 5, and 6 Data Registers (Index=C0h, C1h, C2h, C3h, C4h, and C5h, Default=00h)

Bit	Description
7-0	**GPIO_D7-0 (General Purpose I/O Data)** These bits are the data registers of the GPIO pins. When the GPIO pin is set as input mode, the register is read-only and reflects the state of the pin. When the GPIO pin is set as output mode, the register can be read/written and controls the state of the GPIO pin.

8.11.8 Simple I/O Set 1, 2, 3, 4, 5, and 6 Input/Output Selection Registers (Index=C8h, C9h, CAh, CBh, CCh, and CDh, Default=00h)

Bit	Description
7-0	**SMIO_DIR7-0 (Simple I/O Direction Select)** These bits determine the directions of the Simple I/O pins. 0: Input (default). 1: Output.

8.11.9 IRQ3-7, 9-12 and 14-15 External Routing Input Pin Mapping Registers (Index=E3h-E7h, E9h-ECh and EEh-EFh, Default=00h)

These registers are used to determine the external routing input pin mappings of IRQ3-7, 9-12, and 14-15.

Bit	Description
7	**Reserved**
6	**EN_IRQ_SHR (External Interrupt Request Sharing)** 0: Normal (default). 1: Enable IRQ sharing.
5-0	**IRQIN_LOC (IRQ Input Location)** Please see GPIO Pins Location Mapping Table [Note4] on page 64. The related SIMIO_DIR (Simple I/O Direction Select) should be set as input.

8.11.10 Programmable Chip Select Configuration Registers (Index=F0h, Default=00h)

Bit	Description
7-4	**CS2_CFG3-0 (Programmable Chip Select 2 Configuration)** These bits configure the address decoder of programmable chip select 2. The CS2# will be activated when the LPC I/O cycle addresses match the non-masked corresponding base address bits (determined in the Programmable Chip Select 2 Base Address MSB and LSB registers). **Bits3-0 Masked Address(es)** 0000: no masked address 0001: Address 0 0010: Addresses [1:0] 0011: Addresses [2:0] …… 1100: Addresses [11:0] else: Reserved
3-0	**CS1_CFG3-0 (Programmable Chip Select 1 Configuration)** These bits configure the address decoder of programmable chip select 1. The CS1# will be activated when the LPC I/O cycle addresses match the non-masked corresponding base address bits (determined in the Programmable Chip Select 1 Base Address MSB and LSB registers). **Bits3-0 Masked Address(es)** 0000: no masked address 0001: Address 0 0010: Addresses [1:0] 0011: Addresses [2:0] …… 1100: Addresses [11:0] else: Reserved

8.11.11 User-defined Memory Base Address High Byte Register (Index=F1h, Default=00h)

Bit	Description
7-0	**UDMA31-24 (User-defined Memory Addresses)**

8.11.12 User-defined Memory Base Address Low Byte Register (Index=F2h, Default=00h)

Bit	Description
7-0	**UDMA23-16 (User-defined Memory Addresses)**

8.11.13 User-defined Memory Size High Byte Register (Index=F3h, Default=00h)

Bit	Description
7	**Reserved**
6	**CTL_MOD (Control Signal Mode)** This bit selects the mode of the control signals XRD#_XEN and XWR#_XDIR. If XDIR is selected, a high level indicates a read cycle; a low level indicates a write cycle. 0: XRD#/XWR# mode (default). 1: XEN/XDIR mode.
5	**ADD_MOD (Address Mode)** This bit selects the address mode of the XA[23:0]. If the direct mode is selected, XA[23:0] will transfer the LPC addresses directly. If the indirect mode is selected, XA[23:0] will perform 000_0000h for LPC addresses equal to the User-defined Memory Base Address 000_0001h for LPC addresses equal to the User-defined Memory Base Address +1, and so on. 0: Direct mode (default). 1: Indirect mode.
4	**UDMEN (User-defined Memory Enable)** This bit enables the User-defined Memory segment. 0: Disable (default). 1: Enable.
3-0	**UDM_SIZ11-8 (User-defined Memory Size Configuration)** These bits configure the size after the User-defined Memory Base Addresses (addresses 31-16 are determined in the User-defined Memory Base High and Low byte registers; addresses 15-0 are 0000h.) of the user-defined memory (UDMCS#). Please see the User-defined Memory Size Low Byte Register for details.

8.11.14 User-defined Memory Size Low Byte Register (Index=F4h, Default=00h)

Bit	Description
7-0	**UDM_SIZ7-0 (User-defined Memory Size Configuration)** These bits configure the size after the User-defined Memory Base Addresses (addresses 31-16 are determined in the User-defined Memory Base High and Low Byte registers; addresses 15-0 are 0000h.) of the user-defined memory (UDMS#). **UDM_SIZ11-0 UDMS# activates in** 000h: Base address ~ Base address + FFFFh 001h: Base address ~ Base address + 1_FFFFh 002h: Base address ~ Base address + 2_FFFFh 003h: Base address ~ Base address + 3_FFFFh …… FFEh: Base address ~ Base address + FFE_FFFFh **FFFh: Base address ~ Base address + FFF_FFFFh**

8.12 RTC Configuration Registers (LDN=08h)

8.12.1 RTC Activate (Index=30h, Default=00h or 01h)

Bit	Description
7-1	**Reserved**
0	**RTC_EN (RTC Activation)** When this bit is set, the RTC function is enabled. The default value depends on the state of the RTS1# when LRESET# is activated. The default value is 1b for the High state of RTS1# when LRESET# is activated. It is 0b for the low state of RTS1# when LRESET# is activated. 0: Disabled. 1: RTC enabled.

8.12.2 RTC Primary Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** with "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.12.3 RTC Primary Base Address LSB Register (Index=61h, Default=70h)

Bit	Description
7-1	**Read/write**, mapped as Base Addresses [7:1].
0	**Read only** as "0b."

8.12.4 RTC Secondary Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** with "0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

8.12.5 RTC Secondary Base Address LSB Register (Index=63h, Default=72h)

Bit	Description
7-1	**Read/write**, mapped as Base Addresses [7:1].
0	**Read only** as "0b."

8.12.6 RTC Interrupt Level Select (Index=70h, Default=08h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for RTC.

8.12.7 RTC Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt set for RTC and is **read only** as "02h" when bit 0 of the RTC Special Configuration Register is cleared. When bit 6 is set, this type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	**ACT_LEVEL (Active Level)** 0: Low Level. 1: High Level (default).
0	**ACT_TYPE (Active Type)** 0: Edge Type. 1: Level Type.

8.12.8 RTC Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7	**RTC_IRQ_SHR (RTC Interrupt Request Sharing)** 0: Normal (default). 1: Enable RTC IRQ sharing.
6	**IRQ_TYPE_WR (Interrupt Type Register Write Enable)** 0: Type of interrupt of RTC is fixed (default). 1: Type of interrupt of RTC can be changed.
5	**Reserved**
4	**U128B3_LOCK (Lock Bytes 60h~7Fh in the Upper 128 Byte Bank RAM)** This bit is used to lock bytes 60h~7Fh in the upper 128 byte bank (Bank 1) of RAM. This register can only be written once and can only be reset by hardware reset. 0: No lock (default). 1: Locks reads and writes to the locations 60h~7Fh in the upper 128 byte bank of RAM. Write cycles will have no effect. Read cycles will not return any particular value guaranteed.
3	**U128B2_LOCK (Lock Bytes 40h~5Fh in the Upper 128 Byte Bank RAM)** This bit is used to lock bytes 40h~5Fh in the upper 128 byte bank (Bank 1) of RAM. This register can only be written once and can only be reset by hardware reset. 0: No lock (default). 1: Locks reads and writes to the locations 40h~5Fh in the upper 128 byte bank of RAM. Write cycles will have no effect. Read cycles will not return any particular value guaranteed.
2	**U128B1_LOCK (Lock Bytes 20h~3Fh in the Upper 128 Byte Bank RAM)** This bit is used to lock bytes 20h~3Fh in the upper 128 byte bank (Bank 1) of RAM. This register can only be written once and can only be reset by hardware reset. 0: No lock (default). 1: Locks reads and writes to the locations 20h~3Fh in the upper 128 byte bank of RAM. Write cycles will have no effect. Read cycles will not return any particular value guaranteed.
1	**U128B0_LOCK (Lock Bytes 00h~1Fh in the Upper 128 Byte Bank RAM)** This bit is used to lock bytes 00h~1Fh in the upper 128 byte bank (Bank 1) of RAM. This register can only be written once and can only be reset by hardware reset. 0: No lock (default). 1: Locks reads and writes to the locations 00h~1Fh in the upper 128 byte bank of RAM. Write cycles will have no effect. Read cycles will not return any particular value guaranteed.

RTC Special Configuration Register[cont'd]

Bit	Description
0	**L128_LOCK (Lock Lower 128 Byte Bank RAM)** This bit is used to lock bytes 38h~3Fh in the lower 128 byte bank (Bank 0) of RAM. This register can only be written once and can only be reset by hardware reset. 0: No lock (default). 1: Locks reads and writes to the locations 38h~3Fh in the lower 128 byte bank of RAM. Write cycles will have no effect. Read cycles will not return any particular value guaranteed.

Note 1: Interrupt level mapping

Fh-Dh: not valid
Ch: IRQ12
.
.
3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

Note 2: DMA channel mapping

7h-5h: not valid
4h: no DMA channel selected
3h: DMA3
2h: DMA2
1h: DMA1
0h: DMA0

Note 3: The GPIO Pins Location Mapping Table

Location	Pin Name	Location	Pin Name	Location	Pin Name
001 000	GPIOW10 (pin 1)	011 000	GPIO30 (pin 24)	101 000	GPIO50 (pin 124)
001 001	GPIOW11 (pin 2)	011 001	GPIO31 (pin 25)	101 001	GPIO51 (pin 55)
001 010	GPIOW12 (pin 3)	011 010	GPIO32 (pin 26)	101 010	GPIO52 (pin 34)
001 011	GPIOW13 (pin 4)	011 011	GPIO33 (pin 27)	101 011	GPIO53 (pin 45)
001 100	GPIOW14 (pin 5)	011 100	GPIO34 (pin 28)	101 100	GPIO54 (pin 54)
001 101	GPIOW15 (pin 6)	011 101	GPIO35 (pin 29)	101 101	GPIO55 (pin 9)
001 110	GPIOW16 (pin 7)	011 110	GPIO36 (pin 30)	101 110	GPIO56 (pin 10)
001 111	GPIOW17 (pin 8)	011 111	GPIO37 (pin 31)	101 111	GPIO57 (pin 13)
010 000	GPIO20 (pin 14)	100 000	GPIOW40 (pin 20)	else	Reserved
010 001	GPIO21 (pin 15)	100 001	GPIOW41 (pin 21)	-	-
010 010	GPIO22 (pin 16)	100 010	GPIOW42 (pin 35)	-	-
010 011	GPIO23 (pin 17)	100 011	GPIOW43 (pin 49)	-	-
010 100	GPIO24 (pin 18)	100 100	GPIOW44 (pin 50)	-	-
010 101	GPIO25 (pin 19)	100 101	GPIOW45 (pin 51)	-	-
010 110	GPIO26 (pin 22)	100 110	GPIOW46 (pin 52)	-	-
010 111	GPIO27 (pin 23)	100 111	GPIOW47 (pin 53)	-	-

9. Functional Description

9.1 LPC Interface

The IT8780F supports the peripheral site of the LPC I/F as described in the LPC Interface Specification Rev.1.0 (Sept. 29, 1997). In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK, which is the same as PCICLK.), the IT8780F also supports LDRQ# and SERIRQ.

9.1.1 LPC Transactions

The IT8780F supports some parts of the cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will make reactions according to the DMA requests from the DMA devices in the Super I/O modules and decide whether to ignore the current transaction or not.

The FDC and ECP are 8-bit DMA devices. So, if the LPC Host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and response with a SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA devices: the FDC and the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to trace DMA requests quickly. However, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there are at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages and send those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8780F follows the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature and is able to interface most PC chipsets. The IT8780F encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the Continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the turn-around state of current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enters the Continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when one SIRQ Slave detects its input IRQn/events have been changed, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity = low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

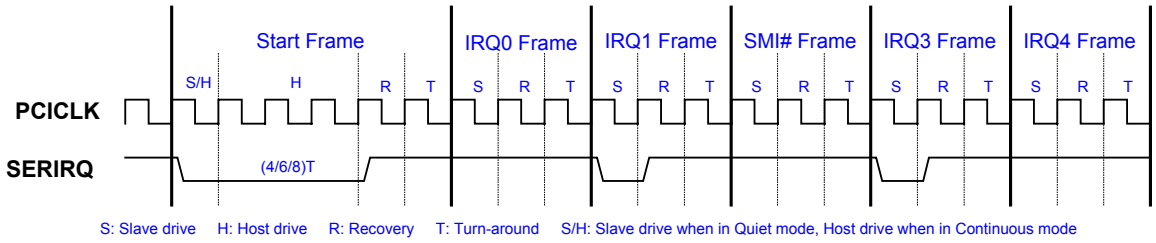


Figure 9-1. Start Frame Timing

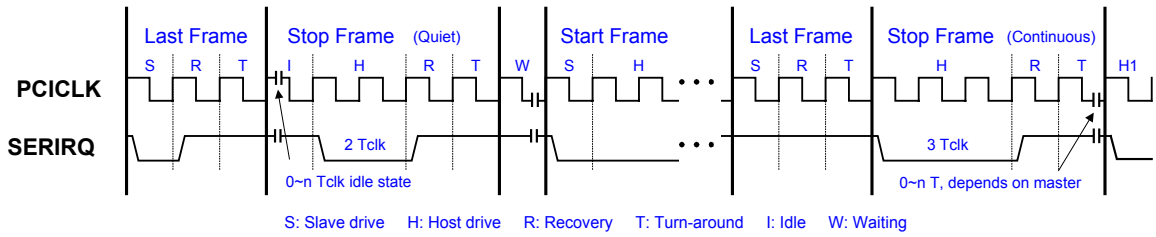


Figure 9-2. Stop Frame Timing

9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn / Events	# of Clocks Past Start	IT8780F
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8780F provides six sets (total 43 pins) of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index 24h, 25h, 26h, and 27h of the Global Configuration Registers) are set. The GPIO functions include the simple I/O function and External Interrupt routing function.

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into six registers, including the polarity (B0h, B1h, B2h, B3h, B4h, and B5h), the pin internal pull-up enable (B8h, B9h, BAh, BBh, BCh and BDh), data (C0h, C1h, C2h, C3h, C4h and C5h) and input/output selection (C8h, C9h, CAh, CBh, CCh and CDh) registers.

The External Interrupt routing function provides a useful feature for motherboard designers. Through this function, the parallel interrupts of other on-board devices can be easily re-routed into the Serial IRQ. Only IRQ3-7, 9-12 and 14-15 can be re-routed. The programming method is to fill the location code (Note 3 at the end of section 1) to the selected IRQn External Routing Input Pin Mapping Register.

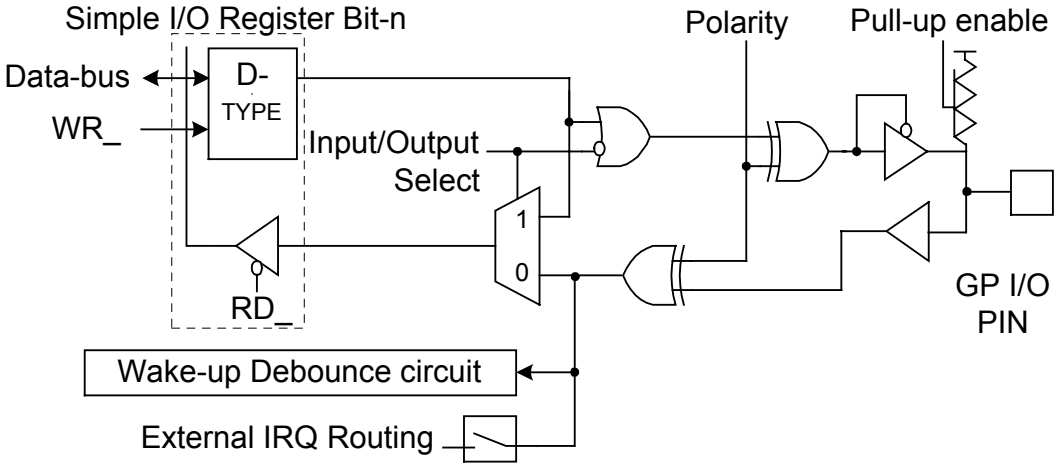


Figure 9-3. General Logic of GPIOW Function

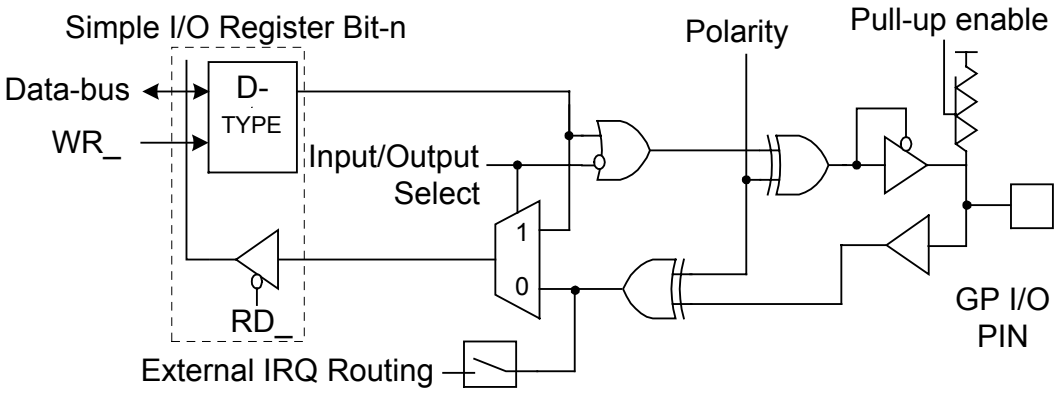


Figure 9-4. General Logic of GPIO Function

9.3.1 Serial Bus

1. Write data: Three continuous bytes are required in writing data to Serial Bus: the IT8780F Serial Bus interface Address byte, the Configuration Index register byte and then the data byte.
2. Read data: If the Configuration Index register of the Serial Bus is known as the desired one, a simply read data cycle can be given (the IT8780F Serial Bus interface Address byte, followed by the data byte read from the configuration registers). Otherwise, write the Address register to the IT8780F configuration registers first (writing the Serial Bus interface Address byte, followed by the Address register byte) and then restart to read data from the IT8780F.

The Serial Bus Interface Address of the IT8780F is 0100111b (or 1010111b, depending on the power-on strapping of pin 34).

9.3.2 The Extended Interface

The IT8780F provides the extended I/F that supports the Flash ROM I/F for the BIOS of the system, User-defined memory extension and Programmable Chip Selects for I/O devices. They are the ISA-like interfaces for external 8-bit peripherals.

9.3.2.1 The Flash ROM I/F and the User-defined Memory Extension

The Flash ROM I/F and User-defined Memory translate the qualified memory transactions of the LPC bus. For the memory transactions, all 32 address lines will be qualified. The Flash ROM I/F supports several fixed memory segments for the legacy system BIOS. The User-defined Memory extension provides a flexible and programmable memory zone for the system designer. The programmable method is to determine the starting address and the memory size.

In User-defined Memory extension, two address-mapping modes are used to translate 32 address lines of LPC memory cycle to 28 address lines of the extended I/F, the direct mode and the indirect mode. In the direct mode, the 28 least signification bits of the LPC address are directly routed to A27-0 of the extended I/F. In the indirect mode, the address on the extended I/F represents the difference between the current address and the starting address of the LPC addresses. For example, if the current address on LPC cycle is 5th after the starting address of the selected zone, the address on the extended will be 0000005h.

The address on the extended I/F is constituted by two ways: direct address lines and external latches. The direct address lines are XA11-XA4 and XA3-XA0. With the external latches, the address lines are multiplexed with XD7-XD0. The 3 address strobe signals of XSTRB2-XSTRB0 are used for A27-A20, A19-A12 and A11-A4 (the same as XA11-XA4). For A11-A4, users can select either one of these two ways.

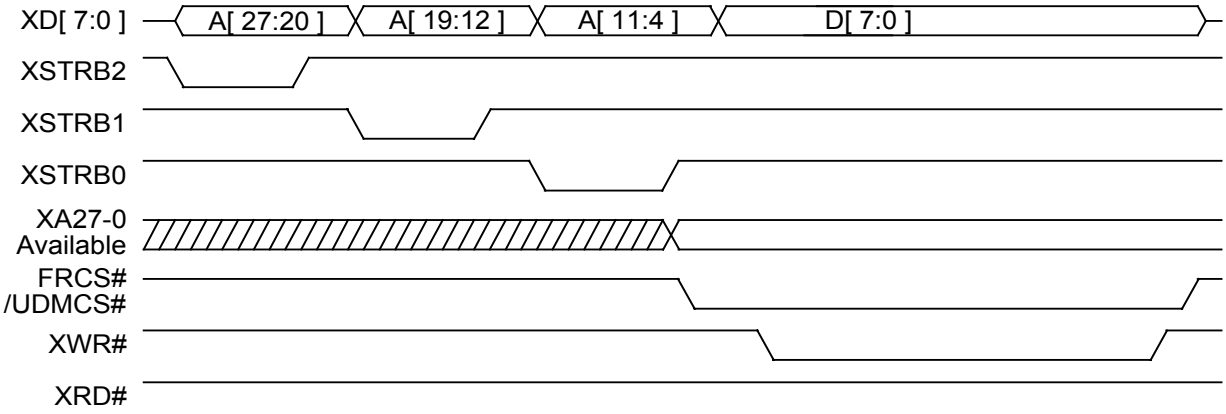


Figure 9-5. Flash ROM I/F and User-defined Memory Extension Write Access Cycle

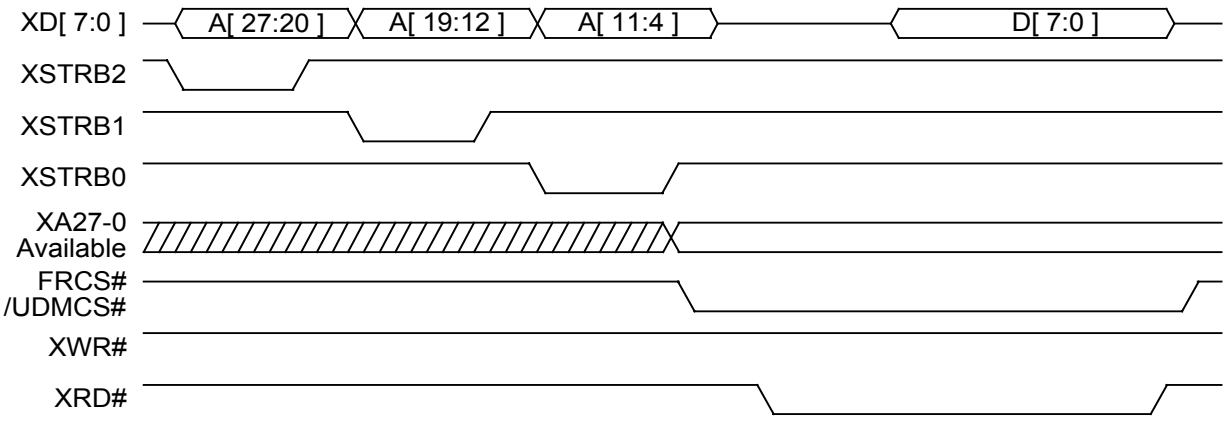


Figure 9-6. Flash ROM I/F and User-defined Memory Extension Read Access Cycle

9.3.2.2 The Programmable Chip Selects Extension

The Programmable Chip Selects translate the qualified I/O transactions of the LPC bus. For the Programmable Chip Selects, the qualification can be programmed to mask up to 12 least significant address lines. For the Programmable Chip Selects extension, only the direct address lines XA11-XA0 can be used. Except the address latches, the Programmable Chip Selects extension I/F is similar to the Flash ROM I/F and User-defined Memory extension.

9.4 System Wake-up Control (SWC) and ACPI

9.4.1 SWC General Description

The System Wake-up Control (SWC) and ACPI functional block detects wake-up events including the external and internal events, and generates system interrupts (SMI#, IRQ) and Power Management signals (PWUREQ#, PSON#) if the related enable registers are set. There are also two LED indicators which can control the LED to be ON, OFF or blinking.

The external events include the followings:

1. Sixteen VSB-powered General Purpose Input/Output Wake-up events
2. Two Modem Ring Indicator events (RI1# and RI2#)
3. Mouse events including movement and button pressing (via MCLK and MDAT)
4. Keyboard events (via KCLK and KDAT)
5. Power and Sleep buttons pressing events (PWBTIN# and SLBTIN#)

The external events include the followings:

1. RTC alarm event
2. Legacy module (FDC, Serial Port 1, Serial Port 2, and Parallel Port) Interrupt event
3. Keyboard interrupt event
4. Mouse interrupt event
5. Software Power-ON and Power-OFF request events

If any of the external and internal events is received, the SWC will set the related status register in PM1b_STST_HIGH or GPE1_STS_0~GPE1_STS_3. Based on these events and the routing information written into its registers, the SWC generates the IRQ (via SERIRQ) and SMI# if the related enable registers are set (GE0_2IRQ~GE03_2IRQ and GE0_2SMI~ GE3_2SMI, E0h~E3h and E4h~E7 registers of LDN4). The SWC also generates the Power Management signals -- PWUREQ# and PSON#. PM1b_EN_HIGH and GPE1_EN_0~GPE1_EN_3 are the enable registers for PWUREQ#. GE0_2PON~GE3_2PON registers (F2h~F6h of LDN4) are the enable registers for PSON#. When VCC is ON, the Power Button Override event (pressing the power button for more than four seconds) will de-assert the signal PSON# directly. When VCC is OFF, a detection of the power button will also assert the signal PSON# directly.

There are two control bits, RSU_MOD1-0 in the Power Control register, used to control the behavior of the signals PSON# and PWUREQ# after waking-up from a Power Fail condition (both VCC and VSB are off). SLP_SX# is the Sleep State input from the south-bridge.

The LED Control Register (LED_CTL) is programmed to control the behaviors of LED1 an LED2. The LED2_ONVSB and LED1_ONVSB determine the operations when VSB is on and is VCC off. LED2BLK1-0 and LED1BLK1-0 control the behaviors when both VSB and VCC are on. So, each LED output can be programmed in different operations between VCC off and on states.

The registers F0h~FFh of the SWC are powered by VPP which is supplied by VSB when VSB is present, and is supplied by VBAT when VSB disappears. The other registers of SWC are powered by VSB.

9.4.2 ACPI Registers

The ACPI registers supported by IT8780F are divided into three groups:
1. PM1 Event Group (block b): PM1b_STS_LOW, PM1b_STS_HIGH, PM1b_EN_LOW, and PM1b_EN_HIGH.
2. PM1 Control Group (block b): PM1b_CNT_LOW and PM1b_CNT_HIGH.
3. General Purpose Event 1 Group: GPE1_STS_0, GPE1_STS_1, GPE1_STS_2, GPE1_STS_3, GPE1_EN_0, GPE1_EN_1, GPE1_EN_2 and GPE1_EN_3.

All the status register bits behave according to the "Sticky status bit" definition (the bit is set by the HIGH level of the hardware signal and can only be cleared by software writing a one to it) in ACPI Specification. IT8780F will generate an activation of PWUREQ# when both the status and enable bits of an event are set simultaneously. All these registers are powered by VSB. The enabled registers are reset to 00h when VSB is powered-up.

Table 9-1. ACPI Registers

Base Address	Offset	R/W	Mnemonic	Register Name
60h and 61h of LDN4	0h	RO	PM1b_STS_LOW	PM1 Status Block b Low Register
	1h	R/W1C	PM1b_STS_HIGH	PM1 Status Block b High Register
	2h	RO	PM1b_EN_LOW	PM1 Enable Block b Low Register
	3h	R/W	PM1b_EN_HIGH	PM1 Enable Block b High Register
62h and 63h of LDN4	0h	RO	PM1b_CNT_LOW	PM1 Control Block b Low Register
	1h	R/W	PM1b_CNT_HIGH	PM1 Control Block b High Register
64h and 65h of LDN4	0h	R/W1C	GPE1_STS_0	General Purpose 1 Status 0 Register
	1h	R/W1C	GPE1_STS_1	General Purpose 1 Status 1 Register
	2h	R/W1C	GPE1_STS_2	General Purpose 1 Status 2 Register
	3h	R/W1C	GPE1_STS_3	General Purpose 1 Status 3 Register
	4h	R/W	GPE1_EN_0	General Purpose 1 Enable 0 Register
	5h	R/W	GPE1_EN_1	General Purpose 1 Enable 1 Register
	6h	R/W	GPE1_EN_2	General Purpose 1 Enable 2 Register
	7h	R/W	GPE1_EN_3	General Purpose 1 Enable 3 Register

9.4.2.1 PM1 Status Block b Low Register (PM1b_STS_LOW)

This register, which contains the lower eight bits of the PM1_STS Block b registers, belongs to PM1 Event Group of the ACPI fixed-feature space registers. PM1_STS Block b register bits are specified by the ACPI but are not implemented in the IT8780F. Bits 5, 4, 0 have a "0" value.

Bit	Description
7-6	**Reserved**
5	**GBL_STS (Global Lock Status)** Not implemented. This bit is always "0".
4	**BM_STS (Bus Master Status)** Not implemented. This bit is always "0".
3-1	**Reserved**
0	**TMR_STS (PM Timer Status)** Not implemented. This bit is always "0".

9.4.2.2 PM1 Status Block b High Register (PM1b_STS_HIGH)

Bit	Description
7	**WAK_STS (Wake-Up Event Status)** Indicates that an enabled wake-up event has occurred. This bit is set only if the system is in a sleep state (S1-S5). Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive (default). 1: The system is in a sleep state and at least one enabled wake-up event is active.
6-4	**Reserved**
3	Ignored. The data written is ignored. The data read is undefined.
2	**RTC_STS (RTC Event Status)** Indicates that an enabled RTC alarm (both AIE of RTC CRB and AF of RTC CRC are set) has occurred. This bit is set by the RTC alarm becoming active. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive (default). 1: An RTC alarm has occurred.
1	**SLPBTN_STS (Sleep Button Event Status)** Indicates that the Sleep button was pressed. This feature is compatible with the ACPI model for both a “single-button” and a “two-button” system. The PWBTIN# signal is internally de-bounced. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive (default). 1: The Sleep button was pressed.
0	**PWRBTN_STS (Power Button Event Status)** Indicates that the Power button was pressed. This feature is compatible with the ACPI model for a “two-button” system. The SLBTIN# signal is internally de-bounced. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive (default). 1: The Power button was pressed.

9.4.2.3 PM1 Enable Block b Low Register (PM1b_EN_LOW)

This register, which contains the lower eight bits of the PM1_EN Block b registers, belongs to PM1 Event Group of the ACPI fixed-feature space registers. PM1_EN Block b register bits are specified by the ACPI, but are not implemented in the IT8780F.Bits 5 and 0 have a ”0” value.

Bit	Description
7-6	**Reserved**
5	**GBL_EN (Global Lock Enable)** Not implemented. This bit is always “0”.
4-1	**Reserved**
0	**TMR_EN (PM Timer Enable)** Not implemented. This bit is always “0”.

9.4.2.4 PM1 Enable Block b High Register (PM1b_EN_ HIGH)

Bit	Description
7-3	**Reserved**
2	**RTC_EN (RTC Event Enable)** Enables the RTC alarm to generate a power management event (SCI or wake-up). 0: Disable event (default). 1: Enable event from RTC alarm.
1	**SLPBTN_EN (Sleep Button Event Enable)** Enables Sleep button pressing to generate a power management event (SCI or wake-up). 0: Disable event (default). 1: Enable event from Sleep button pressing.
0	**PWRBTN_EN (Power Button Event Enable)** Enables Power button pressing to generate a power management event (SCI or wake-up). 0: Disable event (default). 1: Enable event from Power button pressing.

9.4.2.5 PM1 Control Block b Low Register (PM1b_ CNT _LOW)

Bit	Description
7-3	**Reserved**
2	**GBL_RLS (Global Lock Release)** Not implemented. This bit is always “0”.
1	**GBM_RLD (Bus Master Request Control)** Not implemented. This bit is always “0”.
0	**SCI_EN (SCI Enable)** Not implemented. This bit is always “0”.

9.4.2.6 PM1 Control Block b High Register (PM1b_ CNT _HIGH)

Bit	R/W	Description
7-6	-	**Reserved**
5	WO	**SLP_EN (Sleep Enable)** This bit may be set in the same write cycle with a new SLP_TYP2-0 value. 0: Inactive (default). 1: Update the current state code from the SLP_TYP2-0 value.
4-2	R/W	**SLP_TYP2-0 (Sleep Type)** **Bits 2-0 Function** 000 Encoded 3-bit value for Sn(n=0~5) (default) XXX Encoded 3-bit value (except 000) for the remaining 5 sleep state Sn(n=0~5)
1	-	Ignored. The data written is ignored, and the data read is undefined.
0	-	**Reserved**

9.4.2.7 General Purpose 1 Status 0 Register (GPE1_STS_0)

This register, containing bits 0-7 of the GPE1_STS register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the "Sticky status bit" definition (the bit is set by the HIGH level of the hardware signal and is only cleared by writing "1" to it through software) in the ACPI Specification.

Bit	Description
7	**GPIOW17_STS (GPIOW17 Event Status)** This bit indicates that an active event has been detected at pin 7 of the GPIOW set 1. The event has programmable polarity and de-bounce option (see Section 8.11.5 and 8.8.19). The bit is set by an active level at the GPIOW17 pin. Write "1" to clear this bit. Writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An active event has occurred.
6-0	**GPIOW16_STS to GPIOW10_STS (GPIOW16-10 Event Status)** These bits are the same as the above for pins 6-0 of the GPIOW set 1.

9.4.2.8 General Purpose 1 Status 1 Register (GPE1_STS_1)

This register, containing bits 8-15 of the GPE1_STS register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the "Sticky status bit" definition (the bit is set by the HIGH level of the hardware signal and is only cleared by writing "1" to it through software) in the ACPI Specification.

Bit	Description
7	**GPIOW47_STS (GPIOW47 Event Status)** This bit indicates that an active event has been detected at pin 7 of the GPIOW set 4. The event has programmable polarity and de-bounce option (see Section 8.11.5 and 8.8.19). The bit is set by an active level at the GPIOW47 pin. Write "1" to clear this bit. Writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An active event has occurred.
6-0	**GPIOW46_STS to GPIOW40_STS (GPIOW46-40 Event Status)** These bits are the same as the above for pins 6-0 of the GPIOW set 4.

9.4.2.9 General Purpose 1 Status 2 Register (GPE1_STS_2)

This register, containing bits 16-23 of the GPE1_STS register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the "Sticky status bit" definition (the bit is set by the HIGH level of the hardware signal and is only cleared by writing "1" to it through software) in the ACPI Specification.

Bit	Description
7	**PBT_EVT_STS (Power Button Event Status)** Indicates that the power button was pressed. This bit is similar to the PWRBTN_STS bit in the PM1b_HIGH register. The PWBTIN# signal is internally de-bounced. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive (default). 1: The power button was pressed.
6	**SBT_EVT_STS (Sleep Button Event Status)** Indicates that the sleep button was pressed. This bit is similar to the SLPBTN_STS bit in the PM1b_HIGH register. The SLBTIN# signal is internally de-bounced. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive (default). 1: The sleep button was pressed.

General Purpose 1 Status 2 Register (GPE1_STS_2) [cont'd]

Bit	Description
5	**KBD_EVT3_STS (Keyboard Event 3 Status)** This bit indicates that "PM Key 3" was pressed and that the event was identified by the Keyboard Wake-Up Detector. This bit is set only if the Keyboard Wake-Up Detector is in the "Power Management Keys" mode. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: The "PM Key 3" Key was pressed on the Keyboard.
4	**KBD_EVT2_STS (Keyboard Event 2 Status)** This bit indicates that "PM Key 2" was pressed and that the event was identified by the Keyboard Wake-Up Detector. This bit is set only if the Keyboard Wake-Up Detector is in the "Power Management Keys" mode. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: The "PM Key 2" Key was pressed on the Keyboard.
3	**KBD_EVT1_STS (Keyboard Event 1 Status)** This bit indicates that a keyboard event occurred and was identified by the Keyboard Wake-Up Detector. The event type depends on the selected operating mode for the Keyboard Wake-Up Detector. Pressing any key mode. Pressing a sequence of keys in the "password" mode. Pressing the "PM KEY 1" in the "Power Management Keys" mode. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: A keyboard event occurred.
2	**MS_EVT_STS (Mouse Event Status)** This bit indicates that a mouse event occurred and was identified by the Mouse Wake-Up Detector. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: A mouse event occurred.
1	**RI2_EVT_STS (RI2# Event Status)** This bit indicates that an activation of the Ring Indicator signal was received at Serial Port 2. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An activation of the Ring Indicator signal was received at the Serial Port 2.
0	**RI1_EVT_STS (RI1# Event Status)** This bit indicates that an activation of the Ring Indicator signal was received at Serial Port 1. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An activation of the Ring Indicator signal was received at the Serial Port 1.

9.4.2.10 General Purpose 1 Status 3 Register (GPE1_STS_3)

This register, containing bits 24-31 of the GPE1_STS register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the "Sticky status bit" definition (the bit is set by the HIGH level of the hardware signal and is only cleared by software writing "1" to it) in the ACPI Specification.

Bit	Description
7	**SW_OFF_STS (Software OFF Event Status)** This bit indicates that the software wrote a "1" to the SW_OFF_CTL bit in the SWC_CTL register to request a VCC power off sequence. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: "1" was written to the SW_OFF_CTL bit in the SWC_CTL register.
6	**SW_ON_STS (Software ON Event Status)** This bit indicates that the software wrote a "1" to the SW_OFF_CTL bit in the SWC_CTL register to request a VCC power on sequence when the VCC power is off. The SW_ON_STS bit can be written only through the Serial Bus. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: "1" was written to the SW_ON_CTL bit in the SWC_CTL register.
5	**Reserved**
4	**MOD_IRQ_STS (Module IRQ Event Status)** This bit indicates that an IRQ was generated by one of the legacy modules (FDC, Parallel Port, Serial Port 1 and 2). For legacy modules IRQ, this bit is set only if the IRQ is enabled for wake-up (bit 4 of the standard configuration register at index 70h) and the related module is active. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An enable IRQ, from the legacy module.
3	**MS_IRQ_STS (Mouse IRQ Event Status)** This bit indicates that an IRQ was generated by the mouse interface section of the KBC module. This bit is set only if the IRQ is enabled for wake-up (bit4 of the mouse logical device configuration register at index 70h) and the KBC module is active. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An enabled IRQ, from the mouse interface section of the active KBC module.
2	**KBD_IRQ_STS (Keyboard IRQ Event Status)** This bit indicates that an IRQ was generated by the keyboard interface section of the KBC module. This bit is set only if the IRQ is enabled for wake-up (bit 4 of the mouse logical device configuration register at index 70h) and the KBC module is active. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An enabled IRQ, from the keyboard interface section of the KBC module is active.
1	**P12_EVT_STS (Port P12 Event Status)** This bit indicates that an active signal was generated by the KBC module, at the P12 pin. This bit is set only if the KBC module is active. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An active high signal at the P12 pin was generated by the KBC module.
0	**RTC_EVT_STS (RTC Wake-up Alarm Event Status)** This bit indicates that an enabled RTC alarm has occurred. This bit is similar to the RTC_STS bit in the PM1b_STS_HIGH register. Writing "1" will clear this bit; writing "0" will be ignored. 0: Inactive since last cleared (default). 1: An RTC Wake-up alarm has occurred.

9.4.2.11 General Purpose 1 Enable 0 Register (GPE1_EN_0)

This register, containing bits 0-7 of the GPE1_EN register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the “Enable bit” definition (the bit is read/write by software) in the ACPI Specification.

Bit	Description
7	**GPIOW17_EN (GPIOW17 Event Enable).** This bit enables an active at pin 7 of the GPIOW set 1 to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event.
6-0	**GPIOW16_EN to GPIOW10_EN (GPIOW16-10 Event Enable)** These bits are the same as above for pins 6-0 of the GPIOW set 1.

9.4.2.12 General Purpose 1 Enable 1 Register (GPE1_EN_1)

This register, containing bits 8-15 of the GPE1_EN register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the “Enable bit” definition (the bit is read/write by software) in the ACPI Specification.

Bit	Description
7	**GPIOW47_EN (GPIOW47 Event Enable)** This bit enables an active at pin 7 of the GPIOW set 4 to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event.
6-0	**GPIOW46_EN to GPIOW40_EN (GPIOW46-40 Event Enable)** These bits are the same as above for pins 6-0 of the GPIOW set 4.

9.4.2.13 General Purpose 1 Enable 2 Register (GPE1_EN_2)

This register, containing bits 16-23 of the GPE1_EN register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the "Enable bit" definition (the bit is read/write by software) in the ACPI Specification.

Bit	Description
7	**PBT_EVT_EN (Power Button Event Enable)** This bit enables Power button pressing to generate a power management event (PWUREQ#). This bit is similar to the PWRBTN_EN bit in the PM1b_EN_HIGH register. It should be enabled only if the system does not support the PM1b_EVT register block. 0: Disable event (default). 1: Enable event from power button pressing.
6	**SBT_EVT_EN (Sleep Button Event Enable)** This bit enables Sleep button pressing to generate a power management event (PWUREQ#). This bit is similar to the SLPBTN_EN bit in the PM1b_EN_HIGH register. It should be enabled only if the system does not support the PM1b_EVT register block. 0: Disable event (default). 1: Enable event from sleep button pressing.
5	**KBD_EVT3_EN (Keyboard Event 3 Enable)** This bit enables the event of pressing "PM Key 3" (on the Keyboard) to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event from pressing the "PM Key 3" on the Keyboard.
4	**KBD_EVT2_EN (Keyboard Event 2 Enable)** This bit enables the event of pressing "PM Key 2" (on the Keyboard) to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event from pressing the "PM Key 2" on the Keyboard.
3	**KBD_EVT1_EN (Keyboard Event 1 Enable)** This bit enables the event of pressing any key, Key sequence, or "PM Key 1" (on the Keyboard) to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event from pressing the any key, key sequence, or "PM Key 1" on the Keyboard.
2	**MS_EVT_EN (Mouse Event Enable)** This bit enables a mouse event, identified by the Mouse Wake- Up Detector to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable the mouse event identified by the Mouse Wake-Up Detector.
1	**RI2_EVT_EN (RI2# Event Enable)** This bit enables an activation of the Ring Indicator signal, which was received at Serial Port 2, to generate a power management event (PWUREQ#). This bit indicates that an activation of the Ring Indicator signal was received at Serial Port 1. 0: Disable event (default). 1: Enable the Ring Indicator event received at the serial port 2.
0	**RI1_EVT_EN (RI1# Event Enable)** This bit enables an activation of the Ring Indicator signal, which was received at Serial Port 1, to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable the Ring Indicator event received at the serial port 1.

9.4.2.14 General Purpose 1 Enable 3 Register (GPE1_EN_3)

This register, containing bits 24-31 of the GPE1_EN register, belongs to the General Purpose Event 1 Group of the ACPI fixed-feature space registers. The status bits behave according to the "Enable bit" definition (the bit is read/write by software) in the ACPI Specification.

Bit	Description
7	**SW_OFF_EN (Software OFF Event Enable).** This bit enables the event of the software writing a "1" to the SW_OFF_CTL bit in the SWC_CTL register to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event if the software writing a "1" to the SW_OFF_CTL bit in the SWC_CTL register.
6	**SW_ON_EN (Software ON Event Enable).** This bit enables the event of the software writing a "1" to the SW_ON_CTL bit in the SWC_CTL register to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event if the software writing a "1" to the SW_ON_CTL bit in the SWC_CTL register.
5	**Reserved**
4	**MOD_IRQ_EN (Module IRQ Event Enable)** This bit enables an active IRQ from one of the legacy modules to generate a power management event (PWUREQ#) 0: Disable event (default). 1: Enable event by an active IRQ from one of the legacy modules.
3	**MS_IRQ_EN (Mouse IRQ Event Enable)** This bit enables an active IRQ generated by the mouse interface section of the KBC module to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event from an IRQ generated by the mouse interface section of the KBC module.
2	**KBD_IRQ_EN (Keyboard IRQ Event Enable)** This bit enables an active IRQ generated by the keyboard interface section of the KBC module to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event from an IRQ generated by the keyboard interface section of the KBC module.
1	**P12_EVT_EN (Port P12 Event Enable)** This bit enables an event by an active high signal generated at the P12 pin to generate a power management event (PWUREQ#). 0: Disable event (default). 1: Enable event from an active high signal generated at the P12 pin.
0	**RTC_EVT_EN (RTC Alarm Event Enable)** This bit enables an RTC alarm to generate a power management event (PWUREQ#). This bit is similar to the RTC_EN bit in the PM1b_EN_HIGH register. It should be enabled only if the system does not support the PM1b_EVT register block. 0: Disable event (default). 1: Enable event from RTC alarm.

9.5 Real Time Clock (RTC)

9.5.1 General Description

The RTC device incorporates a timer module that includes a time of day clock and a multi-century calendar, alarm facilities, and three programmable timer interrupts, 242-bytes RAM contents which can be backup by the external battery during the power loss, and the power management circuitry which can reduce the standby current when the power is supplied by the VBAT.

The RTC's alarm and calendar registers support both BCD and binary modes, and both 24- and 12-hour formats. There is only an interrupt line requested to handle three interrupt conditions, the alarm interrupt, the periodic interrupt, and the update-ended interrupt. The RTC also incorporates a power switching circuitry which can detect the absence of VSB power and switch the power core of the whole block (including RAM block) to VBAT, and a power-saving circuitry which can reduce the power consumption when the power is switched to VBAT.

The RAM contents are divided into two parts: lower bank (114 bytes) and upper bank (128 bytes). Access to the RAM may be selectively locked. See Section 8.12.8 "RTC Special Configuration Register" for details.

9.5.2 Registers

9.5.2.1 Partition

The RTC device has three battery-backed register banks which can be accessed by two sets of address ports. Battery-backup power enables all these information retention during system power down.

- **Bank 0**: The first 14 bytes of this bank store time and alarm data and contain control registers. The next 114 bytes are general purpose RAM. This bank (00h~7Fh) can be accessed through the addresses RTC Primary Base Address (index) and RTC Primary Base Address +1 (data). The RTC Primary Base Address with default 70h can be reassigned in chip configuration registers.

- **Bank 1**: The total 128 bytes of this bank are another block of general purpose RAM. This bank (00h~7Fh) can be accessed through the addresses RTC Second Base Address (index) and RTC Second Base Address +1 (data). The RTC Second Base Address with default 72h can also be reassigned in chip configuration registers.

- **Bank 2**: The total 9 bytes of this bank include century reading and the second alarm registers. This bank (C0h~C8h) can be accessed through the addresses RTC Second Base Address (index) and RTC Second Base Address +1 (data). It shares with the Bank 1.

9.5.2.2 Register Description

Refer to Table 9-2, the Register Address Map of RTC Bank 0, to see 10 time registers and 4 control registers. To initialize the time, calendar and alarm A registers properly, the SET bit of CRB must be set to "1" to avoid the generation of the update cycle. After the time, calendar, and alarm registers are written, the SET bit must be set to 0 to enable the update cycle. When the time corresponds to the alarm time, the alarm will occur once per day. If the data in the hours-alarm register is between C0 to FF, the alarm will generate once per hour if the data in the minutes and seconds register corresponds to the data in the minutes-alarm and seconds-alarm registers. If both the data of hours-alarm and minutes-alarm registers are located between C0 to FF, the alarm will occur once per minute if the data in the seconds register corresponds to the one in the seconds-alarm register. If all data of the hours-alarm, minutes-alarm and seconds-alarm registers are located between C0 to FF, the alarm will generate once per second.

Table 9-2. RTC Register List, Bank 0 (Primary Address, default = 70h/71h)

Index	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours 12-hr mode	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours 24-hr mode	0-23	00-17	00-23
5	Hours Alarm 12-hr	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours Alarm 24-hr	0-23	00-17	00-23
6	Day of the week (Sunday=1)	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99
A	Control register A (CRA)	R/W * Bit 7 is read only		
B	Control register B (CRB)	R/W * Bit 0 is read only		
C	Control register C (CRC)	Read only		
D	Control register D (CRD)	Read only		
E-7F	General Purpose	R/W 114 byte		

Table 9-3. RTC Register List, Bank 1 (Second Address, default = 72h/73h)

Index	Function	Description
0-7F	General Purpose	R/W 128 bytes

Table 9-4. RTC Register List, Bank 2 (Second Address, default = 72h/73h)

Index	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
C0h	Century	0-99	00-63	00-99
C1h	Seconds Wake-up	0-59	00-3B	00-59
C2h	Minutes Wake-up	0-59	00-3B	00-59
C3h	Hours Wake-up (12-hr mode)	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours Wake-up (24-hr mode)	0-23	00-17	00-23
C4h	Day of the Week Wake-up	1-7	01-07	01-07
C5h	Date of the Month Wake-up	1-31	01-1F	01-31
C6h	Month Wake-up	1-12	01-0C	01-12
C7h	Year Wake-up	0-99	00-63	00-99
C8h	Century Wake-up	0-99	00-63	00-99
C9h	RTC Wake-up status	--	--	--

9.5.2.2.1 RTC Control Register A (CRA), Bank 0

Bit	R/W	Description
7	R/W	**UIP (Update In Progress)** UIP can be cleared by SET=1, but cannot be modified by LRESET#. 1: Update cycle is in progress or will occur soon. 0: Update cycle is not in progress and will not occur for at least 244μs.
6-4	R/W	**DV2-0 (Divider Chain Control)** Select the conditions of divider chain, and these three bits are not affected by RESET. **DV2-0 Mode** 000b Oscillator disabled 001b Oscillator disabled 010b Normal operation, Oscillator on and divider chain enabled 10Xb Test 11Xb Oscillator on and divider chain disabled
3-0	R/W	**RS3-0 (Periodic Interrupt Rates Select)** Select one of fifteen states on the divider or disable the divider output, and these four bits are not affected by LRESET#. **RS3-0 Periodic Rate of Interrupt** 0000b None 0001b 3.90625 ms 0010b 7.8125 ms 0011b 122.070 μs 0100b 244.141 μs 0101b 488.281 μs 0110b 976.562 μs 0111b 1.953125 ms 1000b 3.90635 ms 1001b 7.8125 ms 1010b 15.625 ms 1011b 31.25 ms 1100b 62.5 ms 1101b 125 ms 1110b 250 ms 1111b 500 ms

9.5.2.2.2 RTC Control Register B (CRB), Bank 0

Bit	R/W	Description
7	R/W	**SET** SET cannot be modified by Master Reset or any internal functions. 0: Execute update cycle once per second. 1: Update cycle is disabled and the initial time and calendar bytes can be written.
6	R/W	**PIE (Periodic Interrupt Enable)** PIE can be cleared by Master Reset and cannot be modified by any internal functions. The generation rate of the Periodic Interrupt is determined by DS3-0 in CRA. 0: Disable the generation of the Periodic Interrupt. 1: Enable the generation of the Periodic Interrupt.
5	R/W	**AIE (Alarm Interrupt Enable)** AIE can be cleared by Master Reset and cannot be modified by any internal functions. The Alarm Interrupt is generated immediately after a time update which the Seconds, Minutes, Hours, and Day-of-month time is equal to their respective alarm counterparts. 0: Disable the generation of the Alarm Interrupt. 1: Enable the generation of the Alarm Interrupt.
4	R/W	**UIE (Update-ended Interrupt Enable)** This bit will be cleared by Master Reset. This interrupt is generated at the time when an update occurs. 0: Disable the generation of the Update-ended Interrupt. 1: Enable the generation of the Update-ended Interrupt.
3	R/W	**Unused** The original definition of 146818 is “Square Wave Enable”, but is not supported by the RTC of this chip. Writing to this bit has no effects.
2	R/W	**DM (Data Mode)** This bit selects the data mode and is not affected by Master Reset. 0: Data in the time and calendar registers are in BCD format. 1: Data in the time and calendar registers are in binary format.
1	R/W	**24/12 (24- or 12-hour)** This bit selects the hour format, and it is not affected by Master Reset. 0: 12-hour format. 1: 24-hour format.
0	R/W	**DSE (Daylight Saving Enable)** This bit selects the hour format, and it is not affected by Master Reset. In spring, time advances from 1:59:59 to 3:00:00 on the first Sunday in April. In fall, time returns from 1:59:59 to 1:00:00 on the last Sunday in October. 0: Disable daylight saving mode. 1: Enable daylight saving mode.

9.5.2.2.3 RTC Control Register C (CRC), Bank 0

The RTC supports three interrupt events: Periodic Interrupt, Alarm Interrupt, and Update-ended Interrupt. When an interrupt occurs, the related flag bit is set to "1" in CRC. These flag bits are set despite the status of the corresponding enable bits in CRB. Only when the interrupt enable bit is set and the corresponding interrupt flag bit is set, the IRQF bit in CRC will be activated and IRQ of RTC is pulled low. The state of the interrupt flag bits and RTC IRQ will not be cleared until the read cycle of CRC is completed.

Bit	R/W	Description
7	RO	**IRQF (Interrupt Request Flag)** This bit is inverse of the value on the IRQ output signal of the RTC module. 0: RTC IRQ is inactive. 1: RTC IRQ is active when both PF and PIE are 1; or both AF and AIE are 1; or both UF and UIE are 1.
6	RO	**PF (Periodic Interrupt Flag)** PF can be cleared by Master Reset and reading this register. 0: No transition occurred on the selected tap since last read. 1: At least a transition occurred on the selected tap since last read.
5	RO	**AF (Alarm Interrupt Flag)** AF can be cleared by Master Reset and reading this register. 0: No alarm was detected since last read. 1: An alarm condition was detected.
4	RO	**UF (Update-ended Interrupt Flag)** This bit will be cleared by Master Reset and reading this register. 0: Disable the generation of the Update-ended Interrupt. 1: Enable the generation of the Update-ended Interrupt.
3-0	-	**Reserved**

9.5.2.2.4 RTC Control Register D (CRD), Bank 0

Bit	R/W	Description
7	RO	**VRT (Valid RAM and Time)** This bit is affected by Master Reset, and can only be set if the VBAT voltage is not too low when CRD is read. 0: The voltage of VBAT is too low. 1: The contents of RTC and RAM are valid.
6	-	**Reserved**
5-0	R/W	**DATE_ALARM (Date Alarm Bits)** These six bits, which are not affected by Master Reset, store the date of month alarm value. If set to 000000b, the Date Alarm is "Don't care". The legal values for these six bits are 01 to 31 in BCD format and 01 to 1F in binary format.

9.5.2.2.5 The Function of Wake-up Alarm, Bank 2

Wake-up Alarm registers are used to set the wake up alarm time. When the wake up alarm time specified is up while the hardware will set RTC_EVT_STS of GPE1_STS_2. If the related enabled bits are set, the Wake-up Alarm event may cause activation of PSON#, PWUREQ#, SIOSMI#, and SWC IRQ.

When all of the eight Wake-up Alarm registers (with addresses from C1h to C8h) are set in an appropriate time, the alarm signal will occur at the specified time. The Wake-up Alarm registers can also serve to set bits[7:6] of one or more Wake-up Alarm registers to "11" to create a "Don't Care" situation. Take the Hours Wake-up Alarm register for example. The alarm will be generated once per hour if the first two bits of Hour Wake-up Alarm register are set to "11."

An "OR" function is provided for Day of Week Wake-up Alarm (C4h) and Date of Month Wake-up Alarm (C5h) registers. The alarm will be generated once every day if bits[7:6] of the above two registers are set to "11," which will result in "Don't Care" situation. The alarm is generated on the day of month when the Date of Month Wake-up Alarm (C5h) is written with appropriate data and the Day of Week Wake-up Alarm (C4h) is "Don't Care." (Bits[7:6] are set to "11.") The alarm is generated on the day of week if the Date of Month Wake-up Alarm (C5h) is "Don't Care," (Bits[7:6] are set to "11."), and the Day of Week Wake-up Alarm (C4h) is written with appropriate data. When both of the two registers are written with appropriate data except "Don't Care," the alarm will be generated on either the day of week or the day of month.

9.6 Floppy Disk Controller (FDC)

9.6.1 Introduction

The Floppy Disk Controller provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in PC/AT mode and supports 3-Mode type drives. Additionally, the FDC is software compatible with the 82077.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives and DMA modes, and indicate errors in the data or operation of the FDC/FDD.

The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution and Result. Not all commands utilize all these three phases.

9.6.2 Reset

The IT8780F device implements both software and hardware reset options for the FDC. Either type of the resets will reset the FDC, terminating all operations and placing the FDC into an idle state. A reset during a write to the disk will corrupt the data and the corresponding CRC.

9.6.3 Hardware Reset (LRESET# Pin)

When the FDC receives a LRESET# signal, all registers of the FDC core are cleared (except those programmed by the SPECIFY command). To exit the reset state, the host must clear the DOR bit.

9.6.4 Software Reset (DOR Reset and DSR Reset)

When the reset bit in the DOR or the DSR is set, all registers of the FDC core are cleared. A reset performed by setting the reset bit in the DOR has higher priority over a reset performed by setting the reset bit in the DSR. In addition, to exit the reset state, the DSR bit is self-clearing, while the host must clear the DOR bit.

9.6.5 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is used to separate the encoded clock from the data pulses.

9.6.6 Write Precompensation

Write precompensation is a method that can be used to adjust the effects of bit shift on data as it is written to the disk. It is harder for the data separator to read data that has been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions.
The FDC permits the selection of writes precompensation via the Data Rate Select Register (DSR) bits 2 through 4.

9.6.7 Data Rate Selection

Selecting one of the four possible data rates for the attached floppy disks is accomplished by setting the Diskette Control Register (DCR) or Data Rate Select Register (DSR) bits to 0 and 1. The data rate is determined by the last value that is written to either the DCR or the DSR. When the data rate is set, the data separator clock is scaled appropriately.

9.6.8 Status, Data and Control Registers

9.6.8.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a **read/write** register. It controls drive selection and motor enables as well as a software reset bit and DMA enable. The I/O interface reset may be used at any time to clear the DOR's contents.

Table 9-5. Digital Output Register (DOR)

Bit	R/W	Description
7-6	R/W	**Reserved**
5	R/W	**MOTBEN (Drive B Motor Enable)** 0: Disable Drive B motor. 1: Enable Drive B motor.
4	R/W	**MOTAEN (Drive A Motor Enable)** 0: Disable Drive A motor. 1: Enable Drive A motor.
3	R/W	**DMAEN (Disk Interrupt and DMA Enable)** 0: Disable disk interrupt and DMA (DRQx, DACKx#, TC and INTx). 1: Enable disk interrupt and DMA.
2	R/W	**RESET# (FDC Function Reset)** 0: Reset FDC function. 1: Clear reset of FDC function. This reset does not affect the DSR, DCR or DOR.
1	-	**Reserved**
0	R/W	**DVSEL (Drive Selection)** 0: Select Drive A. 1: Select Drive B.

9.6.8.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register and is included for 82077 software compatibility. The contents of this register are not used internal to the device.

Table 9-6. Tape Drive Register (TDR)

Bit	R/W	Description
7-2	-	**Undefined**
1-0	R/W	**TP_SEL[1:0] (Tape Drive Selection)** TP_SEL[1:0] : Drive selected. 00: None 01: 1 10: 2 11: 3

9.6.8.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register. It indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from the Data register, except when in DMA mode.

Table 9-7. Main Status Register (MSR)

Bit	R/W	Description
7	RO	**RQM (FDC Request for Master)** 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and the host can transfer data.
6	RO	**DIO (Data I/O Direction)** Indicates the direction of data transfer once a RQM has been set. 0: Write. 1: Read.
5	RO	**NDM (Non-DMA Mode)** This bit selects Non-DMA mode of operation. 0: DMA mode selected. 1: Non-DMA mode selected. This mode is selected via the SPECIFY command during the Execution phase of a command.
4	RO	**CB (Diskette Control Busy)** Indicates whether a command is in progress (the FDD is busy) or not. 0: A command has been executed and the end of the Result phase has been reached. 1: A command is being executed.
3-2	-	**Reserved**
1	RO	**DBB (Drive B Busy)** Indicates whether Drive B is in the SEEK portion of a command. 0: Not busy. 1: Busy.
0		**DAB (Drive A Busy)** Indicates whether Drive A is in the SEEK portion of a command. 0: Not busy. 1: Busy.

9.6.8.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register. It is used to determine the data rate, amount of write precompensation, power down mode, and software reset. The data rate of the floppy disk controller is the latest write of either the DSR or DCR. The DSR is unaffected by a software reset. The DSR can be set to 02h by a hardware reset. The "02h" represents the default precompensation, and 250 Kbps indicates the data transfer rate.

Table 9-8. Data Rate Select Register (DSR)

<table>
<tr><th>Bit</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>WO</td><td>S/W RESET (Software Reset)
It is active high and shares the same function with the RESET# of the DOR except that this bit is self-clearing.</td></tr>
<tr><td>6</td><td>WO</td><td>POWE DOWN (Power Down)
When this bit is written with a "1", the floppy controller is put into manual low power mode. The clocks of the floppy controller and data separator circuits will be turned off until a software reset or the Data Register or Main Status Register is accessed.</td></tr>
<tr><td>5</td><td>-</td><td>Undefined</td></tr>
<tr><td>4-2</td><td>WO</td><td>PRE-COMP 2-0 (Precompensation Select)
These three bits are used to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default starting track number, which can be changed by the CONFIGURE command for precompensation.

<table>
<tr><th>PRE_COMP</th><th>Precompensation Delay</th></tr>
<tr><td>111</td><td>0.0 ns</td></tr>
<tr><td>001</td><td>41.7 ns</td></tr>
<tr><td>010</td><td>83.3 ns</td></tr>
<tr><td>011</td><td>125.0 ns</td></tr>
<tr><td>100</td><td>166.7 ns</td></tr>
<tr><td>101</td><td>208.3 ns</td></tr>
<tr><td>110</td><td>250.0 ns</td></tr>
<tr><td>000</td><td>Default</td></tr>
</table>

Default Precompensation Delays
<table>
<tr><th>Data Rate</th><th>Precompensation Delay</th></tr>
<tr><td>1 Mbps</td><td>41.7 ns</td></tr>
<tr><td>500 Kbps</td><td>125.0 ns</td></tr>
<tr><td>300 Kbps</td><td>125.0 ns</td></tr>
<tr><td>250 Kbps</td><td>125.0 ns</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>WO</td><td>DRATE1-0 (Data Rate Select)
<table>
<tr><th>Bits 1-0</th><th>Data Transfer Rate</th></tr>
<tr><td>00</td><td>500 Kbps</td></tr>
<tr><td>01</td><td>300 Kbps</td></tr>
<tr><td>10</td><td>250 Kbps (default)</td></tr>
<tr><td>11</td><td>1 Mbps</td></tr>
</table></td></tr>
</table>

9.6.8.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register. It transfers command information, diskette drive status information, and the result phase status between the host and FDC. The FIFO consists of several registers in a stack. Only one register in the stack is permitted to transfer information or status to the data bus at a time.

Table 9-9. Data Register (FIFO)

Bit	R/W	Description
7-0	R/W	**Data** Command information, diskette drive status, or result phase status data.

9.6.8.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register and shares this address with the Diskette Control Register (DCR).

Table 9-10. Digital Input Register (DIR)

Bit	R/W	Description
7	R/W	**DSKCHG (Diskette Change)** Indicates the inverting value of the bit monitored from the input of the Floppy Disk Change pin (DSKCHG#).
6-0	-	**Undefined.**

9.6.8.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This register is **write only** and shares this address with the Digital Input Register (DIR). The DCR register controls the data transfer rate for the FDC.

Table 9-11. Diskette Control Register (DCR)

Bit	R/W	Description
7-2	-	**Reserved**. Always 0.
1-0	WO	**DRATE (Data Rate Select)** **Bits 1-0** **Data Transfer Rate** 00 500 Kbps 01 300 Kbps 10 250 Kbps 11 1 Mbps

9.6.9 Controller Phases

The FDC handles data transfers and control commands in three phases: Command, Execution and Result. Not all commands utilize these three phases.

9.6.9.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that MSR bit 7 (RQM) = 1 and MSR bit 6 (DIO) = 0, indicating the FDC is ready to receive data. For each command, a defined set of command code and parameter bytes must be transferred to the FDC in a given order. See section 9.6.11 and 9.6.12 for details on the various commands. RQM is set false (0) after each byte-Read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

9.6.9.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfers occur between the host and FDC. The SPECIFY command indicates whether this data transfer occurs in DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

9.6.9.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. The MSR bit 7 (RQM) and MSR bit 6 (DIO) must equal to 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

9.6.9.4 Result Phase Status Registers

For commands that contain a Result phase, these **read only** registers indicate the status of the latest executed command.

Table 9-12. Status Register 0 (ST0)

Bit	R/W	Description
7-6	RO	**IC (Interrupt Code)** 00: Execution of the command has been completed correctly. 01: Execution of the command began, but failed to complete successfully. 10: INVALID command. 11: Execution of the command was not completed correctly due to a polling error.
5	RO	**SE (Seek End)** The FDC executed a SEEK or RE-CALIBRATE command.
4	RO	**EC (Equipment Check)** The TRK0# pin was not set after a RE-CALIBRATE command was issued.
3	RO	**NU (Not Used)**
2	RO	**H (Head Address)** The current head address.
1	RO	**DSB (Drive B Select)** Drive B selected.
0	RO	**DSA (Drive A Select)** Drive A selected.

Table 9-13. Status Register 1 (ST1)

Bit	R/W	Description
7	RO	**EN (End of Cylinder)** Indicates the FDC attempted to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	RO	**NU (Not Used)**
5	RO	**DE (Data Error)** A CRC error occurred in either the ID field or the data field of a sector.
4	RO	**OR (Overrun/ Underrun)** An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by the CPU or DMA within the required time interval.
3	RO	**NU (Not Used)**
2	RO	**ND (No Data)** No data are available to the FDC when either of the following conditions is met: The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are executed. While executing a READ ID command, an error occurs upon reading the ID field. While executing a READ A TRACK command, the FDC cannot find the starting sector.
1	RO	**NW (Not Writeable)** Set when a WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	RO	**MA (Missing Address Mark)** This flag bit is set when either of the following conditions is met: The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track The FDC cannot find any ID addresses on the specified track after two index pulses are detected from the INDEX# pin.

Table 9-14. Status Register 2 (ST2)

Bit	R/W	Description
7	RO	**NU (Not Used)**
6	RO	**CM (Control Mark)** This flag bit is set when either of the following conditions is met: The FDC finds a Deleted Data Address Mark during a READ DATA command. The FDC finds a Data Address Mark during a READ DELETED DATA command.
5	RO	**DD (Data Error in Data Field)** This flag bit is set when a CRC error is found in the data field.
4	RO	**WC (Wrong Cylinder)** This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	RO	**SH (Scan Equal Hit)** This flag bit is set when the condition of "equal" is satisfied during a SCAN command.
2	RO	**SN (Scan Not Satisfied)** This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.
1	RO	**BC (Bad Cylinder)** This flag bit is set when the track address equals to “FFh” and is different from the track address in the FDC.
0	RO	**MD (Missing Data Address Mark)** This flag bit is set when the FDC cannot find a Data Address Mark or Deleted Data Address Mark.

Table 9-15. Status Register 3 (ST3)

Bit	R/W	Description
7	RO	**FT (Fault)** Indicates the current status of the Fault signal from the FDD.
6	RO	**WP (Write Protect)** Indicates the current status of the Write Protect signal from the FDD.
5	RO	**RDY (Ready)** Indicates the current status of the Ready signal from the FDD.
4	RO	**TK0 (Track 0)** Indicates the current status of the Track 0 signal from the FDD.
3	RO	**TS (Two Side)** Indicates the current status of the Two Side signal from the FDD.
2	RO	**HD (Head Address)** Indicates the current status of the Head Select signal to the FDD.
1-0	RO	**US1, US0 (Unit Select)** Indicates the current status of the Unit Select signals to the FDD.

9.6.10 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte, which contains the op-code, and a series of additional bytes, which contain the required set of parameters and results. The descriptions use a common set of parameter byte symbols, which are presented in Table 9-16. The FDC commands may be executed whenever the FDC is in the Command phase. The FDC checks to see that the first byte is a valid command and, if so, proceeds. An interrupt is issued if it is not a valid command.

Table 9-16. Command Set Symbol Descriptions

Symbol	Name	Description
C	Cylinder Number	The current/selected cylinder (track) number: 0 – 255.
D	Data	The data pattern to be written into a sector.
DC3–DC0	Drive Configuration Bit3-0	Designate which drives are perpendicular drives on the PERPENDICULAR MODE command.
DIR	Direction Control	Read/Write Head Step Direction Control. 0 = Step Out; 1 = Step In.
DR0, DR1	Disk Drive Select	The selected drive number: 0 or 1.
DTL	Data Length	When N is defined as 00h, DTL designates the number of data bytes which users are going to read out or write into the Sector. When N is not 00h, DTL is undefined.
DFIFO	Disable FIFO	A “1” will disable the FIFO (default). A “0” will enable the FIFO.
EC	Enable Count	If EC=1, DTL of VERIFY command will be SC.
EIS	Enable Implied Seek	If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	End of Track	The final sector number on a cylinder. During a READ or WRITE operation, the FDC stops data transfer after the sector number is equal to EOT.
GAP2	Gap 2 Length	By PERPENDICULAR MODE command, this parameter changes Gap 2 length in the format.
GPL	Gap Length	The length of Gap 3. During a FORMAT command, it determines the size of Gap 3.
H	Head Address	The Head number 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	Head	The selected Head number 0 or 1. It also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	Head Load Time	The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).
LOCK		If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.
MFM	FM or MFM Mode	If MFM is low, FM Mode (single density) is selected. If MFM is high, MFM Mode (double density) is selected.
MT	Multi-Track	If MT is high, a Multi-Track operation is to be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation on the last sector on side 0.
N	Number	The number of data bytes written into a sector, where: 00 = 128 bytes (PC standard) 01 = 256 bytes 02 = 512 bytes … 07 = 16 Kbytes
NCN	New Cylinder Number	A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	Non-DMA Mode	When ND is high, the FDC operates in the Non-DMA Mode.

Table 9-16. Command Set Symbol Descriptions [cont'd]

Symbol	Name	Description
OW	Overwrite	If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.
PCN	Present Cylinder Number	The cylinder number at the completion of a SENSE INTERRUPT STATUS command. Position of Head at present time.
POLLD	Polling Disable	If POLLD=1, the internal polling routine is disabled.
PRETRK	Precompensation Starting Track Number	Programmable from track 0 –255.
R	Record	The sector number, which will be read or written.
RCN	Relative Cylinder Number	To determine the relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.
SC		The number of sectors per cylinder.
SK	Skip	If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Otherwise, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	Step Rate Time	The Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives (F=1 ms, E=2 ms, etc.).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0–3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (selected by $A_0 = 0$). ST0–3 may be read only after a command has been executed and contain information associated with that particular command.
STP		If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 9-17. Command Set Summary

READ DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	MT	MFM	SK	0	0	1	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

READ DELETED DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	MT	MFM	SK	0	1	1	0	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

READ A TRACK										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	0	MFM	0	0	0	0	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and main system cylinder's contents from index hole to EOT
Result	RO	ST0								Status information after the command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

WRITE DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	MT	MFM	0	0	0	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and main system
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

WRITE DELETED DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	0	0	1	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and main system
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

FORMAT A TRACK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	MFM	0	0	1	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	N								Bytes/Sector
	WO	SC								Sectors/Cylinder
	WO	GPL								Gap 3
	WO	D								Filler Byte
Execution For each Sector Repeat:	WO	C								Input Sector Parameters per-sector
	WO	H								
	WO	R								
	WO	N								
										FDC formats an entire cylinder
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	Undefined								
	RO	Undefined								
	RO	Undefined								
	RO	Undefined								

SCAN EQUAL										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	MT	MFM	SK	1	0	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

SCAN LOW OR EQUAL										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	MT	MFM	SK	1	1	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

SCAN HIGH OR EQUAL										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	1	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

VERIFY										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	0	1	1	0	Command Codes
	WO	EC	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL/SC								
Execution										No data transfer takes place
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	R	H								
	RO	R								
	RO	N								

READ ID									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	MFM	0	0	1	0	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information during execution phase
	RO	H								
	RO	R								
	RO	N								

CONFIGURE									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	0	0	1	0	0	1	1	Configure Information
	WO	0	0	0	0	0	0	0	0	
	WO	0	EIS	DFIFO	POLLD	FIFOTHR				
		PRETRK								
Execution										

RE-CALIBRATE									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	0	0	0	0	1	1	1	Command Codes
	WO	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	0	0	0	1	1	1	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	NCN								
Execution										Head is positioned over proper cylinder on diskette

RELATIVE SEEK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	1	DIR	0	0	1	1	1	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	RCN								
Execution										Head is stepped in or out a programmable number of tracks

DUMPREG										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	1	1	1	0	Command Codes
Execution										Registers placed in FIFO
Result	RO	PCN-Drive 0								
	RO	PCN-Drive 1								
	RO	PCN-Drive 2								
	RO	PCN-Drive 3								
	RO	SRT				HUT				
	RO	HLT							ND	
	RO	SC/EOT								
	RO	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG	
	RO	0	EIS	DFIFO	POLLD	FIFOTHR				
	RO	PRETRK								

LOCK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	LOCK	0	0	1	0	1	0	0	Command Codes
Result	RO	0	0	0	LOCK	0	0	0	0	

VERSION									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	1	0	0	0	0	Command Codes
Result	RO	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	0	0	0	0	1	0	0	0	Command Codes
Result	RO	ST0								Status information at the end of each SEEK operation
	RO	PCN								

SENSE DRIVE STATUS										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	0	0	0	0	0	1	0	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
Result	RO	ST3								Status information about FDD

SPECIFY										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	0	0	0	0	0	0	1	1	Command Codes
	WO	SRT				HUT				
	WO	HLT							ND	

PERPENDICULAR MODE										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	0	0	0	1	0	0	1	0	Command Codes
	WO	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	WO	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into standby state)
Result	RO	ST0								ST0 = 80h

9.6.11 Data Transfer Commands

All data transfer commands utilize the same parameter bytes (except for FORMAT A TRACK command) and return the same result data bytes. The only difference between them is the five bits (bit 0–bit 4) of the first byte.

9.6.11.1 READ DATA

The READ DATA command contains nine command bytes that place the FDC into the Read Data mode. Each READ operation is initialized by a READ DATA command. The FDC locates the sector to be read by matching ID Address Marks and ID fields from the command with the information on the diskette. The FDC then transfers the data to the FIFO. When the data from the given sector have been read, the READ DATA command is completed and the sector address is automatically incremented by 1. The data from the next sector are read and transferred to the FIFO in the same manner. Such a continuous read function is called a "Multi-Sector Read Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops sending data but continues to read data from the current sector and checks the CRC bytes until the end of the sector is reached and the READ operation is completed.

The sector size is determined by the N parameter value as calculated in the equation below:

Sector Size = $2^{(7+N\ value)}$ bytes.

The DTL parameter determines the number of bytes to be transferred. Therefore, if N = 00h, setting the sector size to 128 and the DTL parameter value is less than this, the remaining bytes will be read and checked for CRC errors by the FDC. If this occurs in a WRITE operation, the remaining bytes will be filled with 0. If the sector size is not 128 (N > 00h), DTL should be set to FFh.

In addition to performing Multi-Sector Read operations, the FDC can also perform Multi-Track Read operations. When the MT parameter is set, the FDC can read both sides of a disk automatically.

The combination of N and MT parameter values determines the amount of data that can be transferred during either type of READ operation. Table 9-18 shows the maximum data transfer capacity and the final sector the FDC reads based on these parameters.

Table 9-18. Effects of MT and N Bits

MT	N	Maximum Data Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 on side 0 or side 1
1	1	256 X 52 = 13312	26 on side 1
0	2	512 X 15 = 7680	15 on side 0 or side 1
1	2	512 X 30 = 15360	15 on side 1
0	3	1024 X 8 = 8192	8 on side 0 or side 1
1	3	1024 X16 =16384	16 on side 1

9.6.11.2 READ DELETED DATA

The READ DELETED DATA command is the same as the READ DATA command, except that a Deleted Data Address Mark (as opposed to a Data Address Mark) is read at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.11.3 READ A TRACK

After receiving a pulse from the INDEX# pin, the READ A TRACK command reads the entire data field from each sector of the track as a continuous block. If any ID or Data Field CRC error is found, the FDC continues to read data from the track and indicates the errors at the end. Because the Multi-Track [and Skip] operation[s] is [are] not allowed under this command, the MT and SK bits should be low (0) during the command execution.

This command terminates normally when the number of sectors specified by EOT has not been read. However, if no ID Address Mark has been found by the second occurrence of the INDEX pulse, the FDC will set the IC code in the ST0 to 01 indicating an abnormal termination, and then finish the command.

9.6.11.4 WRITE DATA

The WRITE DATA command contains nine command bytes that place the FDC into the Write Data mode. Each WRITE operation is initialized by a WRITE DATA command. The FDC locates the sector to be written by reading ID fields and matching the sector address from the command with the information on the diskette. Then the FDC reads the data from the host via the FIFO and writes the data into the sector's data field. Finally, the FDC computes the CRC value, storing it in the CRC field and increments the sector number (stored in the R parameter) by 1. The next data field is written into the next sector in the same manner. Such a continuous write function is called a "Multi-Sector Write Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops writing data and fills the remaining data field with 0s. If a check of the CRC value indicates an error in the sector ID Field, the FDC will set the IC code in the ST0 to 01 and the DE bit in the ST1 to 1, indicating an abnormal termination, and then terminate the WRITE DATA command. The maximum data transfer capacity and the DTL, N, and MT parameters are the same as in the READ DATA command.

9.6.11.5 WRITE DELETED DATA

The WRITE DELETED DATA command is the same as the WRITE DATA command, except that a Deleted Data Address Mark (instead of a Data Address Mark) is written at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.11.6 FORMAT A TRACK

The FORMAT A TRACK command is used to format an entire track. Initialized by an INDEX pulse, it writes data to the Gaps, Address Marks, ID fields and Data fields according to the density mode selected (FM or MFM). The Gap and Data field values are controlled by the host-specified values programmed into N, SC, GPL, and D during the Command phase. The Data field is filled with the data byte specified by D. The four data bytes per sector (C, H, R and N) needed to fill the ID field are supplied by the host. The C, R, H and N values must be renewed for each new sector of a track. Only the R parameter value must be changed when a sector is formatted allowing the disk to be formatted with non-sequential sector addresses. These steps are repeated until a new INDEX pulse is received, at which point the FORMAT A TRACK command is terminated.

9.6.11.7 SCAN

The SCAN command allows the data read from the disk to be compared with the data sent from the system. There are three SCAN commands:

SCAN EQUAL Disk Data = System Data

SCAN HIGH OR EQUAL Disk Data ≥ System Data

SCAN LOW OR EQUAL Disk Data ≤ System Data

The SCAN command execution continues until the scan condition has been met, or when the EOT has been reached, or if TC is asserted. Read errors on the disk have the same error condition as the READ DATA command. If the SK bit is set, sectors with Deleted Data Address Marks are ignored. If all sectors read are skipped, the command terminates with the D3 bit of the ST2 being set. The Result phase of the command is shown below:

Table 9-19. SCAN Command Result

Command	Status Register		Condition
	D2	D3	
SCAN EQUAL	0	1	Disk = System
	1	0	Disk ≠ System
SCAN HIGH OR EQUAL	0	1	Disk = System
	0	0	Disk > System
	1	0	Disk < System
SCAN LOW OR EQUAL	0	1	Disk = System
	0	0	Disk < System
	1	0	Disk > System

9.6.11.8 VERIFY

The VERIFY command is used to read logical sectors containing a Normal Data Address Mark from the selected drive without transferring the data to the host. This command acts like a READ DATA command except that no data are transferred to the host. This command is designed for post-format or post write verification. Data are read from the disk, as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value. Because no data are transferred to the host, the TC (Terminal Count of DMA) cannot be used to terminate this command. An implicit TC will be issued to the FDC by setting the EC bit. This implicit TC will occur when the SC value has been decremented to 0. This command can also be terminated by clearing the EC bit and when the EOT value is equal to the final sector to be checked.

Table 9-20. VERIFY Command Result

MT	EC	SC/EOT	Termination Result
0	0	SC = DTL EOT ≤ # Sectors per side	No Error
0	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
0	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination
1	0	SC = DTL EOT > # Sectors per side	No Error
1	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
1	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination

9.6.12 Control Commands

The control commands do not transfer any data. Instead, these commands are used to monitor and manage the data transfer. Three of the Control commands generate an interrupt when READ ID, RE-CALIBRATE and SEEK are finished. It is strongly recommended that a SENSE INTERRUPT STATUS command be issued after these commands capture their valuable interrupt information. The RE-CALIBRATE, SEEK and SPECIFY commands do not return any result bytes.

9.6.12.1 READ ID

The READ ID command is used to find the actual recording head position. It stores the first readable ID field value into the FDC registers. If the FDC cannot find an ID Address Mark by the time a second INDEX pulse is received, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

9.6.12.2 CONFIGURE

The CONFIGURE command determines some special operation modes of the controller. It does not need to be issued if the default values of the controller meet the system requirements.

EIS: Enable Implied Seeks. A SEEK operation is performed before a READ, WRITE, SCAN or VERIFY command.
0 = Disabled (default).
1 = Enabled.
DFIFO: Disable FIFO.
0 = Enabled.
1 = Disabled (default).
POLLD: Disable polling of the drives.
0 = Enabled (default). When enabled, a single interrupt is generated after a reset.
1 = Disabled.
FIFOTHR: The FIFO threshold in the execution phase of data transfer commands. They are programmable from 00 to 0F hex (1 byte to 16 bytes). Defaults to 1 byte.
PRETRK: The Precompensation Start Track Number. They are programmable from track 0 to FF hex (track 0 to track 255). Defaults to track 0.

9.6.12.3 RE-CALIBRATE

The RE-CALIBRATE command retracts the FDC read/write head to the track 0 position, resetting the value of the PCN counter and checking the TRK0# status. If TRK0# is low, the DIR# pin remains low and step pulses are issued. If TRK0# is high, SE [and EC bits] of the ST0 are set high, and the command is terminated. When TRK0# remains low for 79 step pulses, the RE-CALIBRATE command is terminated by setting SE and EC bits of ST0 to high. Consequently, for disks that can accommodate more than 80 tracks, more than one RE-CALIBRATE command is required to retract the head to the physical track 0.

The FDC is in a non-busy state during the Execution phase of this command, which makes it possible to issue another RE-CALIBRATE command in parallel with the current command.

On power-up, software must issue a RE-CALIBRATE command to properly initialize the FDC and drives attached.

9.6.12.4 SEEK

The SEEK command controls the FDC read/write head movement from one track to another. The FDC compares the current head position, which is stored in PCN, with NCN values after each step pulse determines what direction move the head if required. The direction of movement is determined below:

PCN < NCN — Step In: Sets DIR# signal to 1 and issues step pulses.
PCN > NCN — Step Out: Sets DIR# signal to 0 and issues step pulses.
PCN = NCN — Terminate the command by setting the ST0 SE bit to 1.

The impulse rate of step pulse is controlled by Stepping Rate Time (SRT) bit in the SPECIFY command. The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another SEEK command in parallel with the current command.

9.6.12.5 RELATIVE SEEK

The RELATIVE SEEK command steps the selected drive in or out in a given number of steps. The DIR bit is used to determine to step in or out. RCN (Relative Cylinder Number) is used to determine how many tracks step the head in or out from the current track. After the step operation is completed, the controller generates an interrupt, but the command has no Result phase. No other command except the SENSE INTERRUPT STATUS command should be issued while a RELATIVE SEEK command is in progress.

9.6.12.6 DUMPREG

The DUMPREG command is designed for system run-time diagnostics, and application software development and debug. This command has one byte of Command phase and 10 bytes of Result phase, which return the values of parameters set in other commands.

9.6.12.7 LOCK

The LOCK command allows the programmer to fully control the FIFO parameters after a hardware reset. If the LOCK bit is set to 1, the parameters DFIFO, FIFOTHR, and PRETRK in the CONFIGURE command are not affected by a software reset. If the bit is set to 0, those parameters are set to default values after a software reset.

9.6.12.8 VERSION

The VERSION command is used to determine the controller being used. In Result phase, a value of 90 hex is returned in order to be compatible with the 82077.

9.6.12.9 SENSE INTERRUPT STATUS

The SENSE INTERRUPT STATUS command resets the interrupt signal (IRQ) generated by the FDC, and identifies the cause of the interrupt via the IC code and SE bit of the ST0 as shown in Table 9-21.

It may be necessary to generate an interrupt when any of the following conditions occur:

- Before any Data Transfer or READ ID command
- After SEEK or RE-CALIBRATE commands (no result phase exists)
- When a data transfer is required during an Execution phase in the non-DMA mode

Table 9-21. Interrupt Identification

SE	IC Code	Cause of Interrupt
0	11	Polling.
1	00	Normal termination of SEEK or RE-CALIBRATE command.
1	01	Abnormal termination of SEEK or RE-CALIBRATE command.

9.6.12.10 SENSE DRIVE STATUS

The SENSE DRIVE STATUS command acquires drive status information. It has no Execution phase.

9.6.12.11 SPECIFY

The SPECIFY command sets the initial values for the HUT (Head Unload Time), HLT (Head Load Time), SRT (Step Rate Time), and ND (Non-DMA mode) parameters. The possible values for HUT, SRT and HLT are shown in Table 9-22, Table 9-23 and Table 9-24 respectively. The FDC is operated in DMA or non-DMA mode based on the value specified by the ND parameters.

Table 9-22. HUT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	128	256	426	512
1	8	16	26.7	32
…	…	…	…	…
E	112	224	373	448
F	120	240	400	480

Table 9-23. SRT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1	2	3.33	4
F	0.5	1	1.67	2

Table 9-24. HLT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
00	128	256	426	512
01	1	2	3.33	4
02	2	4	6.7	8
…	…	…	…	…
7E	126	252	420	504
7F	127	254	423	508

9.6.12.12 PERPENDICULAR MODE

The PERPENDICULAR MODE command is used to support the unique READ/WRITE/FORMAT commands of Perpendicular Recording disk drives (4 Mbytes unformatted capacity). This command configures each of the four logical drives as a perpendicular or conventional disk drive via the DC3-DC0 bits, or with the GAP and WG control bits. Perpendicular Recording drives operates in "Extra High Density" mode at 1 Mbps, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. This command should be issued during the initialization of the floppy disk controller. Then, when a drive is accessed for a FORMAT A TRACK or WRITE DATA command, the controller adjusts the format or write data parameters based on the data rate. If WG and GAP are used (not set to 00), the operation of the FDC is based on the values of GAP and WG. If WG and GAP are set to 00, setting DCn to 1 will set drive n to the Perpendicular mode. DC3-DC0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset.

Table 9-25. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands

GAP	WG	Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
0	0	Conventional	22 bytes	0 bytes
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 bytes
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

Table 9-26. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands

Data Rate	Drive Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
250/300/500 Kbps	Conventional	22 bytes	0 bytes
	Perpendicular	22 bytes	19 bytes
1 Mbps	Conventional	22 bytes	0 bytes
	Perpendicular	41 bytes	38 bytes

9.6.12.13 INVALID

The INVALID command indicates when an undefined command has been sent to FDC. The FDC will set bit 6 and bit 7 in the Main Status Register to 1 and terminate the command without issuing an interrupt.

9.6.13 DMA Transfers

DMA transfers are enabled by the SPECIFY command and are initiated by the FDC by activating the LDRQ# cycle during a DATA TRANSFER command. The FIFO is enabled directly by asserting the LPC DMA cycles.

9.6.14 Low Power Mode

When writing a 1 to bit 6 of DSR, the controller is set to low power mode immediately. All the clock sources including Data Separator, Microcontroller and Write precompensation unit will be gated. The FDC can be resumed from the low-power state in two ways: one is a software reset via the DOR or DSR, and the other is a read or write to either the Data Register or Main Status Register. The second method is more preferred since all internal register values are retained.

9.7 Serial Port (UART) Description

The IT8780F incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 9-27. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

9.7.1 Data Registers

The TBR and RBR individually hold from five to eight data bits. If the transmitted data are less than eight bits, it aligns to the LSB. Either received or transmitted data are buffered by a shift register, and are latched first by a holding register. The bit 0 of any word is first received and transmitted.

(1) Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

(2) **Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)**

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before the data transmission.

9.7.2 Control Registers: IER, IIR, FCR, DLL, DLM, LCR and MCR

(1) Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0)

The IER is used to enable (or disable) four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Table 9-28. Interrupt Enable Register Description

Bit	Default	Description
7-4	-	**Reserved**
3	0	**Enable MODEM Status Interrupt** Sets this bit high to enable the Modem Status Interrupt when one of the Modem Status Registers changes its bit status.
2	0	**Enable Receiver Line Status Interrupt** Sets this bit high to enable the Receiver Line Status Interrupt which is caused when Overrun, Parity, Framing or Break occurs.
1	0	**Enable Transmitter Holding Register Empty Interrupt** Sets this bit high to enable the Transmitter Holding Register Empty Interrupt.
0	0	**Enable Received Data Available Interrupt** Sets this bit high to enable the Received Data Available Interrupt and Time-out interrupt in the FIFO mode.

(2) Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine interrupt priority and its source. The priority of four existing interrupt levels is listed below:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the type of interrupt is stored in the IIR which is accessed by the Host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the Host. Any new interrupts will not be acknowledged until the Host access is completed. The contents of the IIR are described in the table on the next page.

Table 9-29. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR
0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level
1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time	Read RBR
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR

Note: X = Not Defined

IIR(7), IIR(6): Are set when FCR(0) = 1.
IIR(5), IIR(4): Always logic 0.
IIR(3): In non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
IIR(2), IIR(1): Used to identify the highest priority interrupt pending.
IIR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled environment with a logic 0 state. In such a case, IIR contents may be used as a pointer that points to the appropriate interrupt service routine.

(3) FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to enable, clear the FIFO, and set the RCVR FIFO trigger level.

Table 9-30. FIFO Control Register Description

Bit	Default	Description
7-6	-	**Receiver Trigger Level Select** These bits set the trigger levels for the RCVR FIFO interrupt.
5-4	0	**Reserved**
3	0	This bit does not affect the Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.
2	0	**Transmitter FIFO Reset** This self-clearing bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1."
1	0	**Receiver FIFO Reset** Setting this self-clearing bit to a logic 1 clears all contents of the RCVR FIFO and resets its related counter to 0 (except the shift register).
0	0	**FIFO Enable** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT and RCVR FIFOs are disabled and cleared respectively when this bit is cleared to low. This bit must be a logic 1 if the other bits of the FCR are written to, or they will not be properly programmed. When this register is switched to non-FIFO mode, all its contents are cleared.

Table 9-31. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

(4) Divisor Latches (DLL, DLM) (Read/Write, Address offset=0,1 DLAB=0)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in a 16-bit binary format. They are loaded during the initialization to generate a desired baud rate.

(5) Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The DLL or DLM is a number of 16-bit format, providing the divisor range from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 9-32. Baud Rates Using (24 MHz + 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

(6) Scratch Pad Register (Read/Write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

(7) Line Control Register (LCR) (Read/Write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line. Its contents are described on the next page.

Table 9-33. Line Control Register Description

Bit	Default	Description
7	0	**Divisor Latch Access Bit (DLAB)** Must be set to high to access the Divisor Latches of the baud rate generator during READ or WRITE operations. It must be set low to access the Data Registers (RBR and TBR) or the Interrupt Enable Register.
6	0	**Set Break** Forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will be preserved until a low level resetting LCR(6) enables the serial port to alert the terminal in a communication system.
5	0	**Stick Parity** When this bit and LCR(3) are high at the same time, the parity bit is transmitted, and then detected by receiver, in opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	**Even Parity Select** When parity is enabled (LCR(3) = 1), LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.
3	0	**Parity Enable** A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.
2	0	**Number of Stop Bits** This bit specifies the number of stop bits in each serial character, as summarized in Table 9-34.
1-0	00	**Word Length Select [1:0]** 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 9-34. Stop Bits Number Encoding

LCR (2)	Word Length	No. of Stop Bits
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

(8) MODEM Control Register (MCR) (Read/Write, Address offset=4)

Controls the interface by the modem or data set (or device emulating a modem).

Table 9-35. Modem Control Register Description

Bit	Default	Description
7-5	-	**Reserved**
4	0	**Internal Loopback** Provides a loopback feature for diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs, and are forced to inactive high and the transmitted data are immediately received, allowing the processor to verify the transmit and receive data path of the serial channel.
3	0	**OUT2** The Output 2 bit enables the serial port interrupt output by a logic 1.
2	0	**OUT1** This bit does not have an output pin and can only be read or written by the CPU.
1	0	**Request to Send (RTS)** Controls the Request to Send (RTS#) which is in an inverse logic state with that of MCR(1).
0	0	**Data Terminal Ready (DTR)** Controls the Data Terminal ready (DTR#) which is in an inverse logic state with that of the MCR(0).

9.7.3 Status Registers: LSR and MSR

(1) Line Status Register (LSR) (Read/Write, Address offset=5)

This register provides status indications and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

Table 9-36. Line Status Register Description

Bit	Default	Description
7	0	**Error in Receiver FIFO** In 16450 mode, this bit is always 0. In the FIFO mode, it sets high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.
6	1	**Transmitter Empty** This **read only** bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty. Otherwise, this bit is "0", and has the same function in the FIFO mode.

Table 9-36. Line Status Register Description [cont'd]

Bit	Default	Description
5	1	**Transmitter Holding Register Empty** Transmitter Holding Register Empty (THRE). This read only bit indicates that the TBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to the XMIT FIFO.
4	0	**Line Break** Break Interrupt (BI) status bit indicates that the last character received was a break character, (invalid but entire character), including parity and stop bits. This occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in the IIR, with the IER(2) previously enabled.
3	0	**Framing Error** Framing Error (FE) bit, a logic 1, indicates that the stop bit in the received character is not valid. It resets low when the CPU reads the contents of the LSR.
2	0	**Parity** Error Parity error (PE) indicates by a logic 1 that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever the LSR is read by the CPU.
1	0	**Overrun Error** Overrun Error (OE) bit indicates by a logic 1 that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, the OE occurs when the FIFO is full and the next character has been completely received by the Shift Register. It will be reset when the LSR is read by the CPU.
0	0	**Data Ready** A "1" indicates a character has been received by the RBR. A logic "0" indicates all the data in the RBR or the RCVR FIFO have been read.

(2) MODEM Status Register (MSR) (Read/Write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or the peripheral devices in addition to this current state information. Four of these eight bits MSR(4)-MSR(7) can provide the state change information when a modem control input changes state. It is reset low when the Host reads the MSR.

Table 9-37. Modem Status Register Description

Bit	Default	Description
7	0	**Data Carrier Detect** Data Carrier Detect - Indicates the complement status of Data Carrier Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.
6	0	**Ring Indicator** Ring Indicator (RI#) - Indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.
5	0	**Data Set Ready** Data Set Ready (DSR#) - Indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the Loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# in the MCR.
4	0	**Clear to Send** Clear to Send (CTS#) - Indicates the complement of CTS# input. When the serial channel is in the Loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# in the MCR.
3	0	**Delta Data Carrier Detect** Indicates that the DCD# input state has been changed since the last time read by the Host.
2	0	**Trailing Edge Ring Indicator** Indicates that the RI input state to the serial channel has been changed from a low to high since the last time read by the Host. The change to a logic “1” does not activate the TERI.
1	0	**Delta Data Set Ready** Delta Data Set Ready (DDSR) - A logic "1" indicates that the DSR# input state to the serial channel has been changed since the last time read by the Host.
0	0	**Delta Clear to Send** This bit indicates the CTS# input to the chip has changed state since the last time the MSR was read.

9.7.4 Reset

The reset of the IT8780F should be held to an idle mode reset high for 500 ns until initialization, which causes the initialization of the transmitter and receiver internal clock counters. Table 9-38. Reset Control of Registers and Pinout Signals is shown below.

Table 9-38. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 low, bits 4-7 input signals
SOUT1, SOUT2	Reset	High
RTS1#, RTS2#, DTR1#, DTR2#	Reset	High
IRQ of Serial Port	Reset	High Impedance

9.7.5 Programming

Each serial channel of the IT8780F is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Although the control register can be written in any given order, the IER should be the last register written because it controls the interrupt enables. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

9.7.6 Software Reset

This approach allows the serial port returning to a completely known state without a system reset. This is achieved by writing the required data to the LCR, DLL, DLM and MCR. The LSR and RBR must be read before interrupts are enabled to clear out any residual data or status bits that may be invalid for subsequent operations.

9.7.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, not exactly 1.8432 MHz.

9.7.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When setting FCR(0)=1 and IER(0)=1, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

The receive data available interrupt will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level.

The receiver line status interrupt has higher priority over the received data available interrupt.

The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO.
RCVR FIFO time-out Interrupt: By enabling the RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

The RCVR FIFO time-out interrupt will occur only if there is at least one character in the FIFO whenever the interval between the most recent received serial character and the most recent Host READ from the FIFO is longer than four consecutive character times.

The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO.

(2) XMIT Interrupt

By setting FCR(0) and IER(1) to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt occurs under the conditions described below:

a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.

b. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following condition occurs: THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate, if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication is delayed one character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are 0].

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via the LSR described below:

LSR(7): RCVR FIFO error indication.
LSR(6): XMIT FIFO and Shift register empty.
LSR(5): The XMIT FIFO empty indication.
LSR(4) - LSR(1): Specify that errors have occurred. Character error status is handled in the same way as in the interrupt mode. The IIR is not affected since IER(2)=0.
LSR(0): High whenever the RCVR FIFO contains at least one byte.
No trigger level is reached or time-out condition indicated in the FIFO Polled Mode.

9.8 Smart Card Reader

9.8.1 Features

As an IFD (InterFace Device) built in IT8780F, the Smart Card Reader (SCR) includes a standard UART (Serial Port 2 is set in SCR mode) to control Smart Card interface handshaking and then performs data transfers, and can be connected to smart card socket directly. The Smart Card is capable of providing secured storage facilities for sensitive personal information such as Private keys, Account numbers, Passwords, Medical information, …etc. Then the SCR can be used for a broad range of applications in GSM, ID, pay TV, banking (refer to EMV'96 Spec.), … and so forth. It also provides a Smart Card clock divider for those ICC (Integrated Circuit Card) without internal clocks.

9.8.2 Operation

The SCR is a low-power consumption design. Whenever the IFD is inactive, the clock divider will turn off internal clocks even when the clock of IFD controlling / monitoring state machine is turned off to save power consumption. Also it could be waked up immediately when IC card is removed in case of emergency or when the FET control function is turned on/off.

The VCC power of IC card interface is powered from an external FET to protect the smart card interface. Also, the charge/discharge time for FET to reach 5V/0V is programmable, and FET performs automatically to meet ISO 7816 activation and deactivation sequences. The UART's modem control lines: DTR#, RTS# and DCD# are used for controlling FET on/off, Smart Card Reset signal and IC card insertion detection respectively. When an IC card is being inserted, it will switch the SCRPRES# (Smart Card Present Detect#) and then cause the DCD# signal to trigger an interrupt to the system. Then in the Smart Card interrupt service routine, the driver can assert the DTR# signal to power on the external FET (SCRPFET#) and the RTS# signal to control the Smart Card Reset signal (SCRRST). In the mean time, IT8780F will generate a proper clock frequency to allow the IC card using default serial transfer baud rate to send back an ATR (Answer-To-Reset) sequence. The interface signals are enabled after VCC reaches enough voltage level. Then transfer protocol may be negotiated to promote more efficient transfers. In the same way, when the IC card is removed in case of emergency or when the ICC processing is finished, the driver can de-assert the DTR# to turn off the FET power. But before the FET power-off and the reset, clock and data signals will be de-active, followed by a sufficient FET discharge time guaranteed to protect IC card and IFD.

9.8.3 Connection of IFD to ICC Socket

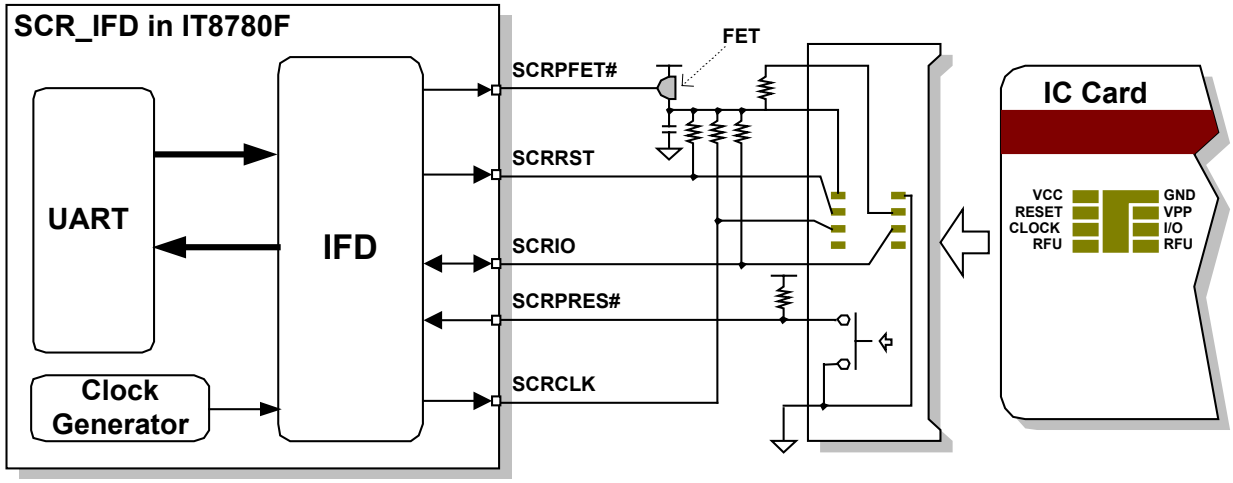


Figure 9-7. Smart Card Reader Application

9.8.4 Baud Rate Relationship Between UART and Smart Card Interface

To perform serial transfers correctly, the baud rate of UART must be set in ways similar to the ICC card.

- **Formula (Variation < 2%)**

$$\text{Baud Rate} = \frac{\text{UART}}{\frac{\frac{24\ \text{MHz}}{13}}{16 * N}} \approx \frac{\text{Smart Card}}{\frac{SCRCLK * D}{F}}$$

N =Divisor of UART, assigned by programming the DLM (Divisor Latch MSB) and DLL (Divisor Latch LSB).
F =Clock Rate Conversion Factor, default = 372.
D =Bit Rate Adjustment Factor, Default is 1.
SCRCLK duty cycle is 45%-55%.

- **ICC With Internal Clock**

ICC may use built-in internal clock, then the Baud rate is 9600 baud, just programming the Divisor Latch Registers of UART in the IT8780F for SCR IFD.

- **ICC Without Internal Clock**

Baud rate is SCRCLK/372 before negotiating, and SCRCLK is limited within 1 MHz - 5MHz. During the ATR sequence, the default F value (Clock Rate Conversion Factor) is 372, and the default D value (Bit Rate Adjustment Factor) is 1.

9.8.5 Waveform Relationship

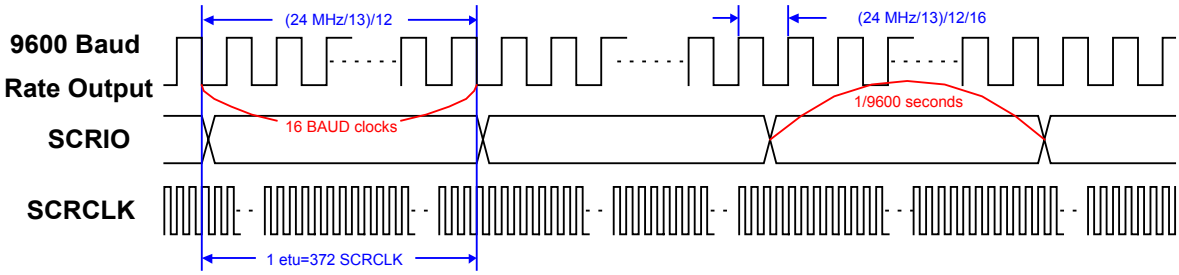


Figure 9-8. 9600 Baud Rate Example

9.8.6 Clock Divider

The SCRCLK is generated as the selection of SCR_CLKSEL1-0, which are determined in the S2 Special Configuration register 3 (LDN2_F2h).

Table 9-39. SCRCLK Selections

SCR_CLKSEL1-0	Selections
00	Stop
01	3.5 MHz
10	7.1 MHz
11	96 MHz / SCR DIV96M Note

Note: SCR DIV96M is determined by S2 Special Configuration Register 4 (LDN2_F4h).

9.8.7 Waveform Example of Activation/Deactivation Sequence

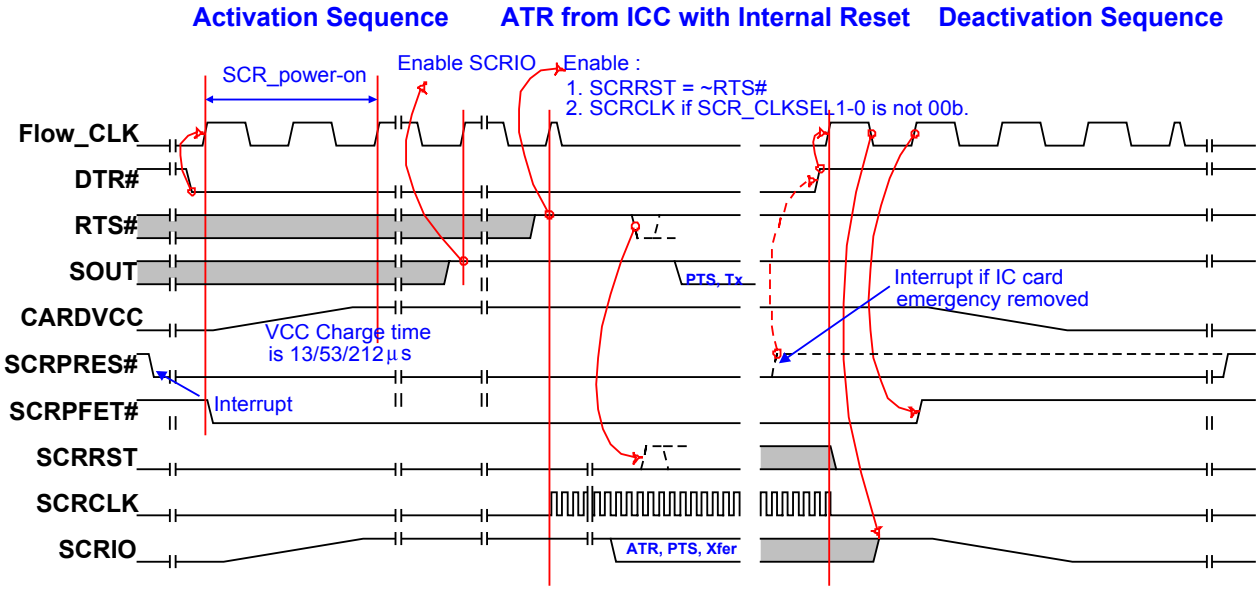


Figure 9-9. Waveform Example of IFD

- **Activation Sequence**

Refer to the waveform above. The SCR IFD in the IT8780F will make sure that the IFD is in data receive mode (i.e. the SOUT from UART is high), and the RTS# should be programmed to high. The SCRCLK is then enabled to output to the IC card (which means that the IC card can count SCRCLK clock numbers to start ATR responses), the data transfer is then enabled, and the SCRRST is the inverse logic state of RTS#. Also, the operation procedure guarantees the correct activation sequence even if the driver cannot program the SCRCLK and SCRRST in the precise time points. In this way, the hardware meets the ICC specification.

- **ATR**

For the IC card with its own internal reset, its ATR begins within 400-40000 SCRCLK cycles. If no ATR is detected, the Smart Card IFD driver can then program the RTS# to low and cause the SCRRST to high.

For some types of IC cards without internal reset signals, it will check out the SCRRST as active low reset, and begin its ATR within 400-40000 SCRCLK cycles from the time point of SCRRST rising edge.
The IT8780F does not support the type of IC Card that may send synchronous ATRs.

- **Deactivation and PTS Structure**

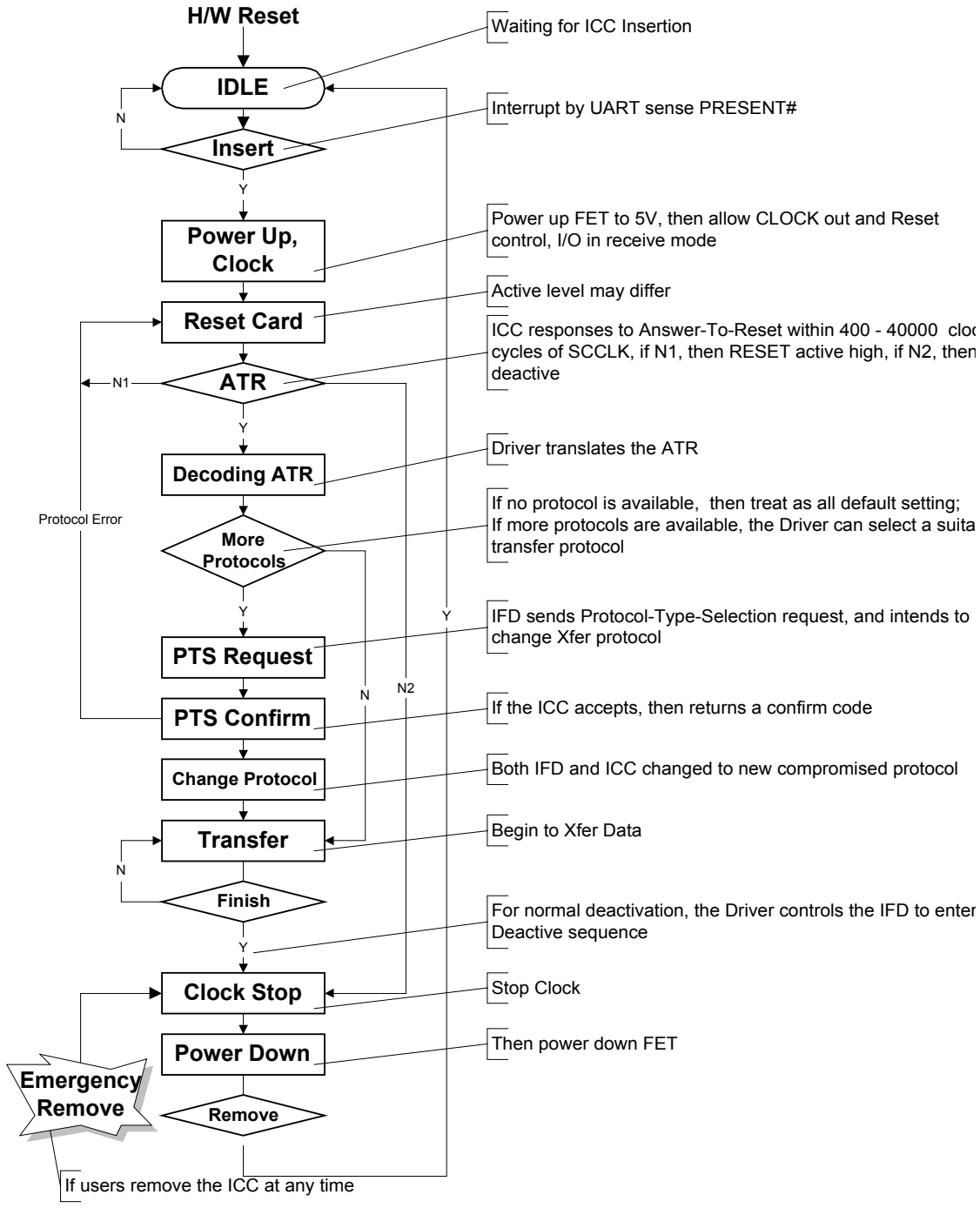
Whenever the IC card is removed or when the IFD driver intends to power off the SCR interface, the IFD will enter the deactivation sequence.

9.8.8 ATR and PTS Structure

The contents of the ATR (Answer-To-Reset) and PTS (Protocol-Type-Select) are defined in ISO/IEC 7816-X standards, which must be fully communicated by the ICC Resource manager, the ICC Service provider or the ICC application software.

After finalizing the coherent protocol, the SCR IFD enters the normal transfer mode. Since the SCRIO is the only data channel for both data transmit and receive as defined in the ICC Specification, the IT8780F can only support the half-duplex function. The SCRRST can be resent when a data transfer error occurs, and then the IFD driver will select a safer, lower-speed protocol to perform the data transfers again.

9.8.9 Smart Card Operating Sequence Example



9.9 Parallel Port

The IT8780F incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). Please refer to the IT8780F Configuration registers and Configuration Description for information on enabling/disabling, changing the base address of the parallel port, and operation mode selection.

Table 9-40. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	108	STB#	WRITE#	nStrobe
2-9	109-116	PD0 - 7	PD0 - 7	PD0 - 7
10	103	ACK#	INTR	nAck
11	102	BUSY	WAIT#	Busy PeriphAck(2)
12	101	PE	(NU) (1)	PError nAckReverse(2)
13	100	SLCT	(NU) (1)	Select
14	107	AFD#	DSTB#	nAutoFd HostAck(2)
15	106	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	105	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	104	SLIN#	ASTB#	nSelectIn

Note 1: NU: Not used.
Note 2: Fast mode.
Note 3: For more information, please refer to the IEEE 1284 standard.

9.9.1 SPP and EPP Modes

Table 9-41. Address Map and Bit Map for SPP and EPP Modes

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1h	RO	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

(1) Data Port (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by the bit 5 of the logic state of the control port register. It forwards directions when the bit is low and reverses directions when the bit is high.

(2) Status Port (Base Address 1 + 01h)

This is a **read only** register. Writing to this register has no effects. The contents of this register are latched during an IOR cycle.
Bit 7 - BUSY#: Inverse of printer BUSY signal, a logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.
Bit 6 - ACK#: Printer acknowledge, a logic "0" means that the printer has received a character and is ready to accept another. A logic "1" means that it is still processing the last character.
Bit 5 - PE: Paper end, a logic "1" indicates the paper end.
Bit 4 - SLCT: Printer selected, a logic "1" means that the printer is on line.
Bit 3 - ERR#: Printer error signal, a logic "0" means an error has been detected.
Bits 2, 1 - Reserved: These bits are always "1" when read.
Bit 0 - TMOUT: This bit is valid only in EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurred and a logic “1” means that a time-out error has been detected. This bit is cleared by an LRESET# or by writing a logic “1” to it. When the IT8780F is selected to non-EPP mode (SPP or ECP), this bit is always a logic "1" when read.

(3) Control Port (Base Address 1 + 02h)

This port provides all output signals to control the printer. The register can be read and written.
Bits 6, 7- Reserved: These two bits are always "1" when read.

Bit 5 - PDDIR: Data port direction control. This bit determines the direction of the data port register. Set this bit "0" to output the data port to PD bus, and "1" to input from PD bus.

Bit 4 - IRQE: Interrupt request enable. Setting this bit "1" enables the interrupt requests from the parallel port to the Host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.
Bit 3 - SLIN: Inverse of SLIN# pin. Setting this bit to "1" selects the printer.
Bit 2 - INIT: Initiate printer. Setting this bit to "0" initializes the printer.
Bit 1 - AFD: Inverse of the AFD# pin. Setting this bit to "1" causes the printer to automatically advance one line after each line is printed.
Bit 0 - STB: Inverse of the STB# pin. This pin controls the data strobe signal to the printer.

(4) EPP Address Port (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the Host writes to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is on this address) causes an EPP ADDRESS WRITE cycle. When the Host reads from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is on this address) causes an EPP ADDRESS READ cycle.

(5) EPP Data Ports 0-3 (Base Address 1 + 04-07h)

The EPP Data Ports are only available in the EPP mode. When the Host writes to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is on this address) causes an EPP DATA WRITE cycle. When the Host reads from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is on this address) causes an EPP DATA READ cycle.

9.9.2 EPP Mode Operation

When the parallel port of the IT8780F is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT# and SLIN# are set by the SPP control port. The direction of the data port is controlled by the bit 5 of the control port register. There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active, the IT8780F will issue Long Wait in SYNC field) high (EPP READ/WRITE cycle) to WAIT# being de-asserted. If a time-out occurs, the current EPP READ/WRITE cycle is aborted and a logic "1" will be read in the bit 0 of the status port register. The Host must write 0 to bits 0, 1, 3 of the control port register before any EPP READ/WRITE cycle (EPP spec.). The pins STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

(1) EPP ADDRESS WRITE

1. The Host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(2) EPP ADDRESS READ

1. The Host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts ASTB# after IOR becomes active.
3. The peripheral drives the PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7, allowing the Host to complete the I/O READ cycle.
4. The peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

(3) EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7.
2. The chip asserts WRITE# (STB#) and DSTB# (AFD#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(4) EPP DATA READ

1. The Host reads a byte from the EPP DATA Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts DSTB# after IOR becomes active.
3. The peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7, allowing the host to complete the I/O READ cycle.
4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.9.3 ECP Mode Operation

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. It provides an automatic high-burst-bandwidth channel that supports DMA or the ECP mode in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and enhance the maximum bandwidth requirement allowed. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8780F does not support hardware RLE compression. For a detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 9-42. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

(1) ECP Register Definitions

Table 9-43. ECP Register Definitions

Name	Address	I/O	ECP Mode	Function
data	Base 1 +000H	R/W	000-001	Data Register
ecpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	RO	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

Note 2: The Base address 2 depends on the Logical Device configuration registers of Parallel Port (0X62, 0X63).

(2) ECP Mode Descriptions

Table 9-44. ECP Mode Descriptions

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: Please refer to the ECP Register Description on pages 137-138 for a detailed description of the mode selection.

(3) ECP Pin Descriptions

Table 9-45. ECP Pin Descriptions

Name	Attribute	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device.
PD0-PD7	I/O	Address or data or RLE data.
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the Host.
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (handshaking with nStrobe). In the reverse direction, this signal is used to determine whether a command or data information is present on PD0-PD7.
PError (nAckReverse)	I	Used to acknowledge nInit from the peripheral which drives this signal low, allowing the host to drive the PD bus.
Select	I	Printer On-Line Indication.
nAutoFd (HostAck)	O	In the reverse direction, it is used for handshaking between the nAck and the Host. When it is asserted, a peripheral data byte is requested. In the forward direction, this signal is used to determine whether a command or data information is present on PD0 - PD7.
nFault (nPeriphRequest)	I	In the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while in ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to host, which has the ultimate control over the transfer direction.
nInit (nReverseRequest)	O	The host may drive this signal low to place the PD bus in the reverse direction. In the ECP mode, the peripheral is permitted to drive the PD bus when nInit is low, and nSelectIn is high.
nSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

(4) Data Port (Base 1+00h, Modes 000 and 001)
Its contents will be cleared by a RESET. In a WRITE operation, the contents of the LPC data fields are latched by the Data Register. The contents are then sent without being inverted to PD0-PD7. In a READ operation, the contents of data ports are read and sent to the host.

(5) ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)
Any data byte written to this port are placed in the FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends this data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

(6) Device Status Register (dsr) (Base 1 +01h, Mode All)
Bits 0, 1 and 2 of this register are not implemented. These bit states are remained at high in a READ operation of the Printer Status Register.
dsr(7): This bit is the inverted level of the Busy input.
dsr(6): This bit is the state of the nAck input.
dsr(5): This bit is the state of the PError input.
dsr(4): This bit is the state of the Select input.
dsr(3): This bit is the state of the nFault input.
dsr(2)-dsr(0): These bits are always 1.

(7) Device Control Register (dcr) (Base 1+02h, Mode All)

Bits 6 and 7 of this register have no function. They are set high during the READ operation, and cannot be written. Contents in bits 0-5 are initialized to 0 when the RESET pin is active.

dcr(7)-dcr(6): These two bits are always high.

dcr(5): Except in the modes 000 and 010, setting this bit low means that the PD bus is in output operation; on the contrary, setting it high means that the PD bus is in input operation. This bit will be forced to low in mode 000.

dcr(4): Setting this bit high enables the interrupt request from peripheral to the host due to a rising edge of the nAck input.

dcr(3): It is inverted and output to SelectIn.

dcr(2): It is output to nInit without inversion.

dcr(1): It is inverted and output to nAutoFd.

dcr(0): It is inverted and output to nStrobe.

(8) Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the Host to this FIFO are sent by a hardware handshaking to the peripheral according to the Standard Parallel Port protocol. This operation is only defined for the forward direction.

(9) ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the Host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The Host can receive these bytes by performing READ operations or DMA transfers from this FIFO.

(10) Test FIFO (tFifo) (Base 2+00h, Mode 110)

The host may operate READ/WRITE or DMA transfers to this FIFO in any directions. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Making a READ from an empty tFifo causes the last data byte to return.

(11) Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

(12) Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is **read only**.

cnfgB(7): A logic “0” read indicates that the chip does not support hardware RLE compression.

cnfgB(6): Reserved.

cnfgB(5)-cnfg(3): A value 000 read indicates that the interrupt must be selected with jumpers.

cnfgB(2)-cnfg(0): A value 000 read indicates that the DMA channel is jumpered 8-bit DMA.

(13) Extended Control Register (ecr) (Base 2+02h, Mode All)

ECP function control register.
ecr(7)-ecr(5): These bits are used for READ/WRITE and mode selection.

Table 9-46. Extended Control Register (ECR) Mode and Description

ECR	Mode and Description
000	Standard Parallel Port Mode. The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	PS/2 Parallel Port Mode. It is similar to the SPP mode, except that the dcr(5) is **read/write**. When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	Parallel Port Data FIFO Mode. This mode is similar to the 000 mode, except that the Host writes or DMA transfers the data bytes to the FIFO. The FIFO data are then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	ECP Parallel Port Mode. In the forward direction, bytes placed into the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	Reserved, not defined.
110	Test mode. In this mode, the FIFO may be read from or written to, but it cannot be sent to the peripheral.
111	Configuration mode. In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode
1: Disables the interrupt generated on the asserting edge of the nFault input.
0: Enables the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted, or if this bit is written from 1 to 0 in the low-level nFault.

ecr(3): dmaEn, READ/WRITE
1: Enables DMA. DMA starts when serviceIntr (ecr(2)) is 0.
0: Disables DMA unconditionally.

ecr(2): ServiceIntr, READ/WRITE
1: Disables DMA and all service interrupts.
0: Enables the service interrupts. This bit will be set to “1” by hardware when one of the three service interrupts has occurred.
Writing “1” to this bit will not generate an interrupt.

Case 1: dmaEn=1
During DMA, this bit is set to 1 (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0
This bit is set to 1 (a service interrupt generated) whenever there are writeIntrThreshold or more bytes space free in the FIFO.

Case 3: dmaEn=0, dcr(5)=1
This bit is set to 1 (a service interrupt generated) whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

ecr(1): full, **read only**
1: The FIFO is full and cannot accept another byte.
0: The FIFO has at least 1 free data byte space.
ecr(0): empty, **read only**
1: The FIFO is empty.
0: The FIFO contains at least 1 data byte.

(14) Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data transmission are software-controlled. Setting mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

From the mode 000 or 001, any other mode may be immediately switched to any other mode. To change direction, the mode must first be set to 001.

In the extended forward mode, the FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In ECP reverse mode, all data must be read from the FIFO before returning to mode 000 or 001. Usually, unneeded data are accumulated during ECP reverse handshaking, when the mode is changed during a data transfer. In such conditions, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

(15) Software Operation (ECP)

Before the ECP operation can begin, it is first necessary for the Host to switch the mode to 000 in order to negotiate with the parallel port. During this process, the Host determines whether the peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfers are PWord wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. The ECP Address/RLE bytes may be automatically sent by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change directions, the Host switches mode to 001. It then negotiates either the forward or reverse channel, sets the direction to 1 or 0, and finally switches mode to 001. If the direction is set to 1, the hardware performs the handshaking for each ECP data byte read, then tries to fill the FIFO. At this time, PWords may be read from the ecpDFifo while it retains data. It is also possible to perform the ECP transfers by handshaking with individual bytes under programmed control in mode = 001, or 000, even though this is a comparatively time-consuming approach.

(16) Hardware Operation (DMA)

The Standard PC DMA protocol (through LDRQ#) is followed. As in the programmed I/O case, software sets THE direction and state. Next, the desired count and memory addresses are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents in the FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from the FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr, DMA is disabled when the DMA controller reaches the terminal count. By not asserting LDRQ# for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing a transfer, the host DMA controller is disabled, serviceIntr is then set to 1, and dmaEn is next set to 0. If the contents in FIFO are empty or full, the DMA will start again. This is first done by enabling the host DMA controller, and then setting dmaEn to 1. Finally, serviceIntr is set to 0. Upon completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low, ensuring that all data successfully reach the peripheral device.

(17) Interrupts

It is necessary to generate an interrupt when any of the following states are reached.

1. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold.
2. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of PWords in the FIFO is greater than or equal to readIntrThreshold.
3. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count.
4. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
5. ackIntEn = 1. In current implementations of using existing parallel ports, the interrupt generated may be either edge or level trigger type.

(18) Interrupt Driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is 0 and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the Test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

Any PC LPC bus implementation that is adjusted to expedite DMA or I/O transfer must ensure that the bandwidth on the ISA is maintained on the interface. Although the LPC (even PCI) bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at the optimum speed.

(19) Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 KB/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

9.10 Keyboard Controller (KBC)

The keyboard controller is implemented using an 8-bit microcontroller that is capable of executing the 8042 instruction set. For general information, please refer to the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter power-down mode by executing two types of power-down instructions. The 8-bit microcontroller has 256 bytes of RAM for data memory and 2 Kbytes of ROM for the program storage.

The ROM codes may come from various vendors (or users), and are programmed during the manufacturing process. To assist in developing ROM codes, the keyboard controller has an external access mode. In the external access mode, the internal ROM is disabled and the instructions executed by the microcontroller come from an externally connected ROM.

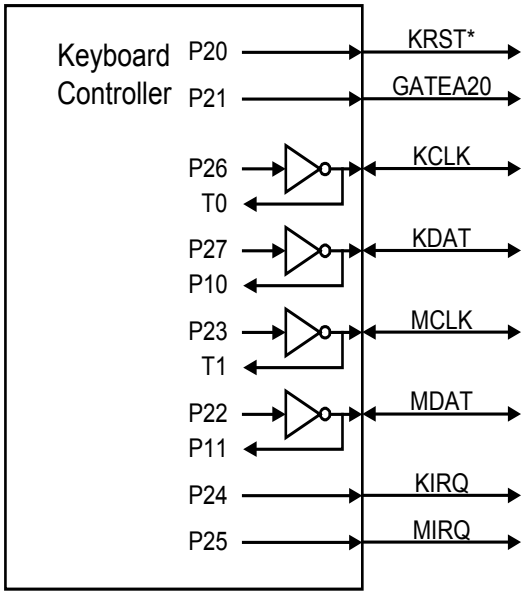


Figure 9-10. Keyboard and Mouse Interface

9.10.1 Host Interface

The keyboard controller interfaces with the system through the 8042 style host interface. Table 9-47 shows how the interface decodes the control signals.

Table 9-47. Data Register READ/WRITE Controls

Host Address Note	R/W*	Function
60h	RO	READ DATA
60h	WO	WRITE DATA, (Clear F1)
64h	RO	READ Status
64h	WO	WRITE Command, (set F1)

Note: These are the default values of the LDN5, 60h and 61h (DATA); LDN5, 62h and 63h (Command). All these registers are programmable.
READ DATA: This is an 8-bit **read only** register. When read, the KIRQ output is cleared and OBF flag in the status register is cleared.
WRITE DATA: This is an 8-bit **write only** register. When written, the F1 flag of the Status register is cleared and the IBF bit is set.
READ Status: This is an 8-bit **read only** register. Refer to the description of the Status register for more information.
WRITE Command: This is an 8-bit **write only** register. When written, both F1 and IBF flags of the Status register are set.

9.10.2 Data Registers and Status Register

The keyboard controller provides two data registers: one is DBIN for data input, and the other is DBOUT for data output. Each of the data registers is 8-bit wide. A write (microcontroller) to the DBOUT will load Keyboard Data Read Buffer, set OBF flag and set the KIRQ output. A read (microcontroller) of the DBIN will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag.

The status register holds information concerning the status of the data registers, the internal flags, and some user-defined status bits. Please refer to Table 9-48. The bit 0 OBF is set to “1” when the microcontroller writes data into DBOUT, and is cleared when the system initiates a DATA READ operation. The bit 1 IBF is set to “1” when the system initiates a WRITE operation, and is cleared when the microcontroller executes an “IN A, DBB” instruction. The F0 and F1 flags can be set or reset when the microcontroller executes the clear and complement flag instructions. F1 also holds the system WRITE information when the system performs the WRITE operations.

Table 9-48. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF

9.10.3 Keyboard and Mouse Interface

KCLK is the keyboard clock pin. Its output is the inversion of pin P26 of the microcontroller, and the input of KCLK is connected to the T0 pin of the microcontroller. KDAT is the keyboard data pin; its output is the inversion of pin P27 of the microcontroller, and the input of KDAT is connected to the P10 of the microcontroller. MCLK is the mouse clock pin; its output is the inversion of pin P23 of the microcontroller, and the input of MCLK is connected to the T1 pin of the microcontroller. MDAT is the Mouse data pin; its output is the inversion of pin P22 of the microcontroller, and the input of MDAT is connected to the P11 of the microcontroller. KRST# is pin P20 of the microcontroller. GATEA20 is the pin P21 of the microcontroller. These two pins are used as software controlled or user defined outputs. External pull-ups may be required for these pins.

9.10.4 KIRQ and MIRQ

KIRQ is the interrupt request for keyboard (Default IRQ1), and MIRQ is the interrupt request for mouse (Default IRQ12). KIRQ is internally connected to P24 pin of the microcontroller, and MIRQ is internally connected to pin P25 of the microcontroller.

10. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage.....-0.3V to 4.6V

Input Voltage (Vi)..... -0.3V to 5.25V

Output Voltage (Vo) ..... -0.3V to VCC + 0.3V

Operation Temperature (Topt).....0°C to +70°C

Storage Temperature..... -55°C to +125°C

Power Dissipation 200mW

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 3.3V ± 5%, Ta = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DO8 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -8 mA
DOD8 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
DO16 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -16 mA
$DO_{4/24}$ Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -4 mA
$DO_{16/24}$ Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -16 mA
DIO8 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -8 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DIOD8 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C) [cont'd]

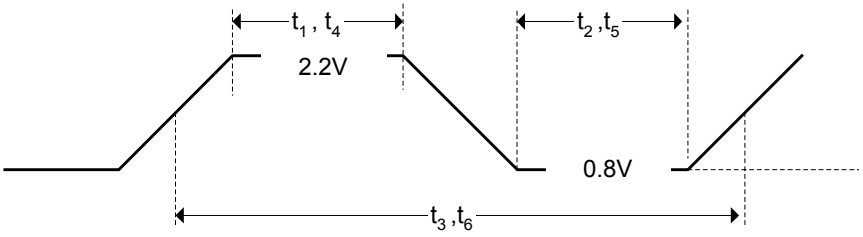
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DIO16 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -16 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DIOD16 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
$DIO_{16/24}$ Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -16 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DI Type Buffer						
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC

11. AC Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

11.1 Clock Input Timings

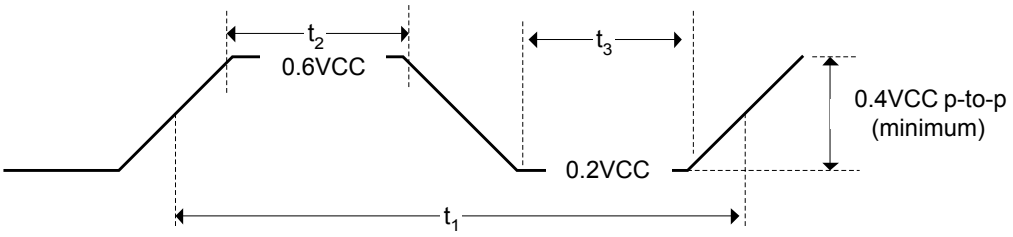
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock High Pulse Width when CLKIN=48 MHz[1]	8			nsec
t_2	Clock Low Pulse Width when CLKIN=48 MHz [1]	8			nsec
t_3	Clock Period when CLKIN=48 MHz [1]	20	21	22	nsec
t_4	Clock High Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_5	Clock Low Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_6	Clock Period when CLKIN=24 MHz [1]	40	42	44	nsec

1. Not tested. Guaranteed by design.



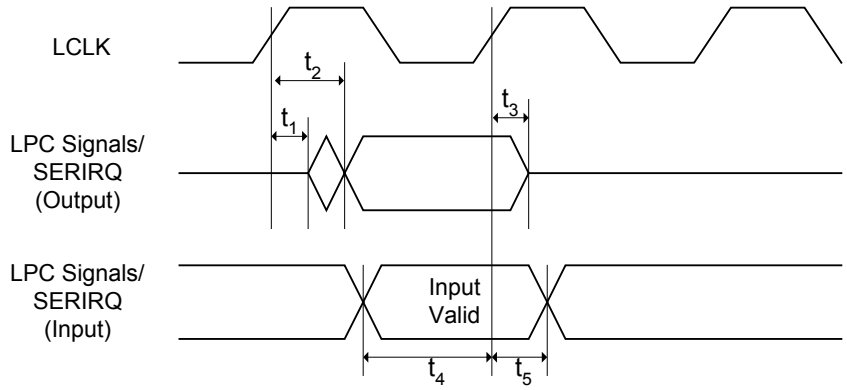
11.2 LCLK (PCICLK) and LRESET# Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			μsec



11.3 LPC and SERIRQ Timings

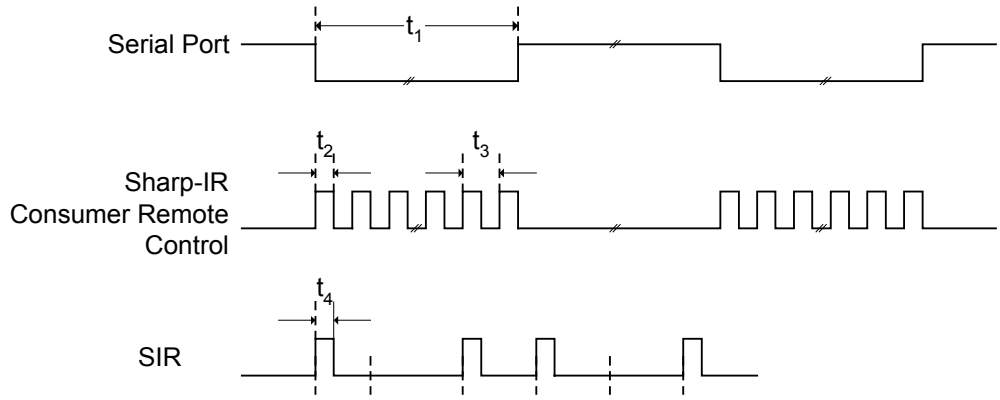
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec



11.4 Serial Port, ASKIR, SIR and Consumer Remote Control Timings

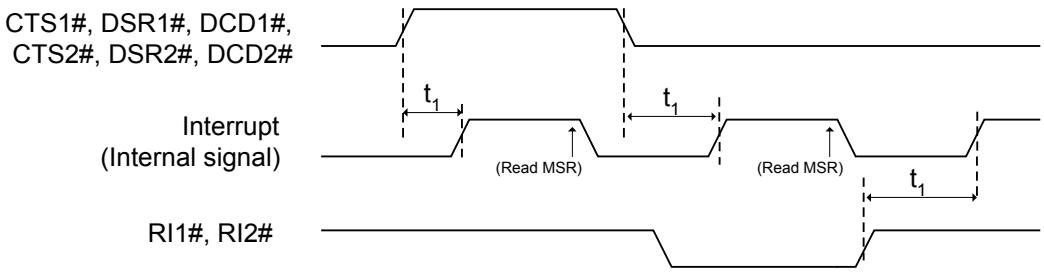
Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single Bit Time in Serial Port and ASKIR	Transmitter	t_{BTN} – 25 Note1	t_{BTN} + 25	nsec
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	nsec
t_2	Modulation Signal Pulse Width in ASKIR	Transmitter	950	1050	nsec
		Receiver	500		nsec
t_3	Modulation Signal Period in ASKIR	Transmitter	1975	2025	nsec
		Receiver	2000X(23/24)	2000X(25/24)	nsec
t_4	SIR Signal Pulse Width	Transmitter, Variable	(3/16) x t_{BTN} – 25	(3/16) x t_{BTN} + 25	nsec
		Transmitter, Fixed	1.48	1.78	µsec
		Receiver	1		µsec

Note 1: t_{BTN} is the nominal bit time in Serial Port, ASKIR, and SIR. It is determined by the setting on the Baud Rate Divisor registers.



11.5 Modem Control Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec

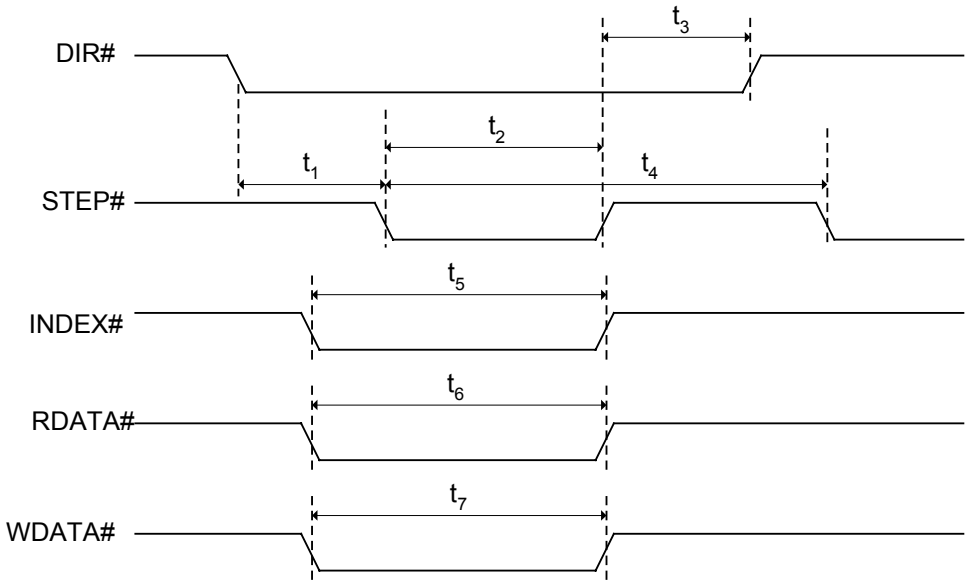


11.6 Floppy Disk Drive Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	DIR# active to STEP# low		4X t_{mclk} Note1		nsec
t_2	STEP# active time (low)		24X t_{mclk}		nsec
t_3	DIR# hold time after STEP#		t_{SRT} Note2		msec
t_4	STEP# cycle time		t_{SRT}		msec
t_5	INDEX# low pulse width	2X t_{mclk}			nsec
t_6	RDATA# low pulse width	40			nsec
t_7	WDATA# low pulse width		1X t_{mclk}		nsec

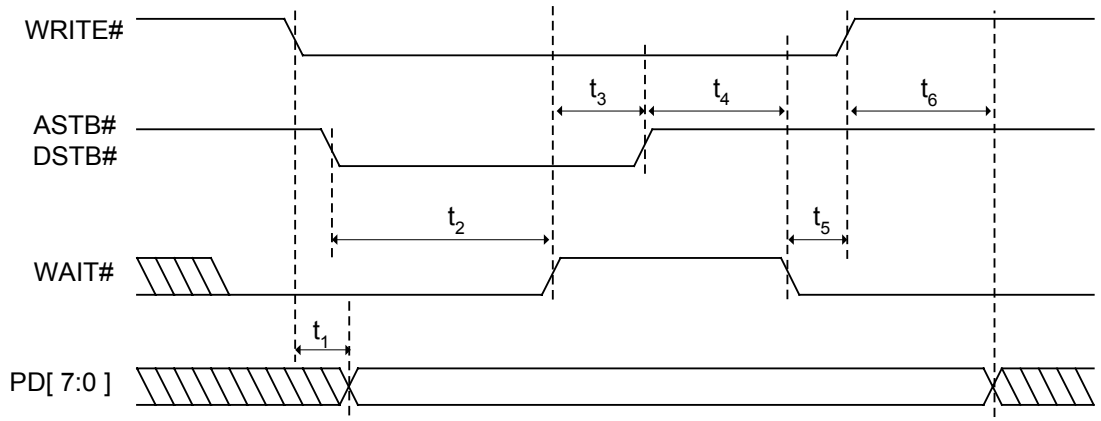
Note 1: t_{mclk} is the cycle of main clock for the microcontroller of FDC. t_{mclk} =8M/ 4M/ 2.4M/ 2M for 1M/ 500K/ 300K/ 250 Kbps transfer rates respectively.

Note 2: t_{SRT} is the cycle of the Step Rate Time. Please refer to the functional description of the SPECIFY command of the FDC.



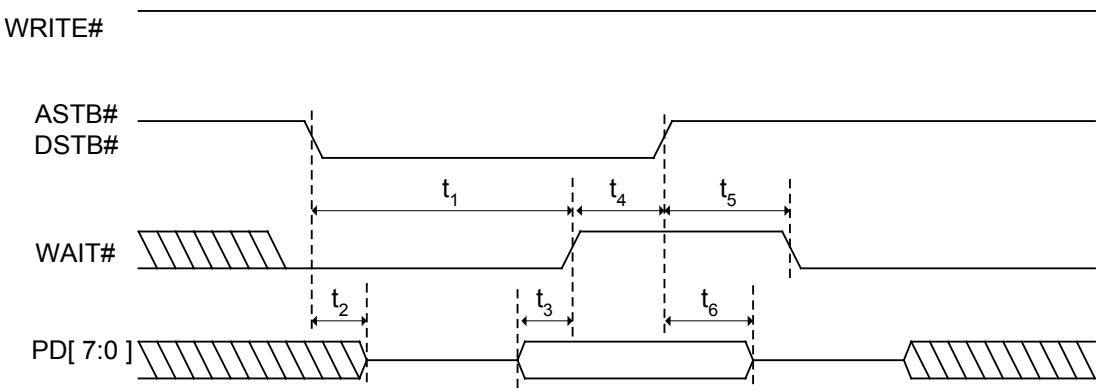
11.7 EPP Address or Data Write Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	WRITE# asserted to PD[7:0] valid			50	nsec
t_2	ASTB# or DSTB# asserted to WAIT# de-asserted	0		10	nsec
t_3	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_4	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_5	WAIT# asserted to WRITE# de-asserted	65			nsec
t_6	PD[7:0] invalid after WRITE# de-asserted	0			nsec



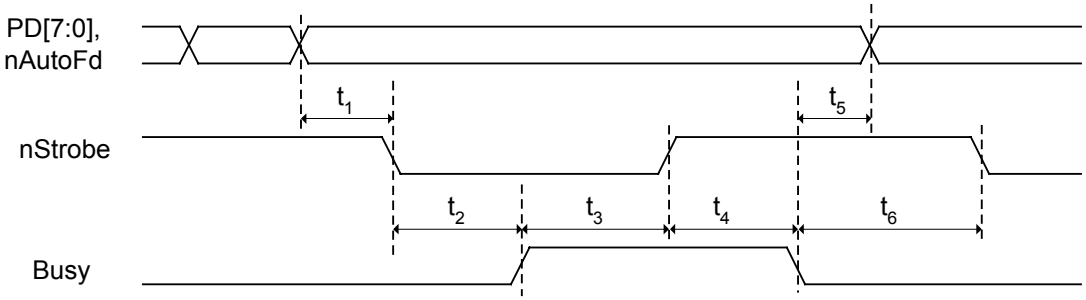
11.8 EPP Address or Data Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	nsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec



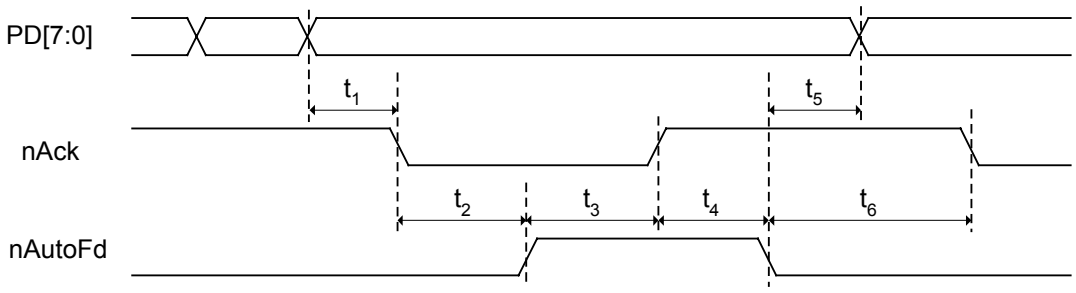
11.9 ECP Parallel Port Forward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec



11.10 ECP Parallel Port Backward Timings

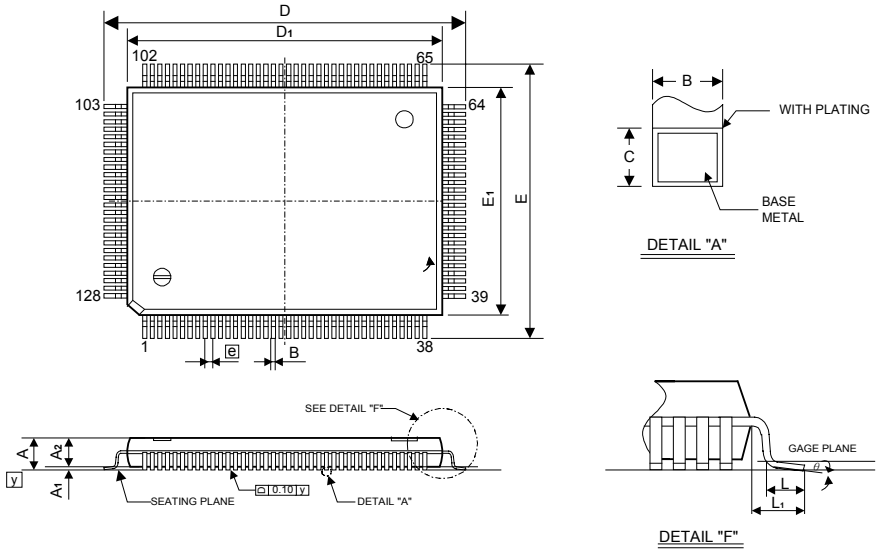
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec



12. Package Information

QFP 128L Outline Dimensions

unit: inches/mm



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A**1**	0.010	-	-	0.25	-	-
A**2**	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion, but mold mismatch is included.
2. Dimension B does not include dambar protrusion.
3. Controlling dimension: millimeter.

13. Ordering Information

Part No.	Package
IT8780F	128 QFP