

# *Fuji Switching Power Supply Control IC*

Green Mode PWM IC

FA5626

## *Application Note*

April.-2011  
Fuji Electric Co., Ltd.

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## Caution)

- The contents of this note subject to change without notice due to improvement.
- The application examples or the parts constants in this note are shown to help your design.  
Variation of parts and service condition are not fully taken into account.  
Before use, a design with due consideration for these variations and conditions shall be conducted.

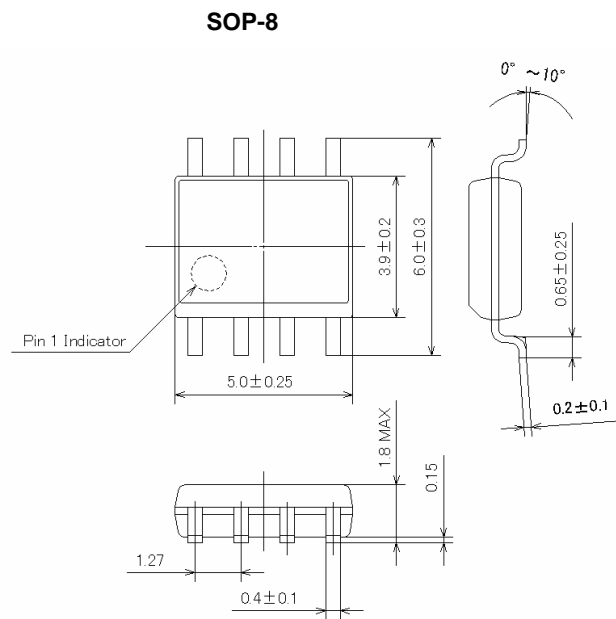
### 1. Overview

FA5626 is a current mode type switching power supply control IC possible to drive a power MOSFET directly. Despite of a small package with 8 pins, it has a lot of functions and it is best suited for power saving at the light load and decreasing external parts. Moreover it enables to realize a reduced space and a high cost-performance power supply.

### 2. Features

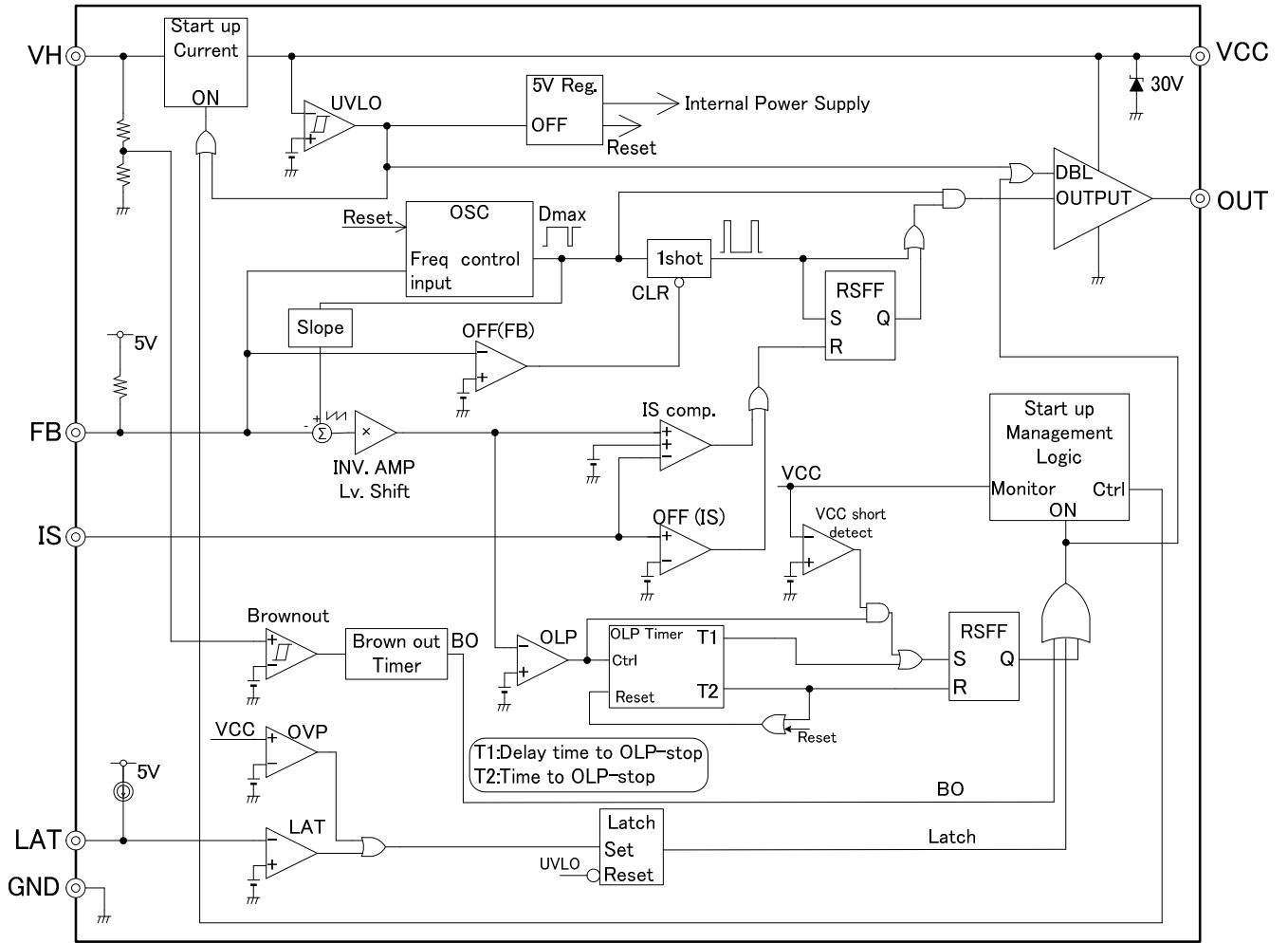
- Excellent Power Saving by lowering the oscillation frequency depending on the load at light load.
- Low power consumption by a built-in startup circuit.
- Overload protection function with a few numbers of external components.
- Brown-In/Out Function without additional external components.
- Current Minus detection. Power Saving of the revision of the input voltage of OLP
- Latch pin for an external signal: Over Temperature Protection, Over Voltage Protection etc.
- External MOSFET driving suitable for Power Supply up to 200W: -1.0A(sink),/+0.5A(source)
- VCC Under-Voltage Lock-Out function (UVLO).
- Low EMI by Frequency diffusion function

### 3. Outline drawing



**4. Block diagram**

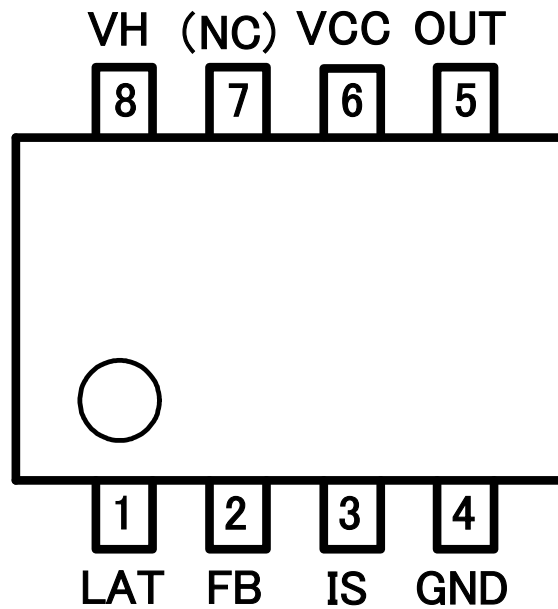
**FA5626 (Overload protection : Auto recovery type)**



**5. Functional description of pins**

Pin No.	Pin Name	I/O	Pin function
1	LAT	I	External latch signal input. (Connect capacitor LAT and GND)
2	FB	I	Feedback control signal input
3	IS	I	Current Limiter Input (Negative voltage sense)
4	GND	—	IC Ground
5	OUT	O	Output
6	VCC	—	Power Supply (Connect capacitor between VCC and GND)
7	(NC)	—	No Connection
8	VH	I	High Voltage input, Brown-out (Series connection of diode and resistance between VH and the bulk capacitor or the rectified AC line)

PIN CONNECTION



## 6. Rating & characteristics

- "+" shows sink and "-" shows source in current prescription.

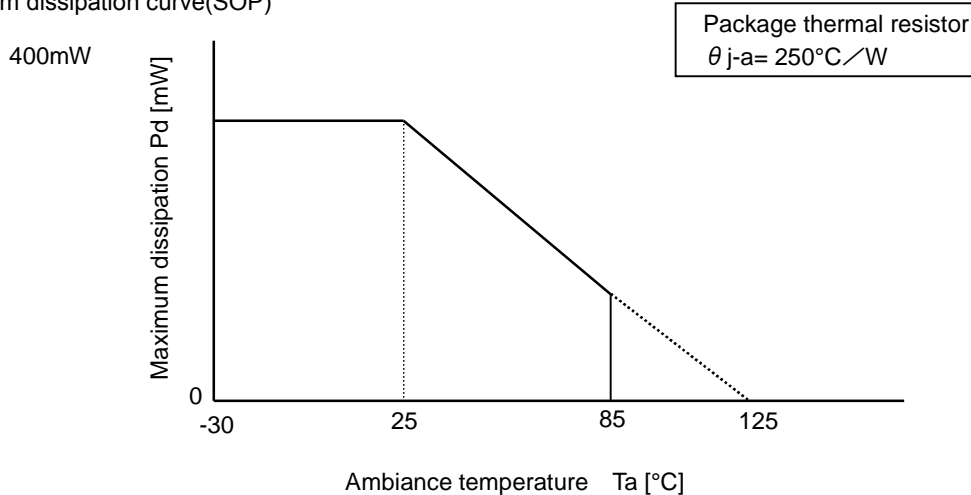
### (1) Absolute Maximum Ratings

Stress exceeding absolute maximum ratings may malfunction or damage the device.

Item	Symbol	Rating	Unit
LAT pin voltage	VLAT	-0.3 to 5.0	V
LAT pin current	ILAT	-100 to 100	uA
FB pin voltage	VFB	-0.3 to 5.0	V
FB pin current	IFB	-500 to 100	uA
IS pin voltage	VIS	-2.0 to 5.0	V
IS pin current	IIS	-100 to 100	uA
Voltage at OUT pin	VOUT	-0.3 to VCC+0.3	V
Peak current at OUT pin *1	IOH	-0.5	A
	IOL	+1.0 (The period that exceeds +1.0A is 100ns or less.)	A
VCC pin voltage	VVCC	-0.3 to 28	V
VCCpin current *1 (Ta=25°C)	At input plus voltage	-30 to 4	mA
	At input minus voltage	-0.1 to 0	
VH pin voltage	VVH	-0.3 to 750	V
VH pin current *1 (Ta=25°C)	IVH	-0.1 to 30	mA
Power dissipation (Ta=25°C)	Pd	400	mW
Maximum junction temperature in operation	Tj	-30 to +125	°C
Storage temperature	Tstg	-40 to +150	°C

\*1 Never exceed power dissipation Pd.

○Maximum dissipation curve(SOP)



## (2) Recommended Operating Conditions

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage (after VCCon)	VCC	12	18	24	V
VH pin voltage	VVH	100	—	650	V
VH pin resistance	RVH	2.2	—	10	kΩ
LAT pin capacitor	CLAT	0.22	1.0	2.2	uF
VCC pin capacitor	CVCC	22	33	56	uF
Ambiance temperature in operation	Ta	-30	—	85	°C

## (3) Electrical Characteristics

T<sub>j</sub>=25degree, VCC=18V(after VCCon), VH=120V,VFB=2.5V, VIS=0V, no load , unless otherwise specified.

Voltage described in condition is DC input.

Notes)

- \*1: This parameter is not 100% tested in production but guaranteed by design.  
It doesn't guarantee the column of '—' to have been specified.

Over temperature protection and external latch-off section. (LAT pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Source current of LAT pin	ILAT	LAT=1.15V,FB=0V	-80	-70	-60	uA
Latch-off level	VthLAT	VLAT=Decreasing	1.00	1.05	1.10	V
Equivalent resistance of LAT pin for Latch-off	RLAT	VthLAT / -Ilat	13.5	15	16.5	kΩ
Latch-off delay timer *1	TdLAT	VLAT=VthLAT	50	65	80	us

Soft-start section (LAT pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output minimum ON pulse LAT pin voltage	Vss1	*2-1	1.9	2.1	2.3	V
Keep minimum ON pulse LAT pin voltage	Vss2	*2-1	2.3	2.5	2.7	V
Operating time of minimum ON pulse *1	Vdss	*2-1	440	490	540	us
Start soft-start LAT pin voltage *1	Vss	*2-1	1.8	2.0	2.2	V
Finish soft-start LAT pin voltage	Vss3	*2-1	1.45	1.6	1.75	V
After soft-start LAT pin voltage	VssL	*2-1	1.45	1.6	1.75	V
	VssH		1.9	2.1	2.3	

- \*2-1: Start and Re-start of after VCCon or Brown-in



## Switching oscillator section (FB pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Center oscillation frequency	Fosc	VFB=2V	60	65	70	kHz
Voltage stability	Fdv	VCC=12 to 24V VFB=2V	-2	—	+2	%
Temperature stability *1	$\Delta$ Fdt	Tj=-30 to 125°C VFB=2V	-5	—	+5	%
Frequency modulation width *1	Fm	VFB=2V	±5	±7	±9	%
Frequency modulation period *1	Tfmodu	VFB=2V	7.0	8.0	9.0	ms
FB pin threshold voltage for stop frequency modulation *1	Vfbmst	VFB=Decreasing	1.45	1.55	1.65	V
FB pin threshold voltage for light load mode	Vfbm	VLAT=1.8V *3-1 VFB=Decreasing	1.7	1.8	1.9	V
FB pin voltage at minimum frequency	Vfmin	VLAT=1.8V *3-1 VFB=Decreasing	1.1	1.2	1.3	V
Oscillation frequency reduction ratio	Kf	$\frac{\Delta f}{\Delta VFB}$ VLAT=1.8V *3-1 $\Delta VFB = Vfbm - Vfmin$	80	110	140	kHz/V
Minimum oscillation frequency	Fmin	VLAT=1.8V *3-1 VFB=0.5V	0.25	0.45	0.65	kHz

\*3-1 After IC starts, the voltage at LAT pin rises to Vss1.

## Pulse width modulation section (FB pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Maximum duty cycle	Dmax	VFB=4.5V	75	85	95	%
Minimum duty cycle	Dmin	VFB=0V	—	—	0	%
Input threshold voltage	VthFB0	VFB=Decreasing DUTY=0%	340	400	460	mV
FB pin source current	I <sub>fb0</sub>	VFB=0V, VLAT=1.8V	-320	-260	-200	uA
Minimum ON pulse width *4-1	Tmin1	Steady VVH< VHVTH1	1200	1700	2200	ns
		Full & Half-wave rectification DC *1				
	Tmin2	Steady VVH>= VHVTH1	900	1250	1600	ns
	Full & Half-wave rectification DC *1	1200	1700	2200		
	Tmin3	Start (Restart) / over load	180	280	380	ns
VH voltage detected change Minimum ON pulse width *1	VHVTH1	*4-1	120	210	260	V

\*4-1: When input voltage at VH pin is DC, this function doesn't operate.

## Over load protection and auto-restart circuit section (FB pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Over load detection threshold voltage *1	VthOLP	VFB=Increasing	3.5	4.2	5.0	V
Over load detection Delay time *1	TdOLP	VFB=VthOLP	60	70	80	ms
Waiting time of auto restart *1	TdOLP2	VFB=VthOLP	1300	1530	1760	ms

**Current sense section (IS pin)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Voltage gain $\Delta VFB/\Delta VIS$	AvIS	VFB=2V to 1.5V	-4.6	-3.8	-3.0	V/V	
Maximum threshold voltage *6-1	VthIS1	VFB= VthOLP, VVH>= VHVTH2	Full & Half-wave rectification	-0.525	-0.500	-0.475	V
			DC *1	-0.552	-0.525	-0.498	
		VFB= VthOLP, VVH< VHVTH2	Full & Half-wave rectification	-0.552	-0.525	-0.498	V
			DC *1				
VH voltage detected change Maximum threshold voltage	VHVTH2	*6-1	138	148	158	V	
Input bias current	IIS	VIS=0V,VFB=0V	-50	-40	-30	uA	
Delay to output *1	TpdIS	Tj=25°C	100	200	300	ns	

\*6-1: When input voltage at VH pin is DC, this function doesn't operate.

**Output circuit section (OUT pin)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low output voltage	VOL	IOL=+100mA VFB=0V	0.4	0.8	1.6	V
High output voltage	VOH	IOH=-100mA, VFB=2V	14.5	16	18	V
Rise time	tr	VCC=24V,VFB=3V, CL=1nF, Tj=25°C	30	60	100	ns
Fall time	tf	VCC=24V,VFB=3V, CL=1nF, Tj=25°C	20	40	70	ns

**VCC circuit section (VCC pin)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start-up threshold voltage	VCCon	VCC=Increasing	16	18	20	V
Shutdown threshold voltage	VCCoff	VCC=Decreasing	8.0	9.0	10.0	V
Hysteresis width	Vhys	VCCon-VCCoff	7.0	9.0	11.0	V
VCC over-voltage protection threshold voltage(OVP)	Vthovp	VCC=Increasing	25	26	27	V
OVP delay timer *1	TdOVP	VCC=Vthovp	50	65	80	us
Short current protection threshold voltage (SCP)	Vthshort	VFB=VthOLP, VCC=Decreasing	10	11	12	V
SCP delay timer *1	TdSCP	VFB=VthOLP, VCC=Vthshort	50	65	80	us

**Power supply current (VCC pin)**

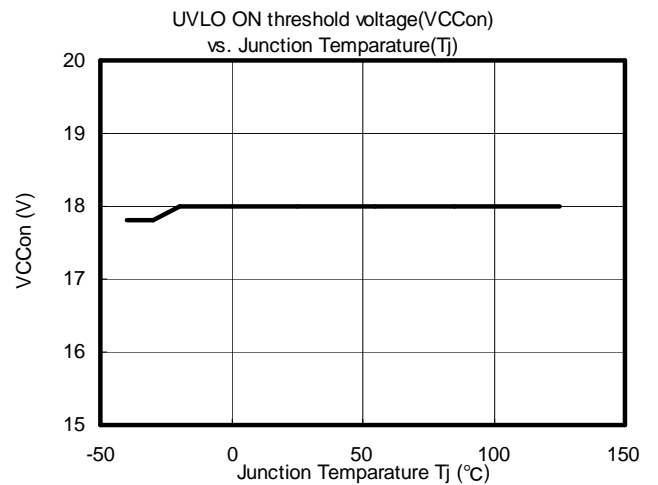
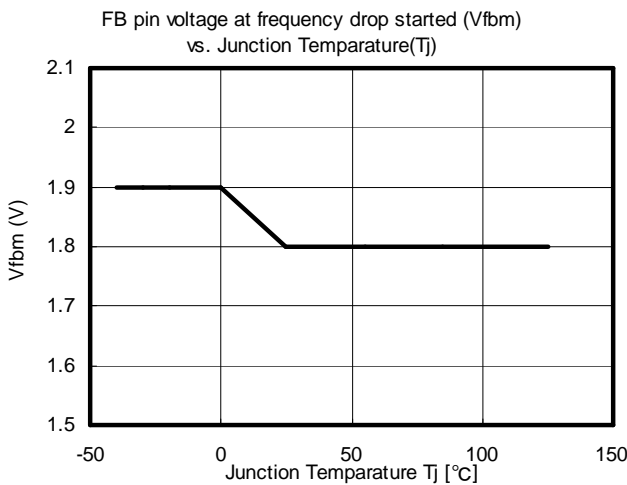
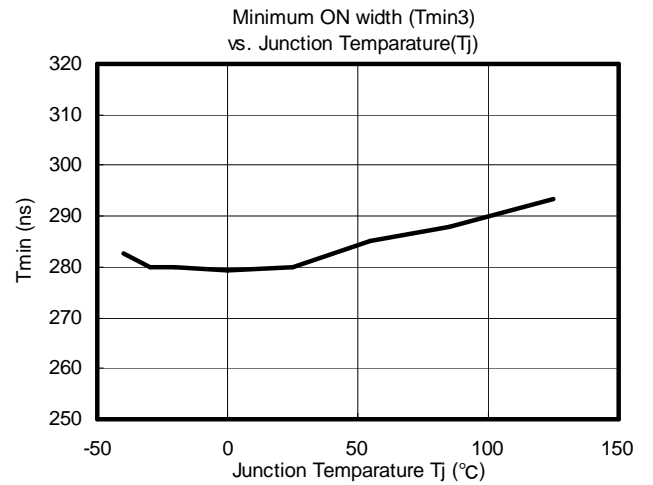
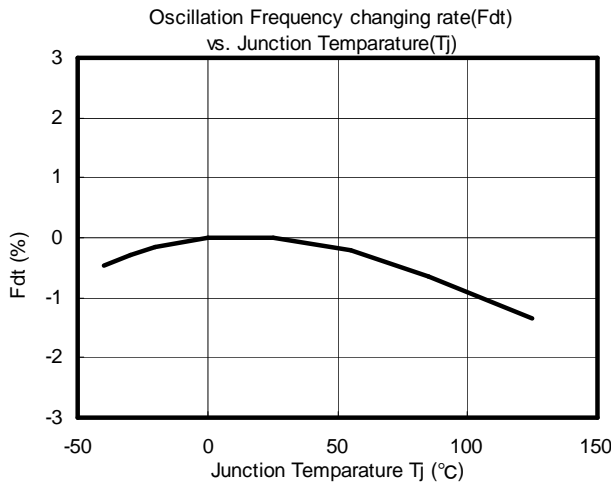
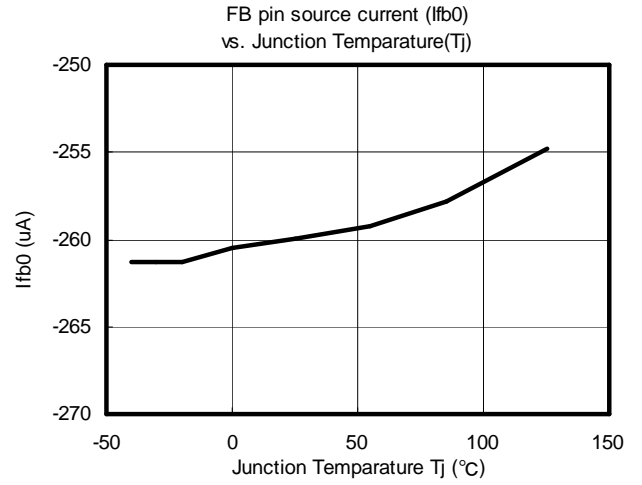
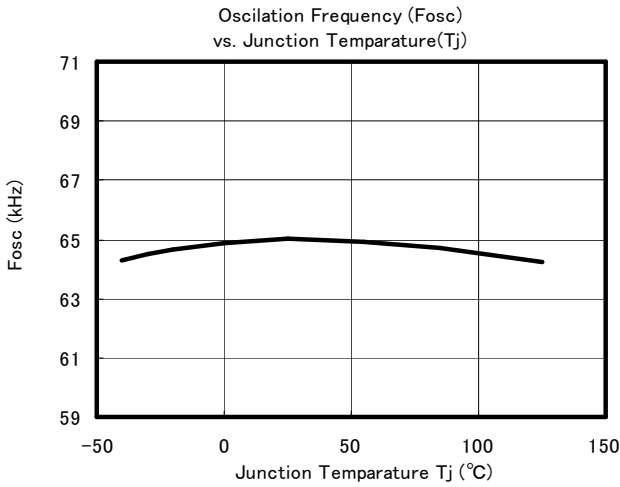
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating-state supply current	ICCop1	Duty=Dmax,FB=2V, OUT=no load	1.0	1.4	1.7	mA
	ICCop2	Duty=0%,FB=0V OUT=no load	0.95	1.35	1.65	mA
Supply current at Brownout or OLP	ICCbo	VH=0V,VFB=0V, VCC=14.5V	0.6	0.8	1.1	mA
Latch mode supply current	ICClat	VH=0V,VFB=0V, VCC=11V	0.6	0.9	1.1	mA

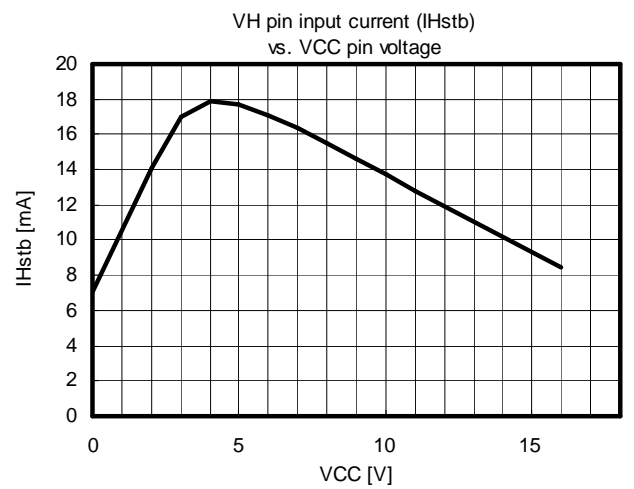
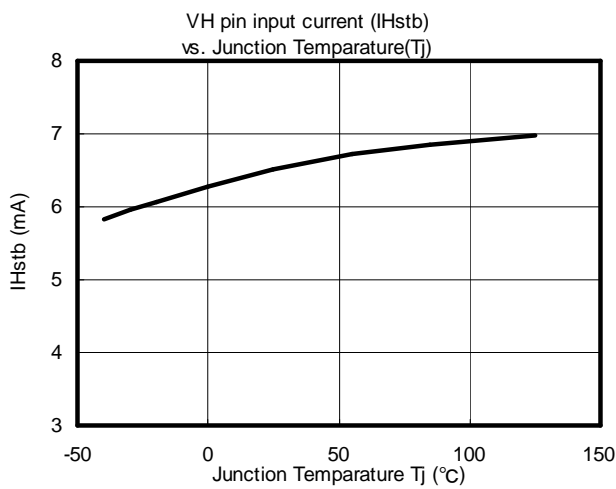
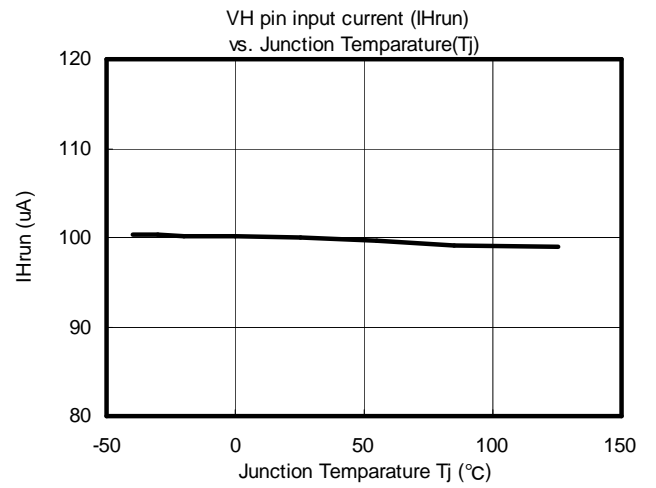
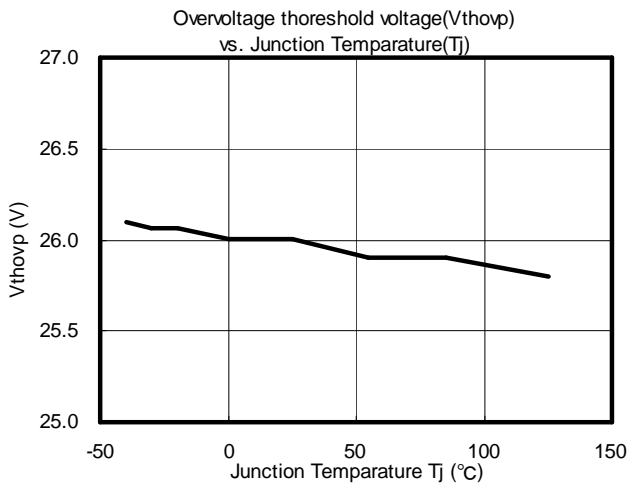
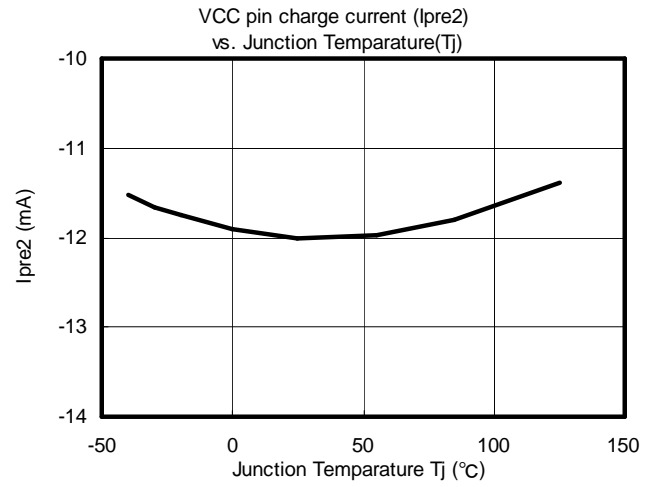
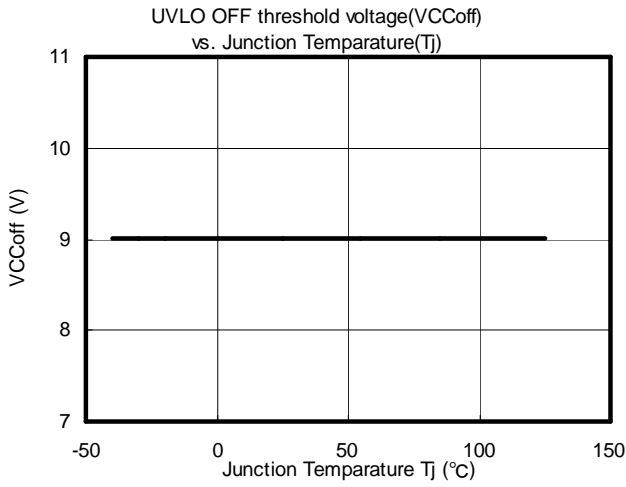
## High-voltage input section (VH pin, VCC pin)

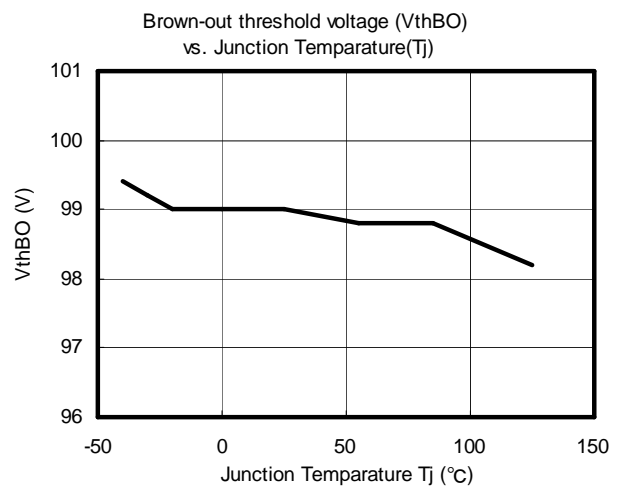
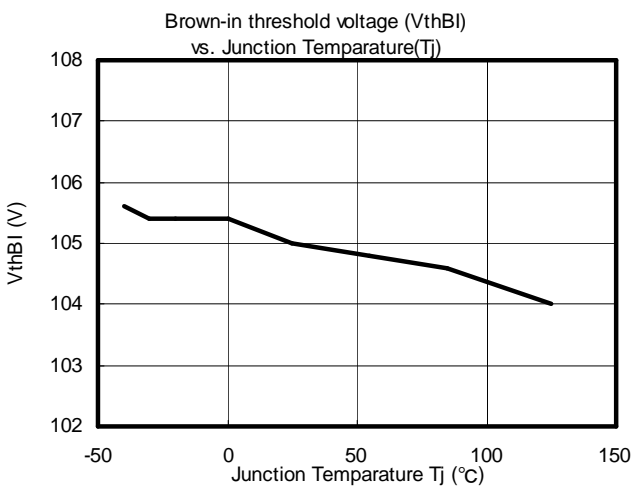
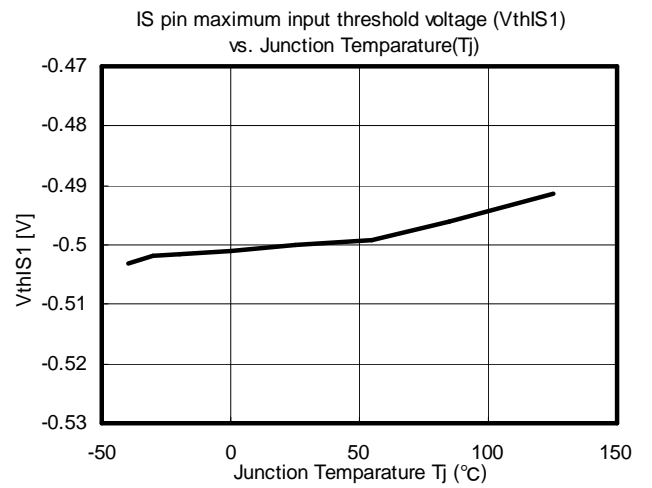
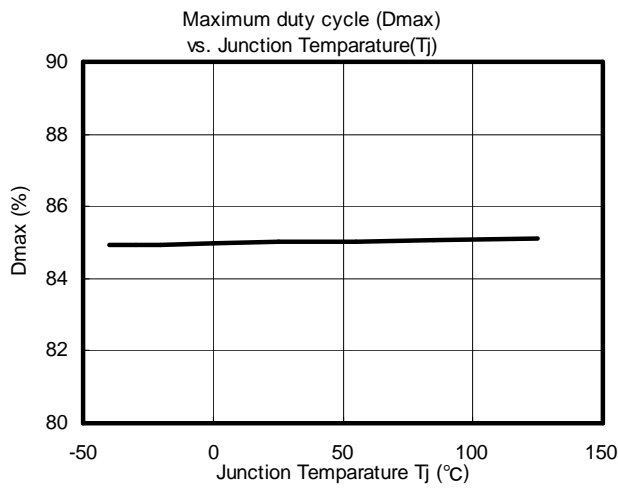
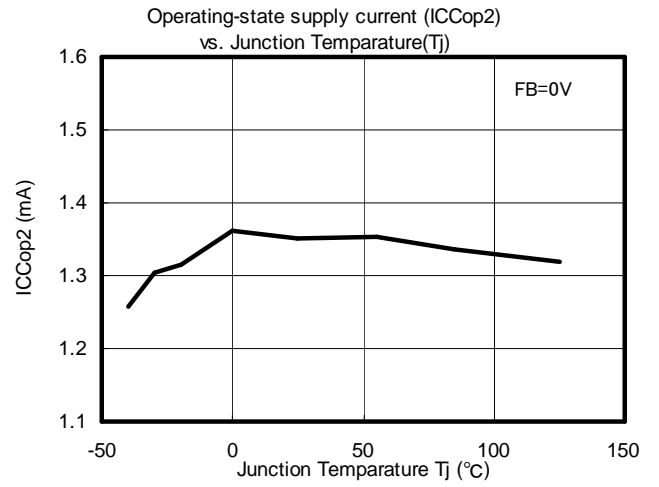
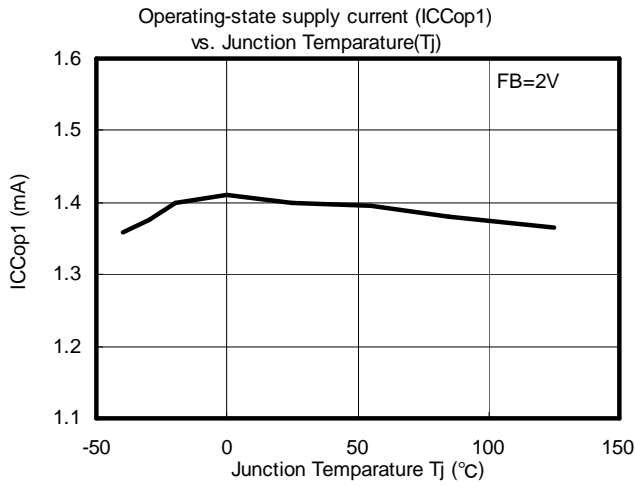
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Current of VH pin	IHrun	VH=450V,VFB=0V	60	100	140	uA
	IHstb	VH=120V, VCC=0V,VFB=0V	3.5	6.5	9.5	mA
		VH=120V,VCC=2 to 8V, VFB=0V	11	17	23	
		VH=120V,VCC=11V, VFB=0V	6	12	18	
		VH=120V,VCC=16V, VFB=0V	3.5	8	14	
Charge current for VCC pin	Ipre1	VCC=16V, VH=120V,VFB=0V	-14	-8	-3.5	mA
	Ipre2	VCC=11V, VH=120V,VFB=0V at Latch	-18	-12	-6	mA
Threshold voltage level at Brown-out (VH pin)	VthBO	VH pin = Decreasing	89	99	109	V
Threshold voltage level at Brown-in (VH pin)	VthBI	VH pin = Increasing	95	105	115	V
Brown-out delay time *1	TpdBO	VH=VthBO	30	50	70	ms
VCC voltage at Brown-out	VCCBH	VH=80V,VFB=2V Upper level	14	15.5	17	V
	VCCBL	VH=80V,VFB=2V Lower level	12	13.5	15	V
VCC voltage at Latch	VCCLHH	VH=120V,VFB=2V 1time clamp	13	14.5	16	V
	VCCLH	VH=120V,VFB=2V Upper level	12	13	14	V
	VCCLL	VH=120V,VFB=2V Lower level	11	12	13	V

**7. Characteristic Curves (DC Characteristics)**

- Unless otherwise specified, Ta=25 degree, Vcc=18V
- "+" shows sink and "-" shows source in current prescription.
- The data stated in this chapter are intended for giving typical IC characteristics and not for guaranteeing performance.







## 8. Operation of each block

### (1) Startup circuit

The IC integrates a startup circuit having withstood voltage of 750V to achieve low power consumption.

Fig.1 to Fig.3 shows connections.

Turning on the power, capacitor C2 connected to the VCC pin is charged and the voltage increases due to the current fed from the startup circuit to the VCC pin. If the ON threshold voltage ( $V_{cc} = 18V$  typ.) of the under-voltage lockout circuit (UVLO) is exceeded, the power for internal operation is turned on, and the IC starts operating.

If the VCC pin voltage exceeds the ON threshold voltage ( $V_{CCon} = 18V$  (typ)) and the IC starts operating, the startup circuit is shut down and the VH pin current decreases to several 10 to several 100 $\mu A$ .

RVH is connected in series to the VH pin to prevent the IC from being damaged by the surge voltage of the AC line.

Fig.1 shows a typical connection where the VH pin is connected to the half-wave rectifier circuit of AC input voltage.

The startup time of this connection is the longest in 3 types of connection.

Fig.2 shows the connection where the VH pin is connected to the full-wave rectifier circuit of AC input voltage. The startup time of this connection is approximately half of the connection shown in Fig.1.

Fig.3 shows the connection where the VH pin is connected to the back of rectification and smoothing of AC input voltage. The startup time of this connection is the shortest in 3 types. In this connection, however, even if the AC input voltage is shut down after the IC enters the latch mode, the voltage charged in C1 is kept impressed to the VH pin, requiring much time for the latch mode to be reset. It takes approximately several minutes to reset the latch mode, although the time varies depending on conditions.

If the overvoltage protection is actuated, causing the IC to enter the latch mode, then the startup circuit is subjected to ON/OFF control to maintain the VCC voltage within the 12V to 13V (typ) range. (P.19 8-(7) over voltage protection)

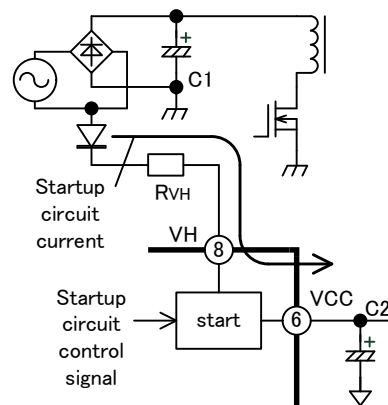


Fig.1 Startup circuit 1 (Half-wave)

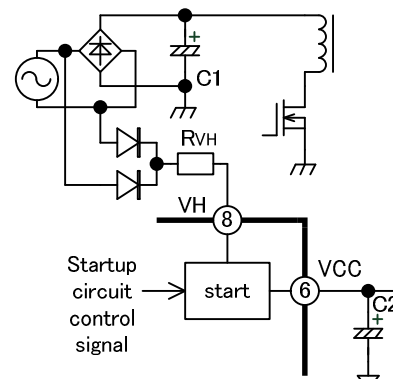


Fig.2 Startup circuit 2 (Full-wave)

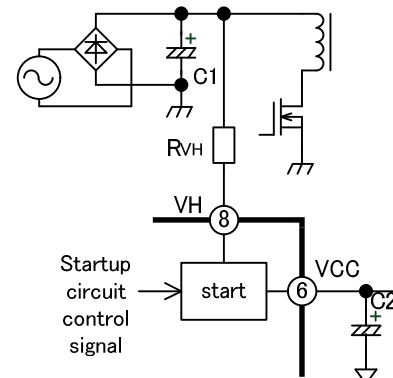


Fig.3 Startup circuit 3 (Rectification)

**(2)Oscillator**

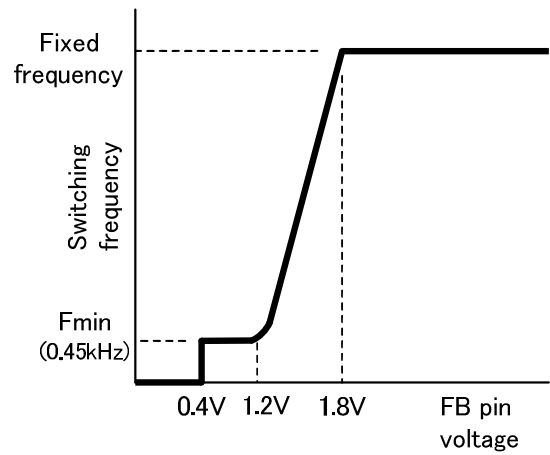
This oscillator is used to determine the switching frequency. The switching frequency in the normal operation mode is set to 65kHz (typ) within the IC.

To minimize the loss of power in the standby state, this IC is equipped with a function of automatically decreasing the switching frequency under light load.

When the FB pin voltage decreases down to 1.8V (typ) or lower under light load, the frequency decreases almost linearly proportional to the FB pin voltage. (See Fig.4) The minimum frequency, Fmin, has been set to 0.45kHz (typ).

When the load further decreases and thus the FB pin voltage decreases down to 0.4V (typ) or lower, the switching is stopped. (See one-shot circuit.)

In addition to trigger signals for determining switching frequency, the oscillator generates pulse signals for determining the maximum duty cycle and ramp signals for performing slope compensation.



**Fig.4 Oscillation frequency**

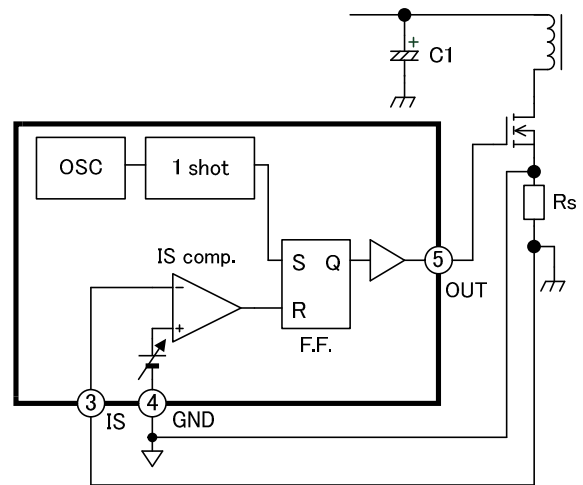
**Frequency diffusion (Spread spectrum)**

FA5626 perform frequency modulation of  $\pm 4.5$  kHz for switching frequency 65 kHz (during the operation in which the FB pin voltage is higher than 1.55 V.). This function enables more noise energy of the switching to disperse compared to the case with fixed frequency and obtains a conduction EMI reduction effect. While the reduction effect depends on the filter parts mounted on the power supply board, effective use of this function allows the reduction of the number of the filter parts and the constants.

**(3) Current comparator & PWM circuit**

The IC performs current mode control. Fig.5 shows a circuit block for basic operations, and Fig.6 shows a timing chart.

The polarity of the current detection voltage of the IS pin is negative. The GND of the IC is connected between the current detection resistor  $R_s$  and the MOSFET. (See Fig.5)



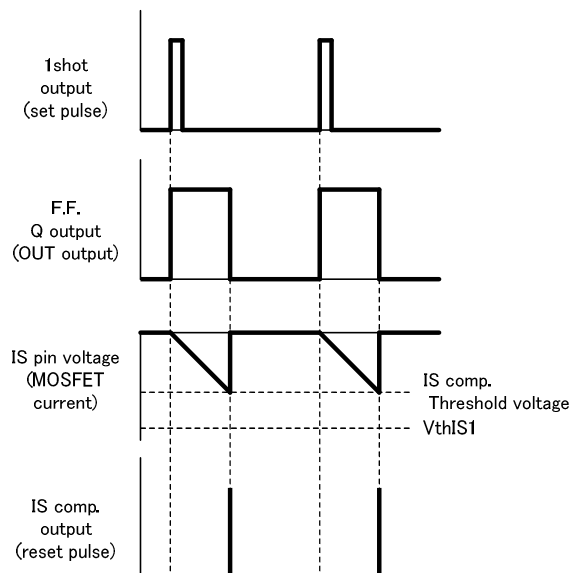
**Fig.5 Current mode basic operation circuit block**

A trigger signal having the switching frequency that is output from the oscillator is input to the PWM (F.F.) through the one-shot circuit as a set signal. Then the output of the PWM as well as the OUT pin voltage reaches the High state.

On the other hand, the current comparator (IS comp.) monitors the MOSFET current, and if the threshold voltage is reached, a reset signal is output. When a reset signal is input, the output of PWM (F.F.) as well as the OUT pin voltage reaches the Low state.

The ON pulse width of the OUT pin is thus controlled with the threshold voltage of the current comparator (IS comp.). The output is controlled by changing the threshold voltage of this IS comp. with feedback signals.

As shown in Fig.7, the FB pin voltage is level-shifted by a reverse amplifier and input into the current comparator (IS comp.) as the threshold voltage. In addition, -0.5V (typ) reference voltage is input inside the IC to regulate the maximum input threshold voltage of the IS pin,  $V_{thIS1}$  (over current control threshold).



**Fig.6 Current mode basic operation timing chart**



The reverse amplifier output or the maximum IS pin input threshold voltage,  $V_{thIS1}$ , whichever is higher, is given precedence as the IS pin threshold voltage.

(Example: When the output of the reverse amplifier is -0.2V in a product whose maximum threshold voltage of the IS pin,  $V_{thIS1}$ , is -0.5V, the output of the reverse amplifier is given precedence and thus the current comparator is reversed when the IS pin voltage reaches -0.2V.)

In normal operation, the output voltage of the power supply is maintained constant by changing the threshold voltage of the current comparator via the FB pin voltage.

When the output voltage decreases, the feedback circuit increases the FB voltage to allow the threshold voltage of the current comparator to scale out to Low, thus increasing the MOSFET current.

The maximum input threshold voltage of the IS pin,  $V_{thIS1}$  (-0.5V typ) controls the maximum current of the MOSFET. If the FB pin voltage increases under overload, the output of the reverse amplifier scales out to Low, decreasing down to lower than  $V_{thIS1}$ . The threshold voltage of the IS pin is thus controlled not to exceed  $V_{thIS1}$ .

The oscillator outputs pulses for determining the maximum duty cycle. Using these pulses, the maximum duty cycle has been set to 85% (typ).

**Reduction of dependency of OCP on input voltage**

This IC has an improved OCP function which changes the maximum input threshold voltage (the current limit threshold voltage) so that OCP dependency on the input voltage will be compensated.

The maximum input threshold voltage is lowers by 5% when  $V_H$  pin voltage ( $V_{VH}$ ) is over 148Vdc (approx. 105Vac) if  $V_H$  pin is connected to AC line.

$V_{thIS1} = -0.525V$  typ. when  $V_{VH} < V_{HVTH2}$

$V_{thIS1} = -0.500V$  typ. when  $V_{VH} \geq V_{HVTH2}$

(See p. 24 "9-(7) Reduction of dependency of overload detection level on input voltage".)

**(4) One shot circuit (minimum ON width)**

When the MOSFET is turned on, a surge current is generated due to discharge corresponding to the capacitance of the main circuit and gate drive current. If this surge current reaches the IS pin threshold voltage, the current comparator output is reversed, and consequently normal pulses may not be generated from the OUT pin.

To avoid this phenomenon, a minimum ON width of OUT pin output is set within the one-shot circuit block of the IC.

If a trigger signal having the switching frequency is input from the oscillator, a pulse having a specific width is output as a PWM latch (F.F.) set signal.

Since the set signal has priority over the input signal of the PWM latch, the output of the PWM latch (F.F.) is not reversed while the set signal from the one-shot circuit is being input, even if a reset signal is input from the current comparator (IS comp.) (See Fig.5)

As a result, the input to the IS pin is kept invalid for the specified period of time immediately after the output pulse is generated from the OUT pin (minimum ON width), and made not to respond to the surge current at turn-on. (See Fig.8)

This minimum ON width function eliminates the need of a

noise filter for the IS pin in principle.

The minimum ON width is usually set to 1250ns or 1700ns (typ) in normal operations, and to 280ns (typ) at startup or rebooting to prevent the transient MOSFET drain voltage from surging.

In addition, an exclusive comparator is integrated to keep the output pulse at zero under no load. (See Fig.9)

This comparator reverses its output when the FB pin voltage decreases down to 400mV (typ), preventing a set pulse to be input to the PWM latch (F.F.). The output is thus maintained in Low state and switching is stopped.

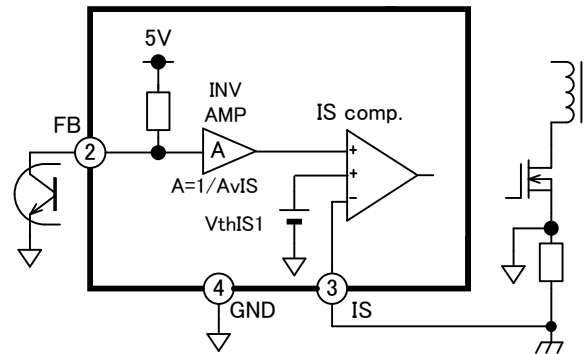


Fig.7 Current comparator

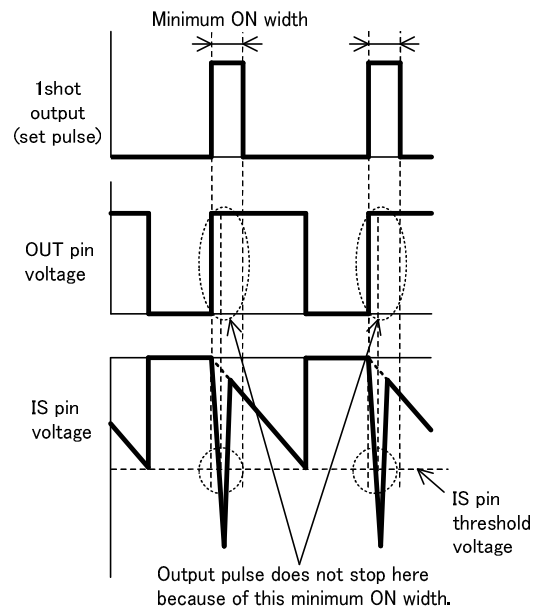


Fig.8 Minimum ON width

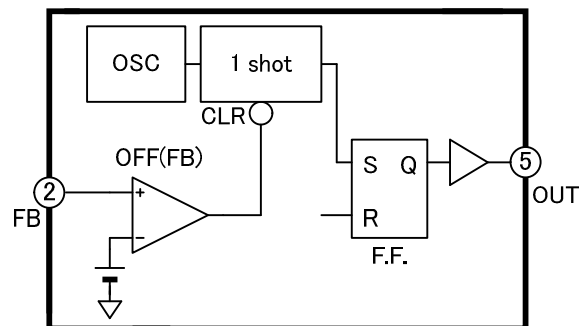


Fig.9 Output shutdown function of FB pin

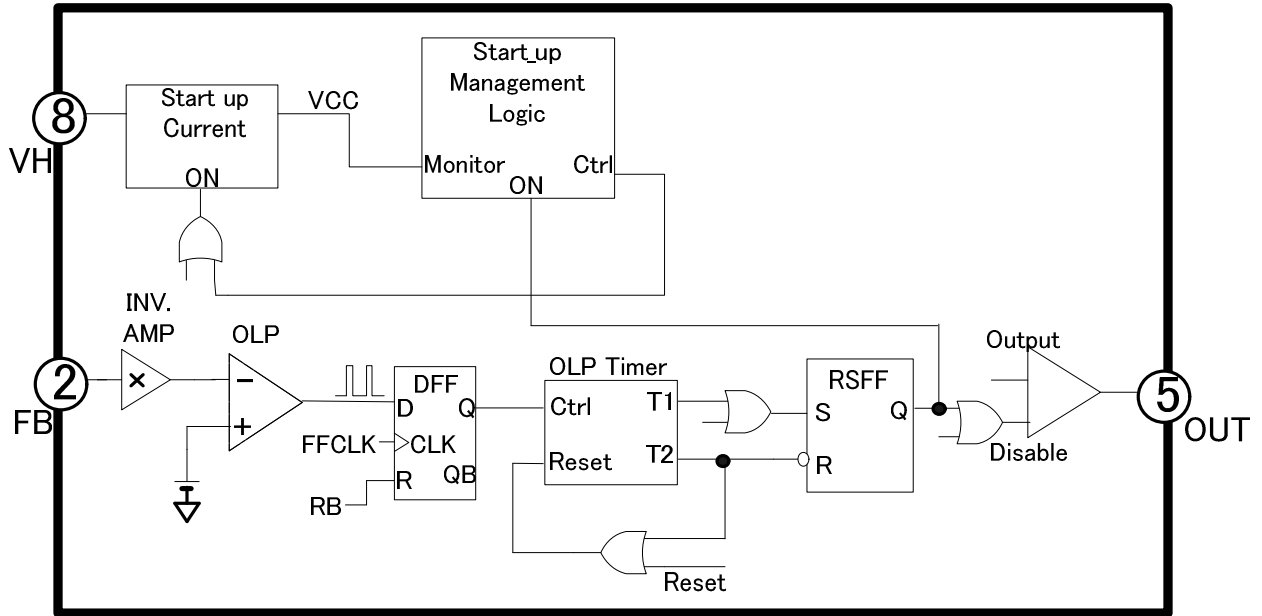
**(5) Overload protection circuit**

FA5626 integrates auto-restart mode overload protection function.

Fig. 10 shows the circuit block diagram and Fig. 11 shows the protection timing chart.

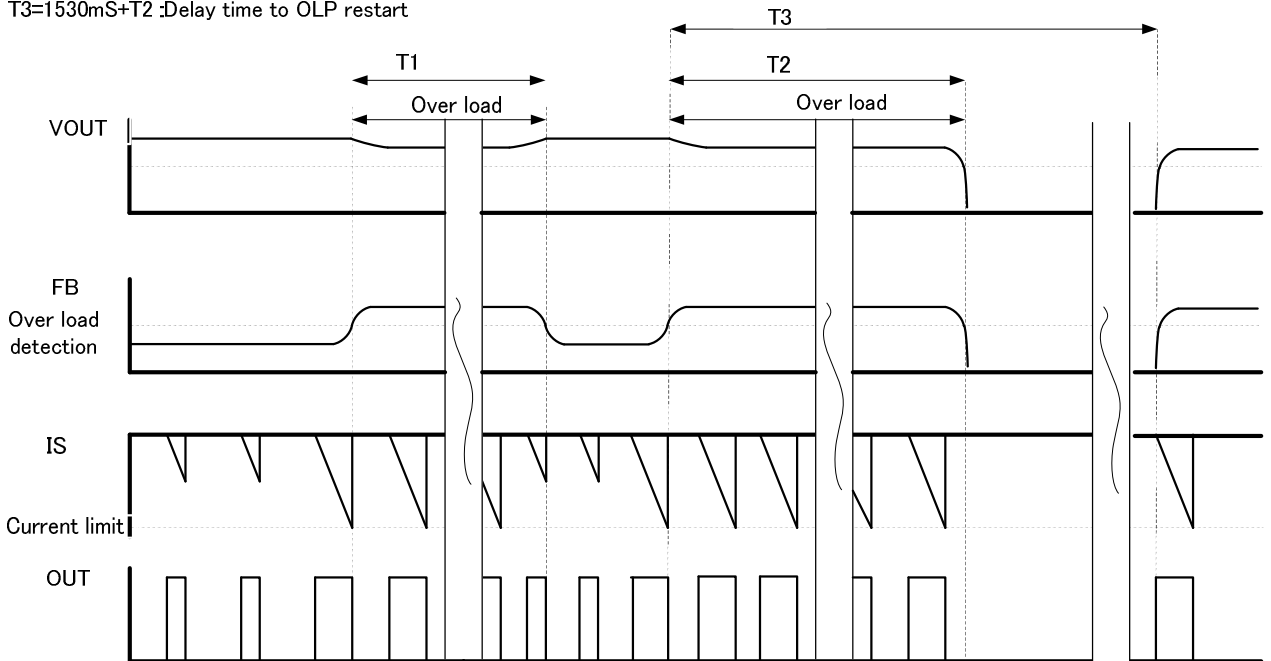
When output current increases by the overload, MOSFET current is limited by the maximum threshold voltage (-0.5V typ.) of IS pin. The output voltage is drops because of current limit and FB pin voltage rises. When FB pin voltage is over the threshold voltage ( $V_{thOLP}$ ), overload is detected. After the overload is detected, internal OLP timer starts counting for the delay time. When OLP delay time (70 msec typ.) has elapsed, the IC stops switching operation and MOSFET is kept off state. When the self-return wait time (1530 ms typ.) has elapsed thereafter, IC re-starts switching operation automatically. IC repeats stop and restart switching operation until overload condition is removed.

Vcc voltage is maintained at between 12V and 13V by ON/OFF control of startup circuit when IC stops switching operation at overload.



**Fig.10 Overload protection circuit (auto recovery)**

T1<70mS:keep operating  
 T2>70mS:Delay time to OLP stop  
 T3=1530mS+T2 :Delay time to OLP restart



**Fig.11 Overload protection timing chart (auto recovery)**

**(6) Short circuit detection**

FA5626 has a protection function for output short-circuit without delay time. If output of PSU is shorted, FB pin voltage goes high. In addition, Vcc voltage drops because auxiliary winding voltage almost zero. IC stops switching operation at the instance when IC detects that FB pin voltage exceeds overload detection voltage and Vcc drops below Vthshort (11V typ.). As in the case of overload, IC restart switching operation after 1600ms and repeats it until short circuit condition is removed.

**(7)Over voltage protection circuit**

The IC integrates an overvoltage protection circuit for monitoring the VCC pin voltage. (See Fig.12) If the VCC voltage increases and exceeds 26V typ, which is the reference voltage of the comparator (OVP), the comparator output is reversed to High level, setting the latch circuit to perform latch shutdown. At this time, the startup circuit is subjected to ON/OFF control to maintain the latch mode, thus keeping the VCC voltage within the 12V or 13V (typ) range. To cancel the latch mode, shut down the input voltage to cause brownout, as in the case of the overload protection.(latch type) Since 65μs (typ) delay time has been set to the set input of the latch circuit, the latch mode is not entered even if the VCC pin exceeds the detection voltage temporarily.

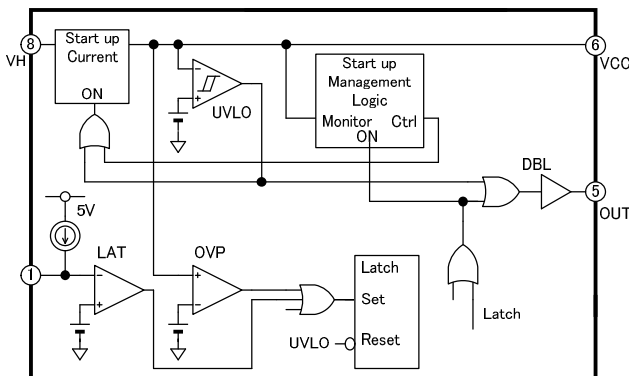


Fig.14 Overvoltage protection circuit

**(8) Latch shutdown circuit by an external signal**

The LAT pin is equipped with a latch shutdown function. (See Fig.13) By decreasing the LAT pin voltage to 1.05V or lower, the IC enters the latch mode. To cancel the latch mode, interrupt the input voltage, thus decreasing the VCC voltage to the OFF threshold voltage (9.0V typ.) or lower. LAT function operates after LAT pin voltage rises to more than 2.1V once. If the external latch shutdown function by the LAT pin is not to be used, connect a capacitor only.

**-Overheat protection-**

Connect an NTC thermistor to the LAT pin to use the overheat protective function. (See Fig.13, P23 9-(4) Lat pin)

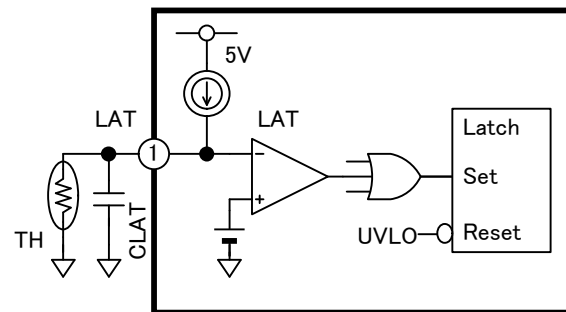


Fig.13 Overheat protection function using a thermistor

**(9) Under voltage lockout circuit (VCC pin)**

The IC integrates an under voltage lockout (UVLO) function to prevent circuit malfunction that might occur when power supply voltage decreases. When the VCC voltage increases from 0V and reaches 18V (typ), the circuit starts operating. When the VCC decreases down to 9V (typ), the circuit stops operating. In a state in which the under voltage lockout function is actuated to stop IC operation, the OUT pin is forcibly made to enter the Low state. The latch mode of the protection circuit is also reset.

**(10)Output circuit**

The push/pull structure output circuit drives the MOSFET directly. The peak output current of the OUT pin is 0.5A (source) and 1.0A (sink) in the maximum absolute ratings. In a state in which the IC is stopped in the under voltage lockout circuit or operation is suspended in the latch mode, or in an auto reset wait state by overload protection function, the OUT pin is brought into the Low level, and the MOSFET is interrupted.

**(11)Brown-out**

FA5626 has a brown-out function that stops switching operation when the AC input voltage drops below normal operating voltage. Fig.14 shows input voltage waveform of VH pin. When VH pin voltage reached brown-in threshold voltage (DC 105V typ.), switching operation is started.

When VH pin voltage drops below brown-out threshold voltage for longer than delay timer, brown-out function stops switching operation.

In case of half wave input, the brownout timer is counted because VH pin voltage drops until 0 V at every period.

But brown-out function doesn't operate because brown-out delay time longer than the half wave period.

Brown-out delay time depends on the oscillation frequency as shown in Fig.15.

Vcc voltage is maintained at between 12V and 13V by ON/OFF control of startup circuit when IC stops switching operation at brown-out function, and IC restarts after VH pin voltage reached brown-in threshold voltage .

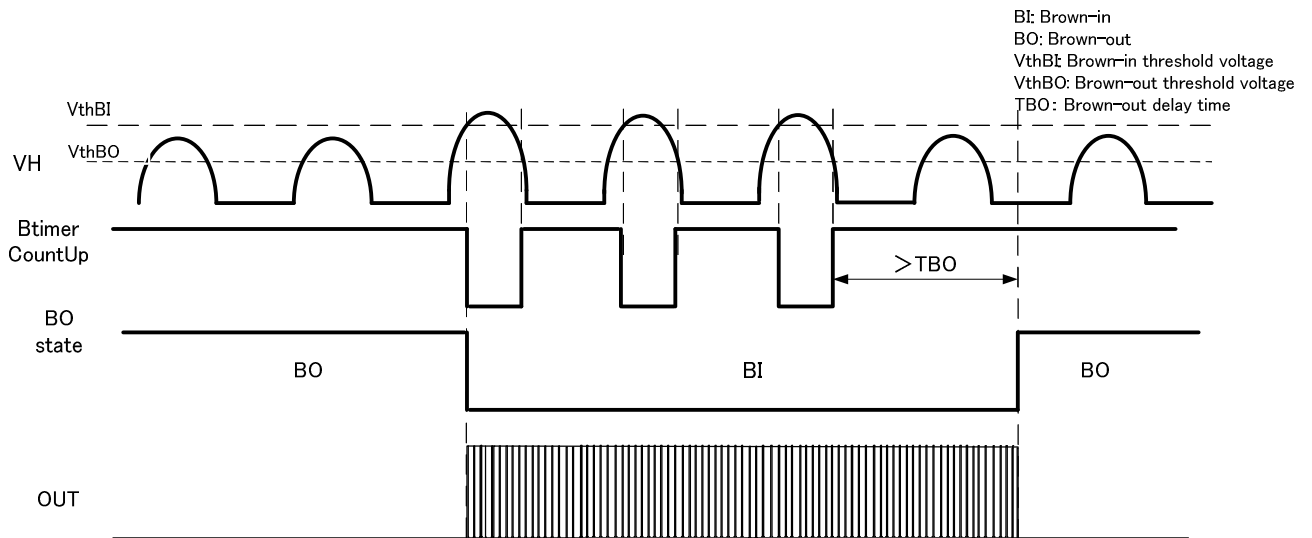


Fig.14 Brown-out operation

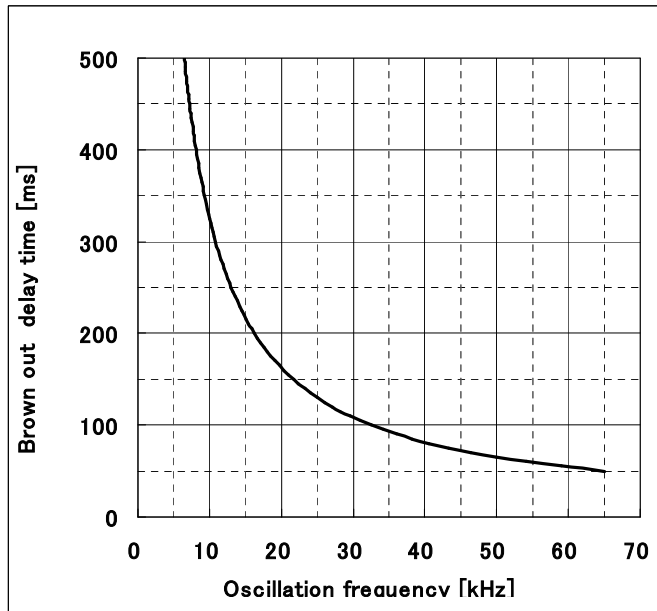


Fig.15 Brown-out delay time

**(12)Soft-start**

This IC has an adjustable soft start function by LAT pin capacitor.

Fig. 16 shows the soft-start timing chart at start up. (1)(2)(3) are soft start period in Fig.16.

When VCC voltage reaches uvlo on threshold voltage , LAT pin voltage rises gradually, and switching starts at LAT pin voltage 2.1 V.

In period (1), a minimum ON width pulse are output 32 times after switching has started. The minimum ON width pulses avoids Vds surge voltage of power MOSFET at start up.

In period (2), LAT pin voltage is discharged from 2.5 V to 2.0 V by constant current (70uA). In this period, the minimum ON width pluses are output continuously.

Period (3) is effective soft-start period.

In period (3), the pulse width gradually widen from minimum ON width.

The soft-start time can be adjusted by capacitor connected to LAT pin.

Approximate effective soft start time (period(3)) can be calculated using the following expression.

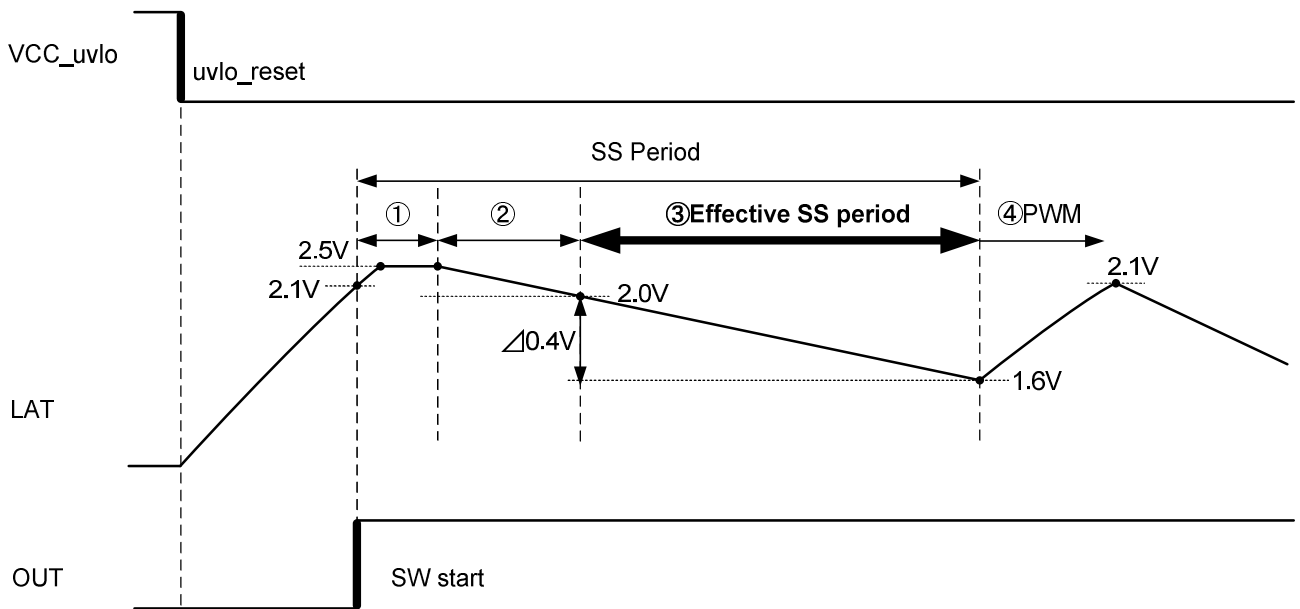
$$T_{ss} = 0.4 \times CLAT / I_{lat}$$

$T_{ss}$  :Soft-start time [sec]

$CLAT$ : Capacitor connected to LAT pin [ $\mu$ F]

$I_{lat}$  :LAT pin source current [ $\mu$ A] (70uA typ.)

(4) PWM operation start



**Fig.16 Soft-start operation**

**9. Advice for designing**

**(1) Start up**

To properly start or stop the power supply, a capacitor having appropriate capacitance must be selected.

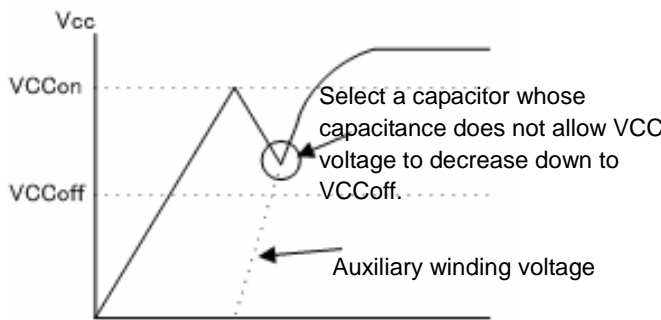
Fig.17 shows the VCC voltage at the time of startup when an appropriate capacitor is connected.

When the power is turned on, the capacitor of the VCC is charged with the current supplied from the startup circuit, and the voltage increases.

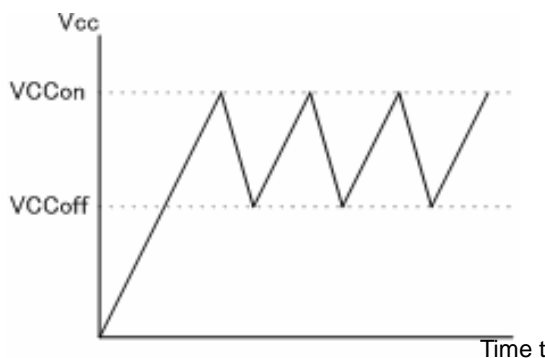
When the VCC reaches the ON threshold voltage, the IC starts operating. The IC is operated based on the voltage supplied from the auxiliary winding. Note that during the period immediately after startup until the voltage of the auxiliary winding starts up, the VCC decreases. Select a capacitor for the VCC that does not allow the VCC to decrease down to the OFF threshold voltage.

Specifically, a VCC pin capacitor whose OFF threshold voltage is 11V or higher is recommended.

If the capacitance of the VCC pin is too small, VCC decreases to lower than the OFF threshold voltage before the voltage of the auxiliary winding starts up as shown by Fig.18. In this case, the VCC repeats up/down operation between ON and OFF threshold voltages, and consequently the power supply cannot be turned on.



**Fig.17 VCC pin voltage at startup**



**Fig.18 VCC pin voltage at startup (when capacitance is too small)**

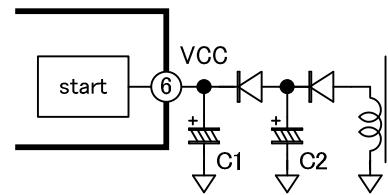
**(2) VCC hold time**

To prevent the VCC pin voltage from decreasing to lower than the UVLO OFF threshold voltage due to sudden load change and other reasons, it may be desirable that the capacitance of the capacitor to be connected to the VCC pin be made larger.

However, if the capacitance of the capacitor of the VCC pin is increased, the startup time is made longer.

In such cases, the circuit shown in Fig.19 can balance the capacitance and the startup time.

By setting C1 to less than C2, the startup time can be kept short. Since current is supplied via C2 after startup, the VCC pin voltage hold time can be kept long even under sudden change conditions.



**Fig.19 VCC circuit**

**(3) Gate drive circuit**

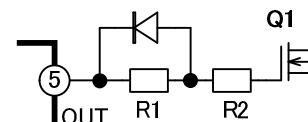
To adjust switching speed and prevent vibration of the gate pin, a resistor is connected between the MOSFET gate pin and the OUT pin of the IC in general.

In some cases, driving current for turning on the MOSFET and that for turning it off are required to be determined separately.

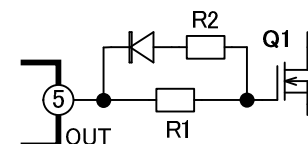
In this case, connect a gate drive circuit shown in Fig.20 or 21 between the gate pin of the MOSFET and the OUT pin.

In Fig.20, the current is limited by R1 and R2 when the power is turned on, while the current is limited only by R2 when it is turned off.

In Fig.21, the current is limited only by R1 when the power is turned on, while the current is limited by R1 and R2 connected in parallel when the power is turned off.



**Fig.20 Gate drive circuit (1)**

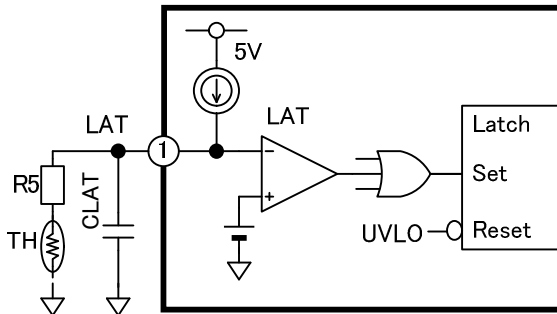


**Fig.21 Gate drive circuit (2)**

**(4) LAT pin**

• To perform overheat protection using an NTC thermistor  
 As shown in Fig.22, thermistor TH1 is connected to the LAT pin to perform overheat protection (latch shutdown). Since the LAT pin source current is 70μA (Typ.), select TH1 whose resistor Rth satisfies the following expression at the desired overheat protection temperature. If temperature setting for overheat protection is not feasible with TH1 only, connect an additional resistor (R5) in series for adjustment.

$$R_{th} @ \text{LAT} + R5 \leq 1.05V / 70\mu A \approx 15.0k\Omega$$

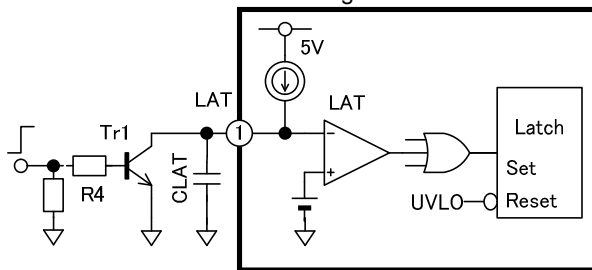


**Fig.22 Overheat protection function using a thermistor**

• To perform latch shutdown using independent abnormality detection signal

As shown in Fig. 23, NPN transistor Tr1 is connected to LAT pin, and a detection signal is inputted to the base of Tr1. The polarity of the input signal must be such that the level will go high at an error.

Note that, because a constant current flows from LAT pin, there is no need of a circuit for clamping LAT pin voltage to above latch shutoff threshold voltage when normal.

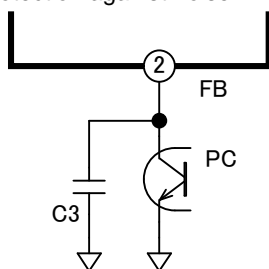


**Fig. 23 Latch shutdown function by an external signal**

**(5) Feedback**

Fig.24 shows the circuit configuration of the FB pin. A photo-coupler PC is connected as a feedback circuit that monitors the output voltage and performs PWM control.

This signal gives threshold voltage for the current comparator. Consequently, if noise is added to this signal, the output pulses are disturbed. Capacitor C3 is generally connected for protection against noise.



**Fig.24 FB pin circuit configuration**

**(6) Current sensing unit**

As described in 8-(4) One-shot circuit, the minimum ON width is set for this IC to minimize malfunction due to surge current that occurs when the power MOSFET is turned on. However, if the surge current that occurs at the time of power ON is large, or noise is applied externally at the time of power ON, malfunction might occur.

In such cases, add RC filters C6 and R7 as shown in Fig.25.

Determine the CR filter constants according to the cutoff frequency and time constant.

The cutoff frequency is given by:

$$f_c = 1 / (2 \times \pi \times C6 \times R7)$$

This frequency must be greater than IC operation frequency of 65 kHz.

Set the RC time constant to 500 nsec or smaller.

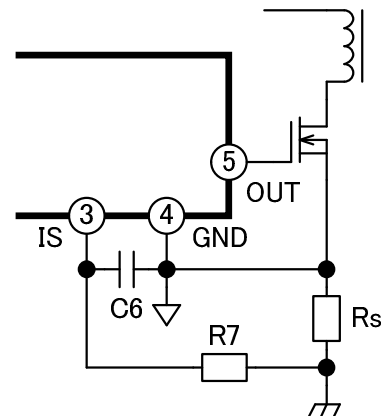
Note that, by the input bias current at IS pin, R7 is subjected to offset with respect to the overload detection threshold voltage. Do not connect an excessive value. Otherwise, the overload detection value may vary considerably.

Recommendations:

R7 = 1 kΩ.

100pF ≤ C6 ≤ 470pF.

To obtain an optimum effect in function, position capacitor C6 as near IC as possible, and minimize the wiring length.



**Fig.25 IS pin filter**

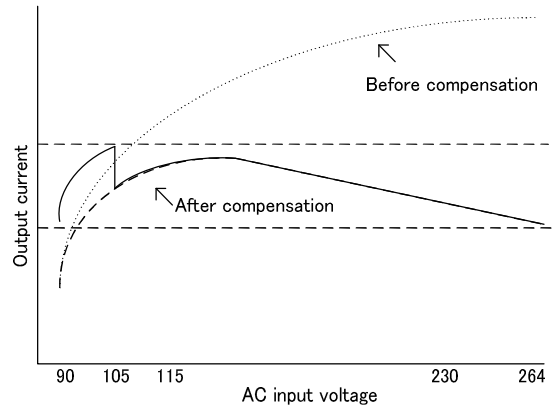
**(7) Reduction of overload detection level on input voltage**

Output current at overload depends on the input voltage because of propagation delay of current limit by IS pin. (Fig.26) The dependency will be compensated by connecting resistor R9 between the auxiliary winding and IS pin. (Fig. 27)

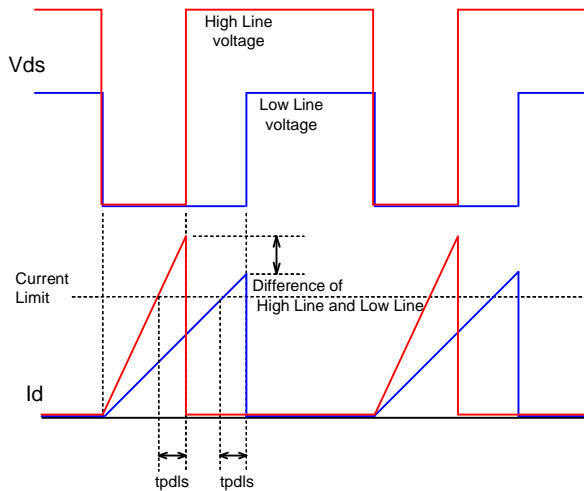
A negative voltage of the auxiliary winding is proportional to the input voltage. Current sense of this IC is negative voltage; therefore line compensation for overload can be achieved by negative auxiliary voltage.

This design can reduce the power loss of the compensation resistor. For example, in case of 1kΩ of resistor R7, 100 kΩ to 1 MΩ is recommended for resistor R9.

Line compensation becomes large as R9 is decreased. (Fig.28)



**Fig.28 Overload detection level on input voltage (2)**



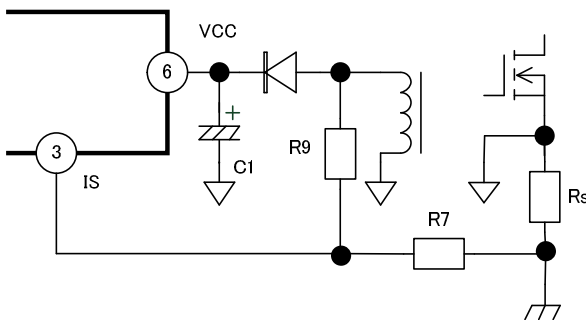
**Fig.26 Overload detection level of input voltage (1)**

**(8) Input power improvement at light load**

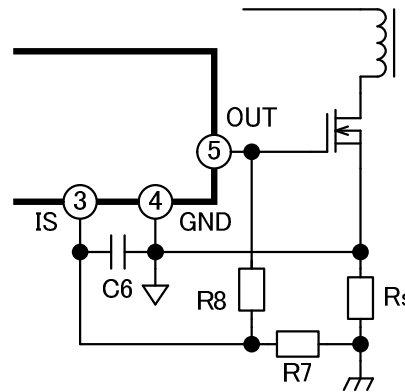
FA5626 can reduce the standby power by lowering the oscillation frequency at light load.

However, in some case internal function of IC may not reduce standby power enough. In such a case, connect resistor R8 between OUT pin and IS pin.

If resistor R7 is 1 kΩ for example, select resistance R8 between several hundred kΩ and 1 MΩ.



**Fig.27 Input voltage compensation circuit of overload detection level**



**Fig.29 Compensation circuit of Input power improvement at light load**



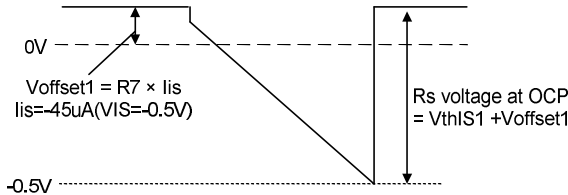
**(9) Approximation of over current detection intensity**

The expression here explains how to calculate the over current detection as below.

**Case where only RC filter is connected (See Fig. 25)**

On IS pin voltage, offset voltage Voffset1 by IS pin input bias current of 45 μA (IS = -0.5 V) appears at resistor R7. In this case, the current limit voltage at resistor Rs is as follows,

$$R_s \text{ voltage at OCP} = V_{thIS1} + V_{offset1}$$



**Fig.30 IS pin voltage when RC filter only is connected.**

Example)

When AC input voltage Vin is a minimum, the primary current will be a maximum.

$$D = \frac{\frac{N_p}{N_s} \times V_o}{\sqrt{2} \times V_{in} + \frac{N_p}{N_s} \times V_o}$$

$$I_{Lp} = \frac{P_o}{\sqrt{2} \times V_{in} \times D \times \eta} + \frac{\sqrt{2} \times V_{in} \times D}{2 \times L_p \times f_{sw}}$$

- D : Duty , Vin :AC Input voltage (rms)
- Np : Turn Number of primary winding
- Ns : Turn Number of secondary winding
- Vo : Output voltage
- Po : Output power (overload detection power)
- η : Efficiency
- Fsw : Switching frequency
- Lp: Primary side inductance

Example) Vin=85V, Np=28T, Ns=5T, Lp=340uH, fsw=65kHz, η=0.9, Vo=19V, Po=100W, R7=1kΩ

$$D = \frac{\frac{28}{5} \times 19}{\sqrt{2} \times 85 + \frac{28}{5} \times 19} = 0.47$$

$$I_{Lp} = \frac{100}{\sqrt{2} \times 85 \times 0.47 \times 0.9} + \frac{\sqrt{2} \times 85 \times 0.47}{2 \times 340 \times 65k} = 3.24$$

$$R_s = \frac{|V_{thIS1} + V_{offset1}|}{I_{Lp}} = \frac{|-0.5 + (-45 \mu A \times 1k)|}{3.24} = 0.168$$

Rs = 0.17 Ω W has to be connected.

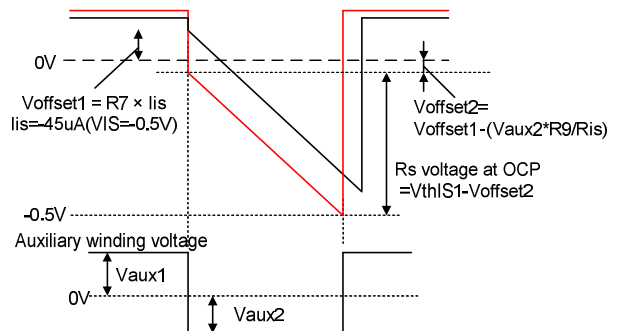
However, in actual circuit, output current at OLP shows tendency to be slightly larger than calculated current because of the propagation delay in IC, etc. Please decide Rs value after test in the actual circuit.

**Case where input voltage dependency reducing resistor R9 is connected (as in Fig. 27)**

If an input voltage dependency reducing resistor is connected, IS pin voltage changes as shown in Fig. 31. In this case, the overload detection voltage level that appears at IS pin is as follows, Rs voltage at OCP = VthIS1 - Voffset2

Example 1) R7=1kΩ, R9=330kΩ, Vaux2=-20V  
 Voffset2=Voffset1-((Vaux2/R9)×R7)  
 =(-45uA×1k) - ((-20V/330k)×1k)= 15.6mV  
 Rs voltage at OCP= -0.5V - (15.6mV)=-0.516V

Example 2) R7=1kΩ, R9=680kΩ, Vaux2=-20V  
 Voffset2=(-45uA×1k) - ((-20V/680k)×1k)= -15.6mV  
 Rs voltage at OCP = -0.5V -(-15.6mV)= -0.484V

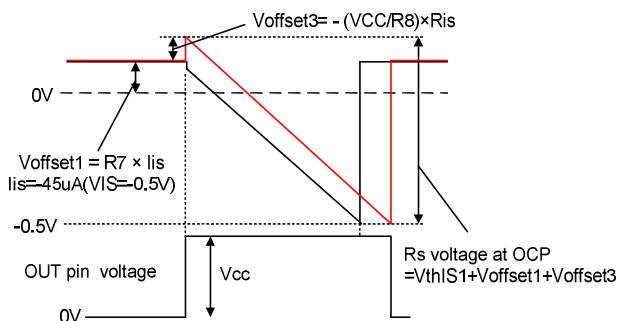


**Fig. 31 IS pin voltage when correction resistor R9 is connected.**

**Case where R8 for input power improvement at light load is connected (See Fig. 29)**

If an input power improvement at light load is applied, the waveform of IS pin voltage changes as shown in Fig. 32. In this case, the current limit voltage at Rs is as follows, Rs voltage at OCP = VthIS1 + Voffset1 + Voffset3

Example) R7=1kΩ, R8=1.0MΩ, VCC=18V  
 Voffset1=-45mV  
 Voffset3=-((18/1.0MΩ)×1k)=-0.018V  
 Rs voltage at OCP = -0.5V - 45mV - 0.018V  
 = -0.563V



**Fig. 32 IS pin voltage when correcting resistor R8 is connected.**

### (10) Prevention of malfunction due to negative potential of the pin

If large negative voltage is applied to each pin of the IC, the parasitic element within the IC may be actuated, thus causing malfunction to occur. Be sure to maintain the voltage to be applied to each pin within the maximum absolute ratings.

### (11) Loss calculation

To use the IC within its ratings, the loss of the IC may have to be found. However, it is not feasible to measure loss directly. The following is an example of finding a rough value of loss by calculation.

The rough value of the total loss of the IC,  $P_d$ , can be calculated using the following expression:

$$P_d \approx VCC \times (IC_{Cop1} + Q_g \times f_{sw}) + V_{VH} \times I_{Hrun}$$

where,

$V_{VH}$ : voltage to be applied to the VH pin,

$I_{Hrun}$ : current fed to the VH pin during operation,

$VCC$ : power voltage,

$IC_{Cop1}$ : Consumption current of the IC

$Q_g$ : electrical charge to be input to the MOSFET gate used, and

$f_{sw}$ : switching frequency.

A rough value can be found using the above expression, and the total loss found by the calculation,  $P_d$ , is slightly larger than the actual value.

Be sure to take into consideration that each characteristic value varies depending on temperatures and other factors.

Example:

When the VH pin is connected to a half-wave rectifier circuit with 100VAC input, the average voltage to be applied to the VH pin is calculated to be approximately 45V, and the average current to be fed to the VH pin is approximately 130 $\mu$ A;

Furthermore, assuming that  $T_j = 25^\circ\text{C}$ ,  $VCC = 18\text{V}$ , and  $Q_g = 80\text{nC}$ , and based on

$$I_{Hrun} = 100\mu\text{A (typ.)}$$

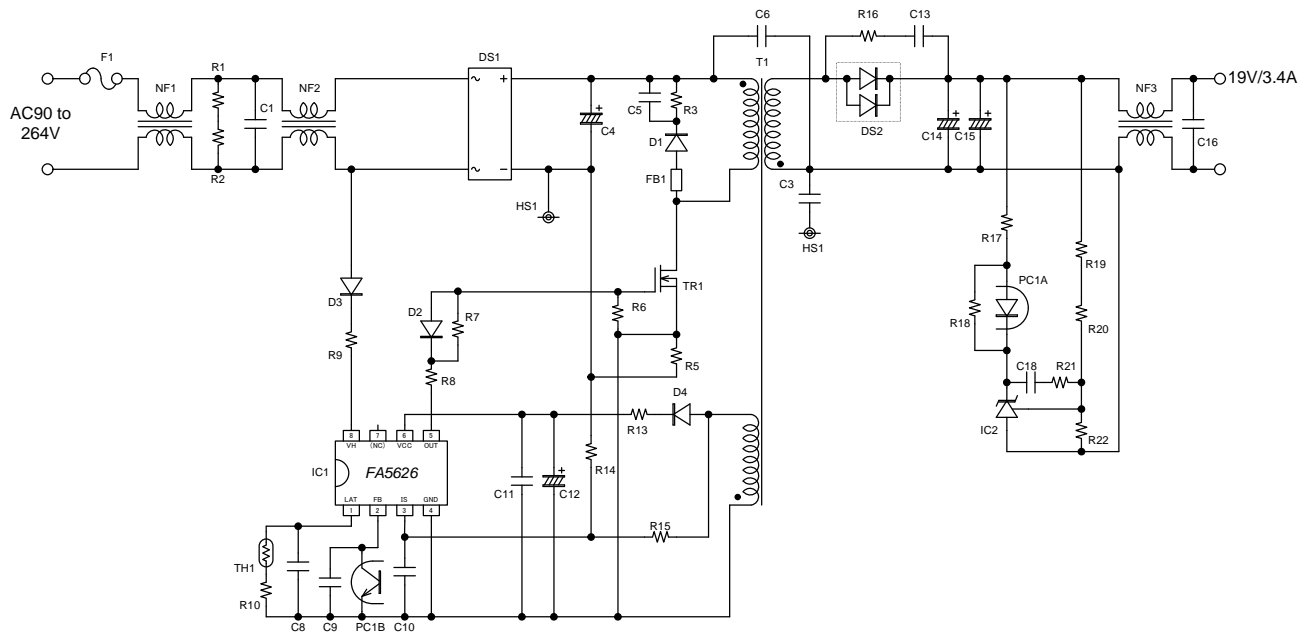
$$IC_{Cop1} = 1.4\text{mA (typ.)}$$

$$f_{sw} = 65\text{kHz (typ.)}$$

the loss of the IC having standard characteristics can be calculated as follows:

$$\begin{aligned} P_d &\approx 18\text{V} \times (1.4\text{mA} + 80\text{nC} \times 65\text{kHz}) + 45\text{V} \times 100\mu\text{A} \\ &\approx 123\text{mW} \end{aligned}$$

**10. Application circuit example**



Caution)

- 1) This application circuit example shows typical directions for use of this IC for reference and does not guarantee the operation and characteristics.
- 2) VH Pin is connected to near by diode bridge (DS1) to avoid VH Pin's surge voltage it happens by change of startup current when startup circuit repeats on-off operating.
- 3) Please connect the diode and resistance with the series between the bulk capacitor or the rectified AC line so that VH Pin must not become a negative voltage.