

# HB56G19 Series

1,048,576-Word x 9-Bit High Density Dynamic RAM Module

## DESCRIPTION

The HB56G19 is a 1M x 9 dynamic RAM module, mounted two 4 Mbit DRAM (HM514400AS) sealed in SOJ package and 1 Mbit DRAM (HM511000AJP) sealed in SOJ package. An outline of the HB56G19 is 30-pin single in-line package having lead types (HB56G19A), socket type (HB56G19B/GB). Therefore, the HB56G19 makes high density mounting possible without surface mount technology. The HB56G19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

## FEATURES

- 30-pin Single In-line Package  
Lead Pitch ..... 2.54mm
- Single 5V (± 10%) Supply
- High Speed  
Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation  
Active Mode ..... 1705 mW/1540 mW/  
1375 mW/1210 mW (max)  
Standby Mode ..... 33 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 2 Variations of Refresh  
RAS Only Refresh  
CAS Before RAS Refresh
- TTL Compatible

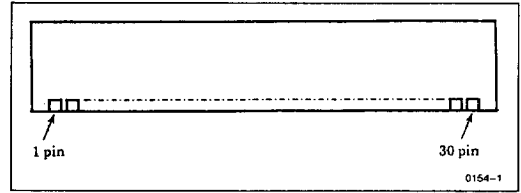
## ORDERING INFORMATION

Part No.	Access Time	Package
HB56G19A-6A	60 ns	30-pin SIP Low Profile Lead Type
HB56G19A-7A	70 ns	
HB56G19A-8A	80 ns	
HB56G19A-10A	100 ns	
HB56G19B/GB-6A	60 ns	30-pin SIP Socket Type
HB56G19B/GB-7A	70 ns	
HB56G19B/GB-8A	80 ns	
HB56G19B/GB-10A	100 ns	

Note: Following the specification of the contact pads.

HB56G19B-XX :solder  
HB56G19GB-XX :gold

## PIN OUT



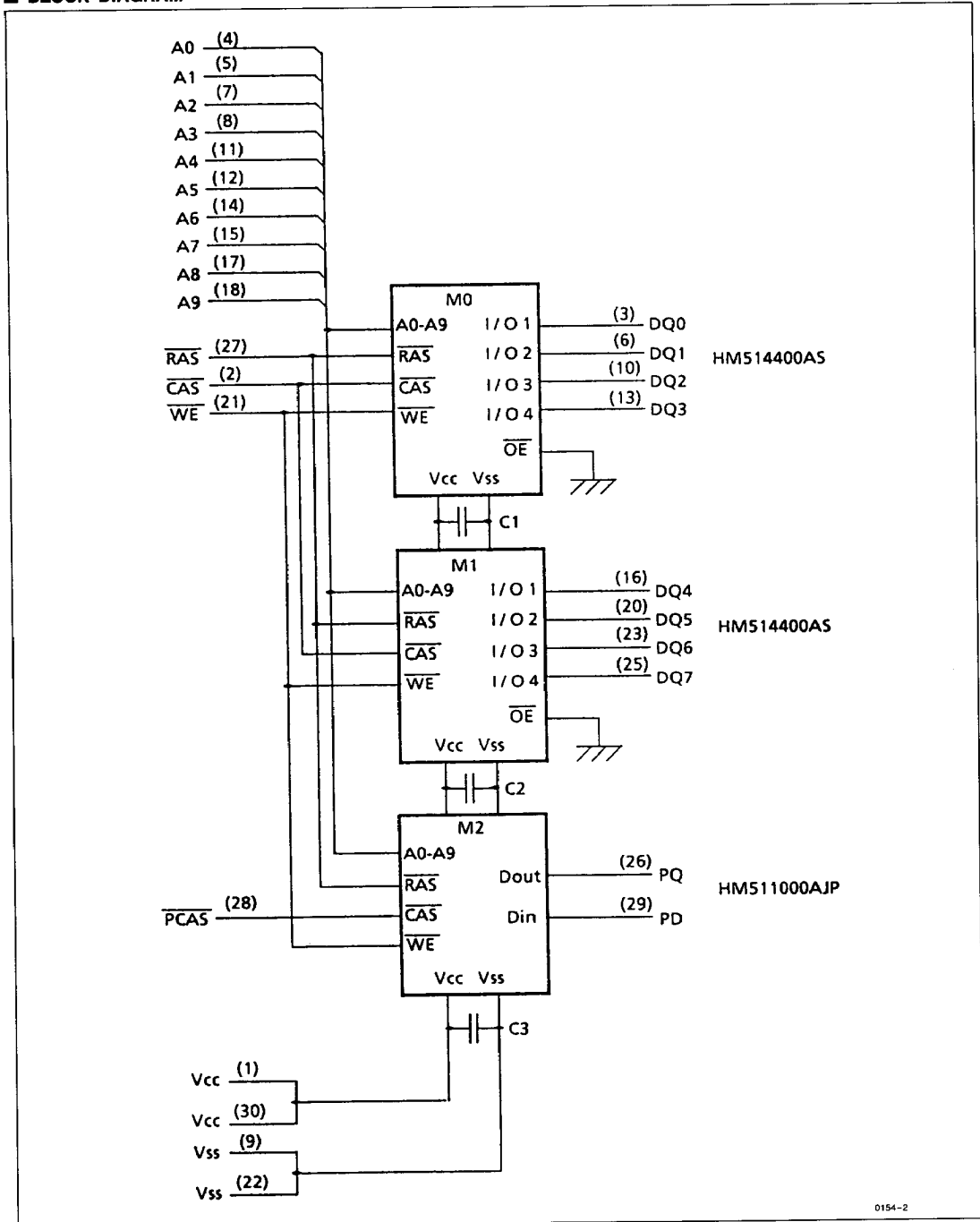
Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>CC</sub>	16	DQ <sub>4</sub>
2	$\overline{\text{CAS}}$	17	A <sub>8</sub>
3	DQ <sub>0</sub>	18	A <sub>9</sub>
4	A <sub>0</sub>	19	NC
5	A <sub>1</sub>	20	DQ <sub>5</sub>
6	DQ <sub>1</sub>	21	$\overline{\text{WE}}$
7	A <sub>2</sub>	22	V <sub>SS</sub>
8	A <sub>3</sub>	23	DQ <sub>6</sub>
9	V <sub>SS</sub>	24	NC
10	DQ <sub>2</sub>	25	DQ <sub>7</sub>
11	A <sub>4</sub>	26	PQ
12	A <sub>5</sub>	27	$\overline{\text{RAS}}$
13	DQ <sub>3</sub>	28	$\overline{\text{PCAS}}$
14	A <sub>6</sub>	29	PD
15	A <sub>7</sub>	30	V <sub>CC</sub>

## PIN DESCRIPTION

Pin Name	Function
A <sub>0</sub> -A <sub>9</sub>	Address Input
A <sub>0</sub> -A <sub>9</sub>	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
CAS, $\overline{\text{PCAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Enable
DQ <sub>0</sub> -DQ <sub>7</sub>	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V <sub>CC</sub>	Power Supply ( + 5V)
V <sub>SS</sub>	Ground
NC	No Connection



■ BLOCK DIAGRAM



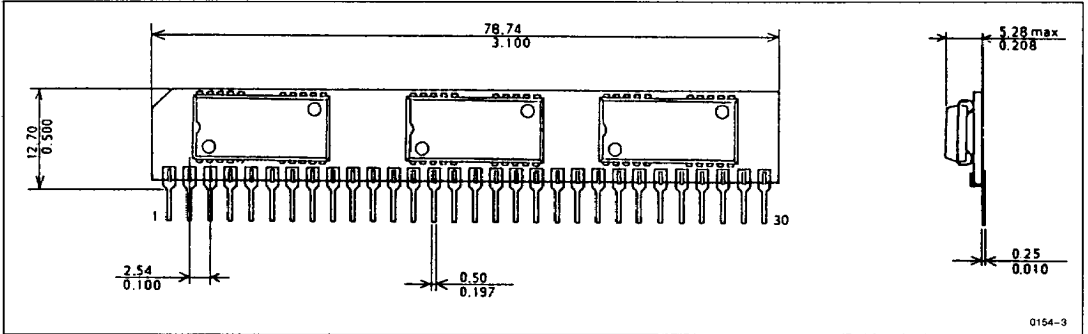
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■ PHYSICAL OUTLINE

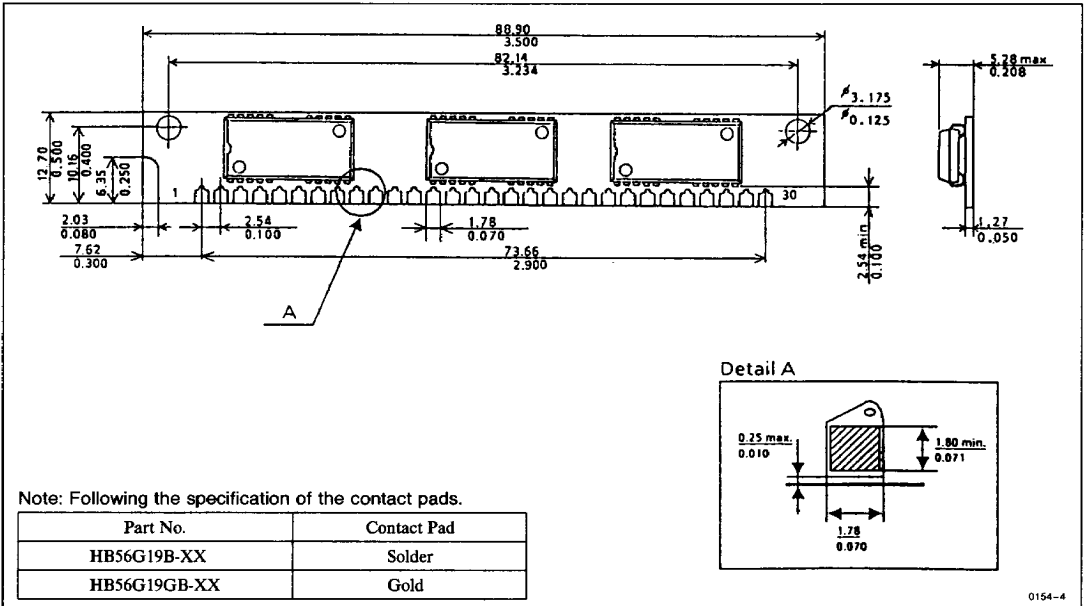
Unit:  $\frac{\text{mm}}{\text{inch}}$

• HB56G19A Series



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• HB56G19B/GB Series



0154-4

Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56G19B-XX	Solder
HB56G19GB-XX	Gold



## ■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	(Input)	V <sub>in</sub>	-1.0 to +7.0	V
	(Output)	V <sub>out</sub>	-1.0 to +7.0	V
Supply Voltage Relative to V <sub>SS</sub>		V <sub>CC</sub>	-1.0 to +7.0	V
Short Circuit Output Current		I <sub>out</sub>	50	mA
Power Dissipation		P <sub>T</sub>	8	W
Operating Temperature		T <sub>opr</sub>	0 to +70	°C
Storage Temperature		T <sub>stg</sub>	-55 to +125	°C

## ■ ELECTRICAL CHARACTERISTICS

### • Recommended DC Operating Conditions (T<sub>A</sub> = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V <sub>SS</sub>	0	0	0	V	
	V <sub>CC</sub>	4.5	5.0	5.5	V	1
Input High Voltage	V <sub>IH</sub>	2.4	—	5.5	V	1
Input Low Voltage	V <sub>IL</sub>	-1.0	—	0.8	V	1

Note: 1. All voltage referenced to V<sub>SS</sub>.

### • DC Electrical Characteristics (T<sub>A</sub> = 0 to +70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V)

Parameter	Symbol	HB56G19A/B/GB								Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I <sub>CC1</sub>	—	310	—	280	—	250	—	220	mA	t <sub>RC</sub> = Min	1, 2
Standby Current	I <sub>CC2</sub>	—	6	—	6	—	6	—	6	mA	TTL Interface R <sub>AS</sub> , C <sub>AS</sub> = V <sub>IH</sub> , D <sub>out</sub> = High-Z	
		—	3	—	3	—	3	—	3	mA	CMOS Interface R <sub>AS</sub> , C <sub>AS</sub> ≥ V <sub>CC</sub> - 0.2V, D <sub>out</sub> = High-Z	
R <sub>AS</sub> Only Refresh Current	I <sub>CC3</sub>	—	310	—	280	—	240	—	210	mA	t <sub>RC</sub> = Min	2
Standby Current	I <sub>CC5</sub>	—	15	—	15	—	15	—	15	mA	R <sub>AS</sub> = V <sub>IH</sub> , C <sub>AS</sub> = V <sub>IL</sub> , D <sub>out</sub> = Enable	1
C <sub>AS</sub> Before R <sub>AS</sub> Refresh Current	I <sub>CC6</sub>	—	300	—	270	—	240	—	210	mA	t <sub>RC</sub> = Min	
Fast Page Mode Current	I <sub>CC7</sub>	—	300	—	270	—	230	—	210	mA	t <sub>PC</sub> = Min	1, 3
Input Leakage Current	I <sub>LI</sub>	-10	10	-10	10	-10	10	-10	10	μA	0V ≤ V <sub>in</sub> ≤ 7V	
Output Leakage Current	I <sub>LO</sub>	-10	10	-10	10	-10	10	-10	10	μA	0V ≤ V <sub>out</sub> ≤ 7V, D <sub>out</sub> = Disable	
Output High Voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	I <sub>out</sub> = -5 mA	
Output Low Voltage	V <sub>OL</sub>	0	0.4	0	0.4	0	0.4	0	0.4	V	I <sub>out</sub> = 4.2 mA	

- Notes: 1. I<sub>CC</sub> depends on output load condition when the device is selected, I<sub>CC</sub> max is specified at the output open condition.  
 2. Address can be changed less than three times while R<sub>AS</sub> = V<sub>IL</sub>.  
 3. Address can be changed ≤ 1 time while C<sub>AS</sub> = V<sub>IH</sub>.



**HB56G19 Series**
**• Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ )

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	$C_{I1}$	—	30	pF	1
Input Capacitance (Clock)	$C_{I2}$	—	36	pF	1
Input/Output Capacitance (DQ <sub>0-7</sub> )	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	$C_{I3}$	—	10	pF	1
Output Capacitance (PQ)	$C_O$	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{\text{CAS}} = V_{IH}$  to disable D<sub>out</sub>.

**• AC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ )<sup>1, 12</sup>  
**Read, Write, and Refresh Cycles (Common Parameters)**

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	$t_{RC}$	120	—	130	—	160	—	190	—	ns	
$\overline{\text{RAS}}$ Precharge Time	$t_{RP}$	50	—	50	—	70	—	80	—	ns	
$\overline{\text{RAS}}$ Pulse Width	$t_{RAS}$	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{\text{CAS}}$ Pulse Width	$t_{CAS}$	20	10000	20	10000	25	10000	25	10000	ns	
Row Address Setup Time	$t_{ASR}$	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	$t_{RAH}$	10	—	10	—	12	—	15	—	ns	
Column Address Setup Time	$t_{ASC}$	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	$t_{CAH}$	15	—	15	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	$t_{RCD}$	20	40	20	50	22	55	25	75	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	$t_{RAD}$	15	30	15	35	17	40	20	55	ns	9
$\overline{\text{RAS}}$ Hold Time	$t_{RSH}$	20	—	20	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	$t_{CSH}$	60	—	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	$t_{CRP}$	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	$t_T$	3	50	3	50	3	50	3	50	ns	7
Refresh Period	$t_{REF}$	—	16	—	16	—	16	—	16	ms	15



## Read Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from RAS	t <sub>RAC</sub>	—	60	—	70	—	80	—	100	ns	2, 3
Access Time from CAS	t <sub>CAC</sub>	—	20	—	20	—	25	—	25	ns	3, 4
Access Time from Address	t <sub>AA</sub>	—	30	—	35	—	40	—	45	ns	3, 5
Read Command Setup Time	t <sub>RCS</sub>	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to CAS	t <sub>RCH</sub>	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to RAS	t <sub>RRH</sub>	10	—	10	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t <sub>RAL</sub>	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t <sub>OFF</sub>	0	20	0	20	0	20	0	25	ns	6

## Write Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t <sub>WCS</sub>	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t <sub>WCH</sub>	15	—	15	—	20	—	20	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	10	—	10	—	15	—	20	—	ns	
Data-in Setup Time	t <sub>DS</sub>	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t <sub>DH</sub>	15	—	15	—	20	—	20	—	ns	11



Refresh Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	t <sub>CSR</sub>	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh Cycle)	t <sub>CHR</sub>	15	—	15	—	20	—	20	—	ns	
RAS Precharge to CAS Hold Time	t <sub>RPC</sub>	10	—	10	—	10	—	10	—	ns	

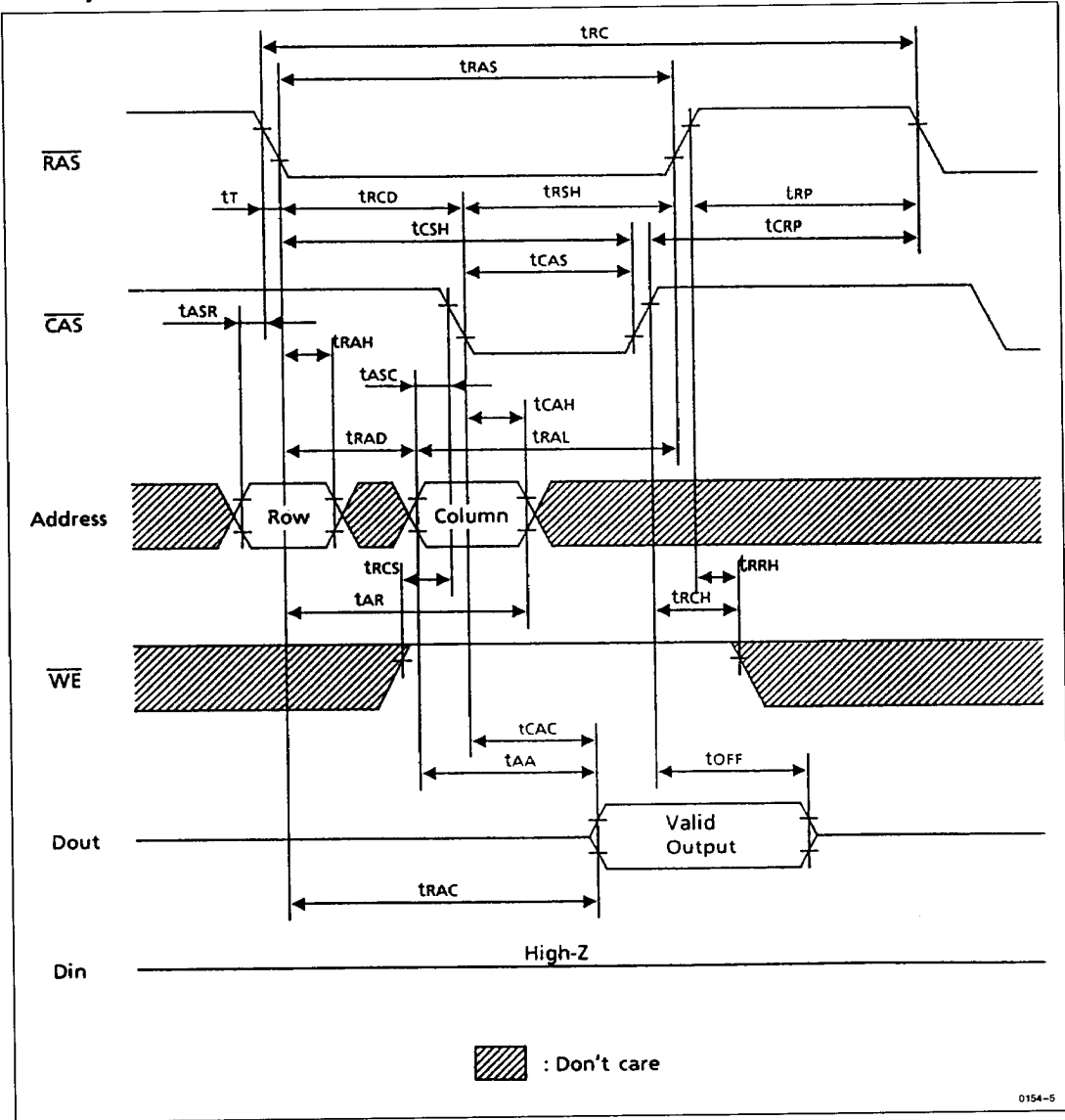
Fast Page Mode Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t <sub>PC</sub>	45	—	50	—	55	—	55	—	ns	
Fast Page Mode CAS Precharge Time	t <sub>CP</sub>	10	—	10	—	10	—	10	—	ns	
Fast Page Mode RAS Pulse Width	t <sub>RASC</sub>	60	100000	70	100000	80	100000	100	100000	ns	13
Access Time from CAS Precharge	t <sub>ACP</sub>	—	40	—	45	—	50	—	50	ns	14
RAS Hold Time from CAS Precharge	t <sub>RHCP</sub>	40	—	45	—	50	—	50	—	ns	

- Notes:
1. AC measurements assume  $t_T = 5$  ns.
  2. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$  and  $t_{RAD} \leq t_{RAD}(\max)$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  4. Assumes that  $t_{RCD} \geq t_{RCD}(\max)$  and  $t_{RAD} \leq t_{RAD}(\max)$ .
  5. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$  and  $t_{RAD} \geq t_{RAD}(\max)$ .
  6.  $t_{OFF}(\max)$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  7.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  8. Operation with the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met,  $t_{RCD}(\max)$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  9. Operation with the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met,  $t_{RAD}(\max)$  is specified as a reference point only, if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled exclusively by  $t_{AA}$ .
  10. Early write cycle only ( $t_{WCS} \geq t_{WCS}(\min)$ ).
  11. These parameters are referenced to  $\overline{CAS}$  leading edge in an early write cycle.
  12. An initial pause of 100  $\mu$ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{RAS}$  clock such as  $\overline{RAS}$  only refresh).
  13.  $t_{RASC}$  is determined by  $\overline{RAS}$  pulse width in fast page mode cycles.
  14. Access time is determined by the longer of  $t_{AA}$  or  $t_{CAC}$  or  $t_{ACP}$ .
  15.  $t_{REF}$  is determined by 1,024 refresh cycles.



**■ TIMING WAVEFORMS**  
**• Read Cycle**

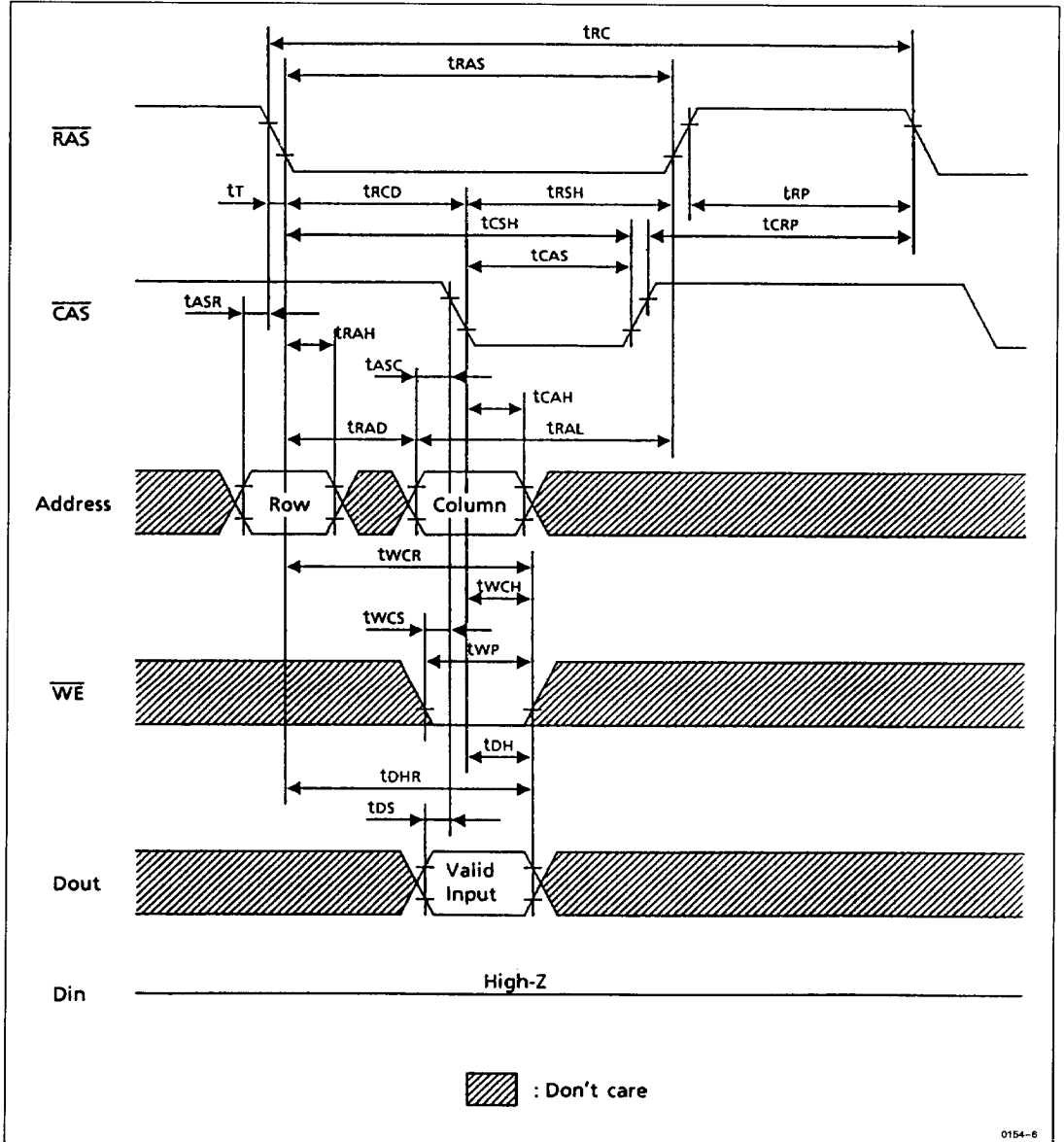


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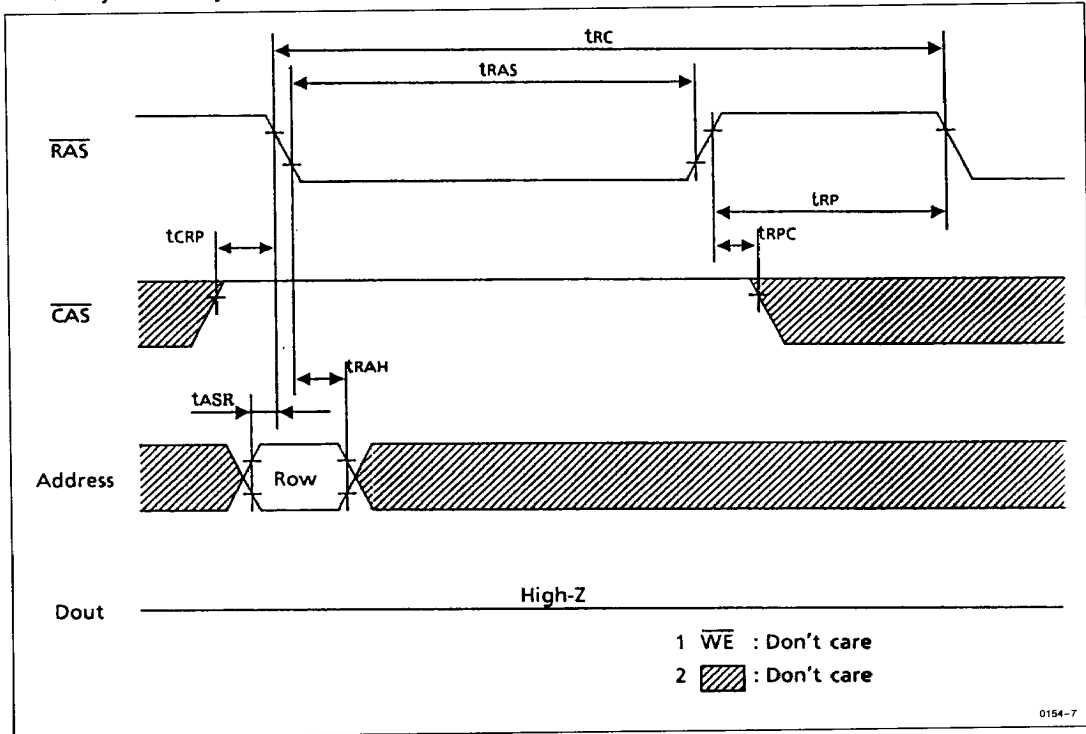
• Early Write Cycle



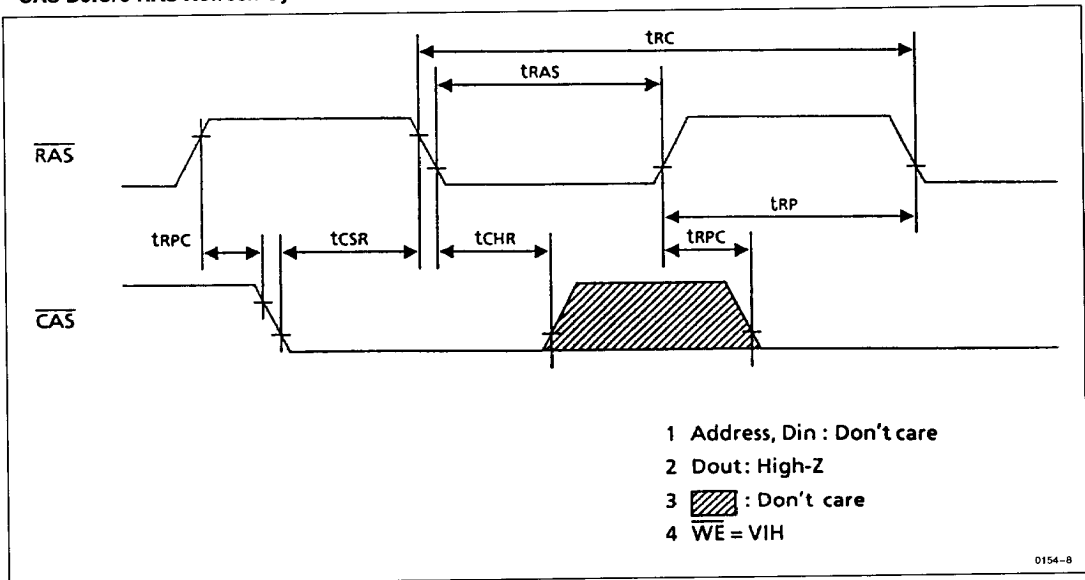
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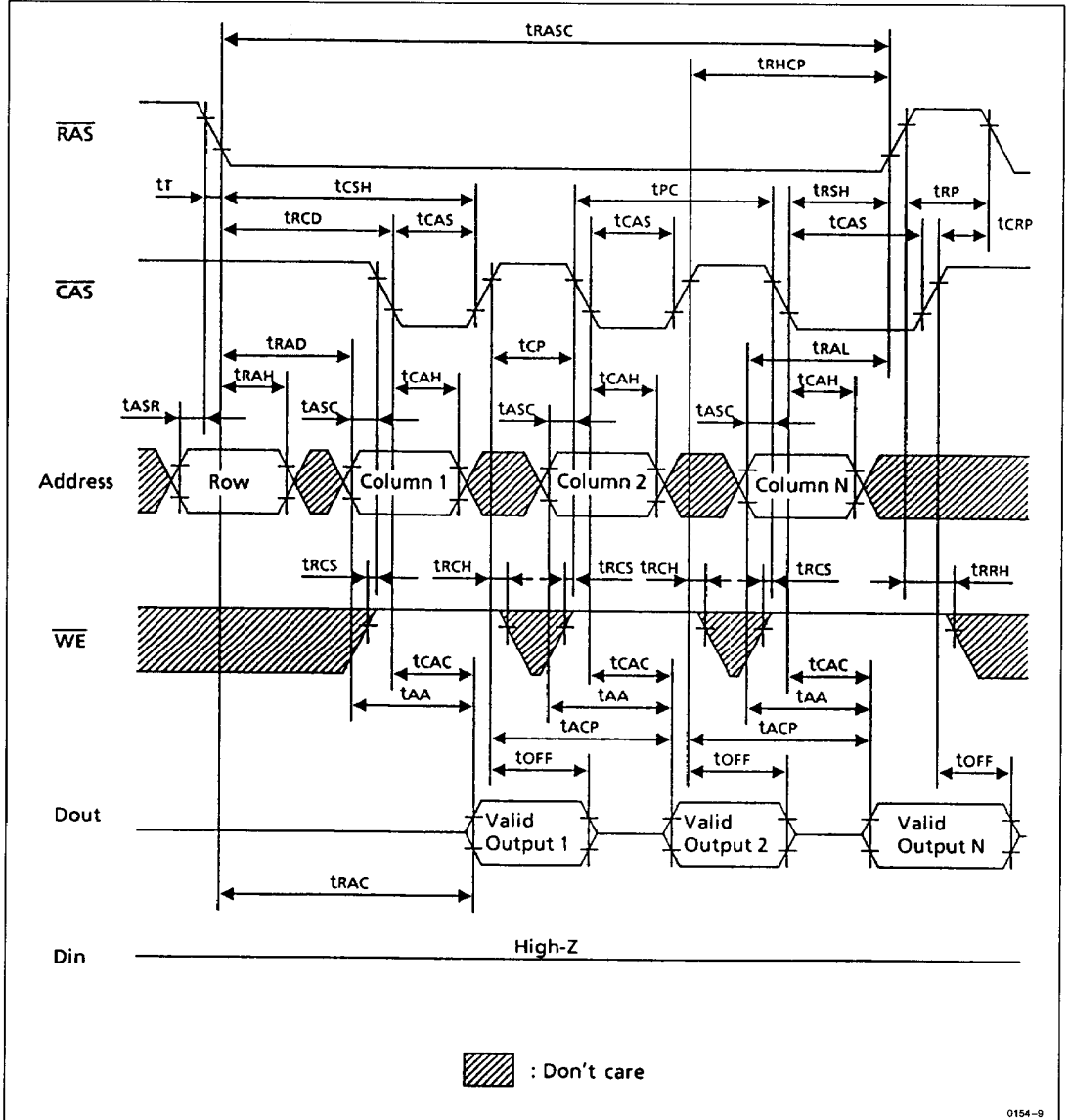
•  $\overline{\text{RAS}}$  Only Refresh Cycle



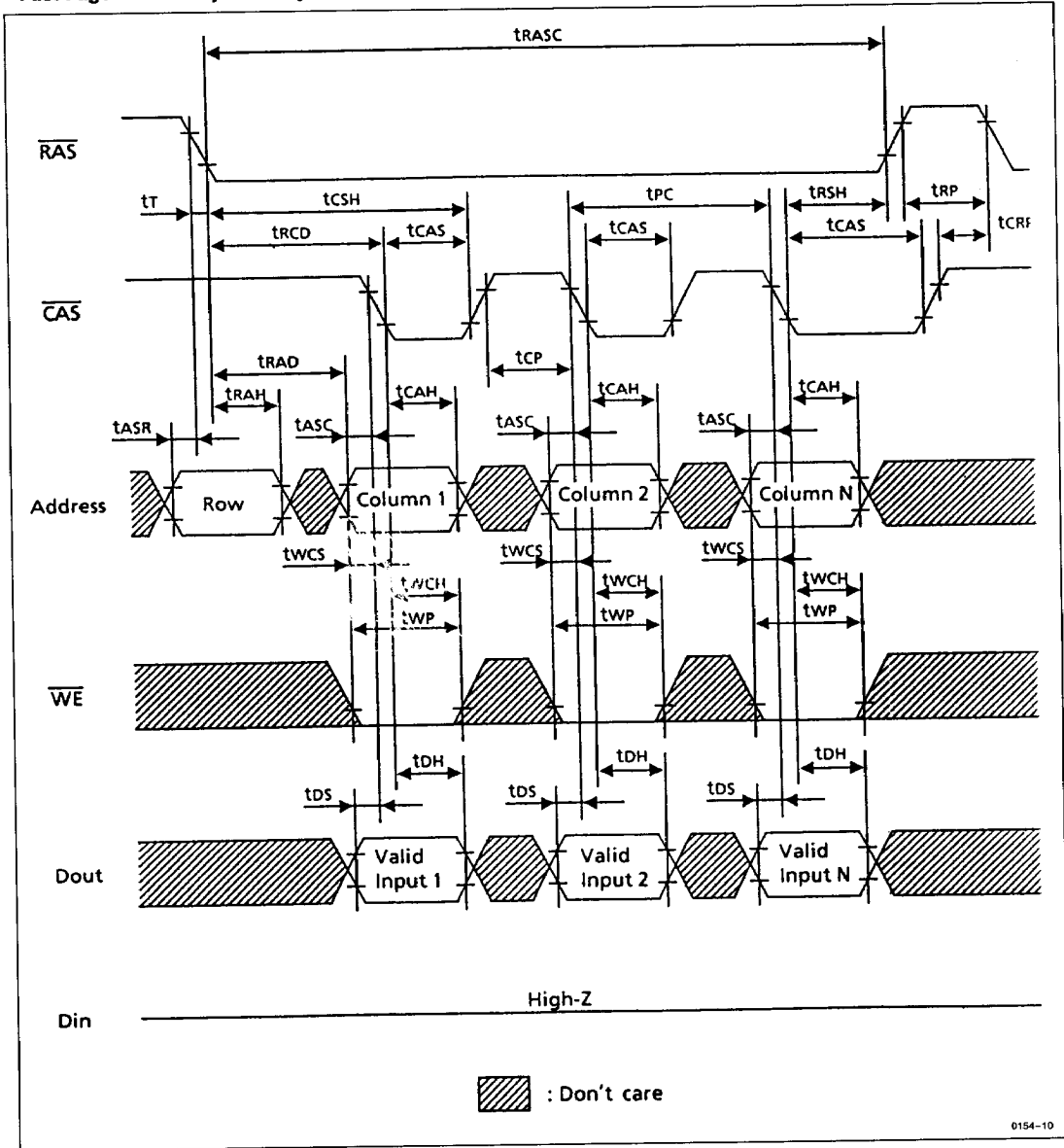
•  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle



• Fast Page Mode Read Cycle



• Fast Page Mode Early Write Cycle



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