Winbond Electronics Corp.

PCI ISDN S/T-CONTROLLER

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1. GENERAL DESCRIPTION

The Winbond's single chip PCI bus ISDN S/T interface controller (W6692) is an all-in-one device suitable for ISDN Internet access. Three HDLC controllers are incorporated in the chip, one for D channel and the other two for B channels. These HDLC controllers facilitate efficient access to signalling and data services. The PCM codec interface provides voice service or other services. The built in PCI 2.1 interface circuit makes glueless design for PCI bus add-on card application.

2. FEATURES

- Full duplex 2B + D S/T-interface transceiver compatible with ITU-T I.430 Recommendation
  - Four wire operation
  - Received clock recovery
  - Layer 1 activation/deactivation procedures
  - D channel access control
  - Supports multiframe synchronization
- Supports LAPD protocol
  - Flag generation/recognition
  - Bit stuffing (zero insertion/deletion)
  - Frame Check Sequence (FCS) generation/check
  - Maskable address recognition
  - FIFO buffer (2 × 128 bytes)
- Two B channel HDLC controllers
  - Maskable address recognition
  - Bit rate options: 56 or 64 kbps
  - Transparent (HDLC mode) or extended transparent mode (clear channel)
  - FIFO buffer (2 × 128 bytes) per B channel
- Two PCM codec interfaces for speech and POTS application
- Various B channel switching capabilities
- GCI interface for connection with U transceiver
- Built in PCI 2.1 slave mode circuit
- Serial EEPROM interface for PCI configuration
- Timer, interrupt input, IO/microprocessor interface for POTS or other peripheral control
- +5 volt power supply
- Advanced CMOS technology
- Low power consumption
- Packaged in 100-pin QFP

3. PIN CONFIGURATION

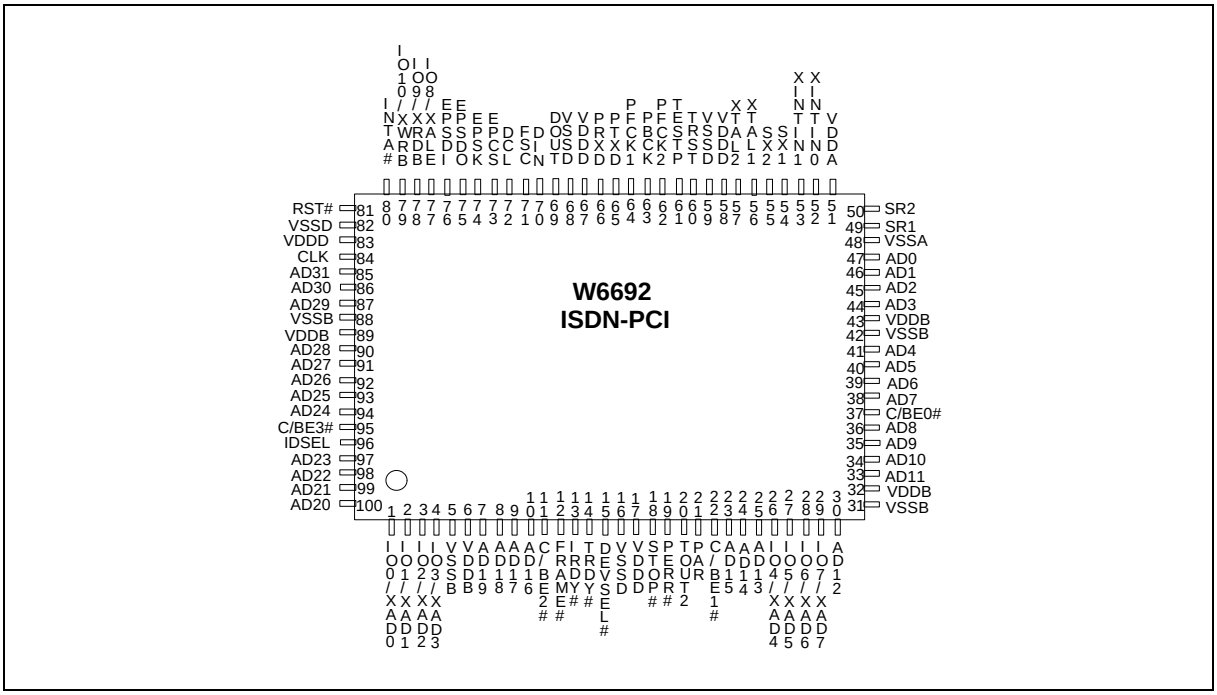


Figure 3.1

4. PIN DESCRIPTION

Table 4.1 W6692 pin descriptions

Notation: The suffix "#" indicates an active LOW signal.

PIN NAME	PIN NO.	TYPE	FUNCTIONS
PCI BUS			
AD31-AD0	85, 86, 87, 90, 91, 92, 93, 94, 97, 98, 99, 100, 7, 8, 9, 10, 23, 24, 25, 30, 33, 34, 35, 36, 38, 39, 40, 41, 44, 45, 46, 47	I/O	Address and Data are multiplexed on the same PCI pins. During the address phase, AD31-0 contain a 32-bit physical address. During the data phase, AD7-AD0 contain the least significant byte and AD31-AD24 contain the most significant byte.
C/BE3#-C/BE0#	95, 11, 22, 37	I	Bus command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE3#-C/BE0# define the bus command. During data phase, C/BE3#-C/BE0# are used as Byte Enable.

Pin Description, contiuned

PIN NAME	PIN NO.	TYPE	FUNCTIONS
PAR	21	I/O	Parity is even parity across AD31-AD0 and C/BE3#-C/BE0#.
FRAME#	12	I	FRAME# is asserted to indicate a bus transaction is beginning.
PCI BUS			
TRDY#	14	O	Target Ready indicates W6692 is able to complete the current data phase of the transaction.
IRDY#	13	I	Initiator Ready indicates the bus master's ability to complete the current data phase of the transaction.
STOP#	18	O	Stop indicates W6692 is requesting the master to stop the current transaction.
DEVSEL#	15	O	Device Select indicates W6692 has decoded its address as the target of the current access.
IDSEL	96	I	Initialization Device Select is used as chip select during configuration read and write transactions.
PERR#	19	O	Parity Error is only for the reporting of data parity errors.
CLK	84	I	PCI Clock. All other PCI signals, except RST#, INTA# are sampled on the rising edge of CLK.
RST#	81	I	PCI Reset. RST# may be asynchronous to CLK when asserted or deasserted.
INTA#	80	O	Interrupt. This is level sensitive, active LOW and open drain output.
GCI BUS			
DCL	72	I	GCI Bus Data Clock of the frequency: 1.536 MHz.
FSC	71	I	GCI Bus Frame Synchronization Clock: 8 KHz.
DIN	70	I	GCI Bus Data Port 0 (ex: must be connectted to Siemens PEB2091's DOUT pin).
DOUT	69	O	GCI Bus Data Port 1 (ex: must be connectted to Siemens PEB2091's DIN pin)
PCM BUS			
PFCK1	64	O	PCM port 1 frame synchronization signal, with 8 KHz repetition rate and 8 bit pulse width.
PFCK2	62	O	PCM port 2 frame synchronization signal, with 8 KHz repetition rate and 8 bit pulse width.
PBCK	63	O	PCM bit synchronization clock of 1.536 MHz.
PTXD	65	O	PCM transmit data output. A maximum of two channels with 64 Kbit/s data rate can be multiplexed on this signal.

Pin Description, contiuned

PIN NAME	PIN NO.	TYPE	FUNCTIONS
PRXD	66	I	PCM receive data input. A maximum of two channels with 64 Kbit/s data rate can be multiplexed on this signal.
ISDN SIGNALS AND EXTERNAL CRYSTAL			
SR1	49	I	S/T bus receiver input (negative).
SR2	50	I	S/T bus receiver input (positive).
SX1	54	O	S/T bus transmitter output (positive).
SX2	55	O	S/T bus transmitter output (negative).
XTAL1	56	I	Crystal or Oscillator clock input. The clock frequency: 7.68 MHz ±100PPM.
XTAL2	57	O	Crystal clock output. Left unconnected when using oscillator.
EXTERNAL EEPROM INTERFACE			
EPCS	73	O	Serial EEPROM chip select (active HIGH).
EPSK	74	O	Serial EEPROM data clock (clock frequency < 250 KHz).
EPSDI	76	I	Serial EEPROM data input (must be connected to external EEPROM's data output).
EPSDO	75	O	Serial EEPROM data output (must be connected to external EEPROM's data input).
FUNCTIONAL TEST			
TESTP	61	I	Used to enable normal operation (1) or enter test mode (0).
TRST	60	O	If terminal equipment function is enabled, the reset pulse width is: – 125 uS when generated by the watchdog timer. – 16 mS when generated by exchange awake indication code change.
PERIPHERAL CONTROL			
TOUT2	20	O	Timer 2 output. A square wave with 50% duty cycle, 2–126 mS period can be generated.
XINTIN0	52	I	A level change (either direction) will generate a maskable interrupt on the PCI bus interrupt request pin INTA#.
XINTIN1	53	I	A level change (either direction) will generate a maskable interrupt on the PCI bus interrupt request pin INTA#.

Pin Description, contiuned

PIN NAME	PIN NO.	TYPE	FUNCTIONS
IO0-IO10	79, 78, 77, 29, 28, 27, 26, 4, 3, 2, 1	I/O	When confiured as simple IO mode (PCTL: XMODE = 0), these pins can read/write data from/to peripheral components. The pin directions are selected via register.
XAD7-XAD0	29, 28, 27, 26, 4, 3, 2, 1	I/O	When configured as microprocessor mode (PCTL: XMODE = 1), address and data are multiplexed on these pins.
XALE	77	O	When configured as microprocessor mode (PCTL: XMODE = 1), this is the Address Latch Enable output.
XRDB	78	O	When configured as microprocessor mode (PCTL: XMODE = 1), this is the read pulse.
XWRB	79	O	When configured as microprocessor mode (PCTL: XMODE = 1), this is the write pulse.
POWER AND GROUND			
VDDD	17, 58, 67, 83	I	Digital Power Supply (5V ±5%).
VDDA	51	I	Analog Power Supply (5V ±5%).
VDDB	6, 32, 43, 89	I	PCI Bus Power Supply.
VSSD	16, 59, 68, 82	I	Digital Ground.
VSSA	48	I	Analog Ground.
VSSB	5, 31, 42, 88	I	PCI Bus Ground.

5. SYSTEM DIAGRAM AND APPLICATIONS

Typical applications include:

- PCI passive S-card for data only service
- PCI passive S-card with one handset/POTS connection
- PCI passive S-card with two POTS connections

The all-in-one characteristic of W6692 makes it excellent for ISDN Internet-access passive card applications. The booming home PC market and powerful CPU capability make it possible to make a very low-cost ISDN Internet access card by using CPU's computing power and user friendly PCI interface. W6692 is designed for this type of scenario. W6692 integrates three HDLC controllers in the chip and interfaces to PCI bus directly. In addition, W6692 provides peripheral control circuits for PCM CODEC and POTS interface.

In the first and second applications, the all-in-one feature of W6692 makes glue circuit unnecessary. In the third application, only a few TTL-like glue circuits are needed for the two POTS interface control.

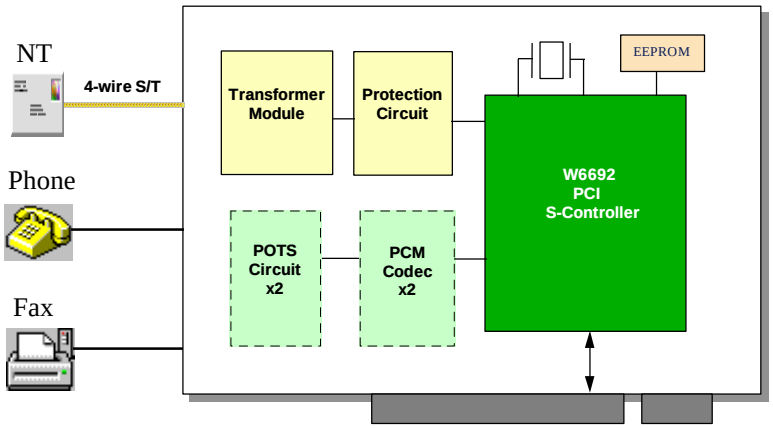


Figure 5.1 ISDN Internet passive S-card with two pots connections

6. BLOCK DIAGRAM

The block diagram of W6692 is shown in Figure 6.1

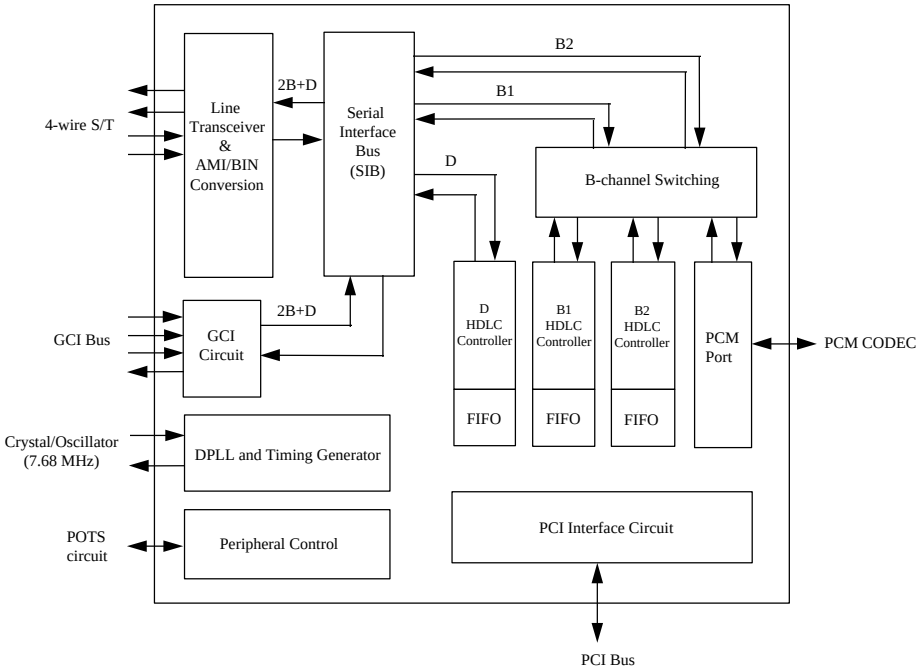


Figure 6.1 W6692 Functional Block Diagram

7. FUNCTIONAL DESCRIPTIONS

7.1 Main Block Functions

The functional block diagram of W6692 is shown in Figure 6.1. The main function blocks are:

- Layer 1 function according to ITU-T I.430
- Serial Interface Bus (SIB)
- B channel switching
- supports GCI bus interface
- PCM port (x 2)
- D channel HDLC controller
- B channel HDLC controllers (x 2)
- PCI interface circuit
- Peripheral control

The layer 1 function includes:

- S/T bus transmitter/receiver
- Timing recovery using Digital Phase Locked Loop (DPLL) circuit
- Layer 1 activation/deactivation
- D channel access control
- Frame alignment
- Multiframe synchronization
- Test functions

The serial interface bus performs the multiplexing/demultiplexing of D and 2B channels.

The B channel switching determines the connection between layer1/GCI, layer 2 and PCM.

The GCI circuit is used to connect a U transceiver. In this case, the layer 1 function of S/T interface is disabled. After power up or reset, the GCI circuit is disabled and the S/T layer 1 function is enabled.

The PCM port provides two 64 kbps clear channels to connect to PCM codec chips.

The D channel HDLC controller performs the LAPD (Link Access Procedure on the D channel) protocol according to ITU-T I.441/Q.921 recommendation.

There are two independent B channel HDLC controllers. They can be used to support HDLC-like protocols such as Internet PPP.

The PCI interface circuit implements PCI specification revision 2.1 slave mode function.

The peripheral control block is used to control other peripheral devices such as CODEC, POTS, LEDs or device with microprocessor interface.

7.2 Layer 1 Functions Descriptions

The layer 1 functions includes:

- Transmitter/Receiver which conform to the electrical specifications of ITU-T I.430
- Receiver clock recovery and timing generation
- Output phase delay (deviation) compensation
- Layer 1 activation/deactivation procedures
- D channel access control
- Frame alignment
- Multiframe synchronization
- Test functions

7.2.1 S/T Interface Transmitter/Receiver

According to ITU-T I.430, pseudo-ternary code with 100% pulse width is used in both directions of transmission on the S/T interface. The binary "1" is represented by no line signal (zero volt), whereas a binary "0" is represented by a positive or negative pulse.

Data transmissions on the S/T interface are arranged as frame structures. The frame is 250 µs long and consists of 48 bits, which corresponds to a 192 kbit/s line rate. Each frame carries two octets of B1 channel, two octets of B2 channel and four D channel bits. Therefore, the 2B+D data rate is 144 kbit/s. The frame structure is shown in Figure 7.1.

The frame begin is marked by a framing bit, which is followed by a DC balancing bit. The first binary "0" following the framing bit balancing bit is of the same polarity as the framing bit balancing bit, and subsequent binary zeros must alternate in polarity.

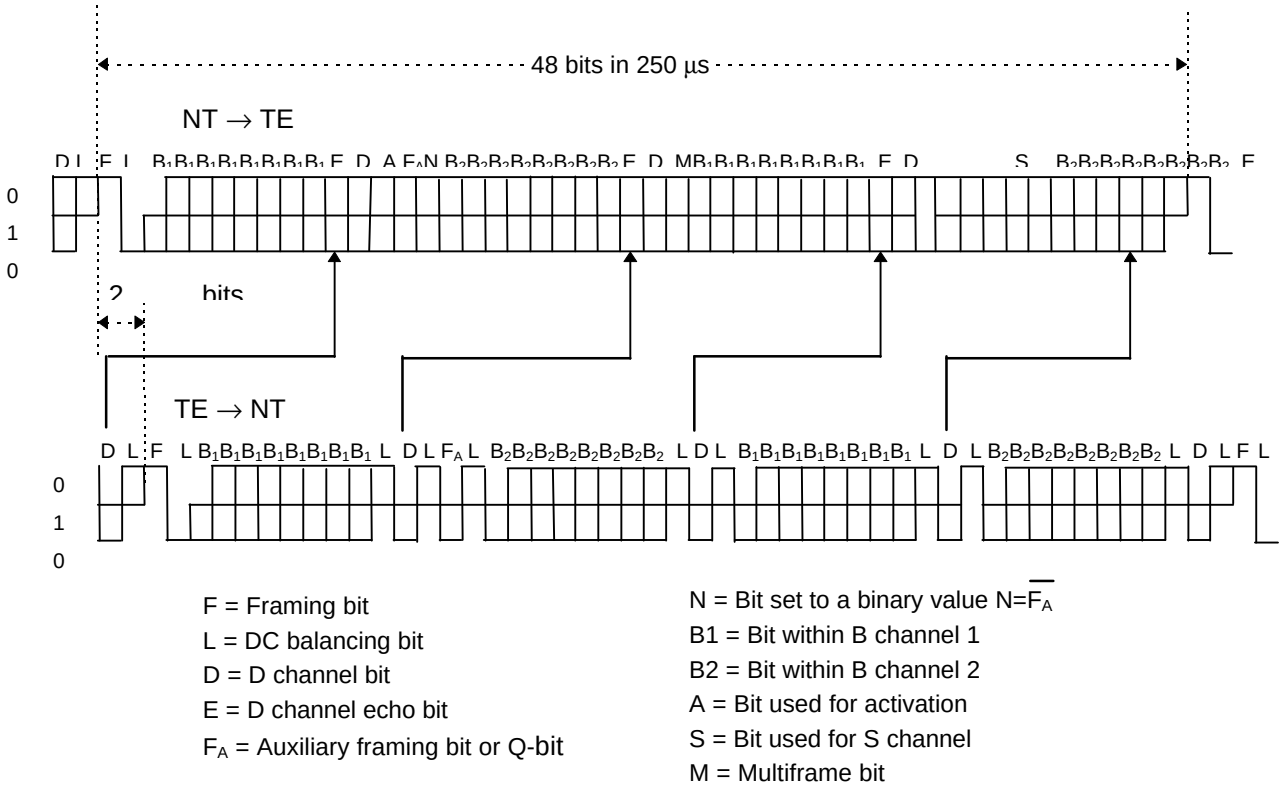
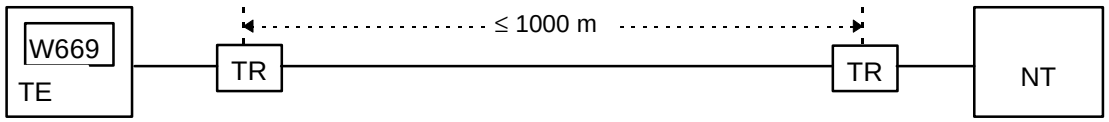
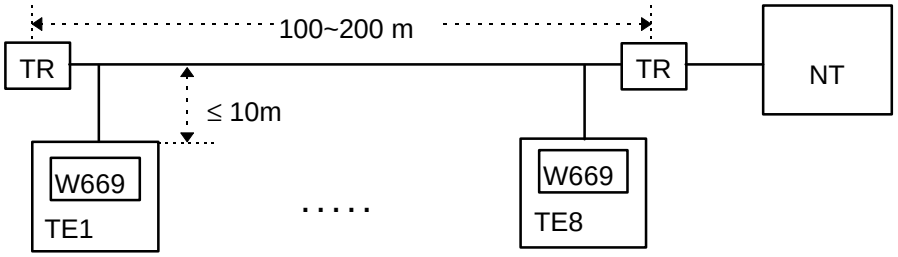


Figure 7.1 Frame structure at s/t interface

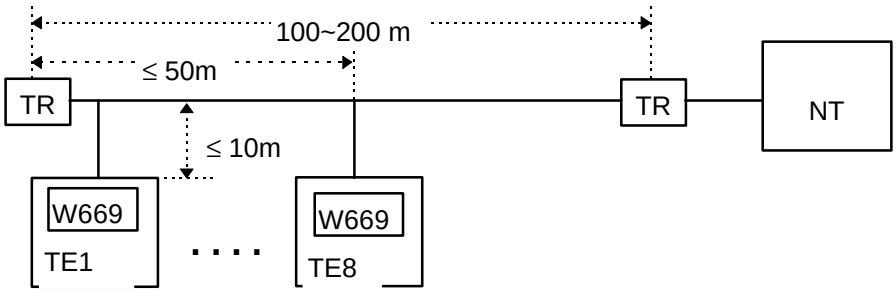
There are three wiring configurations according to I.430: point-to-point, short passive bus and extended pass bus. They are shown in Figure 7.2.



(a) Point-to-point configuration



(b) Short passive bus configuration



(c) Extended passive bus configuration

TR: Terminating

Figure 7.2 W6692 wiring configuration in te applications

The transmitter and receiver are implemented by differential circuits to increase signal to noise ratio (SNR). The nominal differential line pulse amplitude at 100 Ω termination is 750 mV, zero to peak. Transformers with 2:1 turn ration are needed at transmitter and receiver for voltage level translation and DC isolation.

To meet the electrical characteristic requirements in I.430, some additional circuits are needed. At the transmitter side, the external resistors (18 to 33 Ω) are used to adjust the output pulse amplitude and to meet the transmitter active impedance (≥ 20 Ω when transmitting binary zeros). At the receiver side, the 1.8 kΩ resistors protect the device inputs, while the 10 kΩ resistors (1.8 kΩ +8.2 kΩ) limit the peak current in impedance tests. The diode bridge is used for overvoltage protection.

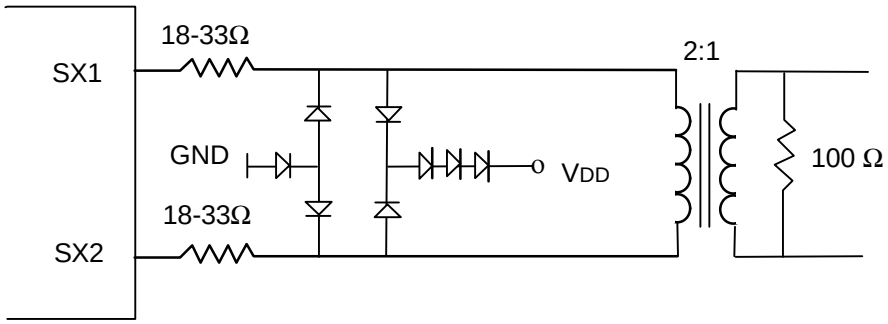


Figure 7.3 External transmitter circuitry

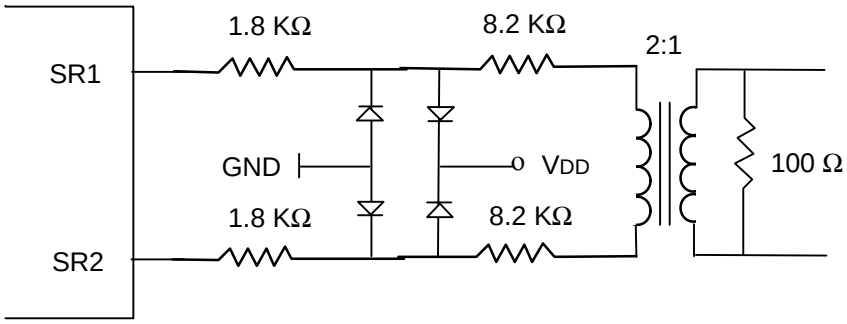


Figure 7.4 External receiver circuitry

After hardware reset, the receiver may enter power down state to save power. In thist state, the internal clocks are turned off, but the analog level detector is still active to detect signal coming from the S interface. The power down state is left either by non-INFO 0 signal from S interface or C/I command from micro-processor.

7.2.2 Receiver Clock Recovery And Timing Generation

A Digital Phase Locked Loop (DPLL) circuit is used to derive the receive clock from the received data stream. This DPLL uses a 7.68 MHz clock as reference. According to I.430, the transmit clock is normally delayed by 2 bit time from the receive clock. The "total phase deviation input to output" is -7% to +15% of a bit period. In some cases, delay compensation may be needed to meet this requirement (see OPS1-0 bits in D_CTL register).

Table 7.1 Output phase delay compensation table

OPS1	OPS0	EFFECT
0	0	No phase delay compensation
0	1	Phase delay compensation 260 nS
1	0	Phase delay compensation 520 nS
1	1	Phase delay compensation 1040 nS

W6692 does not need RC filter on receiver side, therefore zero delay compensation is selected normally. This is the default setting.

The PCM output clocks (PFCK1-2, PBCK) are synchronous to the S-interface timing.

7.2.3 Layer 1 Activation/Deactivation

The layer 1 activation/deactivation procedures are implemented by a finite state machine. The state transitions are triggered by signals received at S interface or commands issued from micro-processor. The state outputs signals to S interface and indication to micro-processor. The CIX register is used by micro-processor to issue command, and the CIR register is used by micro-processor to receive indication.

Some commands are used for special purposes. They are "layer 1 reset", "analog loopback", "send continuous zeros" and "send single zero".

7.2.3.1 States Descriptions and Command/Indication Codes

F3 Deactivated without clock

This is the "deactivated" state of ITU-T I.430. The receive line awake unit is active except during a hardware reset pulse. After reset, once the indication "1111" has been read out, internal clocks will turn off and stay at this state if INFO 0 is received on the S line. The turn off time is approximate 93 mS. The command ECK must be issued to activate the clocks.

F3 Deactivated with clock

This state is identical to "F3 Deactivated without clock" except the internal clocks are enabled. The state is entered by a ECK command. The clocks are enabled approximately 0.5 mS to 4 mS after the ECK command, depending on the crystal capacitances. (It is about 0.5 mS for 12 to 33 pF capacitance).

F3 Awaiting Deactivation

The W6692 enters this state after receiving INFO 0 (in states F5 to F8) for 16 mS (64 frames). This time constant prevents spurious effect on S interface. Any non-INFO 0 signal on the S interface causes transition to "F5 Identifying Input" state. If this transition does not occur in a specific time (500–1000 mS), the micro-processor may issue DRC or ECK command to deactivate layer 1.

F4 Awaiting Signal

This state is reached when an activate request command has been received. In this state, the layer 1 transmits INFO1 and INFO 0 is received from the S interface. The software starts timer T3 of I.430

when issuing activate request command. The software deactivates layer 1 if no signal other than INFO 0 has been received on S interface before expiration of T3.

F5 Identifying Input

After the receipt of any non-INFO 0 signal from NT, the W6692 ceases to transmit INFO 1 and awaits identification of INFO 2 or INFO 4. This state is reached at most 50 μS after a signal different from INFO 0 is present at the receiver of the S interface.

F6 Synchronized

When W6692 receives an activation signal (INFO 2), it responds with INFO 3 and waits for normal frames (INFO 4). This state is reached at most 6 mS after an INFO 2 arrives at the S interface (in case the clocks were disabled in "F3 Deactivated without clock").

F7 Activated

This is the normal active state with the layer 1 protocol activated in both directions. From state "F6 Synchronized" , state F7 is reached at most 0.5 mS after reception of INFO 4. From state "F3 Deactivated without clock" with the clocks disabled, state F7 is reached at most 6 mS after the W6692 is directly activated by INFO 4.

F8 Lost Framing

This is the state where the W6692 has lost frame synchronization and is awaiting resynchronization by INFO 2 or INFO 4 or deactivation by INFO 0.

Special States:

Analog Loop Initiated

On Enable Analog Loop command, INFO 3 is sent by the line transmitter internally to the line receiver (INFO 0 is sent to the line). The receiver is not yet synchronized.

Analog Loop Activated

The receiver is synchronized on INFO 3 which is looped back internally from the transmitter. The indication 'TI" or "ATI" is sent depending on whether or not a signal different from INFO 0 is detected on the S interface.

Send Continuous Pulses

A 96 KHz continuous pulse with alternating polarities is sent.

Send Single Pulses

A 2 KHz isolated pulse with alternating polarities is sent.

Layer 1 Reset

A layer 1 reset command forces the transmission of INFO 0 and disables the S line awake detector. Thus activation from NT is not possible. There is no indication in reset state. The reset state can be left only with ECK command.

Table 7.2 Layer 1 command codes

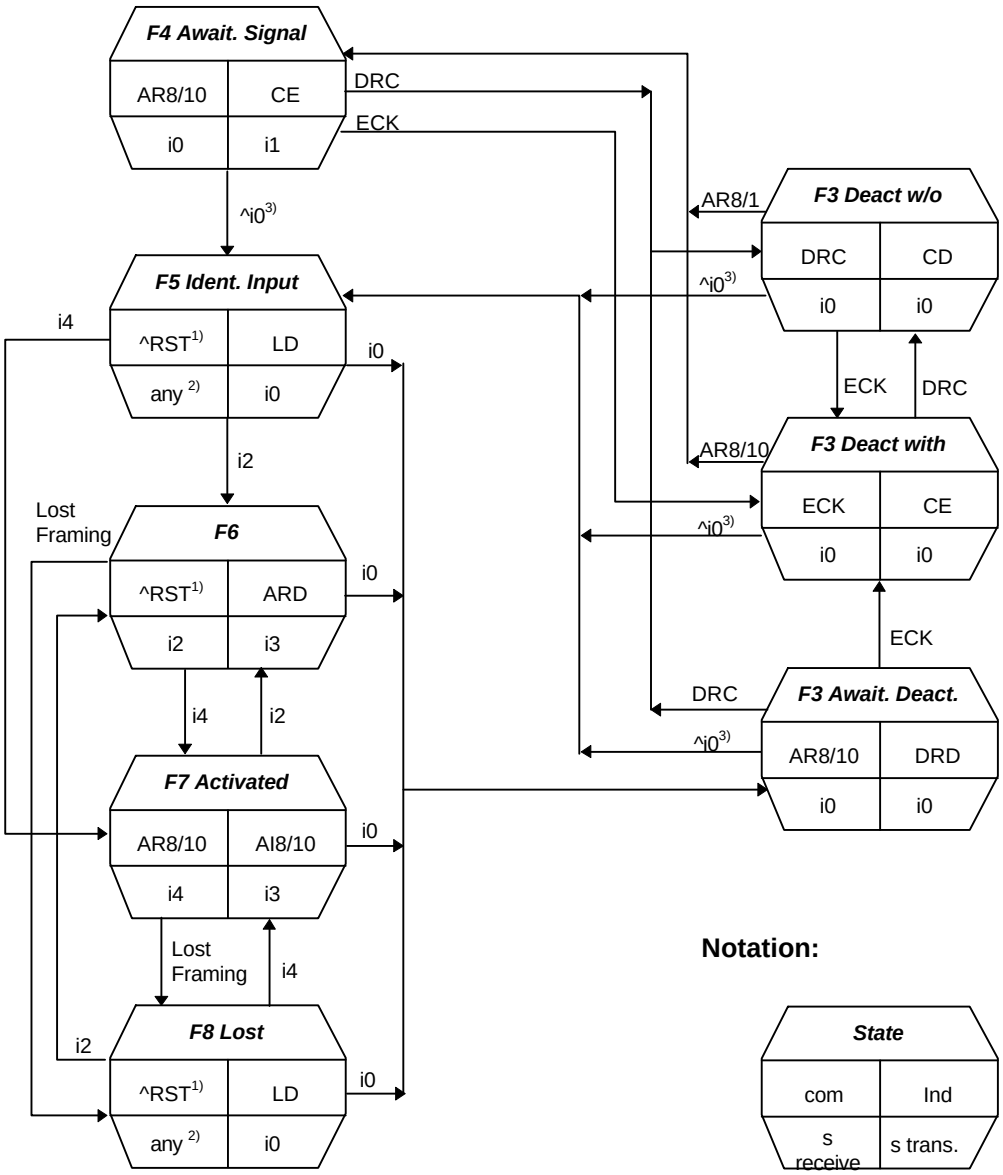
COMMAND	SYM.	CODE	DESCRIPTION
Enable clock	ECK	0000	Enable internal clocks
Layer 1 reset	RST	0001	Layer 1 reset
Send continuous pulses	SCP	0100	Send continuous pulses at 96 KHz
Send single pulses	SSP	0010	Send isolated pulses at 2 KHz
Activate request at priority 8	AR8	1000	Activate layer 1 and set D channel priority level to 8
Activate request at priority 10	AR10	1001	Activate layer 1 and set D channel priority to 10
Enable analog loopback	EAL	1010	Enable analog loopback
Deactivate layer 1	DRC	1111	Deactivate layer 1 and disable internal clocks

Table 7.3 Layer 1 indication codes

INDICATION	SYM.	CODE	DESCRIPTIONS
Clock Enabled	CE	0111	Internal clocks are enabled
Deactivate request downstream	DRD	0000	Deactivation request by S interface, i.e INFO 0 received
Level detected	LD	0100	Signal received, receiver not synchronous
Activate request downstream	ARD	1000	INFO 2 received
Test indication	TI	1010	Analog loopback activated or continuous zeros or single zeros transmitted
Awake test indication	ATI	1011	Level detected during test function
Activate indication with priority class 1	AI8	1100	INFO 4 received, D channel priority is 8 or 9
Activate indication with priority class 2	AI10	1101	INFO 4 received, D channel priority is 10 or 11
Clock disabled	CD	1111	Layer 1 deactivated, internal clocks are disabled

7.2.3.2 State Transition Diagrams

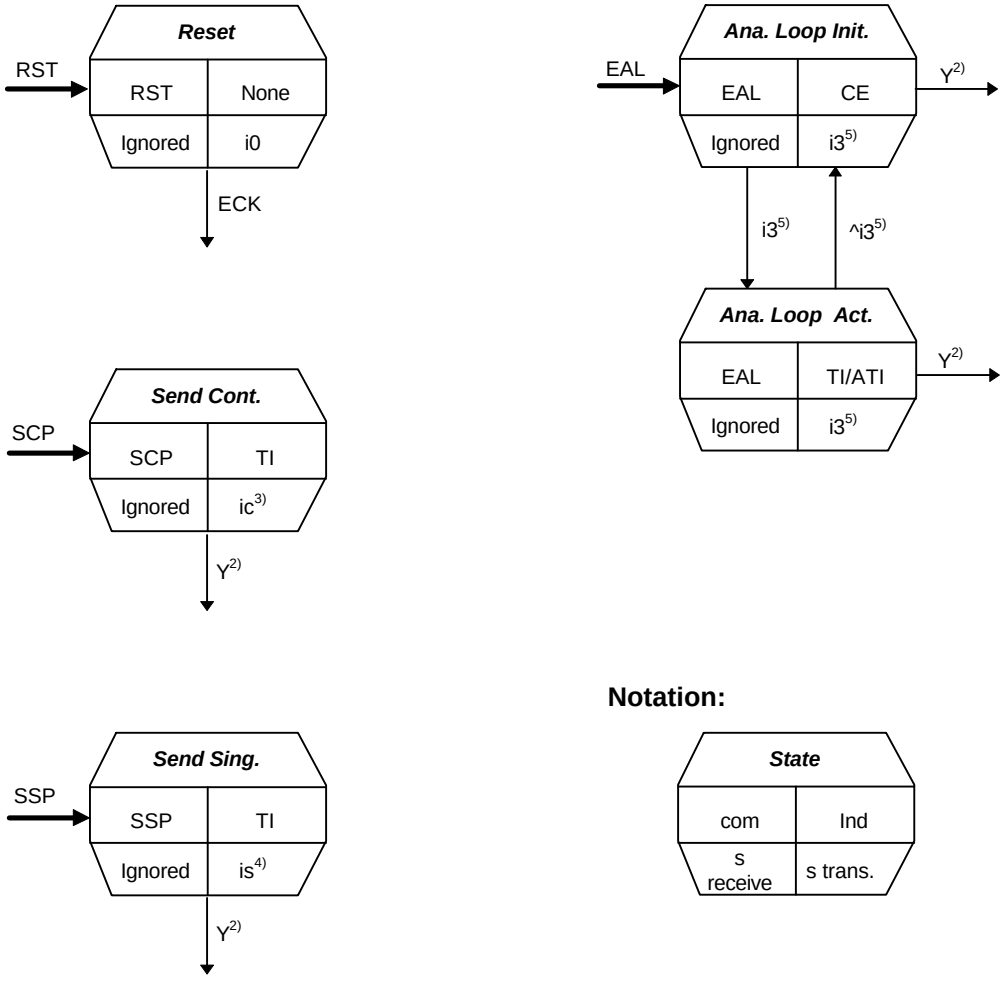
The followings are the state transition diagrams which implement the activation/deactivation state matrix in I.430 (TABLE 5/I.430). The "command" and "s receive" entries in each state octagon keeps the state, the "indication" and "s transmit" entries in each state octagon are the state outputs. For example, at "F3 Deactivated with clock" state, the layer 1 will stay at this state if the command is "ECK" and the INFO 0 is received on S interface. At this state, it provides "CE" indication to the micro-processor and transmits INFO 0 on S interface. A "AR8/10" command causes transition to F4 and non-INFO 0 signal causes transition to F5. Note that the command code writtern by the micro-processor in CIX register and indication code written by layer 1 in CIR register are transmitted repeatedly until a new code is written.



Notes:

1. "^RST" means "NOT layer 1 reset command".
2. "Any" means any signal other than i0, which has not yet been determined.
3. "^i0" means any signal other than i0.

Figure 7.5 layer 1 activation/deactivation state diagram - normal mode



Notes:

1. RST can be issued at any state, while SCP, SCZ and EAL can be issued only at F3 or F7.
2. Y is one of the commands : ECK, DRC, RST.
3. Continuous pulses at 96 KHz.
4. Isolated pulses at 2 KHz.
5. The INFO 3 is transmitted internally only.

Figure 7.6 layer 1 activation/deactivation state diagram - SPECIAL mode

7.2.4 D Channel Access Control

The D channel access control includes collision detection and priority management. The collision detection is always enabled. The priority management procedure as specified in ITU-T I.430 is fully implemented in W6692.

A collision is detected if the transmitted D bit and the received echo bit do not match. When this occurs, D channel transmission is immediately stopped and the echo channel is monitored to attempt the next D channel access. The layer 1 module uses an internal signal to inform layer 2 module of the collision condition (DRDY bit goes inactive in D_STAR register).

There are two priority classes: class 1 and class 2. Within each class, there are normal and lower priority levels.

Table 7.4 D priority classes

	NORMAL LEVEL	LOWER LEVEL
Priority class 1	8	9
Priority class 2	10	11

The selection of priority class is via the AR8/AR10 command. The following table summarizes the commands/indications used for setting the priority classes:

Table 7.5 D Priority commands/indications

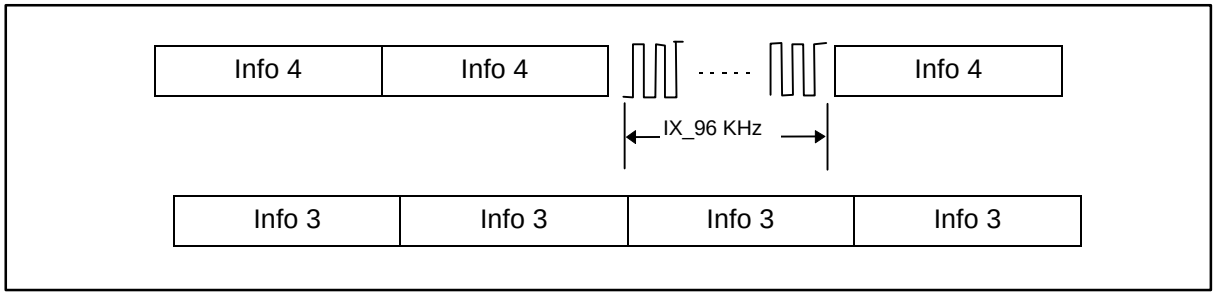
COMMAND	SYM.	CODE	REMARKS
Activate request, set priority 8	AR8	1000	Activation command, set D channel priority to 8
Activate request, set priority 10	AR10	1001	Activation command, set D channel priority to 10
INDICATION	**ABBR.**		**REMARKS**
Activate indication with priority 8	AI8	1100	Info 4 received, D channel priority is 8 or 9
Activate indication with priority 10	AI10	1101	Info 4 received, D channel priority is 10 or 11

7.2.5 Frame Alignment

The following sections describe the behavior of W6692 in respect to the CTS-2 conformance test procedures for frame alignment. Please refer to ETSI-TM3 Appendix B1 for detailed descriptions.

7.2.5.1 FAinfA_1fr

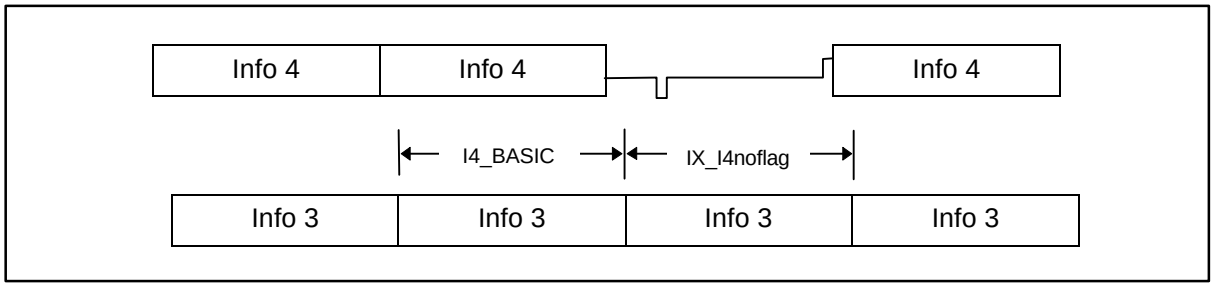
This test checks if TE does not lose frame alignment on receipt of one bad frame. The pattern for the bad frame is defined as IX_96 KHz. This pattern consists of alternating pulses at 96 KHz during the whole frame.



Device	Settings	Result
W6692	None	Pass

7.2.5.2 FAinfB_1fr

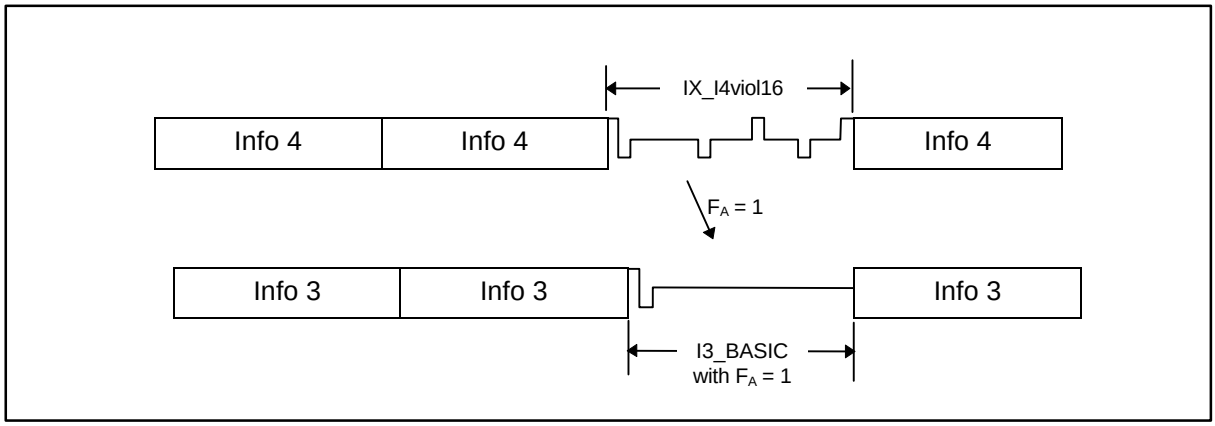
This test checks if TE does not lose frame alignment on receipt of one IX_I4noflag frame which has no framing and balancing bit. The following figure indicates one possible IX_I4noflag waveform.



Device	Settings	Result
W6692	None	Pass

7.2.5.3 FAinfD_1fr

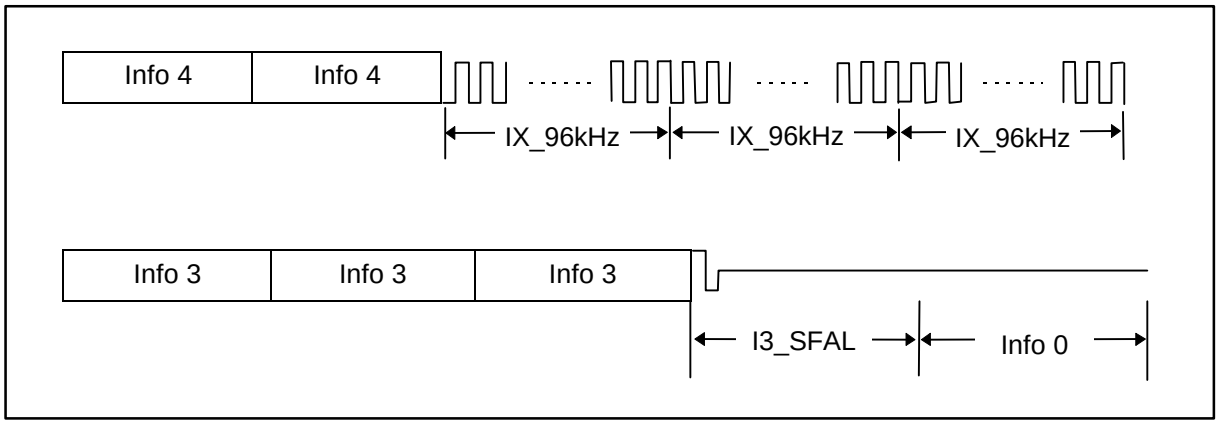
This test checks if TE does not lose frame alignment on receipt of one IX-I4viol16 frame. The IX_I4viol16 frame remains at binary "1" until the first B2 bit which is bit position 16. The pulse sequences are: Framing bit, balancing bit, B2 bit, M bit, S bit, balancing bit. The TE should reflect the received F_A bit (F_A = "1") in the transmitted frame.



Device	Settings	Result
W6692	None	Pass

7.2.5.4 FAinfA_kfr

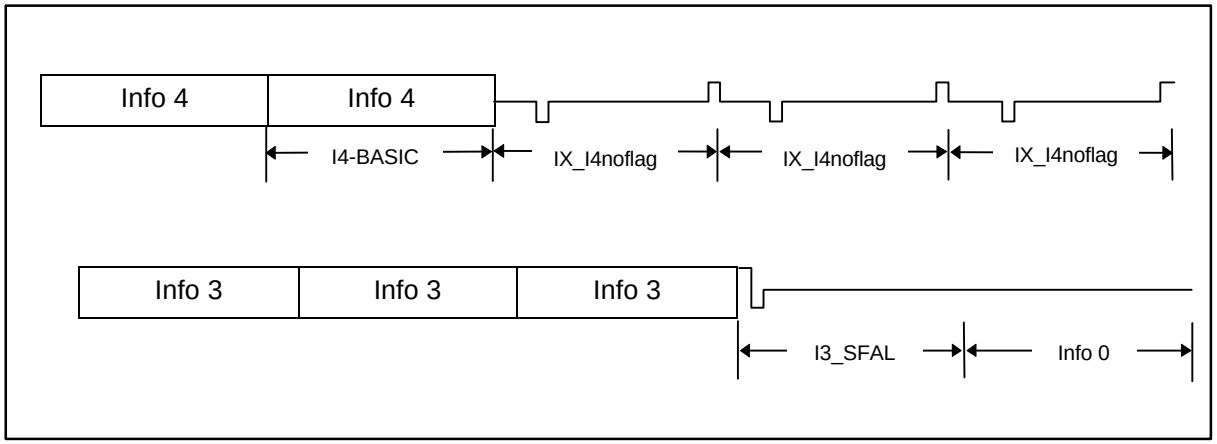
This is to test the number k of IX_96 KHz frames necessary for loss of frame alignment.



Device	Settings	Result
W6692	k = 2	Pass

7.2.5.5 FAinfB_kfr

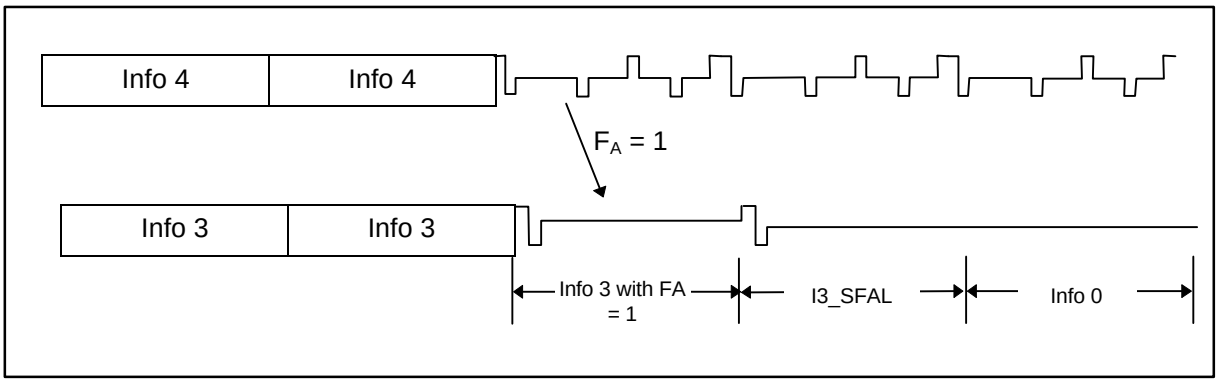
This is to test the number k of IX_I4noflag frames necessary for loss of frame alignment.



Device	Settings	Result
W6692	k = 2	Pass

7.2.5.6 FAinfD_kfr

This is to test the number k of IX_I4noflag frames necessary for loss of frame alignment.

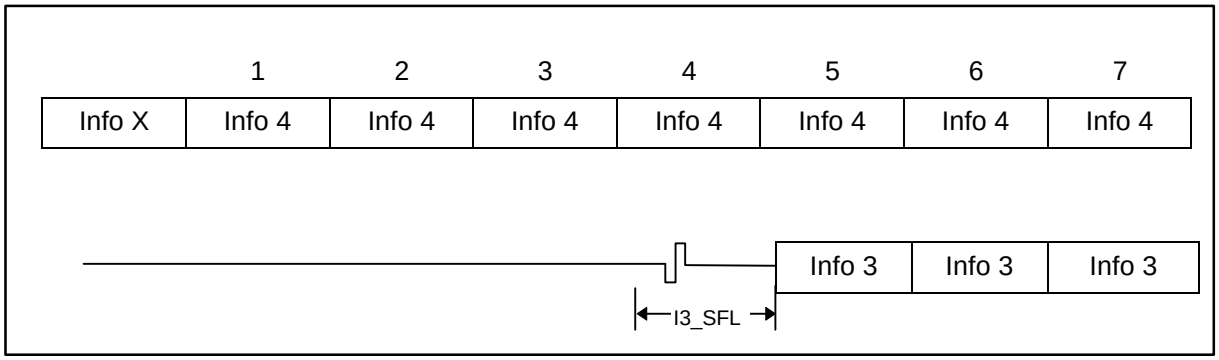


Device	Settings	Result
W6692	k = 2	Pass

7.2.5.7 Faregain

This is to test the number m of good frames necessary for regain of frame alignment. The TE regains frame alignment at m+1 frame.

The W6692 achieves synchronization after 5 frames, i.e m = 4.



Device	Settings	Result
W6692	m = 4	Pass

7.2.6 Multiframe Synchronization

As specified by ITU-T I.430, the Q bit is transmitted from TE to NT in the position normally occupied by the auxiliary framing bit (FA) in one frame out of 5, whereas the S bit is transmitted from NT to TE. The S and Q bit positions and multiframe structure are shown in Table 7.6.

The functions provided by W6692 are:

- Multiframe synchronization: Synchronization is achived when the M bit pattern has been correctly received during 20 consecutive frames starting from frame number 1.

  Note: Criterion for multiframe synchronization is not defined in I.430 Recommendation.
- S bits receive and detect: When synchronization is achieved, the four received S bits in frames 1, 6, 11, 16 are stored as S1 to S4 in the SQR register respectively. A change in the recived four bits (S1-4) is indicated by an interrupt (ISC in D_EXIR register and SCC in CIR register).
- Multiframe synchronization monitoring: Multiframe synchronization is constantly monitored. The synchronization state is indicated by the MSYN bit in the SQR register.
- Q bits transmit and F_A mirroring: When multiframe synchronization is achived, the four bits Q1-4 stored in the SQXR register are transmitted as the four Q bits (F_A-bit position) in frames 1, 6, 11 and 16. Otherwise the F_A bit transmitted is a mirror of the received F_A-bit. At loss of synchronization, the mirroring is resumed at the next F_A-bit.
- The multiframe synchronization can be disabled by setting MFD bit in the D_MODE register.
- According to I.430 Recommendation, the S/Q channel can be used as operation and maintenance signalling channel. At transmitter, a S/Q code for a message shall be repeated at least six times or as many as necessary to obtain the desired response. At receiver, a message shall be considered received only when the proper codes is received three consecutive times.

Table 7.6 Multiframe structure in S/T interface

Frame Number	NT-to-TE F_A-bit position	NT-to-TE M bit	NT-to-TE S bit	TE-to-NT F_A-bit position
1	ONE	ONE	S1	Q1
2	ZERO	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO	ZERO
6	ONE	ZERO	S2	Q2
7	ZERO	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO	ZERO
11	ONE	ZERO	S3	Q3
12	ZERO	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO	ZERO
16	ONE	ZERO	S4	Q4
17	ZERO	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO	ZERO
1	ONE	ONE	S1	Q1
2	ZERO	ZERO	ZERO	ZERO
etc.				

7.2.7 Test Functions

The W6692 provides loop and test functions as follows:

- digital loop via DLP bit in D_MODE register: In the layer 2 block, the transmitted 2B+D data are internally looped (from HDLC transmitter to HDLC receiver), and in the PCM ports, the transmitted B channels are internally looped (from PCM inputs to PCM outputs). The clock timings are generated internally and are independent of the S bus timing. This loop function is used for test of PCM and higher layer functions, excluding layer 1. After hardware reset, W6692 will power down if S bus is not connected or if there is no signal on the S bus. In this case, the C/I command ECK must be issued to power up the chip.

Test Functions, continued

- analog loop via the C/I command EAL: The analog S interface transmitter is internally connected to the S interface receiver. When the receiver has synchronized itself to the internal INFO 3 signal, the message "Test Indication" or "Awake Test Indication" is delivered to the CIR register. No signal is transmitted over the S interface.

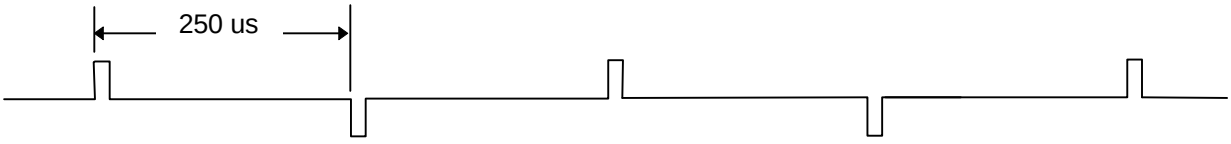
  In this mode, the S interface awake detector is enabled. Therefore if a level (INFO 2/ INFO 4) is detected on the S interface, this will be reported by the "Awake Test Indication (ATI)" indication.

- remote loopback via RLP bit in D_MODE register: The digital 2B data received from the S interface receiver is loopbacked to the S interface transmitter. The D channel is not looped. When RLP is enabled, layer 1 D channel is connected to HDLC port and DLP cannot be enabled.

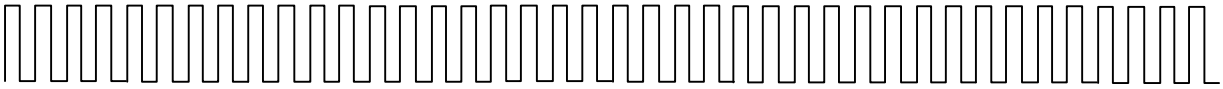
- transmission of special test signals via layer 1 command:

  * Send Single Pulses (SSP): To send isolated single pulses of alternating polarity, with pulse width of one bit time, 250 μS apart, with a repetition frequency of 2 KHz.

  * Send Continuous Pulses (SCP): To send continuous pulses of alternating polarity, with pulse width of bit time. The repetition frequency is 96 KHz.



(a) Single pulses



(b) Continuous pulses

Figure 7.7 SSP and SCP test signals

7.3 Serial Interface Bus

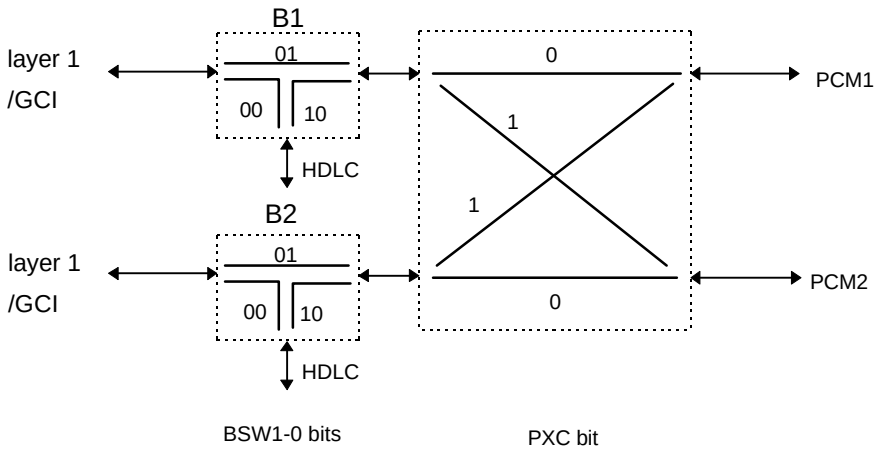
The 192 kbps S/T interface signal consists of two B channels (64 kbps each), one D channel (16 kbps) and other control signals. The multiplexing/demultiplexing functions are carried out in the Serial Interface Bus (SIB) block. In addition, the B1 and B2 channels can be individually set to carry 64 kbps or 56 kbps traffic.

7.4 B Channel Switching

Each B channel in S/T bus or U transceiver can be individually programmed to connect to one of the three data ports: B channel HDLC controller, PCM port 1 or PCM port 2. In addition, the PCM ports can be programmed to connect to the B channel HDLC controller for voice recording/ retrieving from main memory in answering machine applications. In this case, only extended transparent mode can be used.

The switching matrix is controlled by PXC bit in PCTL register and BSW1-0 bits in B1_MODE and B2_MODE registers as follows:

A special mode is provided (BSW1-0 = 11B) in which case the PCM port can receive data from layer 1 and the HDLC receiver can receive data from PCM port simultaneously.



7.5 PCM Port

There are two PCM ports in W6692. Each PCM port can connect to a PCM codec filter chip. These two PCM ports share the same signals except for the frame synchronization clocks. The frame synchronization clocks (PFCK1-2) are 8 KHz and the bit synchronization clock (PBCK) is 1.536 MHz. The bit data rate is 64 kbps per port.

7.6 D Channel HDLC Controller

There are two HDLC protocols that are used for ISDN layer 2 functions: LAPD and LAPB. Their frame formats are shown below.

LAPB modulo 8:

flag (1 octet)	address (1octet)	control (1octet)	information (0 or N octets)	FCS (2 octets)	flag (1 octet)

Control field bits	7	6	5	4	3	2	1	0
I frame	N(R)			P	N(S)			0
S frame	N(R)			P/F	S	S	0	1
U frame	M	M	M	P/F	M	M	1	1

LAPB modulo 128:

flag (1 octet)	address (1octet)	control (1 or 2 octets)	information (0 or N octets)	FCS (2 octets)	flag (1 octet)

	1st octet								2nd octet							
Control field bits	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I frame	N(S)							0	N(R)							P
S frame	X	X	X	X	S	S	0	1	N(R)							P/F
U frame	M	M	M	P/F	M	M	1	1								

LAPD: modulo 128 only

flag (1 octet)	address (2 octets)	control (2 octets)	information (0 or N octets)	FCS (2 octets)	flag (1 octet)

	1st octet								2nd octet							
Control field bits	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I frame	N(S)							0	N(R)							P/F
S frame	0	0	0	0	S	S	0	1	N(R)							P/F
U frame	M	M	M	P/F	M	M	1	1								

7.6.1 D Channel Message Transfer Modes

The D channel HDLC controller operates in transparent mode.

Chracteristics:

- Receive frame address recognition
- Address comparison maskable bit-by-bit
- Flag generation / deletion
- Zero bit insertion/ deletion
- Frame Check Sequence (FCS) generation/ check with CRC_ITU-T

Note. The LAPD protocol uses the CRC_ITU-T for Frame Check Sequence. The polynominal is $X^{16} + X^{12} + X^5 + 1$.

For address recognition, the W6692 provides four programmable registers for individual SAPI and TEI values, SAP1-2 and TEI1-2, plus two fixed values for group SAPI and TEI, SAPG and TEIG. The SAPG equals FEH or FCH which corresponds to SAPI = 63 for layer management procedure. The TEIG equals FFH which corresponds to TEI = 127 for automatic TEI assignment procedure. The address combinations are:

- SAP1 + TEI1
- SAP1 + FFH
- SAP2 + TEI2
- SAP2 + FFH
- FEH (FCH) + TEI1
- FEH (FCH) + TEI2
- FEH (FCH) + FFH

The receive frame address comparisons can be disabled (masked) per bit basis with the D_SAM and D_TAM registers, but comparisons with the SAPG or TEIG cannot be disabled.

7.6.2 Reception of Frames in D Channel

A 128-byte FIFO is provided in the receive direction. The data movement between receive FIFO and micro-processor is handled by interrupts.

There are two interrupt sources: Receive Message Ready (D_RMR) and Receive Message End (D_RME). The D_RMR interrupt indicates that at least 64 bytes of data have been received and the message/ frame is not ended. Upon D_RMR interrupt, the micro-processor reads out 64 bytes of data from the FIFO. The D_RME interrupt indicates the last segment of a message or a message with length ≤ 64 bytes has been received. The length of data is less than or equal to 64 and is specified in the D_RBCL register.

If the length of the last segment of message is 64, only D_RME interrupt is generated and the RBC5-0 bits in D_RBCL register are 000000B.

The data between the opening flag and the CRC field are stored in D_RFIFO. For LAPD frame, this includes the address field, control field and information field.

When a D_RMR or D_RME interrupt is generated, the micro-processor must read out the data from D_RFIFO and issues the Receive Message Acknowledgement command (D_CMDR: RACK bit) to explicitly acknowledge the interrupt. The micro-processor must handle the interrupt before more than 64 bytes of data are received. This corresponds to a maximum micro-processor reaction time of 32 mS at 16 kbps data rate.

If the micro-processor is late in handling the interrupt, the incoming additional bytes will result in a "data overflow" interrupt and status bit.

7.6.3 Transmission of Frames in D Channel

A 128-byte FIFO is provided in the transmit direction. If the transmit FIFO is ready (which is indicated by a D_XFR interrupt), the micro-processor can write up to 64 bytes of data into the FIFO and use the XMS command bit to start frame transmission. The HDLC transmitter sends the opening flag first and then sends the data in the transmit FIFO.

The micro-processor must write the address, control and information field of a frame into the transmit FIFO.

Every time no more than 64 bytes of data are left in the transmit FIFO, the transmitter generates a D_XFR interrupt to request another block of data. The micro-processor can then write further data to the transmit FIFO and enables the subsequent transmission by issuing an XMS command.

If the data written to the FIFO is the last segment of a frame, the micro-processor issues the XME (Transmit Message End) and XMS command bits to finish the frame transmission. The transmitter then transmits the data in the FIFO and appends CRC and closing flag.

If the micro-processor fails to respond the D_XFR interrupt within a given time (32 mS), a data underrun condition will occur. The W6692 will automatically reset the transmitter and send inter frame time fill pattern (all 1's) on D channel. The micro-processor is informed about this condition via an XDUN (Transmit Data Underrun) interrupt in D_EXIR register. The microprocessor must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

It is possible to abort a frame by issuing a D_CMDR: XRST (D channel Transmitter Reset) command. The XRST command resets the transmitter and causes a transmit FIFO ready condition.

After the micro-processor has issued the XME command, the successful termination of transmission is indicated by an D_XFR interrupt.

The inter-frame time fill pattern must be all 1's, according to ITU-T I.430.

Collisions which occur on the D channel of S interface will cause an D_EXIR: XCOL interrupt. A XRST (Transmitter Reset) command must be issued and software must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

7.7 B Channel HDLC Controller

There are two B channel HDLC controllers. Each B channel HDLC controller provides two operation modes:

- Transparent mode

  characteristics:

  * 2 byte address field
  * Receive address comparison maskable bit-by-bit
  * Data between opening flag and CRC (not included) stored in receive FIFO
  * Flag generation/ deletion
  * Frame Check Sequence generation/ check with CRC_ITU-T polynominal
  * Zero bit insertion/ deletion

- Extended transparent mode

  characteristics:

  * All data transmitted/ received without modification
  * No address comparison
  * No flag generation/ detection
  * No FCS generation/ check
  * No bit stuffing

For PCM-HDLC connection, only extended transparent mode can be selected.

The data rate in B channel can be set at 64 kbps or 56 kbps by the B1_MODE (B2_MODE): SW56 bit.

7.7.1 Reception of Frames in B Channel

A 128-byte FIFO is provided in the receive direction. The receive FIFO threshold can be set at 64 or 96 bytes by the Bn_MODE register. If the number of received data reaches the threshold, a Receive Message Ready (RMR) interrupt will be generated.

The operations for reception of frames differ in each mode:

Transparent mode: The received frame address is compared with the contents in receive address registers. In addition, the comparisons can be selectively masked bit-by-bit via address mask registers. Comparison is disabled when the corresponding mask bit is "1".

In addition, flag recognition, CRC check and zero bit deletion are also performed. The result of CRC check is indicated in Bn_STAR:CRCE bit. The data between opening flag and CRC field (not included) is stored in receive FIFO. Two interrupts are used for the reception of data. The RMR interrupt in Bn_EXIR register indicates at least a threshold block of data have been put in the receive FIFO. The RME interrupt in Bn_EXIR register indicates the end of frame has been received. The micro-processor can read out a threshold length of data from receive FIFO at RMR interrupt, or all the data in receive FIFO at RME interrupt. At each RMR/ RME interrupt, micro-processor must issue a Receive Message Acknowledgement(RACK) command to explicitly acknowledge the interrupt.

The micro-processor reaction time for RMR/ RME interrupt depends on the FIFO threshold setting and B channel data rate. For example, it is 8 mS if the FIFO threshold is 64 and the B channel data rate is 64 kbps.

If the micro-processor is late in handling the interrupt, the incoming additional bytes will result in a "data overflow" interrupt and status bit.

Extended transparent mode: In this mode, all data received are stored in the receive FIFO without any modification. Every time up to a threshold length of data has been stored in the FIFO, a Bn_RMR interrupt is generated.

In this mode, there is no RME interrupt.

The micro-processor must react to the RMR interrupt in time, otherwise a "data overflow" interrupt and status bit will be generated.

7.7.2 Transmission of Frames in B Channel

A 128-byte FIFO is provided in the transmit direction. The FIFO threshold can be set at 64 or 96 bytes. The transmitter and receiver use the same FIFO threshold setting.

The transmit operations differ in both modes:

Transparent mode:

In this mode, the following functions are performed by the transmitter automatically:

- Flag generation
- CRC generation
- Zero bit insertion

The fields such as address, control and information are provided by the micro-processor and are stored in transmit FIFO. To start the frame transmission, the micro-processor issues a XMS (Transmit Message Start) command. The transmitter requests another block of data via XFR interrupt when more than a threshold length of vacancies are left in the FIFO.The micro-processor then writes up to a threshold length of data into the FIFO and activates the subsequent transmission of the frame by a XMS command too. The micro-processor indicates the end of the frame transmission by issuing XME (Transmit Message End) and XMS commands at the same time. The transmitter then transmits all the data left in the transmit FIFO and appends the CRC and closing flag. After this, a XFR interrupt is generated.

The inter-frame time fill pattern can be programmed to 1's or flags.

During the frame transmission, the micro-processor reaction time for the XFR interrupt depends on the FIFO threshold setting and B channel data rate. For example, it is 8 mS if the FIFO threshold is 64 and the B channel data rate is 64 kbps. If the micro-processor fails to responds within the given reaction time, the transmit FIFO will be underrun. In this case, the W6692 will automatically reset the transmitter and send the inter frame time fill pattern on B channel. The micro-processor is informed about this via a Transmit Data Underrun interrupt (XDUN bit in Bn_EXIR register). The microprocessor must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

The micro-processor can abort a frame transmission by issuing a Transmitter Reset command (XRES bit in Bn_CMDR register). The XRES command resets the transmitter and sends inter frame time fill pattern on B channel. It also results in a transmit pool ready condition.

Extended transparent mode:

All the data in the transmit FIFO are transmitted without any modification, i.e. no flags and CRCs are inserted, and no bit stuffing is performed.

Transmission is started by a XMS command. The transmitter requests another block of data via XFR interrupt when more than a threshold length of vacancies are left in the FIFO. The micro-processor reacts to this condition by writing up to a threshold length of data into the transmit FIFO and issues a XMS command to continue the message transmission.

The micro-processor reaction time depends on the FIFO threshold setting and B channel data rate. For example, it is 8 mS if the FIFO threshold is 64 and the B channel data rate is 64 kbps. If the micro-processor fails to respond within the given reaction time, the transmit FIFO will hold no data to transmit. In this case, the W6692 will automatically reset the transmitter and send the inter frame time fill pattern on B channel. The micro-processor is informed about this via a Transmit Data Underrun interrupt (XDUN bit in Bn_EXIR register). The microprocessor must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

7.8 GCI Mode Serial Interface Bus

The GCI is a generalization and enchancement of the general purpose serial interface bus. The GCI bus offers capacity for the transfer of maintenance information. In terminal applications, the GCI constitute a powerful backplane bus offering sophisticated control capabilities for peripheral modules. The channel structure of the GCI mode is depicted below:

Channel Structure of the W6692 GCI Mode:

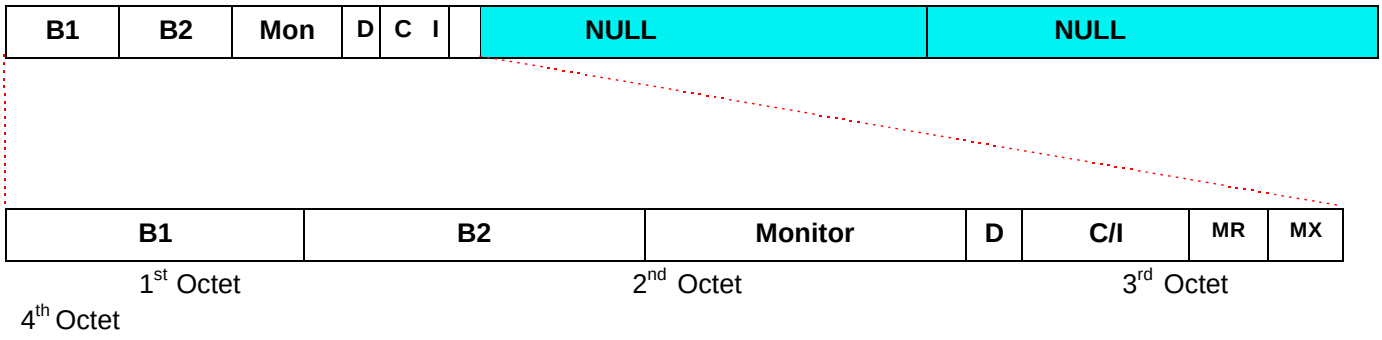


Figure 7.8 GCI Mode Channel Structure

The first two octets constitute the two 64 Kbps B channels.

The third octet is the Monitor channel. It is used for the exchange of data between the W6692 and the other attached device

using the GCI Monitor channel protocol.

The fourth octet (control channel) contains: two bits for the 16 Kbps D channel, a 4-bit C/I channel (Command/Indication channel), and 2-bit MR and MX for supporting the Monitor channel handshaking protocol.

The W6692 GCI Mode Signals are:

DIN/DOUT : 768 Kbps

DCL : 1.536 MHz input

FSC : 8 KHz input

7.8.1 GCI Mode C/I Channel Handling

The Command/Indication channel carries real-time status information between the W6692 and another device connected to the GCI bus interface.

One C/I channel conveys the commands and indications between a layer 1 device and layer 2 device. This C/I channel is access via register CIR (in receive direction, layer 1 to layer 2) and register CIX (in transmit direction, layer 2 to layer 1). The C/I code is 4-bit long.

- In the receive direction, the code from layer 1 is continuously monitored, with an interrupt being generated anytime a change occurs. A new code must be found in two consecutive GCI frames to be consided valid and to trigger a C/I code change interrupt status (double last look criterion).
- In the transmit direction, the code written in CIX is continuously transmitted in the channel.

7.8.2 GCI Mode Monitor Channel Handling

The Monitor channel protocol is a handshake protocol used for high speed information exchange between the W6692 and other devices. In the W6692 GCI mode only one Monitor channel is available. The Monitor channel is necessary for:

- programming and controlling devices attached to the GCI interface.
- data exchange between two microprocessor systems attached to two different devices on one GCI backplane. Use of the Monitor channel avoids the necessity of a dedicated serial communication path between two systems.

The Monitor channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the Monitor Channel Receiver (MOR) and Monitor Channel Transmit (MOX) bits. When data is placed into the Monitor channel and the MX bit is activated. This data will be transmitted repeatedly once per 8 KHz frame until the transfer is acknowledged via the MR bit.

The microprocessor may either enforce a 1 (idle state) in MR, MX by setting the control bit MRC or MXC (MOCR register) to 0, or enable the control of these bits internally by the W6692 according to the Monitor channel protocol. Thus, before a data exchange can begin, the control bit MRC, or MXC should be set to 1 by the microprocessor.

The relevant status bits are:

- for the reception of Monitor data: MDR (Monitor Channel Data Received) ⇔ MER (Monitor Channel End of Reception)
- for the transmission of Monitor data: MDA (Monitor Channel Data Acknowledged) ⇔ MAB (Monitor Channel Data Abort)

About the status bit MAC (Monitor Channel Transmit Active) indicates whether a transmission is progress**.**

- if set MAC = 0, the previous transmission has been terminated. Before starting a transmission, the microprocessor should verify that the transmitter is inactive.
- if set MAC = 1, after having written data into the Monitor Transmit Channel (MOX) register, the microprocessor sets this bit to 1. This enables the MX bit to go active (0), indicating the presence of valid Monitor data (contents of MOX) in the corresponding frame.

The receiing device stores the Monitor byte in its MOR (Monitor Receive Register) and generates a MDR (Monitor Channel Data Receive) interrupt status. Alerted by the MDR interrupt, the microprocessor reads the MOR register. When it is ready to accept data, it sets the MR control bit MRC to 1 to enable the receiver to store succeeding Monitor channel bytes and acknowledge them according to the Monitor channel protocol. In addition, it enables other Monitor channel interrupts by setting Monitor Channel Interrupt Enable to 1.

The first Monitor channel byte is acknowledged by the receiving device setting the MR bit to 0. This causes a MDA (Monitor Channel Data Acknowledge) interrupt status at the transmitter. A new Monitor channel data byte can now be written by the microprocessor in MOX register. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the Monitor channel by returning the MX bit active after sending it once in the inactive state. The receiver stores the Monitor channel byte in MOR register and generates a new MDR interrupt status. When the microprocessor has read the MOR register , the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate a MDA interrupt status. This ″MDA interrupt ⇒ write data ⇒ MDR interrupt ⇒ read data ⇒ MDA interrupt ″ handshake procedure is repeated as long as the transmitter has data to send.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the Monitor channel Transmit Control bit MXC to 0. This enforces an inactive (1) state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a MER (Monitor channel End of Reception) interrupt status is generated by the receiver when the MX is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmittion, making the MAC (Monitor channel Active) bit return to 0.

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to 0. An aborted transmission is indicated by a MAB (Monitor Channel Data Abort) interrupt status at the transmitter.

7.9 PCI Interface Circuit

7.9.1 PCI Slave Mode And Configuration Serial EEPROM

W6692 implements slave (target) mode function which meets PCI local bus specification revision 2.1. All the signals are 5V, 33 MHz compatible. A signle function, type 00h configuration header is implemented for control of the internal ISDN device and external peripheral device(s). Memory mode and/or IO mode can be used for W6692's register access.

After power on reset, W6692 starts to read configuration data from serial EEPROM port. The first word read is Vendor ID, if it equals FFFFH, default configuration data is used, otherwise, the configuration data stored in serial EEPROM is used. The default configuration data is as follows:

Vendor ID	: 1050H (Winbond's ID)
Device ID	: 6692H
Class Code	: 02 80 00H
Revision ID	: 00H
Subsystem Vendor ID	: FFFFH
Subsystem ID	: FFFFH
Memory Base Address Register	: Enabled and Implemented at 10H
IO Base Address Register	: Enabled and Implemented at 14H

A 9346/93C46 type serial EEPROM is used for configuration data storage. The format is as follows:

ADDRESS	15		8	7		0
0	15	Vendor ID				0
1	15	Device ID				0
2	7	Interface Code	0	7	Revision ID	0
3	7	Base Class Code	0	7	Subclass Code	0
4	15	Subsystem Vendor ID				0
5	15	Subsystem ID				0
6	15	Address Register Control				0

Address Register Control:

15	14	13	12 ... 0
MEN	IEN	PRE	not used

Figure 7.9 Serial eeprom data format

Important Note:

In all PC platforms, burst mode is used very often for memory access. Because W6692 does not support burst mode, it is recommended not to use memory access for W6692's internal registers and data.

The Address Register Control determines the Address Registers implementation. Bit 13 is the prefetchable bit in Memory Base Address register.

MEN	IEN	LOCATION 10H	LOCATION 14H	PRE USED
1	1	Memory Base Address Reg.	IO Base Address Reg.	Yes
1	0	Memory Base Address Reg.	Not Implemented	Yes
0	1	IO Base Address Reg.	Not Implemented	No
0	0	Not Implemented	Not Implemented	No
EEPROM empty		Memory Base Address Reg.	IO Base Address Reg.	PRE = 1

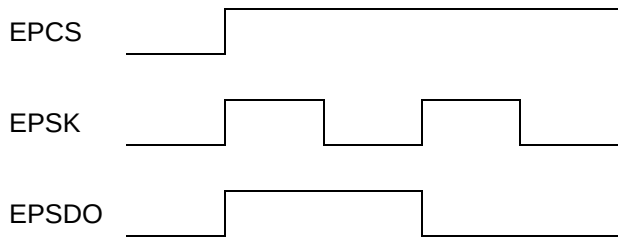
In all cases, Memory Base Address register allocates 4096 byte spaces and IO Base Address register allocates 256 byte space.

W6692 provides one register for on-board programming of the serial EEPROM. This register called EPCTL register is at offset address FCH. The format is:

7 ... 3	2	1	0
Reserved	EN	SK	CS	SDO

The data written at bits 2-0 are directly output on pins EPSK, EPCS and EPSDO if EN = 1. The outputs are disabled if EN = 0. EN bit does not affect the power on configuration read. For example, to generate the following waveform, the write data sequence is:

SEQUENCE	EN	SK	CS	SDO
1	1	0	0	0
2	1	1	1	1
3	1	0	1	1
4	1	1	1	0
5	1	0	1	0



7.9.2 Cascade Structure of Interrupt Sources

The W6692 uses cascade structure to record the causes of various interrupts. The interrupt structure is shown in Figure 7.10.

A read of the ISTA register clears all the interrupts except D_EXI, B1_EXI and B2_EXI bits. These three bits are cleared if their corresponding extended interrupt registers are cleard.

B1_EXI bit is cleared by reading the B1_EXIR register and B2_EXI bit is cleared by reading the B2_EXIR register. Reading of B1_EXIR or B2_EXIR register clears all the bits in it. The B1_EXIM and B2_EXIM registers mask the corresponding bits in the B1_EXIR and B2_EXIR registers.

To clear the D_EXI bit, all the bits in D_EXIR must first be cleared. A read of the D_EXIR register clears all the bits except the ISC bit. The ISC bit is cleared by a read of CIR and SQR registers.

An ISC interrupt may originate from

- a change in the received indication code (ICC bit in CIR register) or
- a change in the received S code (SCC bit in CIR register).

The ICC interrupt can not be disabled while the SCC interrupt can be disbled by clearing the SCIE bit in SQX register.

Bits SCC and ICC are cleared by a read of SQR and CIR.

D_EXIM register masks the corresponding bits in D_EXIR register. If the D_EXIM: ISC bit is set to one, it masks the ICC and SCC interrupts.

The ICC or SCC bit is set whenever a new code is loaded in CIR or SQR. But if the previous register content has not been read out in case of a code change, the new code will not be loaded. The code registers are buffered with a FIFO size of two. Thus if several consecutive code changes are detected, only the first and the last code is obtained at the first and second register read, respectively.

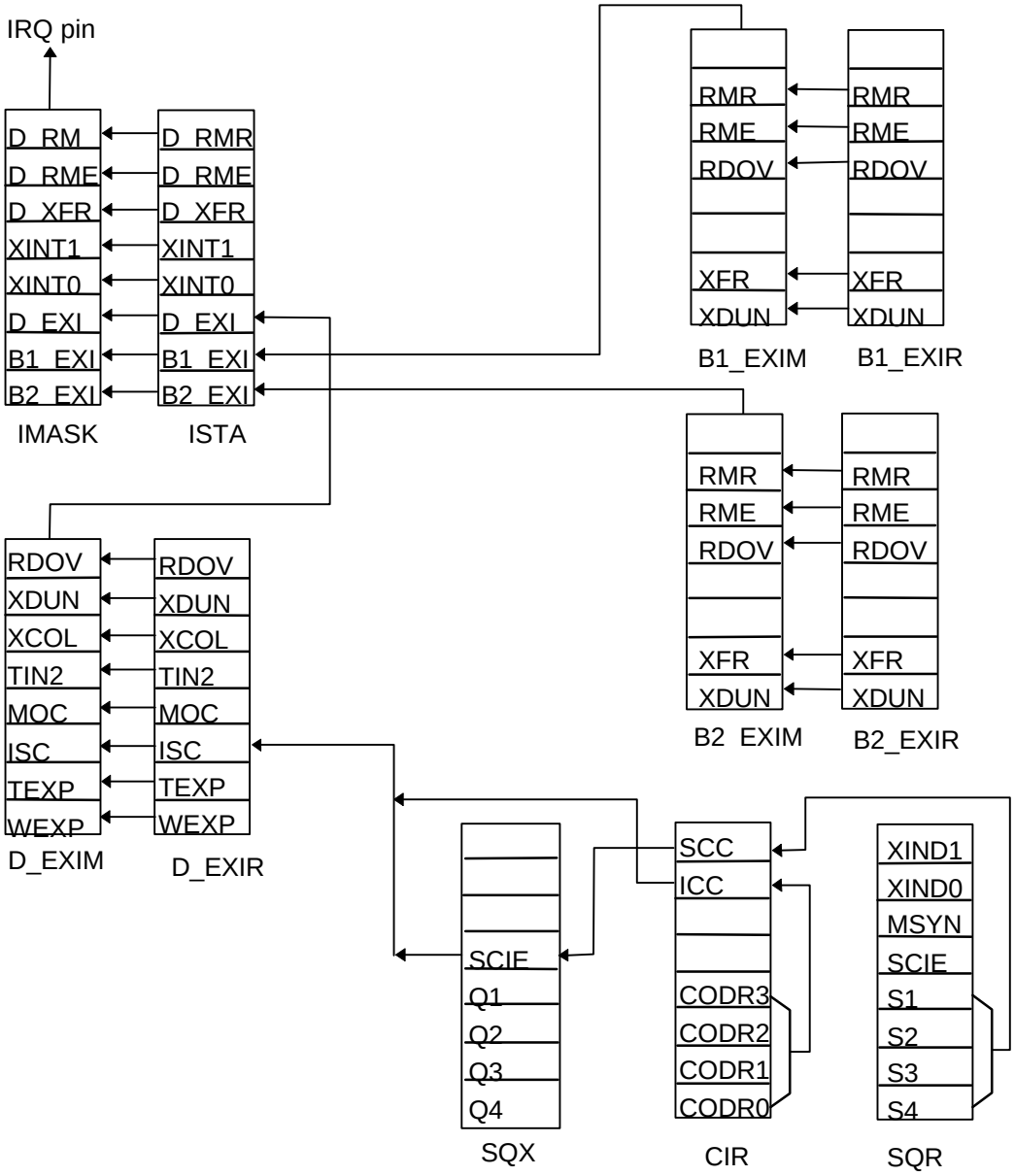


Figure 7.10 W6692 interrupt structure

7.10 Peripheral Control

In PCI card with POTS application, the peripheral devices such as CODEC, DTMF and SLIC can be directly controlled by W6692, therefore preclude the need for another PCI controller chip. The peripheral control function includes timer, interrupt inputs and programmable IOs or microprocessor interface.

There are two timers implemented in W6692: D_TIMR and TIMR2. D_TIMR is a long period timer whcich can be used to control the 1 sec, 2 sec ON/OFF of ring tone. While TIMR2 is a short period timer which can be used to generate the tens hertz of ring signal.

	ADDRESS	INTERRUPT STATUS	INTERRUPT MASK	OUTPUT PIN	PERIOD	CYCLIC
D_TIMR	10H	DEXIR: TEXP	DEXIM: TEXP	No	(0..6) x 2.048 s +(1..32) x 64 mS	Yes (CNT = 7)
TIMR2	4CH	DEXIR: TIN2	DEXIM: TIN2	TOUT2	(1..63) mS	Yes (TMD = 1)

TOUT2 toggles when TIMR2 counts down to zero. For example, if the timer period is 1 mS, then the period of TOUT2 is 2 mS.

There are two interrupt input pins: XINTIN0, XINTIN1. Whenever signal level changes (eith rising or falling), a maskable interrupt is generated which in turn will make an interrupt request on PCI bus if it is unmasked. The interrupt status bits are ISTA: XINT0, ISTA: XINT1. The mask bits are IMASK: XINT0, IMASK: XINT1. In addition, the signal level can be read at bits SQR: XIND0, SQR; XIND1. These pins can be used for monitor of SLIC hook state and/or DTMF data valid status.

The IO interface can be programmed as simple IO (PCTL: XMODE = 0) or 8-bit microprocessor interface (PCTL: XMODE = 1). As simple IOs, the directions of the 11 pins are selected via OE5-0 bits in PCTL register and the read/write data accessed via XADDR and XDATA registers. As output, the register data is output on the pin, as input, the current level of pin is read in. In this mode, a maximum of 11 IO ports are supported.

If programmed as 8-bit microprocessor mode, an 8-bit multiplexed bus is used to control peripheral deveces. The address and data are multiplexed on XAD7-0. XALE is used for address latch and XRDB, XWRB are used for read/write strobe. To access peripheral device, first write the desired address in XADDR register and then read/write data at XDATA register. In this mode, a maximum of 256 byte ports can be supported by adding some glue TTLs on board.

8. REGISTER DESCRIPTIONS

8.1 Chip Control and D_ch HDLC controller

Table 8.1 Register address map: Chip Control and D channel HDLC

SECTION	OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
8.1.1	00	R	D_RFIFO	D channel receive FIFO
8.1.2	04	W	D_XFIFO	D channel transmit FIFO
8.1.3	08	W	D_CMDR	D channel command register
8.1.4	0C	R/W	D_MODE	D channel mode control
8.1.5	10	R/W	D_TIMR	D channel timer control
8.1.6	14	R_clear	ISTA	Interrupt status register
8.1.7	18	R/W	IMASK	Interrupt mask register
8.1.8	1C	R_clear	D_EXIR	D channel extended interrupt
8.1.9	20	R/W	D_EXIM	D channel extended interrupt mask
8.1.10	24	R	D_STAR	D channel status register
8.1.11	28	R	D_RSTA	D channel receive status
8.1.12	2C	R/W	D_SAM	D channel address mask 1
8.1.13	30	R/W	D_SAP1	D channel individual SAPI 1
8.1.14	34	R/W	D_SAP2	D channel individual SAPI 2
8.1.15	38	R/W	D_TAM	D channel address mask 2
8.1.16	3C	R/W	D_TEI1	D channel individual TEI 1
8.1.17	40	R/W	D_TEI2	D channel individual TEI 2
8.1.18	44	R	D_RBCH	D channel receive frame byte count high
8.1.19	48	R	D_RBCL	D channel receive frame byte count low
8.1.20	4C	W	TIMR2	Timer 2
8.1.21	50	R/W	L1_RC	GCI layer 1 ready code
8.1.22	54	R/W	D_CTL	D channel control register
8.1.23	58	R	CIR	Command/Indication receive
8.1.24	5C	W	CIX	Command/Indication transmit
8.1.25	60	R	SQR	S/Q channel receive register
8.1.26	64	W	SQX	S/Q channel transmit register
8.1.27	68	R/W	PCTL	Peripheral control register
8.1.28	6C	R	MOR	Monitor receive channel
8.1.29	70	R/W	MOX	Monitor transmit channel
8.1.30	74	R	MOSR	Monitor channel status register
8.1.31	78	R/W	MOCR	Monitor channel control register
8.1.32	7C	R/W	GCR	GCI mode control register
8.1.33	F4	R/W	XADDR	Peripheral address register
8.1.34	F8	R/W	XDATA	Peripheral data register
8.1.35	FC	W	EPCTL	Serial EEPROM control

Table 8.2 Register summary: Chip Control and D channel HDLC

OFFSET	R/W	NAME	7	6	5	4	3	2	1	0
00	R	D_RFIFO								
04	W	D_XFIFO								
08	W	D_CMDR	RACK	RRST		STT	XMS		XME	XRST
0C	R/W	D_MODE	MMS	RACT		TMS	TEE	MFD	DLP	RLP
10	R/W	D_TIMR	CNT2	CNT1	CNT0	VAL4	VAL3	VAL2	VAL1	VAL0
14	R_clr	ISTA	D_RMR	D_RME	D_XFR	XINT1	XINT0	D_EXI	B1_EXI	B2_EXI
18	R/W	IMASK	D_RMR	D_RME	D_XFR	XINT1	XINT0	D_EXI	B1_EXI	B2_EXI
1C	R_clr	D_EXIR	RDOV	XDUN	XCOL	TIN2	MOC	ISC	TEXP	WEXP
20	R/W	D_EXIM	RDOV	XDUN	XCOL	TIN2	MOC	ISC	TEXP	WEXP
24	R	D_STAR	XDOW		XBZ	DRDY				
28	R	D_RSTA		RDOV	CRCE	RMB				
2C	R/W	D_SAM	SAM7	SAM6	SAM5	SAM4	SAM3	SAM2	SAM1	SAM0
30	R/W	D_SAP1	SA17	SA16	SA15	SA14	SA13	SA12	SA11	SA10
34	R/W	D_SAP2	SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20
38	R/W	D_TAM	TAM7	TAM6	TAM5	TAM4	TAM3	TAM2	TAM1	TAM0
3C	R/W	D_TEI1	TA17	TA16	TA15	TA14	TA13	TA12	TA11	TA10
40	R/W	D_TEI2	TA27	TA26	TA25	TA24	TA23	TA22	TA21	TA20
44	R	D_RBCH	VN1	VN0	LOV	RBC12	RBC11	RBC10	RBC9	RBC8
48	R	D_RBCL	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
4C	W	TIMR2	TMD	0	TCN5	TCN4	TCN3	TCN2	TCN1	TCN0
50	R/W	L1_RC					RC3	RC2	RC1	RC0
54	R/W	D_CTL	WTT1	WTT2	SRST			TPS	OPS1	OPS0
58	R	CIR	SCC	ICC			CODR3	CODR2	CODR1	CODR0
5C	W	CIX					CODX3	CODX2	CODX1	CODX0
60	R	SQR	XIND1	XIND0	MSYN	SCIE	S1	S2	S3	S4
64	W	SQX				SCIE	Q1	Q2	Q3	Q4
68	R/W	PCTL	OE5	OE4	OE3	OE2	OE1	OE0	XMODE	PXC
6C	R	MOR								
70	R/W	MOX								
74	R_clr	MOSR					MDR	MER	MDA	MAB
78	R/W	MOCR					MRIE	MRC	MXIE	MXC
7C	R/W	GCR	MAC			TLP	GRLP	SPU	PD	GE
F4	R/W	XADDR	XA7/IO7	XA6/IO6	XA5/IO5	XA4/IO4	XA3/IO3	XA2/IO2	XA1/IO1	XA0/IO0
F8	R/W	XDATA	XD7	XD6	XD5	XD4	XD3	XD2/IO10	XD1/IO9	XD0/IO8
FC	W	EPCTL					EN	SK	CS	SDO

8.1.1 D_ch receive FIFO D_RFIFO Read Address 00H

The D_RFIFO has a length of 128 bytes.

After a D_RMR interrupt, exactly 64 bytes are available.

After a D_RME interrupt, the number of bytes available equals RBC5-0 bits in the D_RBCL register.

8.1.2 D_ch transmit FIFO D_XFIFO Write Address 04H

The D_XFIFO has a length of 128 bytes.

After an D_XFR interrupt, up to 64 bytes of data can be written into this FIFO for transmission. At the first time, up to 128 bytes of data can be written.

8.1.3 D_ch command register D_CMDR Write Address 08H

Value after reset: 00H

7	6	5	4	3	2	1	0
RACK	RRST		STT	XMS		XME	XRST

RACK Receive Acknowledge

After a D_RMR or D_RME interrupt, the processor must read out the data in D_RFIFO and then sets this bit to acknowledge the interrupt.

RRST Receiver Reset

Setting this bit resets the D_ch HDLC receiver and clears the D_RFIFO data.

STT Start Timer

The D_ch hardware timer is started when this bit is set to one. The timer is stopped when it expires or by a write of the D_TIMR register. Note that the timer must be in external mode.

XMS Transmit Message Start/Continue

Setting this bit will start or continue the transmission of a frame. The opening flag is automatically added by the HDLC controller.

XME Transmit Message End

Setting this bit indicates the end of frame transmission. The D_ch HDLC controller automatically appends the CRC and the closing flag after the data transmission.

Note: If the frame ≤ 64 bytes, XME plus XMS commands must be issued at the same time.

XRST Transmitter Reset

Setting this bit resets the D_ch HDLC transmitter and clears the D_XFIFO. The transmitter will send inter frame time fill pattern (which is 1's) immediately. This command also results in a transmit FIFO ready condition.

8.1.4 D_ch Mode Register D_MODE Read/Write Address 0CH

Value after reset: 00H

7	6	5	4	3	2	1	0
MMS	RACT		TMS	TEE	MFD	DLP	RLP

MMS Message Mode Setting

Determines the message transfer mode of the D_ch HDLC controller:

MMS	MODE	ADDRESS BYTES	FIRST BYTE ADDRESS COMPARISON WITH:	SECOND BYTE ADDRESS COMPARISON WITH:
0	Transparent mode	2	D_SAP1, D_SAP2, SAPG	D_TEI1, D_TEI2, TEIG

Notes:

1. D_SAP1, D_SAP2: two programmable address values for the first received address byte; SAPG = fixed value FC/FEH. D_TEI1, D_TEI2 : two programmable address values for the second received address byte; TEIG = fixed value FFH.
2: The first byte address comparison can be masked by D_SAM register, and the second byte address comparison can be masked by D_TAM register. But the comparisons with SAPG and TEIG cannot be disabled.

RACT Receiver Active

Setting this bit activates the D_ch HDLC receiver. This bit can be read. The receiver must be in active state in order to receive data.

TMS Timer Mode Setting

Sets the operating mode of the D_ch timer. In the external mode (TMS = 0), the timer is controlled by the processor. It is started by setting the STT bit in D_CMDR and is stopped by a write of the D_TIMR register or when it expires. When the timer expires, a maskable D_EXP interrupt is generated.

In the internal mode (TMS = 1), the timer is used for internal test purposes. It should not be selected for normal chip operation.

TEE Terminal Equipment Function Enable

The terminal equipment function is enabled when this bit is "1". The supported functions are:

- Watchdog timer, enabled when TEE = 1 and D_CTL: TPS =1
- Exchange awake, enabled when TEE = 1 and D_CTL: TPS =0

When the watchdog timer has been enabled, the micro-processor has to program the WTT1, 2 bits in a specified manner within 1024 mS to reset and restart the timer. Otherwise, the timer will expire in 1024 mS and a WEXP interrupt together with a 125 µS reset pulse on TRST pin is generated.

The exchange awake condition is initiated by C/I code change condition. A 16 mS reset pulse on TRST pin is generated.

Switching TPS bit will reset the watchdog timer.

The TEE bit is cleared only by a hardware reset.

MFD Multiframe Disable

This bit is used to enable or disable the multiframe structure on S/T interface:

0 : Multiframe is enabled
1 : Multiframe is disabled

DLP Digital Loopback

Setting this bit activates the digital loopback function. The transmitted digital 2B+D channels are looped to the received 2B+D channels. Note that after hardware reset, the internal clocks will turn off if the S bus is not connected or if there is no signal on the S bus. In this case, the C/I command ECK must be issued to enable loopback function.

RLP Remote Loopback

Setting this bit to "1" activates the remote loopback function. The received 2B channels from the S interface are looped to the transmitted 2B channels of S interface. The D channel is not looped in this loopback function.

8.1.5 D_ch Timer Register D_TIMR Read/Write Address 10H

Value after reset: FFH

7	6	5	4	3	2	1	0
CNT2	CNT1	CNT0	VAL4	VAL3	VAL2	VAL1	VAL0

CNT together with VAL determine the time period T2 after which a TEXP interrupt will be generated:

T2 = CNT * 2.048 s + T1 with T1 = (VAL +1) * 0.064 s

The timer is started by setting the STT bit in D_CMDR and will be stopped when a TEXP interrupt is generated or the D_TIMR register is written.

Note: If CNT is set to 7, a TEXP interrupt is generated periodically at every expiration of T1.

This register can be read only after the timer has been started. The read value indicates the timer's current count value. In case layer 1 is not activated, a C/I command "ECK" must be issued in addition to the STT command to start the timer.

8.1.6 Interrupt Status RegisterISTA Read_clear Address 14H

Value after reset: 00H

7	6	5	4	3	2	1	0
D_RMR	D_RME	D_XFR			D_EXI	B1_EXI	B2_EXI

D_RMR D_ch Receive Message Ready

A 64-byte data is available in the D_RFIFO. The frame is not complete yet.

D_RME D_ch Receive Message End

The last part of a frame with length > 64 bytes or a whole frame with length ≤ 64 bytes has been received. The whole frame length is obtained from D_RBCH + D_RBCL registers. The length of data in the D_RFIFO equals:

Data length = RBC5-0 if RBC5-0 ≠ 0

Data length = 64 if RBC5-0 =0

D_XFR D_ch Transmit FIFO Ready

This bit indicates that the transmit FIFO is ready to accept data. Up to 64 bytes of data can be written into the D_XFIFO.

An D_XFR interrupt is generated in the following cases:

- after an XMS command, when ≥64 bytes of XFIFO is empty
- after an XMS together with an XME command is issued, when the whole frame has been transmitted
- after hardware reset

XINT1 XINTIN1 Interrupt

This bit indicates that level change occurs at XINTIN1 pin. Both positive and negative edges will cause an interrupt.

XINT0 XINTIN1 Interrupt

This bit indicates that level change occurs at XINTIN0 pin. Both positive and negative edges will cause an interrupt.

D_EXI D_ch Extended Interrupt

This bit indicates that at least one interrupt bit has been set in D_EXIR register.

B1_EXI B1_ch Extended Interrupt

This bit indicates that at least one interrupt bit has been set in B1_EXIR register.

B2_EXI B2_ch Extended Interrupt

This bit indicates that at least one interrupt bit has been set in B2_EXIR register.

Note: A read of the ISTA register clears all bits except D_EXI, B1_EXI and B2_EXI bits. D_EXI bit is cleared when all bits in D_EXIR register are cleared, B1_EXI bit is cleared by reading B1_EXI register and B2_EXI bit is cleared by reading B2_EXIR register.

8.1.7 Interrupt Mask Register IMASK R/W Address 18H

Value after reset: FFH

7	6	5	4	3	2	1	0
D_RMR	D_RME	D_XFR	XINT1	XINT0	D_EXI	B1_EXI	B2_EXI

Setting the bit to "1" masks the corresponding interrupt source in ISTA register. Masked interrupt status bits are read as zero. They are internally stored and pending until the mask bits are zero.

Setting the D_EXI, B1_EXI or B2_EXI bit to "1" masks all the interrupts in D_EXIR, B1_EXIR or B2_EXIR register, respectively.

8.1.8 D_ch Extended Interrupt Register D_EXIR Read_clear Address 1CH

Value after reset: 00H

7	6	5	4	3	2	1	0
RDOV	XDUN	XCOL		MOC	ISC	TEXP	WEXP

RDOV Receive Data Overflow

Frame overflow (too many short frames) or data overflow occurs in the receive FIFO. In data overflow, the incoming data will overwrite the data in the receive FIFO. If RDOV interrupt occurs, software has to reset the receiver and discard the data received.

XDUN Transmit Data Underrun

This interrupt indicates the D_XFIFO has run out of data. In this case, the W6692 will automatically reset the transmitter and send the inter frame time fill pattern (all 1's) on D channel. The microprocessor must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

XCOL Transmit Collision

This bit indicates a collision on the S-bus has been detected. A XRST command must be issued and software must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

TIN2 Timer 2 Expiration

This bit is set when Timer 2 counts down to zero.

MOC Monitor Channel Status Change

A change in the GCI mode Monitor Channel Status Register (MOSR) has occurred.

A new Monitor channel byte is stored in the MOR register.

ISC Indication or S Channel Change

A change in the layer 1 indication code or multiframe S channel has been detected. The actual value can be read from CIR or SQR registers.

TEXP D_ch Timer Expiration

Expiration occurs in the D_ch timer. The timer must be in external mode.

WEXP Watchdog Timer Expiration

Expiration occurs in the watch dog timer. A reset pulse with 125 µS pulse width is also generated on the TRST pin. See D_CTL register for watch dog timer control.

8.1.9 D_ch Extended Interrupt Mask Register D_EXIM Read/Write Address 20H

Value after reset: FFH

7	6	5	4	3	2	1	0
RDOV	XDUN	XCOL	TIN2	MOC	ISC	TEXP	WEXP

Setting the bit to "1" masks the corresponding interrupt source in D_EXIR register. Masked interrupt status bits are read as zero. They are internally stored and pending until the mask bits are zero.

All the interrupts in D_EXIR will be masked if the IMASK: D_EXI bit is set to "1".

8.1.10 D_ch Status Register D_STAR Read Address 24H

Value after reset: 0XH

7	6	5	4	3	2	1	0
XDOW		XBZ	DRDY				

XDOW Transmit Data Overwritten

At least one byte of data has been overwritten in the D_XFIFO. This bit is set by data overwritten condition and is cleared only by XRST command.

XBZ Transmitter Busy

This bit indicates the D_HDLC transmitter is busy. The XBZ bit is active from the transmission of opening flag to the transmission of closing flag.

DRDY D Channel Ready

This bit indicates the status of layer 1 D channel.

0: The layer 1 D channel is not ready. No transmission is allowed.

1: The layer 1 D channel is ready. Layer 2 can transmit data to layer 1.

8.1.11 D_ch Receive Status Register D_RSTA Read Address 28H

Value after reset: 20H

7	6	5	4	3	2	1	0
	RDOV	CRCE	RMB				

RDOV Receive Data Overflow

A "1" indicates that the D_RFIFO is overflow. The incoming data will overwrite data in the receive FIFO. The data overflow condition will set both the status and interrupt bits. It is recommended that software must read the RDOV bit after reading data from D_RFIFO at RMR or RME interrupt. The software must abort the data and issue a RRST command to reset the receiver if RDOV = 1. The frame overflow condition will not set this bit.

CRCE CRC Error

This bit indicates the result of frame CRC check:

0: CRC correct

1: CRC error

RMB Receive Message Aborted

A "1" means that a sequence of seven 1's was received and the frame is aborted. Software must issue RRST command to reset the receiver.

Note: Normally D_RSTA register should be read by the micro-processor after a D_RME interrupt. The contents of D_RSTA are valid only after a D_RME interrupt and remain valid until the frame is acknowledged via a RACK bit.

8.1.12 D_ch SAPI Address Mask D_SAM Read/Write Address 2CH

Value after reset: 00H

7	6	5	4	3	2	1	0
SAM7	SAM6	SAM5	SAM4	SAM3	SAM2	SAM1	SAM0

This register masks(disables) the first byte address comparison of the incoming frame. If the mask bit is "1" the corresponding bit comparisons with D_SAP1, D_SAP2 are disabled. Comparison with SAPG is always performed.

Note: For the LAPD frame, the least significant two bits are the C/R bit and EA = 0 bit. It is suggested that the comparison with C/R bit be masked. EA = 0 for two octet address frame e.g LAPD, EA = 1 for one octet address frame.

8.1.13 D_ch SAPI1 Register D_SAP1 Read/Write Address 30H

Value after reset: 00H

7	6	5	4	3	2	1	0
SA17	SA16	SA15	SA14	SA13	SA12	SA11	SA10

This register contains the first choice of the first byte address of received frame. For LAPD frame, SA17 - SA12 is the SAPI value, SA11 is C/R bit and SA10 is zero.

8.1.14 D_ch SAPI2 Register D_SAP2 Read/Write Address 34H

Value after reset: 00H

7	6	5	4	3	2	1	0
SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20

This register contains the second choice of the first byte address of received frame. For LAPD frame, SA27 - SA22 is the SAPI value, SA21 is C/R bit and SA20 is zero.

8.1.15 D_ch TEI Address Mask D_TAM Read/Write Address 38H

Value after reset: 00H

7	6	5	4	3	2	1	0
TAM7	TAM6	TAM5	TAM4	TAM3	TAM2	TAM1	TAM0

This register masks(disables) the second byte address comparison of the incoming frame. If the mask bit is "1" the corresponding bit comparisons with D_TEI1, D_TEI2 are disabled. Comparison with TEIG is always performed.

Note: For the LAPD frame, the least significant bit is the EA = 1 bit.

8.1.16 D_ch TEI1 Register D_TEI1 Read/Write Address 3CH

Value after reset: 00H

7	6	5	4	3	2	1	0
TA17	TA16	TA15	TA14	TA13	TA12	TA11	TA10

TA17 - TA10

This register contains the first choice of the second byte address of received frame. For LAPD frame, TA17 - TA11 is the TEI value, TA10 is EA = 1.

8.1.17 D_ch TEI2 Register D_TEI2 Read/Write Address 40H

Value after reset: 00H

7	6	5	4	3	2	1	0
TA27	TA26	TA25	TA24	TA23	TA22	TA21	TA20

TA27 - TA20

This register contains the second choice of the second byte address of received frame. For LAPD frame, TA27 - TA21 is the TEI value, TA20 is EA = 1.

8.1.18 D_ch Receive Frame Byte Count High D_RBCH Read Address 44H

Value after reset: 00H

7	6	5	4	3	2	1	0
VN1	VN0	LOV	RBC12	RBC11	RBC10	RBC9	RBC8

VN1-0 Chip Version Number

This is the chip version number. It is read as 00B.

LOV Length Overflow

A "1" in this bit indicates ≥ 4097 bytes are received and the frame is not yet complete. This bit is valid only after an D_RME interrupt and remains valid until the frame is acknowledge via the RACK command.

RBC12-8 Receive Byte Count

Four most significant bits of the total frame length. These bits are valid only after an D_RME interrupt and remain valid until the frame is acknowledge via the RACK command.

8.1.19 D_ch Receive Frame Byte Count Low D_RBCL Read Address 48H

Value after reset: 00H

7	6	5	4	3	2	1	0
RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0

RBC7-0 Receive Byte Count

Eight least significant bits of the total frame length. Bits RBC5-0 also indicate the length of the data currently available in D_RFIFO. These bits are valid only after an D_RME interrupt and remain valid until the frame is acknowledged via the RACK command.

8.1.20 Timer 2 TIMR2 Write Address 4CH

Value after reset: 00H

7	6	5	4	3	2	1	0
TMD	0	TCN5	TCN4	TCN3	TCN2	TCN1	TCN0

TMD Timer 2 Mode

0: One shot count down mode. The timer starts when it is written a non-zero count value and stops when it reaches zero.

1: Cyclic timer mode. The timer starts when it is written a non-zero count value and counts cyclically (periodically) with the count value.

In both cases, a maskable interrupt TIN2 is generated and TOUT2 pin toggles every time the timer reaches zero. When timer starts, TOUT2 changes to LOW and toggles at timer expiration. Therefore, the period of TOUT2 is twice of count value.

In both cases, timer counts with the new value if it is written again before expiration.

TCN5-0 Timer 2 Count Value

0: Timer is off.

1-31: Timer count value in unit of mS.

8.1.21 Layer 1_Ready Code L1_RC Read/Write Address 50H

Value after reset: 0CH

7	6	5	4	3	2	1	0
				RC3	RC2	RC1	RC0

RC3-0 Ready Code

When GCI bus is being enabled, these four programmable bits are allowed to program different Layer 1_Ready Code (AI: Activation Indication) by user. For example: Siemens PEB2091: AI = 1100, Motorola MC145572: AI = 1100.

8.1.22 D_ch Control Register D_CTL Read/Write Address 54H

Value after reset: 00H

7	6	5	4	3	2	1	0
WTT1	WTT2	SRST			TPS	OPS1	OPS0

WTT1, 2 Watchdog Timer Trigger 1, 2

When the watchdog timer has enabled (D_MODE: TEE = 1 and D_CTL: TPS = 1), the micro-processor has to program the WTT1, 2 bits in the following sequences within 1024 mS to reset and restart the timer. Otherwise, the timer will expire after 1024 mS and a WEXP interrupt together with a 125 µS reset pulse on TRST pin are generated:

SEQUENCE	WTT1	WTT2
1	1	0
2	0	1

Switching TPS bit from 0 to 1 or from 1 to 0 resets the watchdog timer.

SRST Software Reset

When this bit is set to "1", a software reset signal is activated. The effects of this reset signal are equivalent to the hardware reset pin , except that it does not reset the PCI interface circuit.

This bit is not auto-clear, the software must write "0" to this bit to exit from the reset mode.

Note: When SRST = 1, the chip is in reset state. Read or write to any of the registers is inhibited at this time. The SRST bit is write only.

TPS TRST Reset Pulse Select

This bit selects the source of reset pulse on TRST pin. It is valid only when the terminal equipment functions are enabled.

0: Exchange awake

A 16 mS reset pulse is generated when the a layer 1 indication code change has been detected.

1: Watchdog timer

A 125 μS reset pulse is generated as a result of the watchdog timer expiration.

Switching TPS bit from 0 to 1 or from 1 to 0 resets the watchdog timer.

OPS1-0 Output Phase Delay Compensation Select1-0

These two bits select the output phase delay compensation.

OPS1	OPS0	EFFECT
0	0	No output phase delay compensation
0	1	Output phase delay compensation 260 nS
1	0	Output phase delay compensation 520 nS
1	1	Output phase delay compensation 1040 nS

8.1.23 Command/Indication Receive Register CIR Read Address 58H

Value after reset: 0FH

7	6	5	4	3	2	1	0
SCC	ICC			CODR3	CODR2	CODR1	CODR0

SCC S Channel Change

A change in the received 4-bit S channel has been detected. The new code can be read from the SQR register. This bit is cleared by a read of the SQR register.

ICC Indication Code Change

A change in the received indication code has been detected. The new code can be read from the CIR register. This bit is cleared by a read of the CIR register.

CODR3-0 Layer 1 Indication Code

Value of the received layer 1 indication code.

Note: If S/T layer 1 function is disabled and GCI bus is enabled (GE bit = 1 in GCR register), CIR register is used to receive layer 1 indication code from U transceiver. In this case, SCC bit is not used and the supported indication codes are:

Indication	Symbol	Code	Descriptions
Deactivation confirmation	DC	1111	Idle code on GCI interface
Power up indication	PU	0111	U transceiver power up

8.1.24 Command/Indication Transmit Register CIX Write Address 5CH

Value after reset: 0FH

7	6	5	4	3	2	1	0
				CODX3	CODX2	CODX1	CODX0

CODX3-0 Layer 1 Command Code

Value of the command code transmitted from layer 2 to layer 1.

Note: If S/T layer 1 function is disabled and GCI bus is enabled (GE bit = 1 in GCR register), CIX register is used to issue layer 1 command code to U transceiver. In this case, the supported command code is:

Command	Symbol	Code	Descriptions
Activate request command	AR	1000	Activate request command

8.1.25 S/Q Channel Receive Register SQR Read Address 60H

Value after reset: XFH

7	6	5	4	3	2	1	0
XIND1	XIND0	MSYN	SCIE	S1	S2	S3	S4

XIND1 XINTIN1 Data

This bit reflects the current level of XINTIN1 pin.

XIND0 XINTIN0 Data

This bit reflects the current level of XINTIN0 pin.

MSYN Multiframe Synchronization

When this bit is "1", a multiframe synchronization is achived, i.e the the S/T receiver has synchronized to the received F_A and M bit patterns.

SCIE S Channel Change Interrupt Enable

This bit reflects the bit written in the SQX register.

S1-4 Received S Bits

These are the S bits received in NT to TE direction in frames 1, 6, 11 and 16. S1 is in frame 1, S2 is in frame 6 etc.

8.1.26 S/Q Channel Transmit RegisterSQX Write Address 64H

Value after reset: 0FH

7	6	5	4	3	2	1	0
			SCIE	Q1	Q2	Q3	Q4

SCIE S Channel Change Interrupt Enable

This bit is used to enable/disable the generation of CIR:SCC status bit and interrupt.

0: Status bit and interrupt are disabled.

1: Status bit and interrupt are enabled.

Q1-4 Transmitted Q Bits

These are the transmitted Q channels in F_A bit positions in frames 1, 6, 11 and 16. Q1 is in frame 1, Q2 is in frame 6 etc.

8.1.27 Peripheral Control Register PCTL Read/Write Address 68H

Value after reset: 00H

7	6	5	4	3	2	1	0
OE5	OE4	OE3	OE2	OE1	OE0	XMODE	PXC

OE5 Direction Control for IO10

Used when XMODE = 0 only.

0: Pin IO10 is input.

1: Pin IO10 is output.

OE4 Direction Control for IO9-8

Used when XMODE = 0 only.

0: Pin IO9-8 are inputs.

1: Pin IO9-8 are outputs.

OE3 Direction Control for IO7-6

Used when XMODE = 0 only.

0: Pin IO7-6 are inputs.

1: Pin IO7-6 are outputs.

OE2 Direction Control for IO5-4

Used when XMODE = 0 only.

0: Pin IO5-4 are inputs.

1: Pin IO5-4 are outputs.

OE1 Direction Control for IO3-2

Used when XMODE = 0 only.

0: Pin IO3-2 are inputs.

1: Pin IO3-2 are outputs.

OE0 Direction Control for IO1-0

Used when XMODE = 0 only.

0: Pin IO1-0 are inputs.

1: Pin IO1-0 are outputs.

XMODE Peripheral Bus Mode

0: Simple programmable IO. This is the default state. XADDR register and XDATA register are used for data access.

1: 8-bit multiplexed microprocessor bus. Pins IO7-0 are used as XAD7-0, IO8 as XALE, IO9 as XRDB and IO10 as XWRB. XADDR register is used for peripheral address generation and XDATA register is used for peripheral data access.

PXC PCM Cross-connect

This bit determines whether or not the PCM ports are cross-connected with the B channel ports. The setting of PXC is independent of the BSW1-0 bits.

PXC	CONNECTION
0	PCM1 ↔ B1, PCM2 ↔ B2
1	PCM1 ↔ B2, PCM2 ↔ B1

8.1.28 Monitor Receive Channel MOR Read Address 6CH

Value after reset: FFH

7	6	5	4	3	2	1	0

Contains the Monitor channel data received in GCI Monitor channel according to the Monitor channel protocol.

8.1.29 Monitor Transmit Channel MOX Read/Write Address 70H

Value after reset: FFH

7	6	5	4	3	2	1	0

Contains the Monitor channel data transmitted in GCI Monitor channel according to the Monitor channel protocol.

8.1.30 Monitor Channel Status Register MOSR Read_clear Address 74H

Value after reset: 00H

7	6	5	4	3	2	1	0
				MDR	**MER**	**MDA**	**MAB**

MDR Monitor channel Data Receive

MER Monitor channel End of Reception

MDA Monitor channel Data Acknowledged

The remote end has acknowledged the Monitor byte being transmitted.

MAB Monitor channel Data Abort

8.1.31 Monitor Channel Control Register MOCR Read/Write Address 78H

Value after reset: 00H

7	6	5	4	3	2	1	0
				MRIE	**MRC**	**MXIE**	**MXC**

MRIE Monitor channel Receive Interrupt Enable

Monitor channel interrupt status MDR, MER generation is enabled (1) or masked (0).

MRC MR Bit Control

Determines the value of the MR bit:

0: MR bit always 1. In addition, the MDR interrupt is blocked, except for the first byte of a packet (if MRE = 1).

1: MR internally controlled by the W6692 according to Monitor channel protocol. In addition, the MDR interrupt is enabled for all received bytes according to the Monitor channel protocol (if MRE = 1).

MXIE Monitor channel Transmit Interrupt Enable

Monitor interrupt status MDA, MAB generation is enabled (1) or masked (0).

MXC MX bit Control

Determines the value of the MX bit:

0: MX always 1.

1: MX internally controlled by the W6692 according to Monitor channel protocol.

8.1.32 GCI Mode Control Register GCR Read/Write Address 7CH

Value after reset: 00H

7	6	5	4	3	2	1	0
MAC			TLP	GRLP	SPU	PD	GE

MAC Monitor Transmit Channel Active (Read Only)

Data transmission is in progress in GCI mode Monitor channel.

0: the previous transmission has been terminated. Before starting a transmission, the microprocessor should verify that the transmitter is inactive.

1: after having written data into the Monitor Transmit Channel (MOX) register, the microprocessor sets this bit to 1.

This enables the MX bit to go active (0), indicating the presence of valid Monitor channel data (contents of MOX) in the correspond frame.

TLP Test Loop

When set this bit to 1 both the DOUT and DIN lines are internally connected together, and the constants T1 and T2 in D_TIMR are reduced. The GCI mode loop-back test function: DOUT is internally connected with DIN, external input on DIN is ignored.

When TLP = 1 (GCI mode Test Loop-back Active):

T2 = 16348 ∗ CNT ∗ DCL +T1, with T1 = 512 ∗ (VAL + 1) ∗ DCL (here: DCL denotes the period of the DCL clock.)

GRLP GCI Mode Remote Loop-back

Setting this bit to 1 activates the remote loop-back function. The 2B+D channels data received from the GCI bus interface are looped to the transmitted channels.

SPU Software Power Up

PD Power Down

SPU	PD	DESCRIPTION
0	1	After U transceiver power down, W6692 will receive the indication DC (Deactivation Confirmation) from GCI bus and then software has to set SPU → 0, PD →1 to enter Power Down state.
1	0	Setting SPU → 1, PD →0 will pull the GCI bus DOUT line to low. This will enforce connected layer 1 devices (U transceiver) to deliver GCI bus clocking.
0	0	After reception of the indication PU (Power Up indication) the reaction of the microprocessor should be: - to write an AR (Activate Request command) as C/I command code in the CIX register. - to reset the SPU bit and wait for the following ICC (indication code change) interrupt.
1	1	unused.

GE GCI Mode Enable

Setting this bit to 1 will enable the GCI bus interface. In the same time, the S/T layer 1 function is disabled.

8.1.33 Peripheral Address Register XADDR Read/Write Address F4H

Value after reset : Undefined

The register content depends on PCTL: XMODE setting.

XMODE = 0: Simple IO mode

7	6	5	4	3	2	1	0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

IO1-0 Read or Write Data of Pins IO1-0

Input data of pins IO1-0 if PCTL: OE0 = 0.

Output data of pins IO1-0 if PCTL: OE0 = 1.

IO3-2 Read or Write Data of Pins IO3-2

Input data of pins IO3-2 if PCTL: OE1 = 0.

Output data of pins IO3-2 if PCTL: OE1 = 1.

IO5-4 Read or Write Data of Pins IO5-4

Input data of pins IO5-4 if PCTL: OE2 = 0.

Output data of pins IO5-4 if PCTL: OE2 = 1.

IO7-6 Read or Write Data of Pins IO3-0

Input data of pins IO7-6 if PCTL: OE3 = 0.

Output data of pins IO7-6 if PCTL: OE3 = 1.

XMODE = 1: 8-bit multiplexed microprocessor mode

7	6	5	4	3	2	1	0
XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0

XA7-0 Peripheral Address

To access peripheral device, first write the peripheral address in this register and then perform read or write at XDATA register. The address written in this register is output on XAD7-0 in address phase of data access and can be latched by XALE signal.

8.1.34 Peripheral Data Register XDATA Read/Write Address F8H

Value after reset: Undefined

The register content depends on PCTL: XMODE setting.

XMODE = 0: Simple IO mode

7	6	5	4	3	2	1	0
					IO10	IO9	IO8

IO9-8 Read or Write Data of Pins IO9-8

Input data of pins IO9-8 if PCTL: OE4 = 0.

Output data of pins IO9-8 if PCTL: OE4 = 1.

IO10 Read or Write Data of Pins IO10

Input data of pins IO10 if PCTL: OE5 = 0.

Output data of pins IO10 if PCTL: OE5 = 1.

XMODE = 1: 8-bit multiplexed microprocessor mode

7	6	5	4	3	2	1	0
XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

XD7-0 Peripheral Data

During data phase of peripheral access, they are outputs to XAD7-0 if write, or inputs from XAD7-0 if read.

8.1.35 Serial EEPROM Control Register EPCTL Write Address 68H

Value after reset: X0H

7	6	5	4	3	2	1	0
				EN	SK	CS	SDO

EN Enable Output

0: Disable outputs on pins EPSK, EPCS, EPSDO.

1: Enable outputs on pins EPSK, EPCS, EPSDO.

SK Output Data of EPSK

When enabled, this bit is output on pin EPSK.

CS Output Data of EPCS

When enabled, this bit is output on pin EPCS.

SDO Output Data of EPSDO

When enabled, this bit is output on pin EPSDO.

8.2 B1 HDLC controler

Table 8.3 Register address map: B1 channel HDLC

SECTION	OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
8.2.1	80	R	B1_RFIFO	B1 channel receive FIFO
8.2.2	84	W	B1_XFIFO	B1 channel transmit FIFO
8.2.3	88	W	B1_CMDR	B1 channel command register
8.2.4	8C	R/W	B1_MODE	B1 channel mode control
8.2.5	90	R_clear	B1_EXIR	B1 channel extended interrupt
8.2.6	94	R/W	B1_EXIM	B1 channel extended interrupt mask
8.2.7	98	R	B1_STAR	B1 channel status register
8.2.8	9C	R/W	B1_ADM1	B1 channel address mask 1
8.2.9	A0	R/W	B1_ADM2	B1 channel address mask 2
8.2.10	A4	R/W	B1_ADR1	B1 channel address 1
8.2.11	A8	R/W	B1_ADR2	B1 channel address 2
8.2.12	AC	R	B1_RBCL	B1 channel receive frame byte count low
8.2.13	B0	R	B1_RBCH	B1 channel receive frame byte count high

Table 8.4 Register summary: B1 channel HDLC

OFFSET	R/W	NAME	7	6	5	4	3	2	1	0
80	R	B1_RFIFO								
84	W	B1_XFIFO								
88	W	B1_CMDR	RACK	RRST	RACT			XMS	XME	XRST
8C	R/W	B1_MODE	MMS	ITF	EPCM	BSW1	BSW0	SW56	FTS1	FTS0
90	R_clr	B1_EXIR		RMR	RME	RDOV			XFR	XDUN
94	R/W	B1_EXIM		RMR	RME	RDOV			XFR	XDUN
98	R	B1_STAR		RDOV	CRCE	RMB		XDOW		XBZ
9C	R/W	B1_ADM1	MA17	MA16	MA15	MA14	MA13	MA12	MA11	MA10
A0	R/W	B1_ADM2	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20
A4	R/W	B1_ADR1	RA17	RA16	RA15	RA14	RA13	RA12	RA11	RA10
A8	R/W	B1_ADR2	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
AC	R	B1_RBCL	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
B0	R	B1_RBCH			LOV	RBC12	RBC11	RBC10	RBC9	RBC8

8.2.1 B1_ch receive FIFO B1_RFIFO Read Address 80H

The B1_RFIFO is a 128-byte depth FIFO memory with programmable threshold. The threshold value determines when to generate an interrupt.

When more than a threshold length of data has been received, a RMR interrupt is generated. After an RMR interrupt, 64 or 96 bytes can be read out, depending on the threshold setting.

In transparent mode, when the end of frame has been received, a RME interrupt is generated. After an RME interrupt, the number of bytes available is less than or equal to the threshold value.

8.2.2 B1_ch transmit FIFO B1_XFIFO Write Address 84H

The B1_XFIFO is a 128-byte depth FIFO with programmable threshold value. The threshold setting is the same as B1_RFIFO.

When the number of empty locations is equal to or greater than the threshold value, a XFR interrupt is generated. After a XFR interrupt, up to 64 or 96 bytes of data can be written into this FIFO for transmission.

8.2.3 B1_ch command register B1_CMDR Write Address 88H

Value after reset: 00H

7	6	5	4	3	2	1	0
RACK	RRST	RACT			XMS	XME	XRST

RACK Receive Message Acknowledge

After a RMR or RME interrupt, the micro-processor reads out the data in B1_RFIFO, it then sets this bit to explicitly acknowledge the interrupt.

RRST Receiver Reset

Setting this bit resets the B1_ch HDLC receiver.

RACT Receiver Active

The B1_ch HDLC receiver is active when this bit is set to "1". This bit is write only. The receiver must be in active state in order to receive data.

XMS Transmit Message Start/Continue

In transparent mode, setting this bit initiates the transparent transmission of B1_XFIFO data. The opening flag is automatically added to the message by the B1_ch HDLC controller. Zero bit insertion is performed on the data. This bit is also used in subsequent transmission of the frame.

In extended transparent mode, settint this bit activates the transmission of B1_XFIFO data. No flag, CRC or zero bit insertion is added on the data.

XME Transmit Message End

In transparent mode, setting this bit indicates the end of the whole frame transmission. The B1_ch HDLC controller transmits the data in FIFO and automatically appends the CRC and the closing flag sequence in transparent mode.

In extended transparent mode, setting this bit stops the B1_XFIFO data transmission.

XRST Transmitter Reset

Setting this bit resets the B1_ch HDLC transmitter and clears the B1_XFIFO. The transmitter will send inter frame time fill pattern on B channel. This command also results in a transmit FIFO ready condition.

8.2.4 B1_ch Mode Register B1_MODE Read/Write Address 8CH

Value after reset: 00H

7	6	5	4	3	2	1	0
MMS	ITF	EPCM	BSW1	BSW0	SW56	FTS1	FTS0

MMS Message Mode Setting

Determines the message transfer modes of the B1_ch HDLC controller:

0: Transparent mode. In receive direction, address comparison is performed on each frame. The frames with matched address are stored in B1_RFIFO. Flag deletion, CRC check and zero bit deletion are performed. In transmit direction, the data is transmitted with flag insertion, zero bit insertion and CRC generation.

1: Extended transparent mode. In receive direction, all data are received and stored in the B1_RFIFO. In transmit direction, all data in the B1_XFIFO are transmitted without alteration.

ITF Inter-frame Time Fill

Defines the inter-frame time fill pattern in transparent mode.

0: Mark. The binary value "1" is transmitted.

1: Flag. This is a sequence of "01111110".

EPCM Enable PCM Transmit/Receive

0: Disable data transmit/ receive to/from PCM port. The frame synchronization clock PFCK1 is held LOW.

1: Enable data transmit/ receive to/from PCM port. The frame synchronization clock PFCK1 is active.

BSW1-0 B Channel Switching Select

These two bits determine the connection in B1 channel:

BSW1	BSW0	CONNECTION
0	0	layer 1 ↔HDLC
0	1	layer 1 ↔ PCM
1	0	HDLC ↔ PCM
1	1	layer 1 → PCM, PCM → HDLC

Note: The connection with micro-controller is through HDLC controller. When HDLC connects with layer 1, either transparent or extended transparent mode can be used. When HDLC connects with PCM port, only extended transparent mode can be used and the EPCM bit must be set to enable PCM function.

SW56 Switch 56 Traffic

0: The data rate in B1 channel is 64 kbps.

1: The data rate in B1 channel is 56 kbps. The most significant bit in each octet is fixed at "1".

Note: In 56 kbps mode, only transparent mode can be used.

FTS1-0 FIFO Threshold Select

These two bits determine the B1 channel receive and transmit FIFO's threshold setting. An interrupt is generated when the number of received data or the number of vacancies in XFIFO reaches the threshold value.

FTS1	FTS0	THRESHOLD (BYTE)
0	0	64
0	1	Reserved
1	0	96
1	1	Not allowed

8.2.5 B1_ch Extended Interrupt Register B1_EXIR Read_clear Address 90H

Value after reset: 00 H

7	6	5	4	3	2	1	0
	RMR	RME	RDOV			XFR	XDUN

RMR Receive Message Ready

At least a threshold lenth of data has been stored in the B1_RFIFO.

RME Receive Message End

Used in transparent mode only. The last block of a frame has been received. The frame length can be found in B1_RBCH + B1_RBCL registers. The number of data available in the B1_RFIFO equals frame lenth modulus threshold. The result of CRC check is indicated by B1_STAR:CRCE bit.

When the number of last block of a frame equals the threshold, only RME interrupt is generated.

RDOV Receive Data Overflow

Data overflow occurs in the receive FIFO. The incoming data will overwrite the data in the receive FIFO.

XFR Transmit FIFO Ready

This interrupt indicates that up to a threshold length of data can be written into the B1_XFIFO.

XDUN Transmit Data Underrun

This interrupt occurs when the B1_XFIFO has run out of data. In this case, the W6692 will automatically reset the transmitter and send the inter frame time fill pattern on B channel. The software must wait until transmit FIFO ready condition (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

8.2.6 B1_ch Extended Interrupt Mask Register B1_EXIM Read/Write Address 94H

Value after reset: FFH

7	6	5	4	3	2	1	0
	RMR	RME	RDOV			XFR	XDUN

Setting the bit to "1" masks the corresponding interrupt source in B1_EXIR register. Masked interrupt status bits are read as zero when B1_EXIR register is read. They are internally stored and pending until the mask bits are zero.

All the interrupts in B1_EXIR will be masked if the IMASK: B1_EXI bit is set to "1".

8.2.7 B1_ch Status Register B1_STAR Read Address 98H

Value after reset: 20H

7	6	5	4	3	2	1	0
	RDOV	CRCE	RMB		XDOW		XBZ

RDOV Receive Data Overflow

A "1" indicates that the D_RFIFO is overflow. The incoming data will overwrite data in the receive FIFO. The overflow condition will set both the status and interrupt bits. It is recommended that software must read the RDOV bit after reading data from D_RFIFO at RMR or RME interrupt. The software must abort the data and issue a RRST command to reset the receiver if RDOV = 1.

CRCE CRC Error

Used in transparent mode only. This bit indicates the result of frame CRC check:

0: CRC correct

1: CRC incorrect

RMB Receive Message Aborted

Used in transparent mode only. A "1" means that a sequence of ≥seven 1's was received and the frame is aborted by the B1_HDLC receiver. Software must issue RRST command to reset the receiver.

Note: Bits CRCE and RMB are valid only after a RME interrupt and remain valid until the frame is acknowledged via RACK command

XDOW Transmit Data Overwritten

At least one byte of data has been overwritten in the B1_XFIFO. This bit is cleared only by XRST command.

XBZ Transmitter Busy

The B1_HDLC transmitter is busy when XBZ is read as "1". This bit may be polled. The XBZ bit is active when an XMS command was issued and the message has not been completely transmitted.

8.2.8 B1_ch Address Mask Register 1 B1_ADM1 Read/Write Address 9CH

Value after reset : 00H

7	6	5	4	3	2	1	0
MA17	MA16	MA15	MA14	MA13	MA12	MA11	MA10

MA17-10 Address Mask Bits

Used in transparent mode only. These bits mask the first byte address comparisons. If the mask bit is "1", the corresponding bit comparison with B1_ADR1 is disabled.

0: Unmask comparison

1: Mask comparison

8.2.9 B1_ch Address Mask Register 2 B1_ADM2 Read/Write Address A0H

Value after reset: 00H

7	6	5	4	3	2	1	0
MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20

MA27-20 Address Mask Bits

Used in transparent mode only. These bits mask the second byte address comparisons. If the mask bit is "1", the corresponding bit comparison with B1_ADR2 is disabled.

0: Unmask comparison

1: Mask comparison

8.2.10 B1_ch Address Register 1 B1_ADR1 Read/Write Address A4H

Value after reset: 00H

7	6	5	4	3	2	1	0
RA17	RA16	RA15	RA14	RA13	RA12	RA11	RA10

RA17-10 Address Bits

Used in transparent mode only. These bits are used for the first byte address comparisons.

8.2.11 B1_ch Address Register 2 B1_ADR2 Read/Write Address A8H

Value after reset: 00H

7	6	5	4	3	2	1	0
RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20

RA27-20 Address Bits

Used in transparent mode only. These bits are used for the second byte address comparisons.

8.2.12 B1_ch Receive Frame Byte Count Low B1_RBCL Read Address ACH

Value after reset: 00H

7	6	5	4	3	2	1	0
RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0

RBC7-0 Receive Byte Count

Used in transparent mode only. Eight least significant bits of the total number of bytes in a received frame. These bits are valid only after a RME interrupt and remain valid until the frame is acknowledge via the RACK bit.

8.2.13 B1_ch Receive Frame Byte Count High B1_RBCH Read Address B0H

Value after reset: 00H

7	6	5	4	3	2	1	0
		LOV	RBC12	RBC11	RBC10	RBC9	RBC8

LOV Message Length Overflow

Used in transparent mode only. A "1" in this bit indicates a received message ≥ 4097 bytes. This bit is valid only after RME interrupt and is cleared by the RACK command.

RBC12-8 Receive Byte Count

Used in transparent mode only. Five most significant bits of the total number of bytes in a received frame. These bits are valid only after a RME interrupt and remain valid until the frame is acknowledge via the RACK bit.

Note: The frame length equals RBC12-0. This length is between 1 to 4096. After a RME interrupt, the number of data available in B1_RFIFO is frame length modulus threshold.

Remainder = RBC12-0 MOD threshold

no. of available data = remainder if remainder ≠ 0 or

no. of available data = threshold if remainder = 0

The remainder equals RBC5-0 if threshold is 64.

8.3 B2 HDLC controller

Table 8.5 Register address map: B2 channel HDLC

OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
C0	R	B2_RFIFO	B2 channel receive FIFO
C4	W	B2_XFIFO	B2 channel transmit FIFO
C8	W	B2_CMDR	B2 channel command register
CC	R/W	B2_MODE	B2 channel mode control
D0	R_clear	B2_EXIR	B2 channel extended interrupt
D4	R/W	B2_EXIM	B2 channel extended interrupt mask
D8	R	B2_STAR	B2 channel status register
DC	R/W	B2_ADM1	B2 channel address mask 1
E0	R/W	B2_ADM2	B2 channel address mask 2
E4	R/W	B2_ADR1	B2 channel address 1
E8	R/W	B2_ADR2	B2 channel address 2
EC	R	B2_RBCL	B2 channel receive frame byte count low
F0	R	B2_RBCH	B2 channel receive frame byte count high

Table 8.6 Register summary: B2 channel HDLC

OFFSET	R/W	NAME	7	6	5	4	3	2	1	0
C0	R	B2_RFIFO								
C4	W	B2_XFIFO								
C8	W	B2_CMDR	RACK	RRST	RACT			XMS	XME	XRST
CC	R/W	B2_MODE	MMS	ITF	EPCM	BSW1	BSW0	SW56	FTS1	FTS0
D0	R_clr	B2_EXIR		RMR	RME	RDOV			XFR	XDUN
D4	R/W	B2_EXIM		RMR	RME	RDOV			XFR	XDUN
D8	R	B2_STAR		RDOV	CRCE	RMB		XDOW		XBZ
DC	R/W	B2_ADM1	MA17	MA16	MA15	MA14	MA13	MA12	MA11	MA10
E0	R/W	B2_ADM2	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20
E4	R/W	B2_ADR1	RA17	RA16	RA15	RA14	RA13	RA12	RA11	RA10
E8	R/W	B2_ADR2	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
EC	R	B2_RBCL	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
F0	R	B2_RBCH			LOV	RBC12	RBC11	RBC10	RBC9	RBC8

The B2 channel HDLC register's definitions and functions are the same as those of B1 channel HDLC. Please refer to section 8.2 for a detailed description.

8.4 PCI Configuration Register

W6692 provides PCI interface for PCI-base system and only supports slave mode. There are two optional Base Address Registers (Memory or I/O) for host access to W6692 internal registers.

Reads to reserved or unimplemented registers return data value of 0. Write to these registers are completed normally and the data are discarded.

After power on reset, W6692 automatically reads the configuration data from serial EEPROM interface. The first word read is Vendor ID. If Vendor ID = $FFFF_H$, W6692 assumes EEPROM is empty and will use built-in default configuration data., otherwise, configuration data from EEPROM is used. Please refer to Section 7.9.1 for serial EEPROM data format.

Table 8.7 PCI Configuration Space

ADDRESS\BIT	31 24	23 16	15 8	7 0
00_H	Device ID		Vendor ID	
04_H	Status		Command	
08_H	Class Code			Revision ID
$0C_H$	--	Header Type	--	
10_H	Base Address Register 0			
14_H	Base Address Register 1			
18_H - 28_H	Not implemented. Read as 0.			
$2C_H$	Subsystem ID		Subsystem Vendor ID	
30_H - 38_H	Not implemented. Read as 0.			
$3C_H$	--	--	Interrupt Pin	Interrupt Line

8.4.1 Device/Vendor ID Register Read Address 00_H

PCI Configuration Address: 00_H

Default: 6692 1050_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device ID															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 31-16 Device ID

Device ID is loaded from EEPROM after power on reset, if EEPROM is not empty.

Device ID is Winbond's device ID: 6692_H, if EEPROM is empty.

Bits 15-0 Vendor ID

Vendor ID is allocated by the PCI SIG to ensure uniqueness. The value is loaded from EEPROM after power on reset , if EEPROM is not empty.

Vendor ID is Winbond's vendor ID: 1050_H , if EEPROM is empty.

8.4.2 Status/Command Register Read/Write Address 04_H

PCI Configuration Address: 04_H

Default: 0200 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPE	--	--	--	STA	DEVSEL		--	FBT	UDF	66M	--				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
--						--	--	--	PEE	--				MAE	IOAE

Bits 31-16 are Status register and bits 15-0 are Command register. Reads to Status register behave normally. Bits in Status register are cleared if the corresponding write data bits are '1' in a write operation.

Bits 15-0 are Command register. When 00_H is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. The power up value of Command register is 00_H.

Bit 31 DPE Detected Parity Error R/W_clr

1 = A parity error is detected.

0 = No parity error is detected.

Bit 30 SSE Signaled System Error

Not implemented. Read as 0.

Bits 29-28 Master Aborted, Target Aborted

Not implemented. Read as 0.

Bit 27 STA Signaled Target Abort R/W_clr

1 = Target Abort is signalled.

0 = Target Abort is not signalled.

Bits 26-25 DEVSEL Timing Read_only

01 = Medium DEVSEL# timing.

Bits 24 PERR# Asserted

Not implemented. Read as 0.

Bit 23 FBT Fast Back-to-back Transaction Read_only

0 = Unable to accept fast back-to-back transaction.

Bit 22 UDF User Definable Features Read_only

0 = Unable to support User Definable Features.

Bit 21 66M 66 MHz Function Read_only

0 = Support 33 MHz only.

Bits 20-16 Reserved Read as 0

Bits 15-10 Reserved Read as 0

Bits 9 Fast Back-to-back

Not implemented. Read as 0.

Bit 8 SEE SERR# Driver Enable

Not implemented. Read as 0.

Bits 7 Address/data Stepping

Not implemented. Read as 0

Bit 6 PEE Parity Error Response Enable R/W

1 = Enable parity error response
0 = Disable parity error response

Bits 5-2 VGA Palette, Memory Write and Invalidate, Special Cycle

Not implemented. Read as 0.

Bit 1 MAE Memory Access Enable R/W

1 = Enable memory access response

0 = Disable memory access response

Bit 0 IOAE I/O Access Enable R/W

1 = Enable I/O access response

0 = Disable I/O access response

8.4.3 Class Code/Revision ID Register Read Address 08_H

PCI Configuration Address: 08_H

Default: 0280 0000 $_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Base Class Code									Sub-Class Code						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Programming Interface									Revision ID						

Bits 31-8 Class Code Read_only

This value is loaded from EEPROM after power on reset, if EEPROM is not empty.

The default value is 028000 $_H$ to specify that the W6692 is an ISDN network communication device, if EEPROM is empty.

Bits 7-0 Revision ID Read_only

This value is assigned by the ISDN system manufacturer and identifies the revision number of the system.

This value is loaded from EEPROM after power on reset, if EEPROM is not empty.

The default value is 00 $_{H,}$ if EEPROM is empty.

8.4.4 Header Type/Latency Timer Register Read Address $0C_H$

PCI Configuration Address: $0C_H$

Default: 0000 0000 $_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIST									Header Type						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Latency Timer									Cache Line Size						

Bits 31-24 BIST Built-in Self Test Read_only

This register is always read as 0. It means that W6692 does not support BIST function.

Bits 23-16 Header Type Read_only

The value of this register is 00_H. This means a signle function device, with header type 00_H.

Bits 15-8 Latency Timer Read_only

This register is not implemented and is read as 0.

Bits 7-0 Cache Line Size Read_only

This register is not implemented and is read as 0.

8.4.5 Base Address Register 0 Read/Write Address 10_H

Depending on EEPROM status and MEN, IEN bits in EEPROM, there are different implementations:

MEN	IEN	LOCATION 10H	LOCATION 14H	PRE USED
1	1	Memory Base Address Reg.	IO Base Address Reg.	Yes
1	0	Memory Base Address Reg.	Not Implemented	Yes
0	1	IO Base Address Reg.	Not Implemented	No
0	0	Not Implemented	Not Implemented	No
EEPROM empty		Memory Base Address Reg.	IO Base Address Reg.	PRE = 1

If EEPROM is empty, the power on reset value at 10_H = 0000 0008$_H$, and the power on reset value at 14_H = 0000 0001$_H$

Memory Base Adress Register:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Memory Base Address															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Base Address				Hardwired to 0								PRE	Type		0

This register can be used to relocate memory address space to any location that is aligned to 4K bytes for mapping W6692's internal registers.

Bits 31-12 Memory Base Address R/W

These bits are read/write and are used to relocate the memory address space at 4K byte boundary.

Bits 11-4 Read_only

These bits are read_only and are hardwired to 0.

Bit 3 Prefetchable Read_only

This bit is hardwred to 1, if EEPROM is empty, otherwise, it is loaded from EEPROM.

Bits 2-1 Type Read_only

These two bits are hardwired to 00, indicating the memory range can locate anywhere in 32 bit address space.

Bit 0 Memory Space Indicator Read_only

This bit is hardwired to 0, indicating a memory space is allocated.

IO Base Address Register:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I/O Base Address															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Base Address								Hardwired to 0						0	1

This register can be used to relocate I/O address space to any location that is aligned to 256 bytes for mapping W6692's internal registers.

Bits 31-8 IO Base Address R/W

These bits are read/write and are used to relocate the IO address space at 256 byte boundary.

Bits 7-2 Read_only

These bits are read_only and are hardwired to 0.

Bit 1 Reserved Read_only

This bit is reserved and is hardwired to 0.

Bit 0 IO Space Indicator Read_only

This bit is hardwired to 1, indicating a I/O space is allocated.

8.4.6 Base Address Register 1 Read/Write Address 14_H

See the above section.

8.4.7 Subsystem/Subsystem Vendor ID Register Read Address $2C_H$

PCI Configuration Address: $2C_H$

Default: FFFF FFFF $_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Subsystem ID															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Subsystem Vendor ID															

Bits 31-16 Subsystem ID Read_only

Subsystem ID is loaded from EEPROM after power on reset, if EEPROM is not empty.

The default value is FFFF $_H$, if EEPROM is empty.

Bits 15-0 Subsystem Vendor ID Read_only

Subsystem Vendor ID is assigned by the manufacturer to ensure uniqueness. The value is loaded from EEPROM after power on reset, if EEPROM is not empty.

The default value is FFFF $_H$, if EEPROM is empty.

8.4.8 Interrupt Line Register Read/Write Address $3C_H$

PCI Configuration Address: $3C_H$

Default: 0000 0100 $_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Max_Latency Timer								Min_GNT Timer							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt Pin								Interrupt Line							

Bits 31-24 Max_Latency Timer Read_only

This register is hardwired to 0, indicating no major requirements for the settings of Latency Timers.

Bits 23-16 Min_GNT Timer Read_only

This register is hardwired to 0.

Bits 15-8 Interrupt Pin Read_only

This register is hardwired to 01_H to specify that INTA# is the interrupt pin used.

Bits 7-0 Interrupt Line R/W

This 8-bit register is used to communicate interrupt line routing information. Power On Self Test (POST) software must write the routing information into this register as it initializes and configures the system.

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Rating

PARAMETER	SYMBOL	LIMIT VALUES	UNIT
Voltage on Any Pin with Respect to Ground	V_S	-0.4 to V_{DD} +0.4	V
Ambient Temperature Under Bias	T_A	0 to 70	°C
Maximum Voltage on V_{DD}	V_{DD}	6	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 Power Supply

The power supply is 5V ±5%.

9.3 DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5V ±5%, V_{SSA} = 0V, V_{SSD} = 0V

PARAMETER	SYM.	MIN.	MAX.	UNIT	TEST CONDITIONS	REMARKS
Low Input Voltage	VIL	-0.4	0.8	V		
High Input Voltage	VIH	2.0	VDD +0.4	V		
Low Output Voltage	VOL		0.4	V	IOL = 12 mA	
High Output Voltage	VOH	2.4		V		
Power Supply Current: Power Down	ICC		4.0	mA	VDD = 5V, Inputs at VDD/VSS, No output loads except at SX1, 2 (50 Ω load)	
Power Supply Current: Operational	ICC		17	mA	VDD = 5V, Inputs at VDD/VSS, No output loads except at SX1, 2 (50 Ω load)	
Input Leakage Current	ILI		10	µA	0V < VIN < VDD to 0V	All pins except SX1, 2, SR1, 2
Output Leakage Current	ILO		10	µA	0 V < VOUT < VDD to 0V	All pins except SX1, 2, SR1, 2
Absolute Value of Output Pulse Amplitude (V_{SX2}-V_{SX1})	VX	2.03 2.10	2.31 2.39	V V	RL = 50 Ω [1)] RL = 400 Ω [1)]	SX1, 2
Transmitter Output Current	IX	7.5	13.4	mA	RL = 5.6 Ω [1)]	SX1, 2
Transmitter Output Impedence	RX	30 23		KΩ Ω	Inactive or during binary ONE During binary ZERO (RL = 50 Ω)	SX1, 2

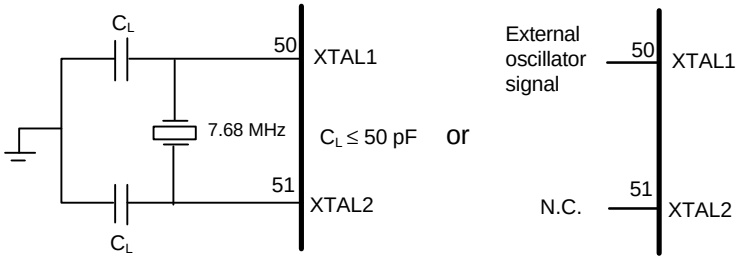
Note: [1)] Due to the transformer, the load resistance seen by the circuit is four times RL.

Capacitances

T_A = 25 °C, V_{DD} = 5V ±5%, V_{SSA} = 0V, V_{SSD} = 0V, fc = 1 MHz, unmeasured pins grounded.

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARKS
Input Capacitance	C_{IN}		7	pF	All pins except SR1, 2
I/O Pin Capacitance	C_{IO}		7	pF	All pins except SR1, 2
Output Capacitance Against V_{SSA}	C_{OUT}		10	pF	SX1, 2
Input Capacitance	C_{IN}		7	pF	SR1, 2
Load Capacitance	C_L		50	pF	XTAL1, 2

Recommended oscillator circuits



Crystal specifications

PARAMETER	SYMBOL	VALUES	UNIT
Frequency	f	7.680	MHz
Frequency Calibration Tolerance		Max. 100	ppm
Load Capacitance	C_L	Max. 50	pF
Oscillator Mode		Fundamental	

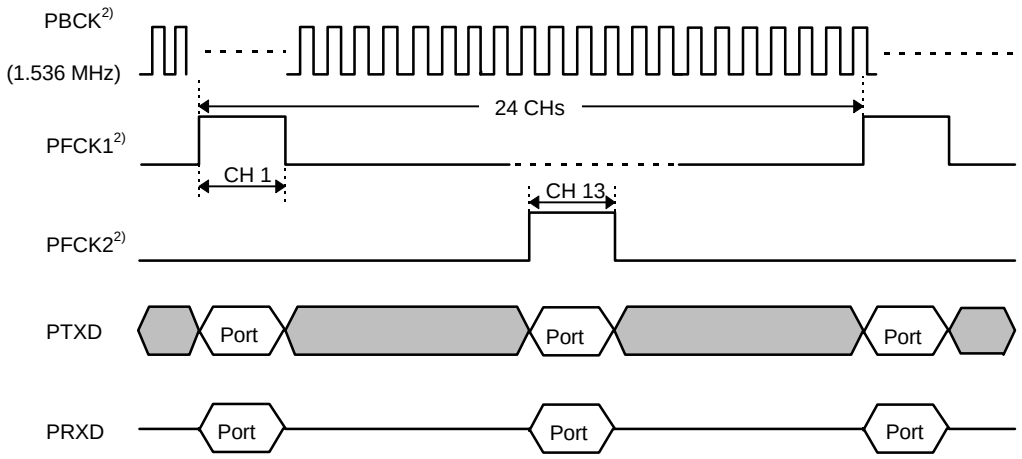
Note: The load capacitance C_L depends on the crystal specification. The typical values are 33 to 47 pF.

External ocsillator input (XTAL1) clock characteristics

PARAMETER	MIN.	MAX.
Duty cycle	1:2	2:1

9.4 Preliminary Switching Characteristics

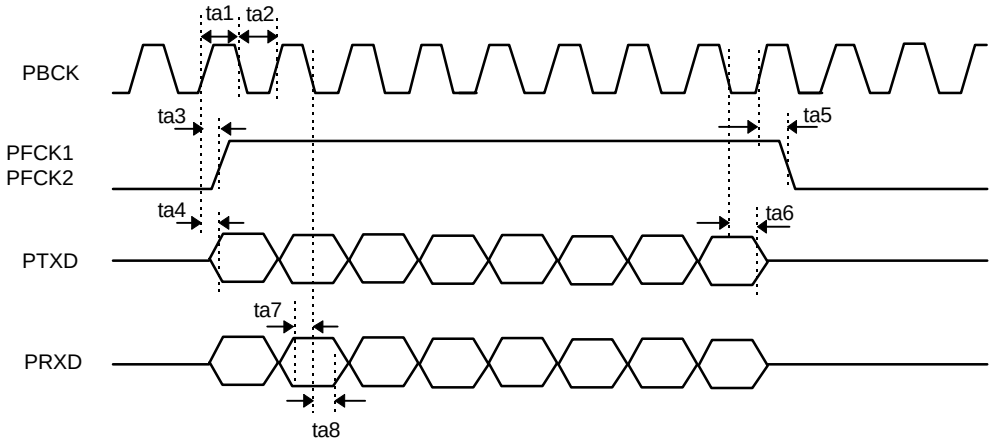
9.4.1 PCM Interface Timing



Notes:

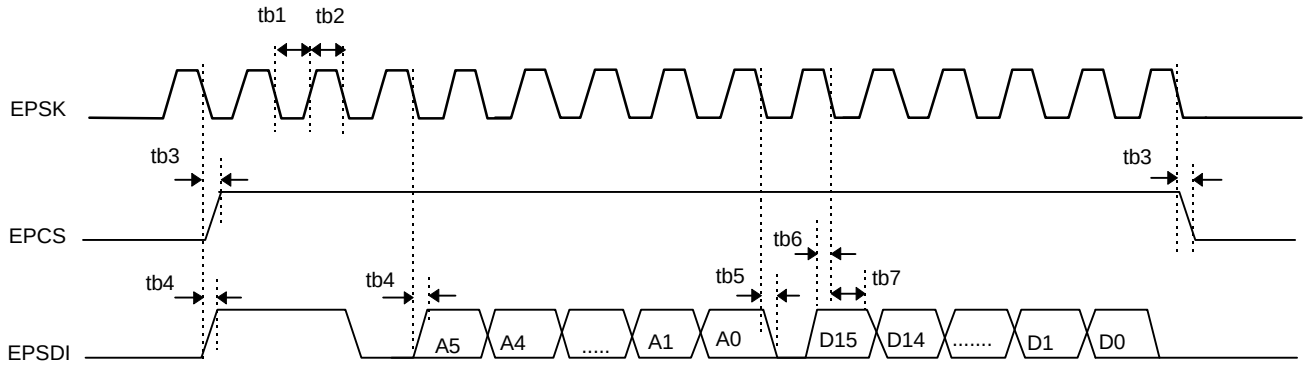
1. These drawings are not to scale.
2: The frequency of PBCK is 1536 KHz which includes 24 channels of 64 kbps data. The PFCK1 and PFCK2 are located at channel 1 and channel 13, each with a 8 x PBCK duration.

Detailed PCM timing



PARAMETER	PARAMETER DESCRIPTIONS	MIN.	MAX.	REMARKS
ta1	PBCK pulse high	260		Unit = nS
ta2	PBCK pulse low	260		
ta3	Frame clock asserted from PBCK		20	
ta4	PTXD data delay from PBCK		20	
ta5	Frame clock deasserted from PBCK		20	
ta6	PTXD hold time from PBCK	10		
ta7	PRXD setup time to PBCK	20		
ta8	PRXD hold time from PBCK	10		

9.4.2 Serial EEPROM Timing

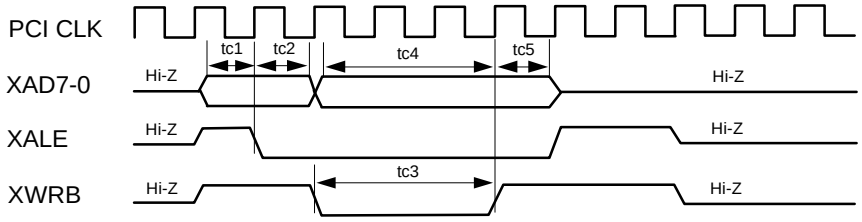


PARAMETER	PARAMETER DESCRIPTIONS	MIN.	MAX.	REMARKS
tb1	EPSK low	2500		Unit = nS
tb2	EPSK high	2500		
tb3	EPCS output delay		30	
tb4	EPSD output delay		30	
tb5	EPSD tri-state delay		30	
tb6	EPSD input setup time	30		
tb7	EPSD input hold time	30		

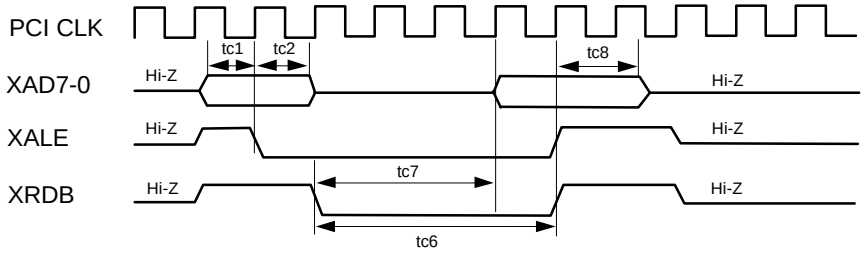
9.4.3 Peripheral Interface Timing

8-bit microprocessor timing when XMODE = 1:

Peripheral Write



Peripheral Read

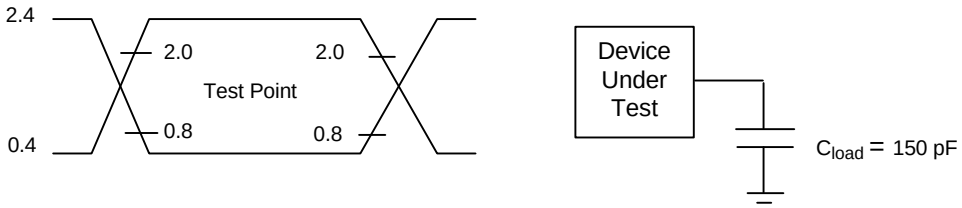


PARAMETER	PARAMETER DESCRIPTIONS	MIN.	MAX.	TYPICAL	REMARKS
tc1	XA7-0 setup time			30	Unit = nS
tc2	XA7-0 hold time			30	
tc3	XWRB pulse width			90	
tc4	Write data setup time			90	
tc5	Write data hold time			30	
tc6	XRDB pulse width			120	
tc7	Read data delay time		90		
tc8	Read data hold time	0			

9.5 AC Timing Test Conditions

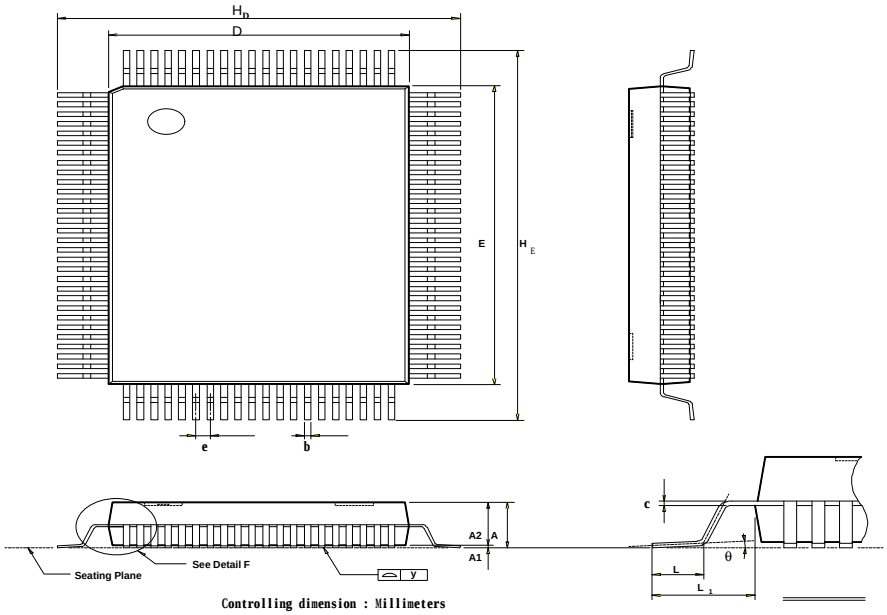
(T_A = 0 to 70 °C, V_{DD} = 5V ±5%)

Inputs are driven to 2.4V for logical 1 and 0.4V for logical 0. Measurements are made at 2.0V for logical 1 and 0.8V for logical 0. The AC testing input/output waveforms are shown below:



10. PACKAGE DIMENSIONS

100L QFP (14 × 20 × 2.75 mm footprint 4.8 mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.010	0.014	0.018	0.25	0.35	0.45
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.746	0.740	0.756	18.40	18.80	19.20
H_E	0.960	0.976	0.992	24.40	24.80	25.20
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	—	0.064	—	—	2.40	—
y	—	—	0.003	—	—	0.08
q	0°	—	7°	0°	—	7°

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Note: All data and specifications are subject to change without notice.