74LVC1G38

2-input NAND gate (open drain)

Rev. 01 — 18 October 2004 **Product data sheet**

1. General description

The 74LVC1G38 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device as translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G38 provides the 2-input NAND function.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Open drain outputs
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +125 °C.

PHILIPS

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay inputs A, B to output Y	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ		-	3.0	-	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω		-	1.8	-	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω		-	2.5	-	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω		-	2.3	-	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω		-	1.5	-	ns
C_I	input capacitance			-	2.5	-	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V	[1] [2]	-	6	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G38GW	–40 °C to +125 °C	SC-88A	plastic surface mounted package; 5 leads	SOT353
74LVC1G38GV	–40 °C to +125 °C	SC-74A	plastic surface mounted package; 5 leads	SOT753
74LVC1G38GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

5. Marking

Table 3: Marking

Type number	Marking code
74LVC1G38GW	YB
74LVC1G38GV	YB
74LVC1G38GM	YB

6. Functional diagram

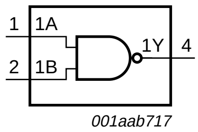


Fig 1. Logic symbol.

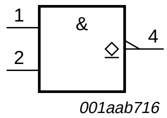


Fig 2. IEC logic symbol.

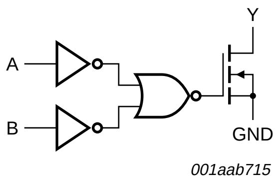


Fig 3. Logic diagram (one driver).

7. Pinning information

7.1 Pinning

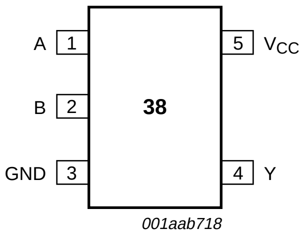


Fig 4. Pin configuration SC-88A and SC-74A.

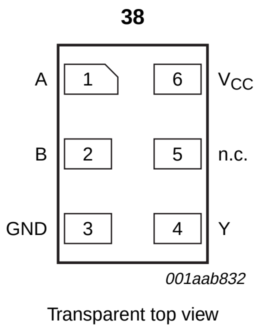


Fig 5. Pin configuration XSON6.

7.2 Pin description

Table 4: Pin description

Symbol	Pin SC-88A, SC-74A	Pin XSON6	Description
A	1	1	data input A
B	2	2	data input B
GND	3	3	ground (0 V)
Y	4	4	data output Y
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

8. Functional description

8.1 Function table

Table 5: Function table [1]

Input		Output
A	**B**	**Y**
L	L	Z
L	H	Z
H	L	Z
H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF state.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	active mode	[1] [2]	–0.5	+6.5	V
		Power-down mode	[1] [2]	–0.5	+6.5	V
I_O	output diode current	$V_O = 0$ V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C		-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

10. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V

Table 7: Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage					
		active mode	0	-	5.5	V
		disable mode; V_{CC} = 1.65 V to 5.5 V	0	-	5.5	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		−40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	-	10	ns/V

11. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	-	-	-	
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	±0.1	±10	μA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	μA
C_I	input capacitance		-	2.5	-	pF

Table 8: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	-	-	-	
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	-	±100	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±200	μA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±200	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	200	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	5000	μA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

12. Dynamic characteristics

Table 9: Dynamic characteristics

GND = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
t_{PZL}, t_{PLZ}	propagation delay inputs A, B to output Y	see Figure 6 and 7				
		V_{CC} = 1.65 V to 1.95 V	1.0	3.0	10.0	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	1.8	6.0	ns
		V_{CC} = 2.7 V	0.5	2.5	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.3	4.5	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	1.5	3.9	ns
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V [2] [3]	-	6	-	pF

Table 9: Dynamic characteristics *...continued*

GND = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PZL}, t_{PLZ}	propagation delay inputs A, B to output Y	see Figure 6 and 7				
		V_{CC} = 1.65 V to 1.95 V	1.0	-	12.5	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	-	7.5	ns
		V_{CC} = 2.7 V	0.5	-	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	-	5.7	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	-	4.9	ns

[1] All typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

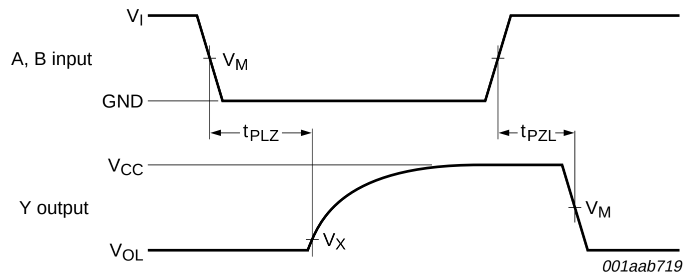
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[3] The condition is V_I = GND to V_{CC}.

13. AC waveforms



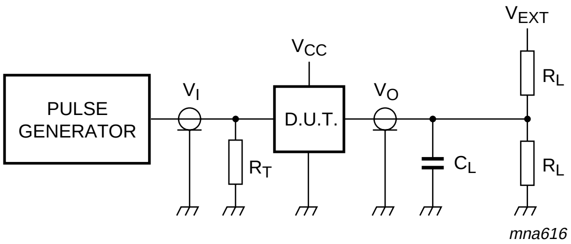
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 6. The input (A, B) to output (Y) propagation delays.

Table 10: Measurement points

Supply voltage	Input	Output	
V_{CC}	**V_M**	**V_M**	**V_X**
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3 V



Test data is given in Table 11.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

V_{EXT} = Test voltage for switching times.

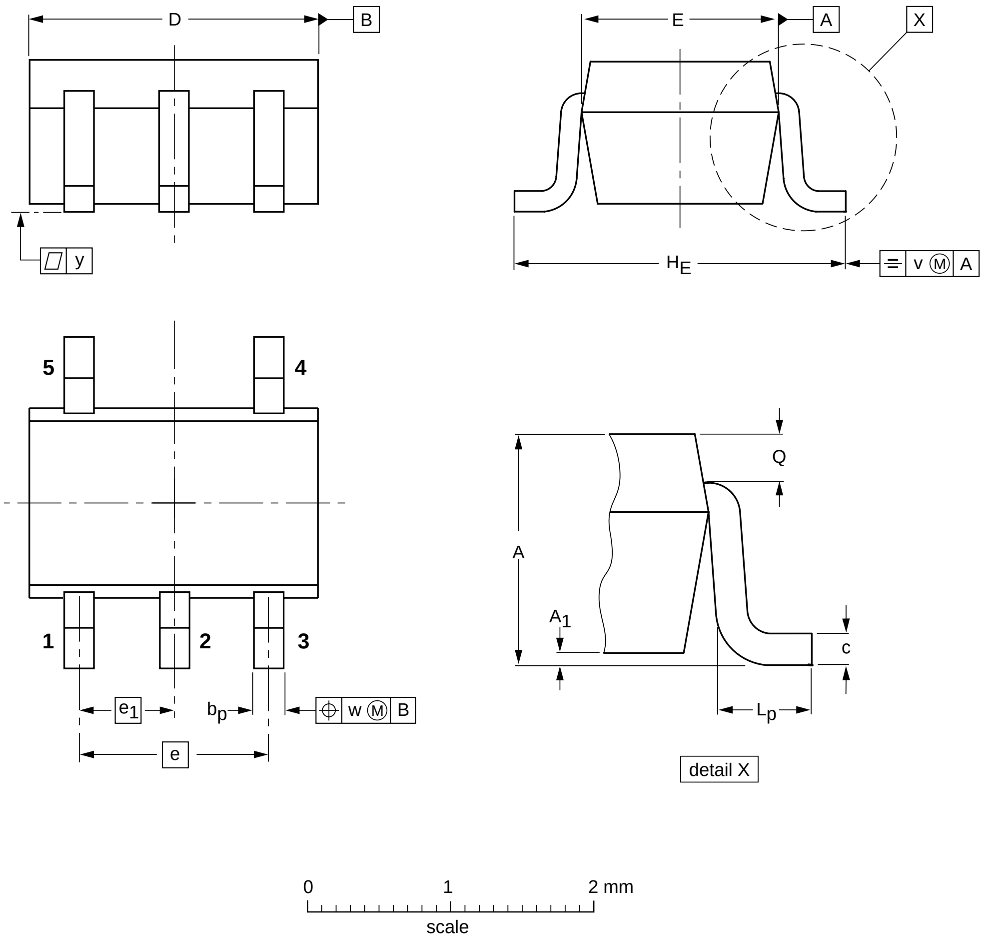
Fig 7. Load circuitry for switching times.

Table 11: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2 × V_{CC}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2 × V_{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}

14. Package outline

Plastic surface mounted package; 5 leads **SOT353**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

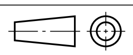
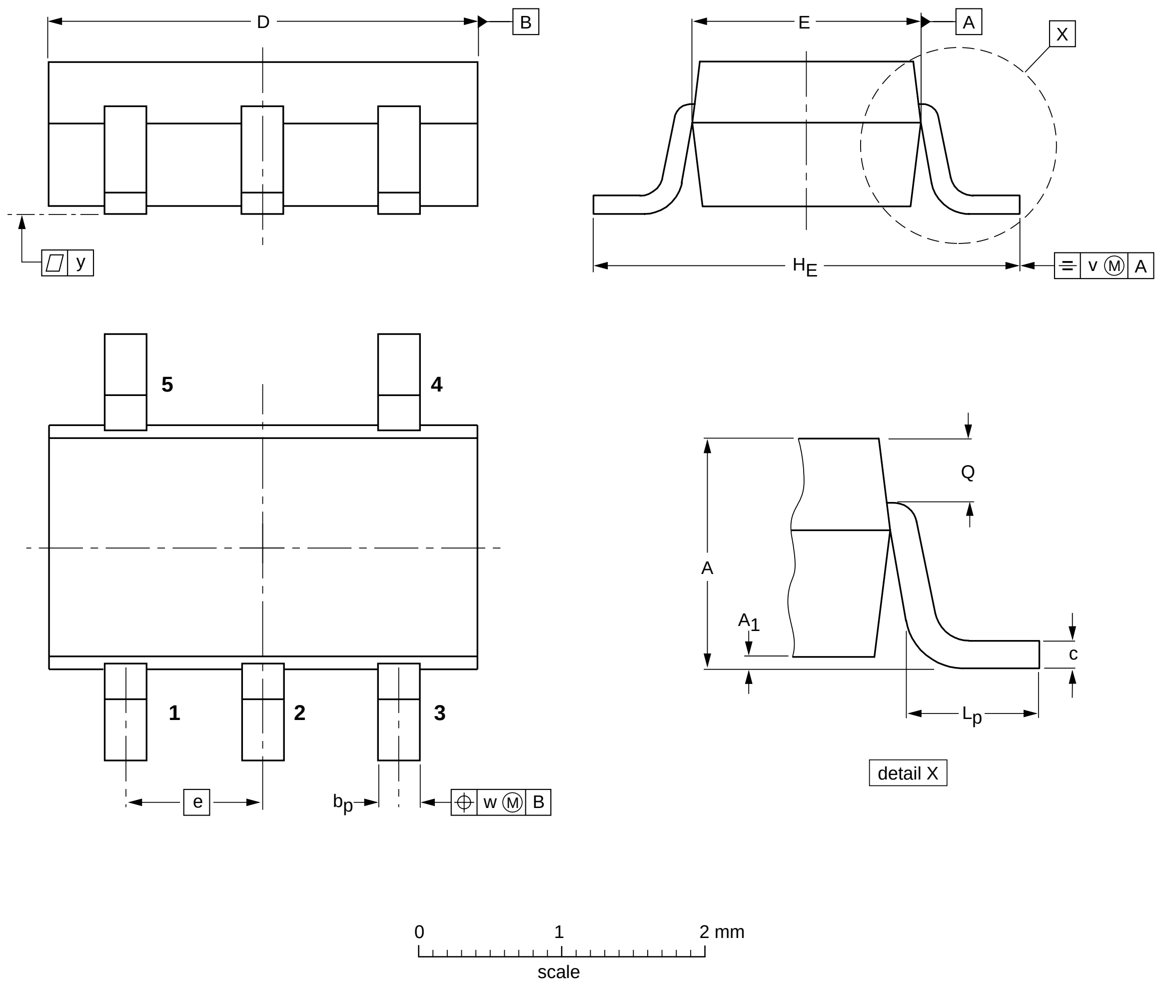
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Fig 8. Package outline SOT353 (SC-88A).

Plastic surface mounted package; 5 leads **SOT753**



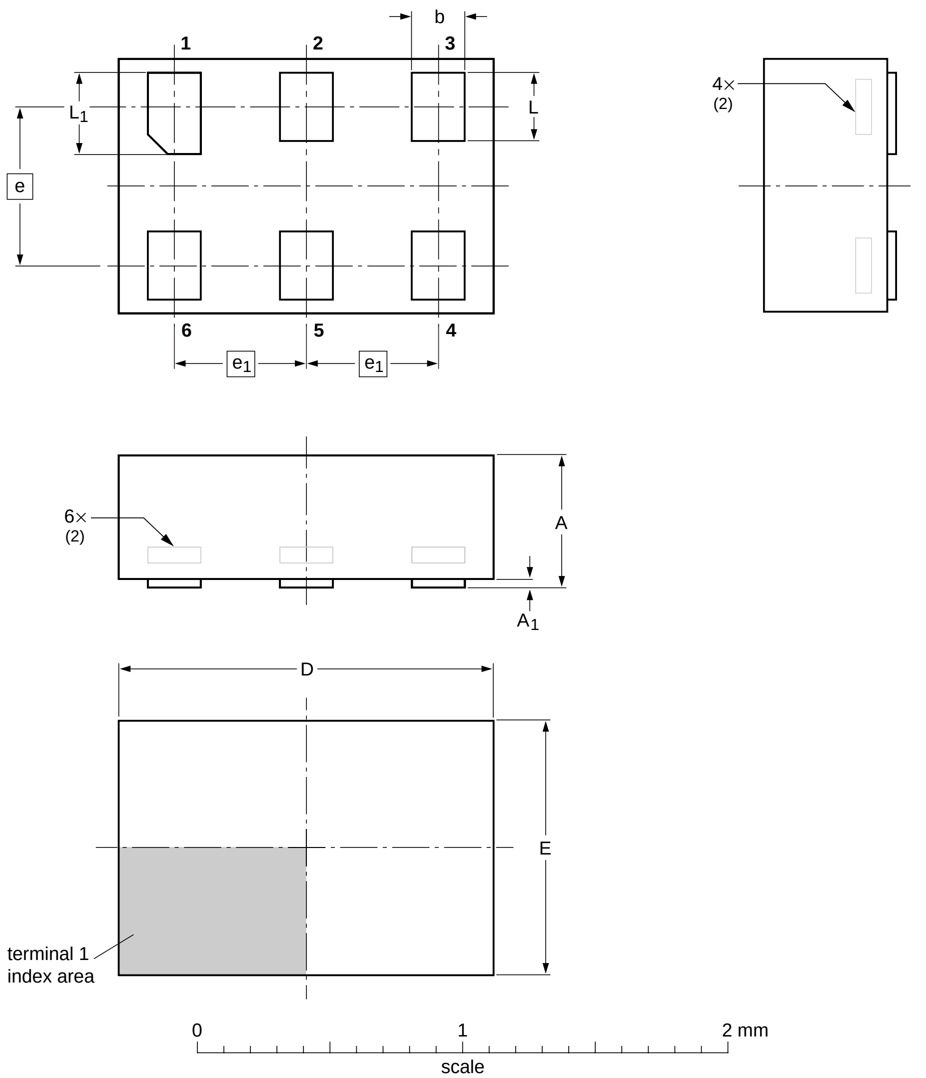
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

Fig 9. Package outline SOT753 (SC-74A).

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

Fig 10. Package outline SOT886 (XSON6).

15. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC1G38_1	20041018	Product data sheet	-	9397 750 13802	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Contents

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