EPSON

E0C6233

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Core CPU Architecture
- SVD Circuit/Comparator
- Event Counter

■ DESCRIPTION

The E0C6233 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 4-bit core CPU. It also contains the ROM, RAM, LCD driver, event counter, SVD circuit, stopwatch counter and time base counter. With wide voltage range and low power consumption, the E0C6233 provides an excellent solution for the low-power consumption systems with manganese dry cell.

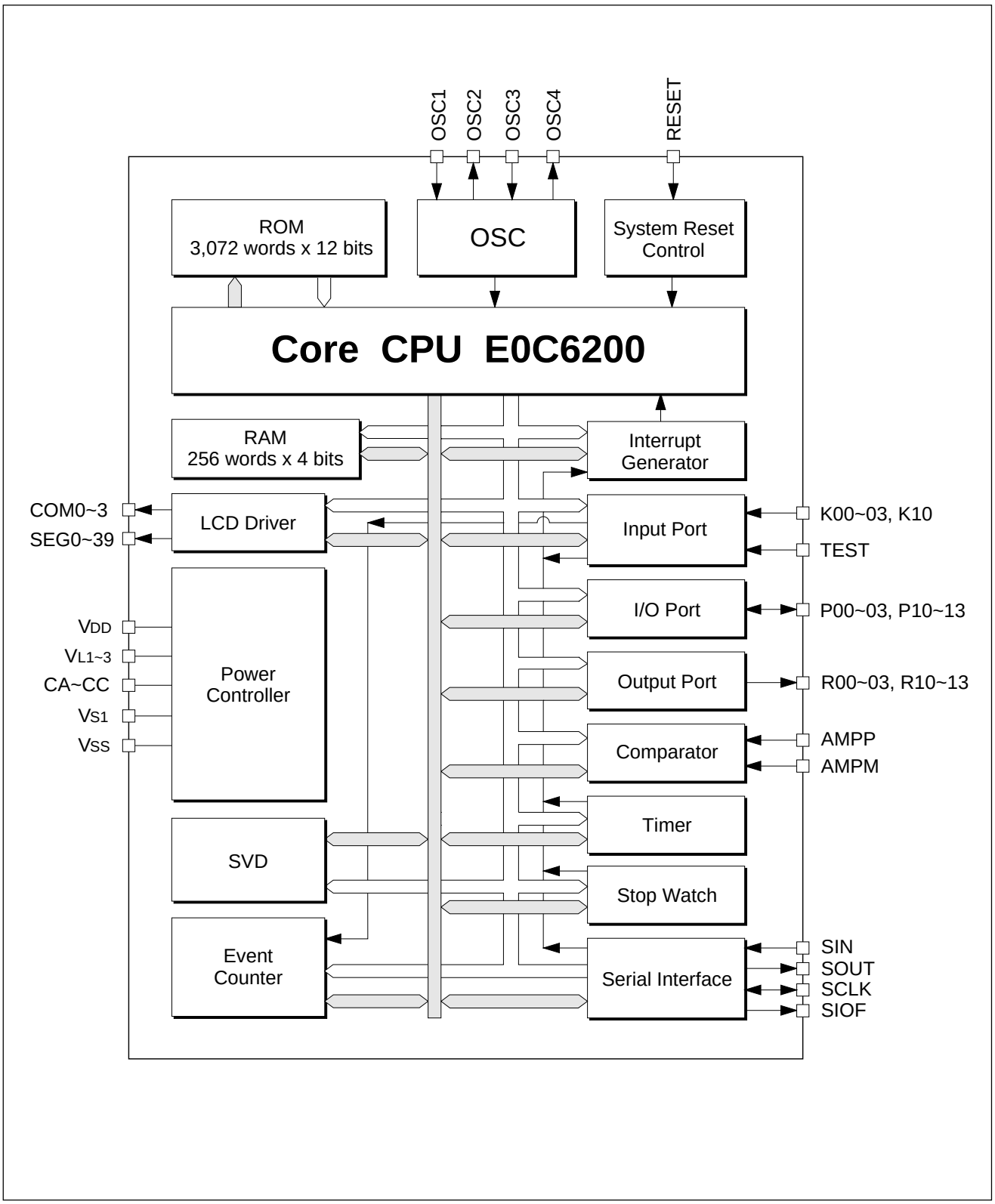
■ FEATURES

- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz (Typ.)/500kHz (Typ.) (selectable by software)
- Instruction set ..... 108 instructions
- Instruction cycle time ..... 153µsec, 214µsec or 366µsec at 32kHz (depending on instruction)
  10µsec, 14µsec or 24µsec at 500kHz (depending on instruction)
- ROM capacity ..... 3,072 × 12 bits
- RAM capacity ..... 256 × 4 bits
- Input port ..... 5 bits (pull-down resistors are available by mask option)
- Output port ..... 4 bits (general purpose)
  2 bits (buzzer output): BZ, $\overline{BZ}$
  1 bit (lamp output)
  1 bit (clock output)
- I/O port ..... 8 bits
- LCD driver ..... 40 segments × 3 commons/40 segments × 4 commons (1/3 or 1/4 duty is selectable by mask option)
- Built-in time base counter
- Built-in serial interface ..... Clock synchronous
- Built-in stopwatch counter
- Built-in watchdog timer
- Event counter ..... 8 lines
- Built-in AMP ..... Operational AMP for MOS input analog comparator
- Built-in SVD ..... 1.2 ± 0.1V/2.4 ± 0.1V (supply voltage detector)
- Interrupts ..... External : Input interrupt 2 lines
  Internal : Timer interrupt 2 lines
  Serial interface interrupt 1 line
- Current consumption ..... E0C62L33 HALT mode (32kHz) : 1.0µA (Typ.)
  E0C6233 HALT mode (32kHz) : 1.5µA (Typ.)
  E0C62A33 HALT mode (32kHz) : 2.0µA (Typ.)
  OPERATING mode (500kHz) : 135µA (Typ.)
- Package ..... QFP5-100pin (plastic)
  Die form

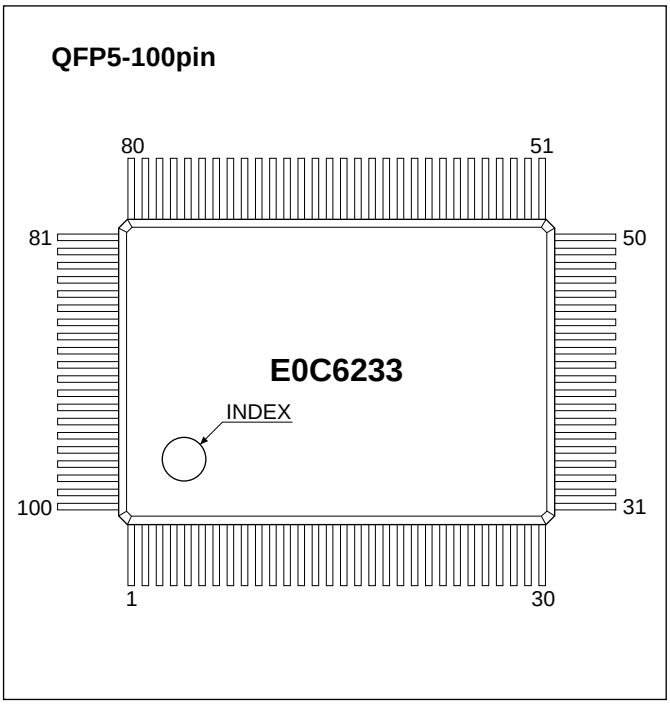
■ LINE UP

Model	Supply voltage	Clock
E0C62L33	1.5V (0.9V to 1.7V)	32kHz (Crystal oscillation)
E0C6233	3.0V (1.8V to 3.5V)	32kHz (Crystal oscillation)
E0C62A33	3.0V (2.2V to 3.5V)	32kHz (Crystal oscillation) & 500kHz (Ceramic or CR oscillation)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	26	SEG38	51	N.C.	76	SIOF
2	N.C.	27	SEG39	52	N.C.	77	SCLK
3	TEST	28	N.C.	53	N.C.	78	N.C.
4	N.C.	29	AMPP	54	N.C.	79	N.C.
5	N.C.	30	N.C.	55	R11	80	N.C.
6	SEG18	31	AMPM	56	R10	81	SOUT
7	SEG19	32	K10	57	R13	82	SIN
8	SEG20	33	K03	58	V_{SS}	83	SEG0
9	SEG21	34	K02	59	RESET	84	SEG1
10	SEG22	35	K01	60	OSC4	85	SEG2
11	SEG23	36	K00	61	OSC3	86	SEG3
12	SEG24	37	P03	62	V_{S1}	87	SEG4
13	SEG25	38	P02	63	OSC2	88	SEG5
14	SEG26	39	P01	64	OSC1	89	SEG6
15	SEG27	40	P00	65	V_{DD}	90	SEG7
16	SEG28	41	P13	66	V_{L3}	91	SEG8
17	SEG29	42	P12	67	V_{L2}	92	SEG9
18	SEG30	43	P11	68	V_{L1}	93	SEG10
19	SEG31	44	P10	69	CC	94	SEG11
20	SEG32	45	R03	70	CB	95	SEG12
21	SEG33	46	R02	71	CA	96	SEG13
22	SEG34	47	N.C.	72	COM3	97	SEG14
23	SEG35	48	R01	73	COM2	98	SEG15
24	SEG36	49	R00	74	COM1	99	SEG16
25	SEG37	50	R12	75	COM0	100	SEG17

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	65	I	Power source (+) terminal
V_{SS}	58	I	Power source (-) terminal
V_{S1}	62	O	Oscillation and internal logic system regulated voltage output terminal
V_{L1}	68	O	LCD system regulated voltage output terminal (approx. -1.05 V)
V_{L2}	67	O	LCD system booster output terminal (V_{L1} x 2)
V_{L3}	66	O	LCD system booster output terminal (V_{L1} x 3)
CA–CC	69–71	–	Booster capacitor connecting terminal
OSC1	64	I	Crystal oscillation input terminal
OSC2	63	O	Crystal oscillation output terminal
OSC3	61	I	Ceramic or CR oscillation input terminal (Switchable by mask option, 62A33 only)
OSC4	60	O	Ceramic or CR oscillation output terminal (Switchable by mask option, 62A33 only)
K00–K03, K10	32–36	I	Input terminal
P00–P03, P10–P13	37–44	I/O	I/O terminal
R00–R03	45, 46, 48, 49	O	Output terminal
R10	56	O	Output terminal (DC or BZ output may be selected by mask option)
R13	57	O	Output terminal (DC or $\overline{BZ}$ output may be selected by mask option)
R11	55	O	Output terminal
R12	50	O	Output terminal (DC or FOUT output may be selected by mask option)
AMPP	29	I	Analog comparator non-inverted input terminal
AMPM	31	I	Analog comparator inverted input terminal
SEG0–39	6–27, 83–100	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0–3	72–75	O	LCD common output terminal
SIN	82	I	Serial interface input terminal
SOUT	81	O	Serial interface output terminal
SCLK	77	I/O	Serial interface clock input/output terminal
SIOF	76	O	Serial interface status output terminal
RESET	59	I	Initial reset input terminal
TEST	3	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

E0C6233/62A33

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP5-100pin).

E0C62L33

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP5-100pin).

● Recommended Operating Conditions

E0C6233

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

E0C62L33

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.7	-1.5	-1.1	V
		V_{DD}=0V, With software control *1	-1.7	-1.5	-0.9 *2	V
		V_{DD}=0V, When the analog comparator is used	-1.7	-1.5	-1.2	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

∗1: When switching to heavy load protection mode. Note, however, that the ON time for SVD in the heavy load protection must be limited to 10 msec per second of operation time.
∗2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C62A33

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	f_{OSC1}		–	32.768	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	50	500	600	kHz

● DC Characteristics

E0C6233/62A33

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, P00–03, P10–13 SIN, SCLK	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, P00–03, P10–13 SIN, SCLK	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.9•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–03, K10, P00–03, P10–13 SIN, SCLK, AMPP, AMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–03, K10	4		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–03, P10–13 RESET, TEST	25		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, P00–03, P10–13 SIN, SCLK, AMPP, AMPM RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R10, R11, R13			-1.8	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SIOF, SCLK			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R10, R11, R13	6.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SIOF, SCLK	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG39			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG39			-200	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		200			µA

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(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, P00–03, P10–13 SIN, SCLK	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, P00–03, P10–13 SIN, SCLK	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.9•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–03, K10, P00–03, P10–13 SIN, SCLK, AMPP, AMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–03, K10	2		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–03, P10–13 RESET, TEST	12		60	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, P00–03, P10–13 SIN, SCLK, AMPP, AMPM RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R10, R11, R13			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SIOF, SCLK			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R10, R11, R13	1,400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SIOF, SCLK	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG39			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG39			-100	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		100			µA

● Analog Circuit Characteristics and Current Consumption

E0C6233 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		1.5	4.0	µA
		During operation *1			6.0	10.0	µA

*1: The SVD circuit and analog comparator are in the OFF status.

E0C6233 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		11.2	34.0	µA
		During operation *1			14.5	40.0	µA

*1: The SVD circuit is in the ON status (HVLD="1", SVDON="0"). The analog comparator is in the OFF status.

E0C62L33 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		1.0	3.0	µA
		During operation *1			3.0	8.0	µA

*1: The SVD circuit and analog comparator are in the OFF status.

E0C62L33 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT *1	Without panel load		2.0	7.0	µA
		During operation *1			8.0	18.0	µA

*1: The SVD circuit is in the ON status (HVLD="1", SVDON="0"). The analog comparator is in the OFF status.

E0C62A33 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.0	µA
		During operation at 32kHz *1	OSCC="0"		8.0	15.0	µA
		During operation at 500kHz *1	Without panel load		135	300	µA

*1: The SVD circuit and analog comparator are in the OFF status.

E0C62A33 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		11.5	35.0	µA
		During operation at 32kHz *1	OSCC="0"		16.0	45.0	µA
		During operation at 500kHz *1	Without panel load		130	330	µA

*1: The SVD circuit is in the ON status (HVLD="1", SVDON="0"). The analog comparator is in the OFF status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6233 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		18		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62L33 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		18		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.1 to -1.7V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-1.7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.
Note, however, that the ON time for SVD must be limited to 10 msec per second of operation time.

E0C62A33 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		18		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62A33 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, Ta=25°C)

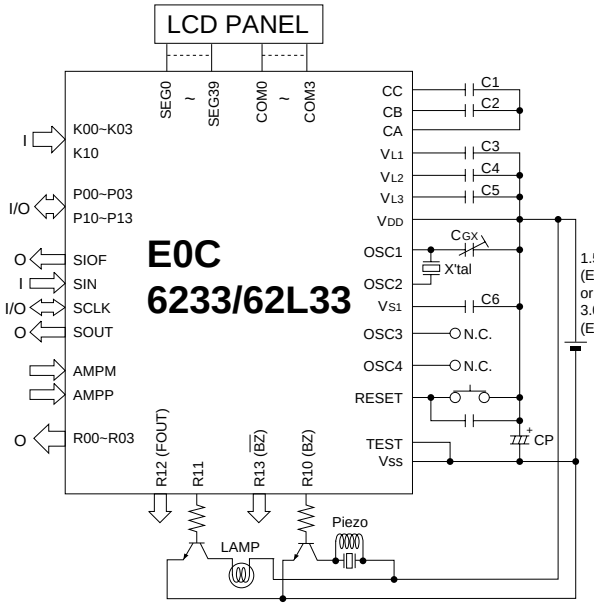
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	430kHz	30	%
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			3	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

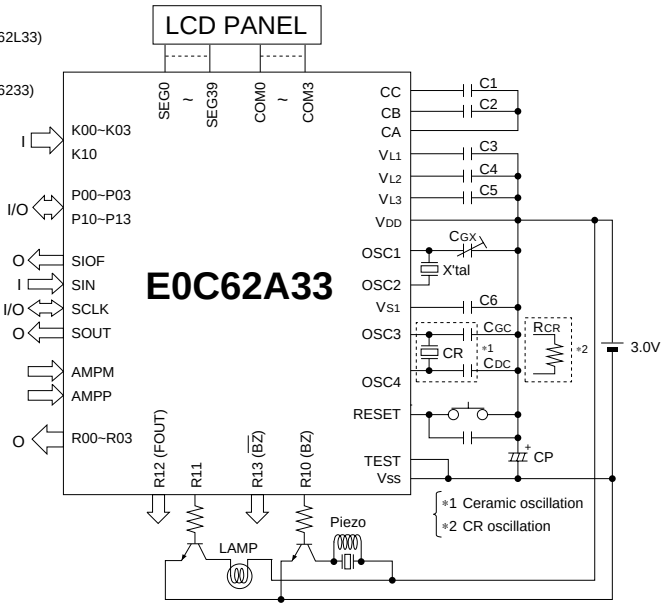
E0C62A33 (Ceramic oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 500kHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			5	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM



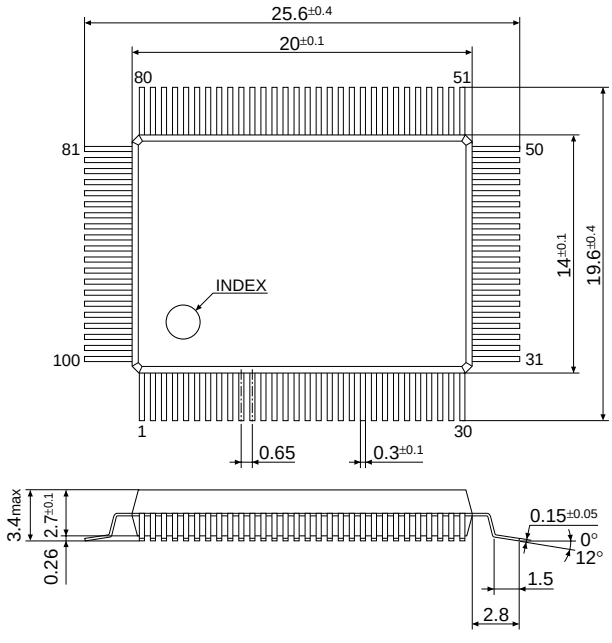


X'tal	Crystal oscillator	32.768kHz, CI(Max.)=35kΩ
C_{GX}	Trimmer capacitor	5~25pF
CR	Ceramic oscillator	500kHz
C_{GC}	Gate capacitance	100pF
C_{DC}	Drain capacitance	100pF
R_{CR}	Resistance for CR oscillation	82kΩ
C1~C6		0.1µF
CP		3.3µF

Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP5-100pin



Unit: mm

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