FEATURES

- **3.3V power supply:**
  Split V_{CC} = +2V, GND = 0V
  V_{EE} = –1.3V for 3.3V
  V_{EE} = –3V for 5.0V
- **Simple switch configuration**
- **PECL signal outputs**
- **Simple RDIN+, RDIN– PECL inputs**
- **Simple REFCLK TTL input**
- **SY87700: Clock and data recovery from 32Mbps up to 175Mbps NRZ data stream, clock generation from 32Mbps to 175Mbps**
- **SY87701: Clock and data recovery from 32Mbps up to 1.25Gbps NRZ data stream, clock generation from 32Mbps to 1.25Gbps**

DESCRIPTION

The SY87700 and SY87701 Clock and Data Recovery (CDR) chips are both high-performance ICs that are designed to provide protocol-independent clock and data recovery at any data rate between 32Mbps and 175Mbps for the SY87700 and 32Mbps to 1.25Gbps for the SY87701.

This document provides design and implementation information, as well as a detailed description of the SY87700/701 evaluation board.

The evaluation board is intended to provide a convenient test and evaluation platform for the SY87700/701 CDR device. This board can be used for many types of jitter tests, including SONET compliance of the SY87700/701, as well as PLL characterization.

FUNCTIONAL BLOCK DIAGRAM

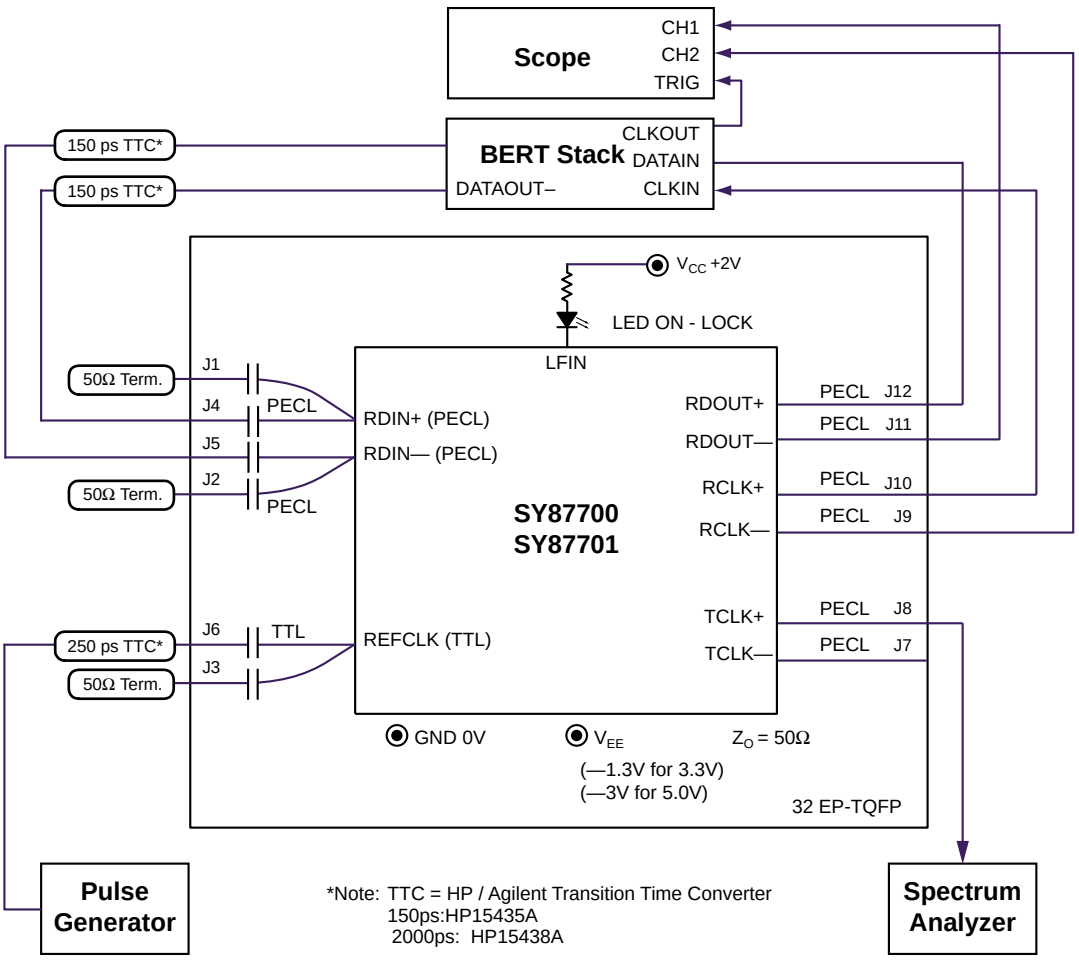


Figure 1. SY87700/SY87701 Evaluation Board and Test Set-Up

FUNCTIONAL DESCRIPTION

The evaluation board simplifies test and measurement of the SY87700 and SY87701. This section covers the various parts of the SY87700/701 evaluation board, and includes detailed information about these blocks. Performance of the SY87700/701 can be easily evaluated by following the step-by-step instructions found in the "Test Configuration" section.

Power Supply

The SY87700L and SY87701L are 3.3V devices. Therefore, V_{CC} should all be connected to 2.0V, and GND connected to 0V, and V_{EE} should be connected to –1.3V. The SY87700V and SY87701V are 5.0V devices, therefore, V_{CC} should be connected to 2V, and GND to 0V, and V_{EE} should be connected to –3V.

Board Design and Layout

The evaluation board uses a force-sense design on the signal inputs where the signal pins (source pins) on the SY87700/701 are located on 50Ω line, on the last layer. The sense lines, however, are located on layer 1. The force-sense design is handy for monitoring inputs to the SY87700/701 (such as input jitter). However, a 50Ω terminator needs to be added to all unused sense outputs or the line will act as a quarter wave stub notch filter.

LED

The SY87700/701 evaluation board features one LED for monitoring the Link Fault Indicator (LFIN) pin. The LED will turn on when the PLL has locked-on to the RDIN input data stream, which indicates that LFIN has gone active HIGH. Additionally, LFIN can only go active when CD is HIGH and RDIN is within the 1000ppm frequency range of the PLL.

Signal Inputs

Signal RDIN is 3.3V/5V PECL DC-coupled. Therefore, the current level for DC-coupled applications is V_{CC} –2V.

RDIN-DRIVEN

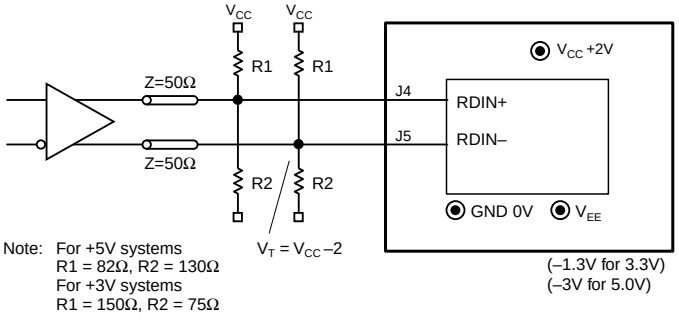


Figure 2. Test Set-Up

RDIN-BERT

If you are using a high frequency bit error rate tester (such as the Agilent 70843B Error Performance Analyzer) to drive RDIN±, you will need to insert a 250ps Transition Time Converter (TTC) to slow its edge down.

REFCLK

If you are using a high frequency clock or pulse generator such as the Agilent 8133 to drive REFCLK, you will need to insert a 2000ps Transition Time Converter (TTC) to slow its edge down.

Signal Outputs

The SY87700/701 features PECL outputs for both RDOUT± and RCLK± and TCLK±. Unused pins should be left FLOATING.

Test Configuration

This section contains step-by-step instructions for configuring the SY87700 and SY87701 for clock and data from the data stream of a BERT stack.

1. Set switches on evaluation board for desired data and clock frequencies. There are seven switches in SW1:
    1. FREQSEL1
    2. FREQSEL2
    3. FREQSEL3
    4. CLKSEL
    5. DIVSEL2
    6. DIVSEL1
    7. CD

    See "All Possible Legal Frequency and Divide Selections" section on page 5, on how to set these switches. In addition, CLKSEL should be set HIGH which configures TCLK output as the recovered CLK from RDIN. If CLKSEL is low, TCLK will be the synthesized clock output. Additionally, CD should be set HIGH to allow the PLL to recover RDIN. If CD is low, RDIN is forced low.
2. Connect GND to 0V.
3. Connect VCC to +2V.
4. For 3.3V operation, connect VEE = –1.3V.
   For 5.0V operation, connect VEE = –3.0V.
5. Connect REFCLK (TTL) inputs to reference clock.
   Note: If using Agilent 8133A Pulse Generator, use 250ps Time Transistion Converters on the 8133 outputs.
6. Connect TCLK (PECL) outputs to data inputs on test equipment.
7. Connect RDINV (PECL) inputs to data source.
8. Connect RDOUT (PECL) to outputs on test equipment.
9. Connect RCLK outputs to clock inputs on test equipment.

FREQUENTLY ASKED QUESTIONS

What Do I Do with the Exposed Pad on the Bottom of the Package?

The purpose of the exposed pad at the bottom of the package is to conduct heat more efficiently out of the package. Solder or use thermal conductive epoxy. Although the pad is connected to V_{EE}, will not be any degradation in either output generated jitter or input jitter tolerance performance.

I Just Got my Evaluation Board and I Cannot Get Anything to Work.

First check the power supplies. This evaluation board uses one power supply. You should see a current draw of about 200mA when the part is running normally. After that, check voltage swing levels of REFCLK. It is important to focus on getting the synthesizer (CMU) to work first (REFCLK to TCLK), before the data recovery side. TCLK synthesizer sets up the coarse adjust for the VCO in the CDR (or CRU), so if TCLK is not oscillating at the right frequency, the CDR will not lock. Another tip: use a frequency counter like HP53132A to measure frequency of TCLK– it is often more foolproof than using the DSO. If using a DSO scope, like the Agilent CSA803, or the 11801 from Tektronix, trigger off of the REFCLK clock source.

After the synthesizer is operating as expected, make sure to change the trigger on the oscilloscope to trigger on the data generation instrument, such as second HP8133A, a Microwave Logic 1400, or HP70004A,70841 BERT stack. The BERT stack has a “clock output”, that be used to trigger the scope. The instrument generating REFCLK is not phase/ frequency locked to the data generation side, so it would be impossible to examine an “eye” diagram.

Check the eye of the output source directly first, before going into the device. Most data generation instruments have deskew capability. It is important to deskew both the instrument and the ± coaxial cables into the DSO, otherwise you’ll have too much apparent deterministic jitter.

Aside from setting the DIVSEL, and FREQSEL incorrectly, everything should operate as expected at this point.

What is the Time Domain Reflectometry Test?

TDR (Time Domain Reflectometry) is used to verify impedance continuity along a signal path. Many interconnects, such as SMA, if not launched correctly onto the PCB will exhibit inductive-like resonance with an abrupt capacitive discontinuity. This discontinuity will subtract signal from the inputs and outputs and effectively close the resulting data eye.

What Should I Use to Generate REFCLK in My Design?

This depends on data rate, jitter budget, and cost. However, REFCLK input jitter will affect the overall jitter performance of the system. A fundamental tone crystal-based oscillator is ideal. Measure the jitter of the oscillator with a Wavecrest DTS2077. A measurement above the 3ps noise floor of the instrument is too high. Remember that the REFCLK input is multiplied by the DIVSEL selected value, so the resulting jitter increases by 20log (divide ratio). If you use a clock derived from an ASIC, verify the single cycle and accumulated cycle jitter.

Crystal based oscillators typically have poor AC power supply rejection ratio, and if you are providing board power via 400kHz switching supplies you may have to provide some level of filtering, not just bypassing, for the supplies. Also verify that the oscillator output has no “pedestals” in the response due to improper impedance matching and/or inadequate drive capability of the oscillator.

Do not use CMOS-based PLLs. They almost always have too much high frequency deterministic jitter for this application. Also fanning out one oscillator to several locations on your board is not a good idea. Crosstalk and inadequate drive can adversely affect performance. We recommend Raltron, Mutron, CTS, Plantronics, Frequency Management, etc., as vendors of crystal-based fundamental tone oscillators.

Can you Suggest a Bypass/Decoupling Scheme?

The SY87700/701 data sheet contains the evaluation board schematic, and a bill of materials list is included in this document. We have found this arrangement to be an excellent starting point. In addition, most system designs could be dramatically improved by spacing the power planes between ground planes to lower the self-inductance of the power distribution.

What Layout Tips Do You Have?

1. Establish controlled impedance stripline, microstrip, or co-planar construction techniques for high-speed signal paths.
2. All differential paths are critical timing paths, and skew should be matched to within ±10psec.
3. Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of signal traces.
4. Maintain compact filter networks as close to filter pins as possible.
5. Provide ground plane relief under the filter path to reduce stray capacitance and be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input by isolating the XTAL oscillator from power supply noise by adequately decoupling.
7. Keep the XTAL oscillator close to SY87700/701.
8. High speed operation may require use of fundamental-tone crystal-based oscillator for optimum performance. (Third overtone oscillators typically have more jitter.)
9. Isolate the input, output, and REFCLK signal traces from other clock and data signals on your board if these other traces are within 3x the trace width. Isolation can be achieved by putting ground traces in between.

Should I Adjust the Loop Lilter?

The values found in the data sheets are the result of extensive modeling as well as lab testing. Therefore, we recommend starting with those values. Selecting values to simply reduce jitter does not work since there is a trade-off in jitter generation and jitter tolerance. However, for telecom applications under Bellcore,ITU/CCIT specifications it may be advantageous to adjust the values to trade off jitter transfer for jitter generation.

How Do You Suggest We Qualify and Evaluate Performance?

Evaluation should start by measuring the jitter of the REFCLK input. The Clock Multiplier Unit (CMU) is simply a PLL. It multiplies the incoming REFCLK frequency, and jitter will usually worsen. The HP8133A pulse generator is ideal, and the user should include a Transition Time Converter on the 8133s output to slow its edges down. Make sure the rise/fall times are reasonable (not 28ps rise/fall found on the 12Gbps HP BERT clocks!) and 150ps TTCs will ensure this. Measure the TCLK output jitter using either the ± side, with the other side terminated. Suitable instruments for measuring the TCLK jitter are the CSA803, 11801, or the Wavecrest 2077. See Figure 1 for descriptions of set-up. Characterization of the jitter must include accumulation of many cycles or periods down to a specified low pass corner frequency. Wavecrest makes this easy with their 6.1 version software since the user can specify a low pass corner for the collected jitter. The Wavecrest instrument cannot be set up for single period measurements, but must look at the difference between the rising edges of the REFCLK and the TCLK using both channels and performing a histogram of the propagation time between the input REFCLK (which is the HP8133A trigger divided by one) and the output TCLK.

Evaluation of the CDR is similar, except that the RCLK and RDOUT outputs are used instead. The procedure for measuring the RCLK jitter is identical to the above procedure for TCLK jitter.

Evaluation of the output jitter on RDOUT using RCLK as a trigger source isn't trivial, as the minimum time between the scope trigger and measurement is 24ns for the Agilent 86100A scope. Therefore the user must delay the data by the same amount, so that the jitter on RDOUT is measured with respect to the correct clock edge. This is important, as the SY87700/701 will retime the edges on RDOUT so that they better align with RCLK. The Wavecrest DTS2077 can also be used.

The setup for SONET jitter compliance tests is shown in Figure 1. Agilent provides software for automated Bellcore jitter compliance tests. Contact Agilent for details.

DESCRIPTION OF CONNECTORS

Connector	Name	Type	Connects to 28-pin SOIC	32-pin TQFP	Description
J1	RDIN+_S	PECL	Pin 4	Pin 2	RDIN+ (Sense)
J2	RDIN–_S	PECL	Pin 5	Pin 3	RDIN– (Sense)
J3	REFCLK–S	TTL	Pin 7	Pin 5	REFCLK– (Sense)
J4	RDIN+_F	PECL	Pin 4	Pin 2	RDIN+ (Force)
J5	RDIN–_F	PECL	Pin 5	Pin 3	RDIN– (Force)
J6	REFCLK_F	PECL	Pin 7	Pin 5	REFCLK– (Force)
J7	TCLK–	PECL	Pin 18	Pin 17	TCLK– (Output)
J8	TCLK+	PECL	Pin 19	Pin 18	TCLK+ (Output)
J9	RCLK–	PECL	Pin 21	Pin 20	RCLK– (Output)
J10	RCLK+	PECL	Pin 22	Pin 21	RCLK+ (Output)
J11	RDOUT–	PECL	Pin 24	Pin 23	RDOUT– (Output)
J12	RDOUT+	PECL	Pin 25	Pin 24	RDOUT+ (Output)

ALL POSSIBLE LEGAL FREQUENCY AND DIVIDER SELECTIONS

FREQSEL1	FREQSEL2	FREQSEL3	f_{VCO}/f_{RCLK}	f_{RCLK} Data Rates (Mbps)
0	1	1	6	125 –175
1	0	0	8	94 – 157
1	0	1	12	63 – 104
1	1	0	16	47 – 78
1	1	1	24	32 – 52
0	1	0	—	undefined
0	0	X(2)	—	undefined

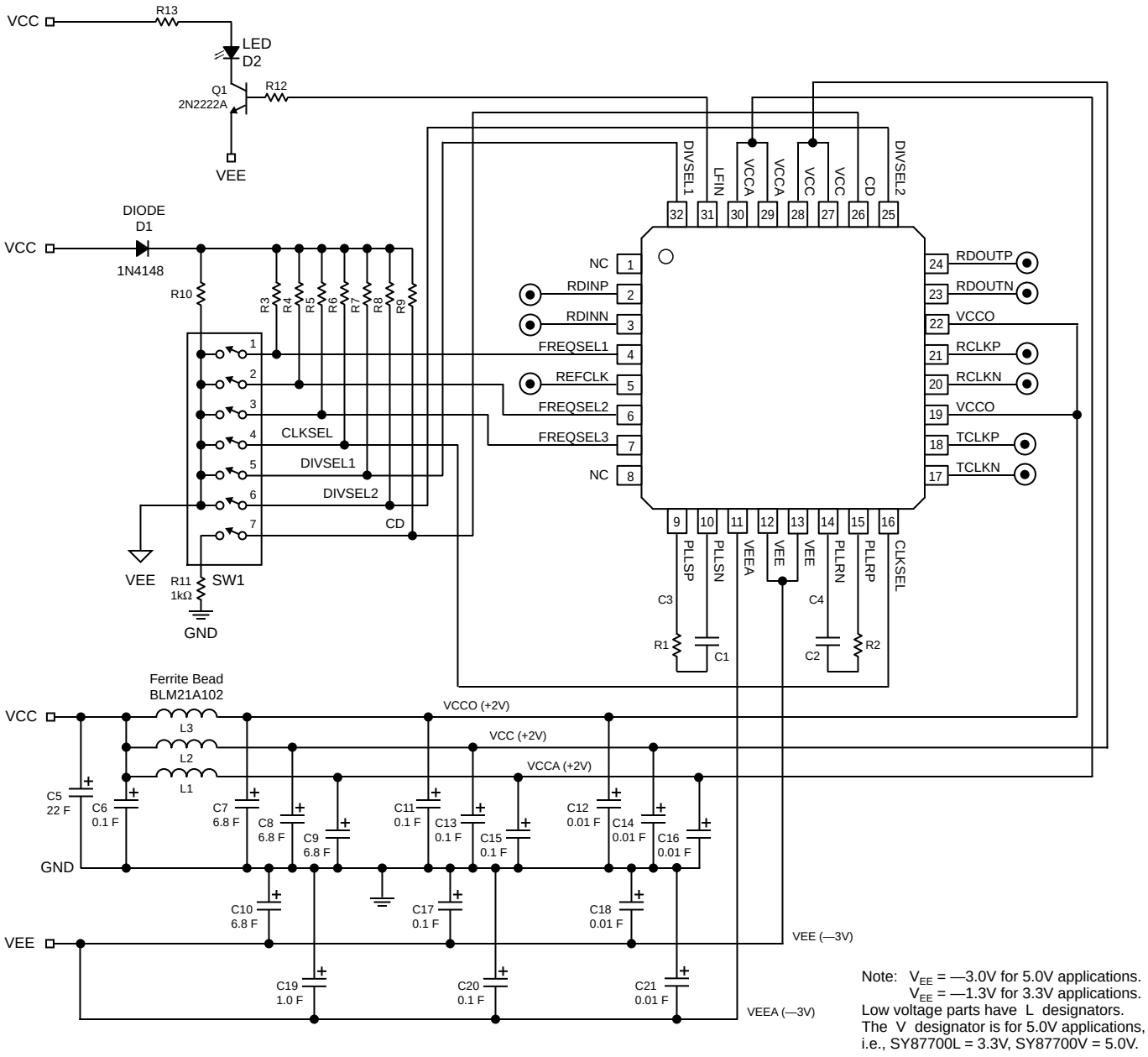
NOTES:

1. SY87700L operates from 32-175MHz. For higher speed applications, the SY87701L operates from 32-1250MHz.
2. X is a DON'T CARE.

DIVSEL1	DIVSEL2	f_{RCLK} / f_{REFCLK}
0	0	8
0	1	10
1	0	16
1	1	20

Table 1. M-Divider, f_{RCLK} / f_{REFCLK} Divider Setting

32-PIN APPLICATION EXAMPLE



Note: V_{EE} = —3.0V for 5.0V applications.
V_{EE} = —1.3V for 3.3V applications.
Low voltage parts have L designators.
The V designator is for 5.0V applications,
i.e., SY87700L = 3.3V, SY87700V = 5.0V.

Note:

C3, C4 are optional

C1 = C2 = 0.47µF
R1 = 820Ω
R2 = 1.2kΩ
R3 through R10 = 5kΩ
R12 = 12kΩ
R13 = 130Ω

BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1	Digi-Key PCC2147CT-ND	Panasonic(1)	0.47µF, size 0.603	1
C2	Digi-Key PCC2147CT-ND	Panasonic(1)	0.47µF, size 0.603	1
C3, C4	Optional			2
C5	Digi-Key PCC223BVCT-ND	Panasonic(1)	0.1µF, size 0.603	1
C6, C11, C13 C15, C17, C20	Digi-Key PCC1762CT-ND	Panasonic(1)	0.47µF, size 0.603	6
C7, C8, C9, C10	Digi-Key PCC1800CT-ND	Panasonic(1)	6.8µF, size 0.603	4
C12, C14, C16 C18, C21	Digi-Key PCC100CVCT-ND	Panasonic(1)	0.01µF, size 0.603	5
C19	Digi-Key PCC1787CT-ND	Panasonic(1)	1.0µF, size 0.603	1
R1	Digi-Key P825HCT-ND	Panasonic(1)	825Ω, size 0.603	1
R2	Digi-Key P1.21KHCT-ND	Panasonic(1)	1.21kΩ, size 0.603	1
R3 – R10	Digi-Key P5.11KHCT-ND	Panasonic(1)	5.11kΩ, size 0.603	8
R11	Digi-Key P1KHCT-ND	Panasonic(1)	1kΩ, size 0.603	1
R12	Digi-Key P12.1KHCT-ND	Panasonic(1)	12.1kΩ, size 0.603	1
R13	Digi-Key P130HCT-ND	Panasonic(1)	130Ω, size 0.603	1
U1	**SY87700/701**	**Micrel Semiconductor(2)**	**5V/3.3V 32–175Mbps AnyRate™ Clock and Data Recovery**	1

Note 1. Panasonic, tel: 714-373-7366, http://www.panasonic.com

Note 2. Micrel, tel: 408-944-0800, http://www.micrel.com

SPECIAL CONSIDERATIONS(1), (3)

θ_{JA} (°C/W) by Velocity (LFPM)

Package	0	200	500
28-Pin SOIC(2)	80	—	—
32-Pin EP-TQFP(3)	27.6	22.6	20.7

Note 1. Airflow of 500lfpm recommended for 28-pin SOIC.

Note 2. The 28-pin SOIC package is NOT recommended for new designs.

Note 3. Please use appropriate heat sink/thermal grease to insure device reliability.

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com