HB56G51232 Series

524,288-word × 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-
Rev. 0.0
Dec. 1, 1995

Description

The HB56G51232B/SB is a 512 k × 32 dynamic RAM module, mounted 4 pieces of 4-Mbit DRAM (HM514260CJ/CLJ) sealed in SOJ package. An outline of the HB56G51232B/SB is 72-pin single in-line package. Therefore, the HB56G51232B/SB makes high density mounting possible without surface mount technology. The HB56G51232B/SB provides common data inputs and outputs. Decoupling capacitors are mounted beside each SOJ.

Features

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: 70 ns/80 ns (max)
- Low power dissipation
  - Active mode: 1.6 W/1.4 W (max)
  - Standby mode: 42 mW (max)
    4.2 mW (max) (L version)
- Fast page mode capability
- 512 refresh cycle: 8 ms
  128 ms (L-version)
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

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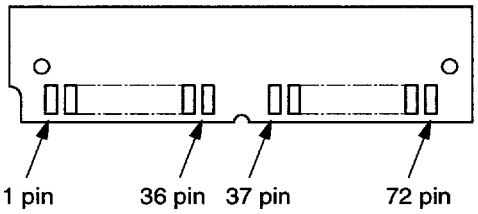
Ordering Information

Type No.	Access time	Package	Contact pad
HB56G51232B-7C/7CL	70 ns	72-pin SIP socket type	gold
HB56G51232B-8C/8CL	80 ns		
HB56G51232SB-7C/7CL	70 ns	72-pin SIP socket type	solder
HB56G51232SB-8C/8CL	80 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V_{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{RAS1}$	63	DQ14
10	V_{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{WE}$	65	DQ15
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	NC	50	DQ24	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ9	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V_{SS}

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Pin Description

Pin name	Function
A0 – A8	Address input
A0 – A8	Refresh address input
DQ0 – DQ31	Data-in/data-out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$ – $\overline{RAS3}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56G51232B/SB	
Pin No.	Pin name	70 ns	80 ns
67	PD1	NC	NC
68	PD2	V_{SS}	V_{SS}
69	PD3	V_{SS}	NC
70	PD4	NC	V_{SS}

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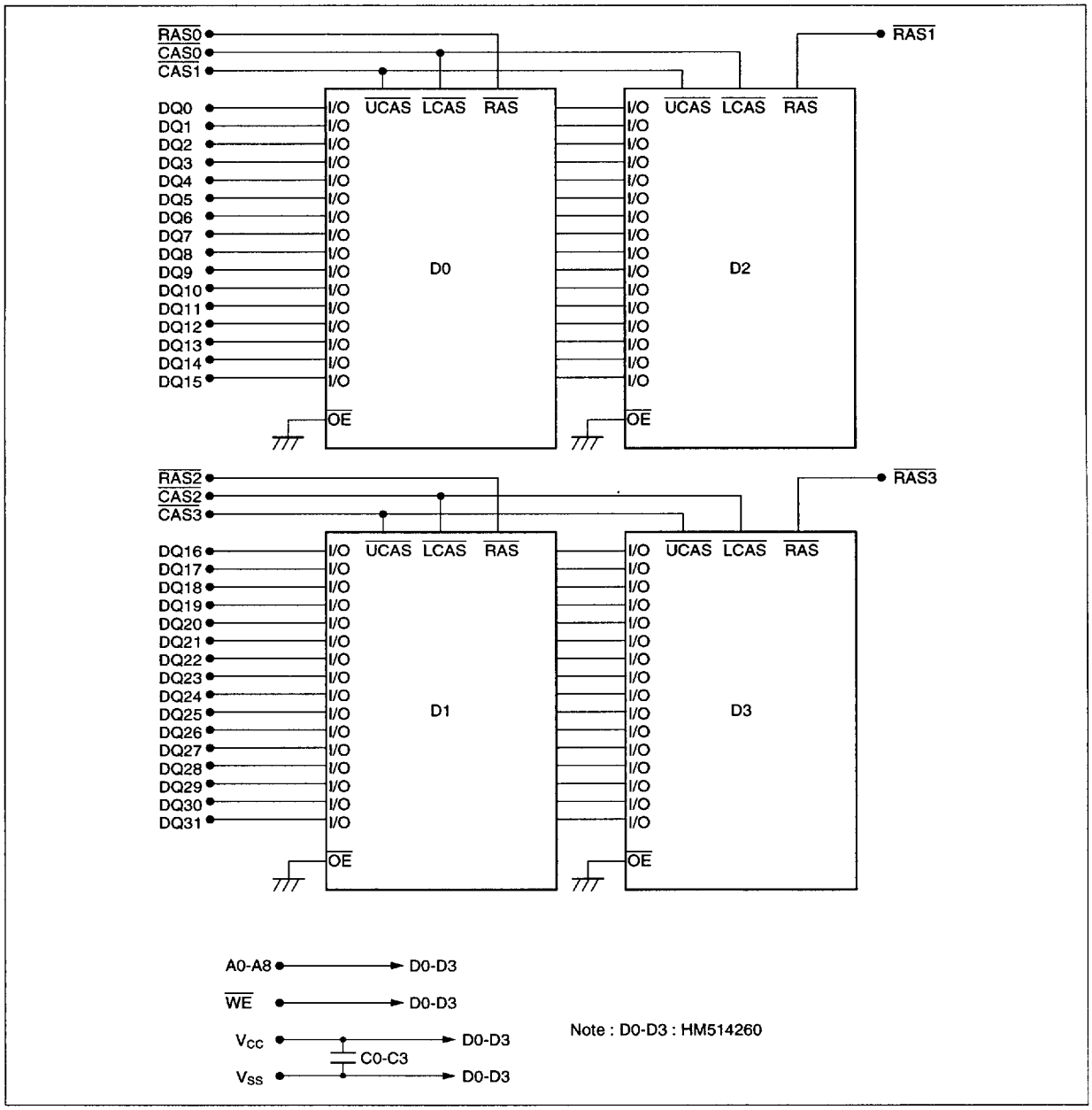
Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	2	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Condtions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	45	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	48	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	27	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	34	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	29	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56G51232B/SB						
		70ns		80ns				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	290	—	260	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	8	—	8	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	4	—	4	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	0.8	—	0.8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	270	—	230	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	20	—	20	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$-refresh current	I_{CC6}	—	270	—	230	mA	t_{RC} = min	2
Page mode current	I_{CC7}	—	270	—	250	mA	t_{PC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	1.2	—	1.2	mA	CMOS interface CBR refresh: t_{RC} = 250 µs, t_{RAS} ≤ 1 µs $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = High-Z	4
Input leakage current	I_{LI}	–10	10	–10	10	mA	0 V ≤ Vin ≤ 6.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	mA	0 V ≤ Vout ≤ 6.5 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 ≤ V_{IL} ≤ 0.2 V, Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

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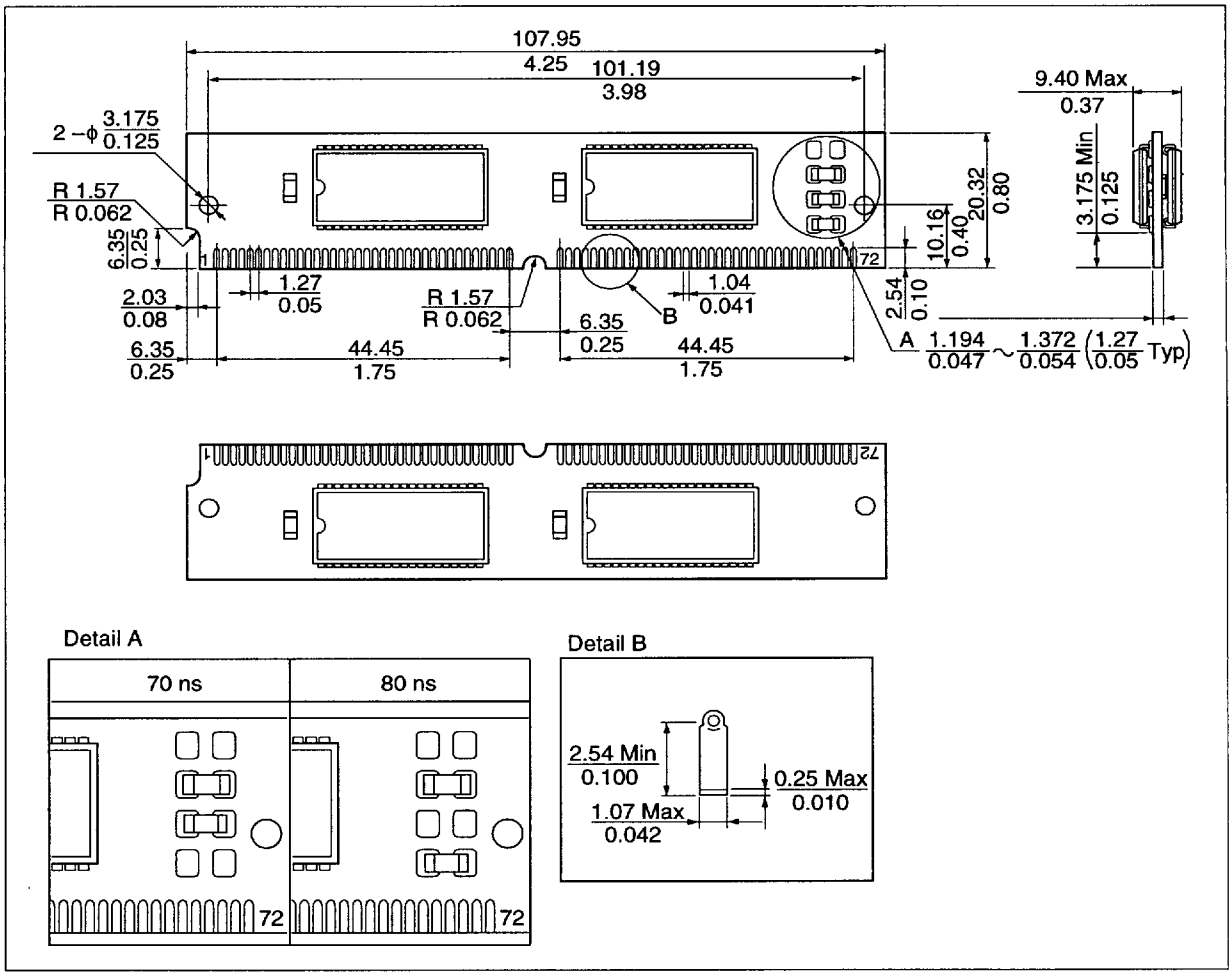
AC Characteristics

- Refer to the HM514260C data sheet.
- The HB56G51232 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
  Delayed write cycle is not available. ($\overline{OE}$ pin is fixed to V_{SS}).

Physical Outline

Unit: mm/inch



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