



MPC5604B/C

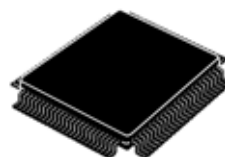
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MPC5604B/C Microcontroller Data Sheet

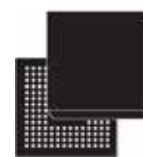
32-bit MCU family built on the Power Architecture™ for automotive body electronics applications

Features:

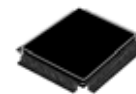
- Single issue, 32-bit CPU core complex (e200z0)
 - Compliant with the Power Architecture™ embedded category
 - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 512 Kbytes on-chip flash supported with the flash controller
- Up to 48 Kbytes on-chip SRAM
- Memory protection unit (MPU) with 8 region descriptors and 32-byte region granularity
- Interrupt controller (INTC) with 148 interrupt vectors, including 16 external interrupt sources and 18 external interrupt/wakeup sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- Boot assist module (BAM) supports internal flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS-lite)
- 10-bit analog-to-digital converter (ADC)
- 3 serial peripheral interface (DSPI) modules
- Up to 4 serial communication interface (LINFlex) modules
- Up to 6 enhanced full CAN (FlexCAN) modules with configurable buffers
- 1 inter IC communication interface (I²C) module
- Up to 123 configurable general purpose pins supporting input and output operations (package dependent)



208 MAPBGA
17 x 17 x 1.7 mm



144 LQFP
20 x 20 x 1.4mm



100 LQFP
14 x 14 x 1.4 mm

- Real Time Counter (RTC) with clock source from 128 kHz or 16 MHz internal RC oscillator supporting autonomous wakeup with 1 ms resolution with max timeout of 2 seconds
- Up to 6 periodic interrupt timers (PIT) with 32-bit counter resolution
- 1 System Module Timer (STM)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board boundary Scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

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1 General description

1.1 Introduction

The MPC5604B/C is a family of next generation microcontrollers built on the Power Architecture™ embedded category. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

The MPC5604B/C family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of the MPC5604B/C automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. MPC5604B/C Device Comparison¹

| Feature | Device | | | | | | | | | |
|---------------------------------|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------------------|------------------|
| | MPC560 2BxLL | MPC560 2BxLQ | MPC560 2CxLL | MPC560 3BxLL | MPC560 3BxLQ | MPC560 3CxLL | MPC560 4BxLL | MPC560 4BxLQ | MPC560 4BxMG | MPC560 4CxLL |
| CPU | e200z0h | | | | | | | | | |
| Execution speed ² | Static - 64 MHz | | | | | | | | | |
| Code Flash | 256 KB | | 256 KB | 384 KB | | 384 KB | 512 KB | | | 512 KB |
| Data Flash | 64 KB (4 × 16 KB) | | | | | | | | | |
| RAM | 24 KB | | 32 KB | 28 KB | | 40 KB | 32 KB | | 48 KB | 48 KB |
| MPU | 8-entry | | | | | | | | | |
| ADC | 28 ch, 10-bit | 36 ch, 10-bit | 28 ch, 10-bit | 28 ch, 10-bit | 36 ch, 10-bit | 28 ch, 10-bit | 28 ch, 10-bit | 36 ch, 10-bit | 36 ch, 10-bit | 28 ch, 10-bit |
| CTU | Yes | | | | | | | | | |
| Total timer I/O ³ | 28 ch, 16-bit | 56 ch, 16-bit | 28 ch, 16-bit | 28 ch, 16-bit | 56ch, 16-bit | 28 ch, 16-bit | 28 ch, 16-bit | 56 ch, 16-bit | 56 ch, 16-bit | 28 ch, 16-bit |
| eMIOS | | | | | | | | | | |
| • PWM + MC + IC/OC ⁴ | 5 ch | 10 ch | 5 ch | 5 ch | 10 ch | 5 ch | 5 ch | 10 ch | 10 ch | 5 ch |
| • PWM + IC/OC ⁴ | 20 ch | 40 ch | 20 ch | 20 ch | 40 ch | 20 ch | 20 ch | 40 ch | 40 ch | 20 ch |
| • IC/OC ⁴ | 3 ch | 6 ch | 3 ch | 3 ch | 6 ch | 3 ch | 3 ch | 6 ch | 6 ch | 3 ch |
| SCI (LINFlex) | 3 | | 4 | 4 | | 4 | 4 | | | 4 |
| SPI (DSPI) | 3 | | | | | | | | | |
| CAN (FlexCAN) | 2 | | 6 | 3 | | 6 | 3 | 3 | 6 | 6 |
| I ² C | 1 | | | | | | | | | |
| 32 kHz oscillator | Yes | | | | | | | | | |
| GPIO ⁵ | 79 | 123 | 79 | 79 | 123 | 79 | 79 | 123 | 123 | 79 |
| Debug | JTAG | | | | | | | | Nexus2+ | JTAG |
| Package | 100 LQFP | 144 LQFP | 100 LQFP | 100 LQFP | 144 LQFP | 100 LQFP | 100 LQFP | 144 LQFP | 208 MAP BGA ⁶ | 100 LQFP |

¹ Feature set dependent on selected peripheral multiplexing—table shows example implementation

² Based on 105 °C ambient operating temperature

³ Refer to eMIOS section of device reference manual for information on the channel configuration and functions

⁴ IC - Input Capture; OC - Output Compare; PWM - Pulse Width Modulation; MC - Modulus counter

⁵ I/O count based on multiplexing with peripherals

⁶ 208 MAPBGA available only as development package for Nexus2+

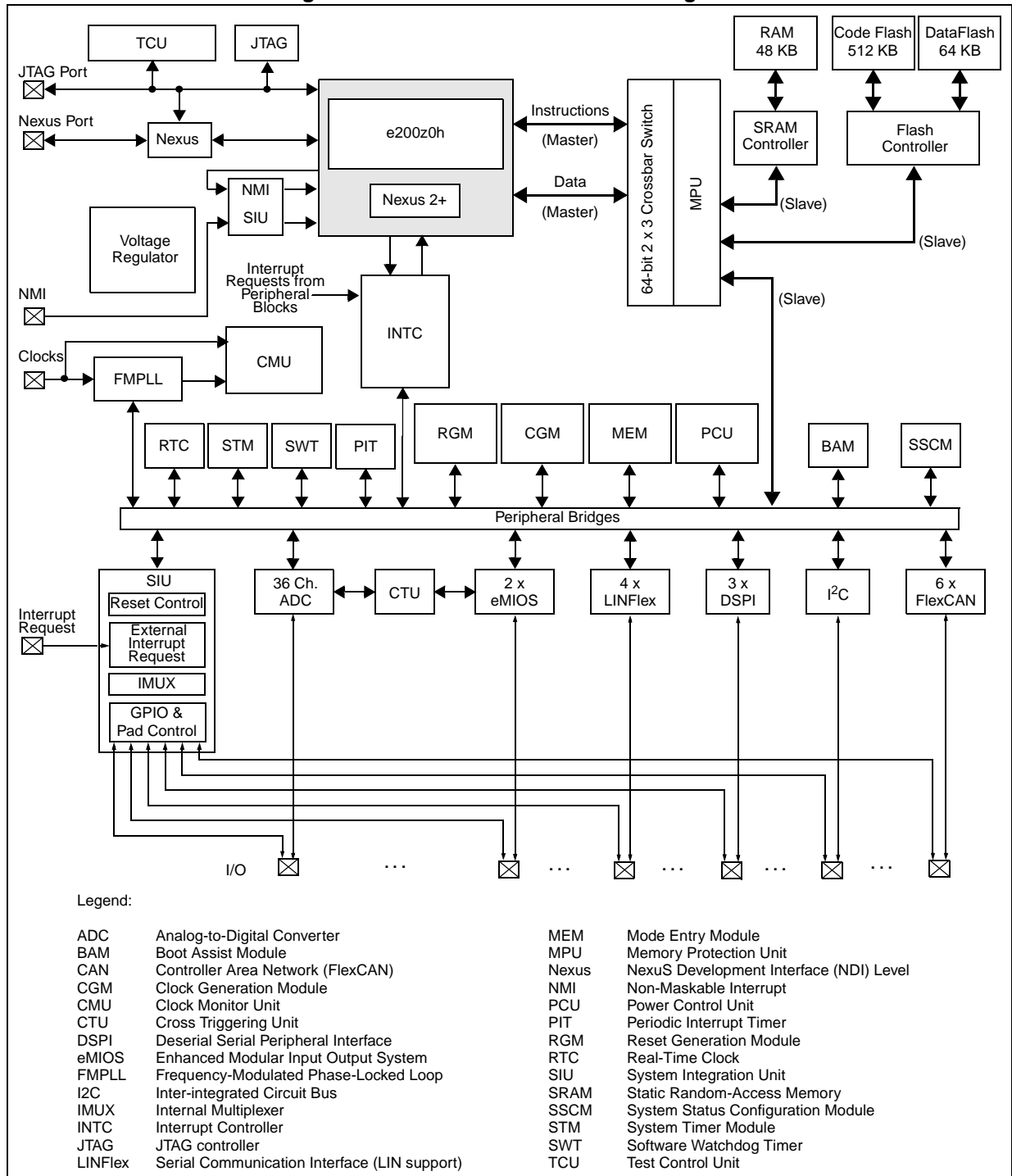
2 Device blocks

2.1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5604B/C device series.

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Figure 1. MPC5604B/C series block diagram



2.2 Device block summary

Table 2 summarizes the functions of all blocks present in the MPC5604B/C series of microcontrollers. Please note that the presence and number of blocks varies by device and package.

Table 2. MPC5604B/C series block summary

| Block | Function |
|--|--|
| Crossbar (XBAR) switch | Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width |
| Analog-to-digital converter (ADC) | Multi-channel, 10-bit analog-to digital-converter |
| Boot assist module (BAM) | A block of read-only memory containing VLE code which is executed according to the boot mode of the device |
| Clock generation module (CGM) | Provides logic and control required for the generation of system and peripheral clocks |
| Clock monitor unit (CMU) | Monitors clock source (internal and external) integrity |
| Cross triggering unit (CTU) | Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT |
| Deserial serial peripheral interface (DSPI) | Provides a synchronous serial interface for communication with external devices |
| Enhanced modular input output system (eMIOS) | Provides the functionality to generate or measure events |
| Flash memory | Provides non-volatile storage for program code, constants and variables |
| FlexCAN (controller area network) | Supports the standard CAN communications protocol |
| FMPLL (frequency-modulated phase-locked loop) | Generates high-speed system clocks and supports programmable frequency modulation |
| Internal multiplexer (IMUX) SIU subblock | Allows flexible mapping of peripheral interface on the different pins of the device |
| Inter-integrated circuit (I ² C™) bus | A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices |
| Interrupt controller (INTC) | Provides priority-based preemptive scheduling of interrupt requests |
| JTAG controller | Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode |
| LINflex controller | Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load |
| Memory protection unit (MPU) | Provides hardware access control for all memory references generated in a device |
| Mode entry module (MEM) | Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications |
| Non-Maskable Interrupt (NMI) | Handles external events that must produce an immediate response, such as power down detection |
| Nexus development interface (NDI) level | Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard |

Table 2. MPC5604B/C series block summary (continued)

| Block | Function |
|---|--|
| Periodic interrupt timer (PIT) | Produces periodic interrupts and triggers |
| Power control unit (PCU) | Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU |
| Real-time counter (RTC) | A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode) |
| Reset generation module (RGM) | Centralizes reset sources and manages the device reset sequence of the device |
| Static random-access memory (SRAM) | Provides storage for program code, constants, and variables |
| System integration unit (SIU) | Provides control over all the electrical pad controls and up to 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration |
| System status configuration module (SSCM) | Provides system configuration and status data (such as memory size and status, device mode and security status, DMA status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable |
| System timer module (STM) | Provides a set of output compare events to support AutoSAR and operating system tasks |
| System watchdog timer (SWT) | Provides protection from runaway code |
| Test control unit (TCU) | An extension of the JTAG controller module, the TCU provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. |

3 Package pinouts

The available LQFP pinouts and the 208 MAPBGA ballmap are provided in the following figures. For pin signal descriptions, please refer to the device reference manual.

Figure 2. LQFP 144-pin configuration (top view)

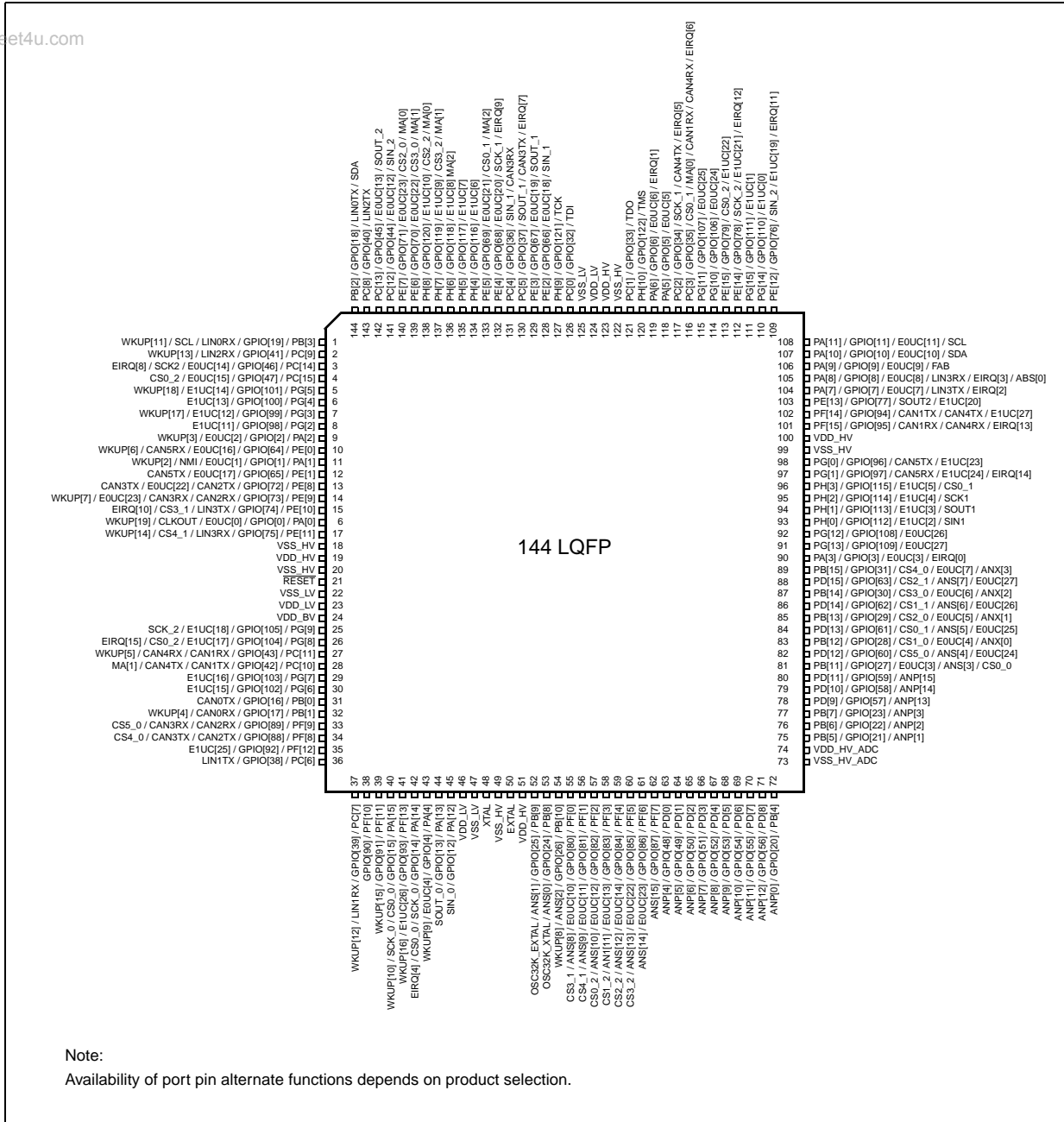


Figure 3. LQFP 100-pin configuration (top view)

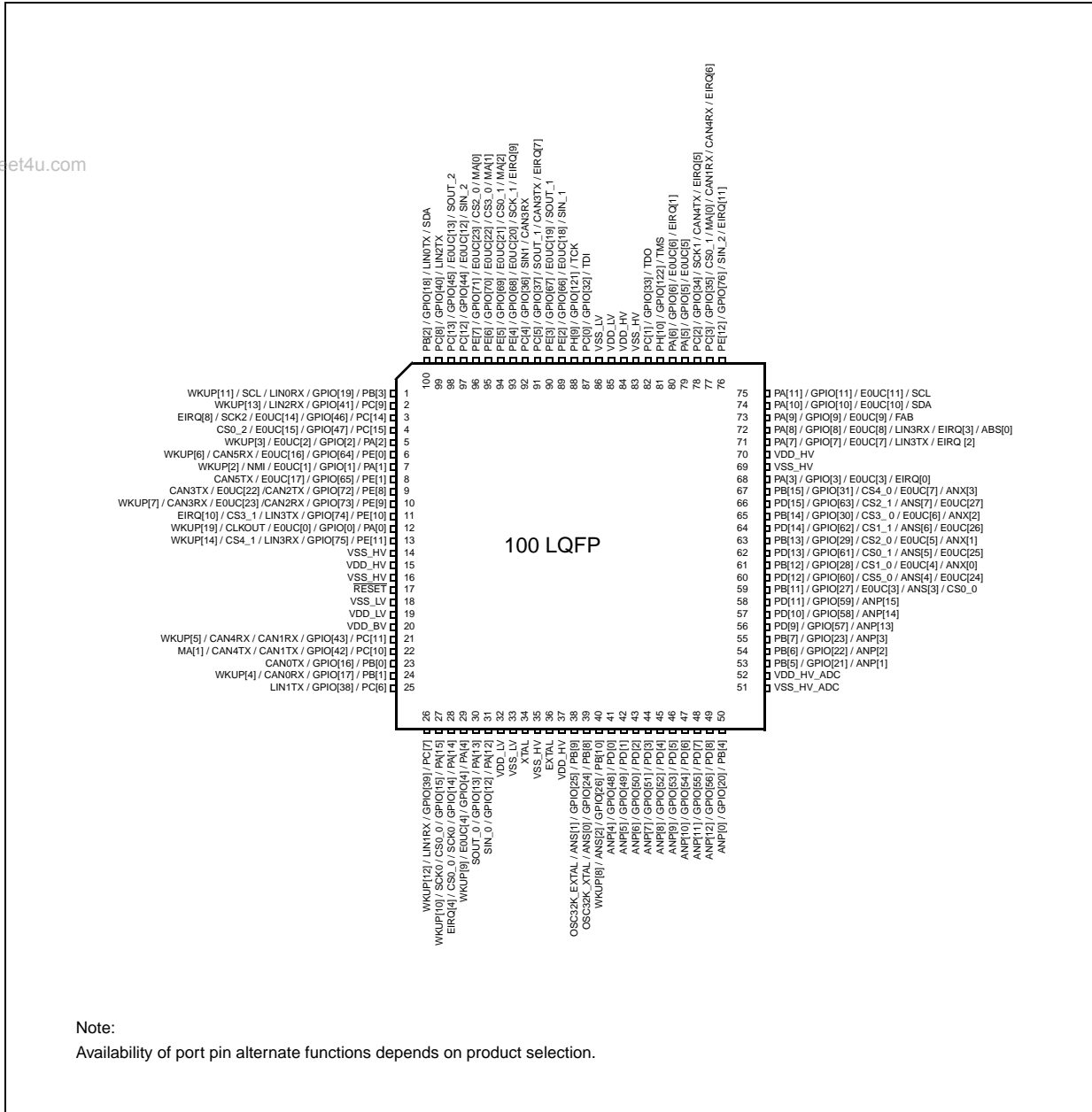


Figure 4. 208 MAPBGA configuration^{1,2}

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | | | | | | | | | | | | | | | | |
|---|--------|--------|--------|--------|--------|--------|--------|--------|--------------|-------|-------|--------|--------|------------|------------|--------|---|--|--|--|-------|-------|-------|-------|---|--|--|--|--------|----|----|------|---|
| A | PC[9] | PC[13] | NC | NC | PH[8] | PH[4] | PC[5] | PC[0] | NC | NC | PC[2] | NC | PE[15] | NC | NC | NC | A | | | | | | | | | | | | | | | | |
| B | PC[0] | PB[2] | NC | PC[12] | PE[6] | PH[5] | PC[4] | PH[9] | PH[10] | NC | PC[3] | PG[11] | PG[15] | PG[14] | PA[11] | PA[10] | B | | | | | | | | | | | | | | | | |
| C | PC[14] | VDD_HV | PB[3] | PE[7] | PH[7] | PE[5] | PE[3] | VSS_LV | PC[1] | NC | PA[5] | NC | PE[14] | PE[12] | PA[9] | PA[8] | C | | | | | | | | | | | | | | | | |
| D | NC | NC | PC[15] | NC | PH[6] | PE[4] | PC[2] | VDD_LV | VDD_HV | NC | PA[6] | NC | PG[10] | PF[14] | PE[13] | PA[7] | D | | | | | | | | | | | | | | | | |
| E | PG[4] | PG[5] | PG[3] | PG[2] | | | | | | | | | PG[1] | PG[0] | PF[15] | VDD_HV | E | | | | | | | | | | | | | | | | |
| F | PE[0] | PA[2] | PA[1] | PE[1] | | | | | | | | | | | | | | | | | PH[0] | PH[1] | PH[3] | PH[2] | F | | | | | | | | |
| G | PE[9] | PE[8] | PE[10] | PA[0] | | | | | | | | | | | | | | | | | | | | | | | | | VDD_HV | NC | NC | MSEO | G |
| H | NC | PE[11] | VDD_HV | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | RESET | VSS_LV | NC | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | EVTI | NC | VDD_BV | VDD_LV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | PG[9] | PG[10] | NC | EVTO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | PG[7] | PG[6] | PC[10] | PC[11] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | PB[1] | PF[9] | PB[0] | NC | NC | PA[4] | VSS_LV | EXTAL | VDD_HV | PF[3] | PF[4] | NC | | | | | | | | | | | | | | | | | | | | | |
| P | PF[8] | NC | PC[7] | NC | NC | PA[14] | VDD_LV | XTAL | PB[10] | PF[1] | PF[8] | PD[0] | PD[3] | VDD_HV_ADC | PB[6] | PB[7] | P | | | | | | | | | | | | | | | | |
| R | PF[12] | PC[8] | PF[10] | PF[11] | VDD_HV | PA[15] | PA[13] | NC | OSCS2K_XTAL | PF[3] | PF[7] | PD[2] | PD[4] | PD[7] | VSS_LV_ADC | PB[5] | R | | | | | | | | | | | | | | | | |
| T | NC | NC | NC | MCKO | NC | PF[13] | PA[12] | NC | OSCS2K_EXTAL | PF[2] | PF[6] | PD[1] | PD[5] | PD[6] | PD[8] | PB[4] | T | | | | | | | | | | | | | | | | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | | | | | | | | | | | | | | | | |

1. NC = Not connected

2. 208 MAPBGA available only as development package for Nexus2+

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

CAUTION

All of the following figures are indicative and must be confirmed during either silicon validation, silicon characterization or silicon reliability trial.

4.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 3 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter Classifications

| Classification tag | Tag description |
|--------------------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

4.3.1 NVUSRO[PAD3V5V] field description

Table 4 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 4. PAD3V5V field description¹

| Value ² | Description |
|--------------------|------------------------------|
| 0 | High voltage supply is 5.0 V |
| 1 | High voltage supply is 3.3 V |

¹ See the device reference manual for more information on the NVUSRO register.

² Default manufacturing value before Flash initialization is '1' (3.3 V)

The DC electrical characteristics are dependent on the PAD3V5V bit value.

4.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 5 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 5. OSCILLATOR_MARGIN field description¹

| Value ² | Description |
|--------------------|---|
| 0 | Low consumption configuration (4 MHz/8 MHz) |
| 1 | High margin configuration (4 MHz/16 MHz) |

¹ See the device reference manual for more information on the NVUSRO register.

² Default manufacturing value before Flash initialization is '1'

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

4.4 Absolute maximum ratings

Table 6. Absolute maximum ratings

| Symbol | Parameter | Conditions | Value | | Unit |
|---------------------|-----------|---|----------------------|----------------------|------|
| | | | Min | Max | |
| V _{SS} | SR | Digital ground on VSS_HV pins | 0 | 0 | V |
| V _{DD} | SR | Voltage on VDD_HV pins with respect to ground (V _{SS}) | -0.3 | 6.0 | V |
| V _{SS_LV} | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS}) | V _{SS} -0.1 | V _{SS} +0.1 | V |
| V _{DD_BV} | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground (V _{SS}) | -0.3 | 5.5 | V |
| | | Relative to V _{DD} | -0.3 | V _{DD} +0.3 | |
| V _{SS_ADC} | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS}) | V _{SS} -0.1 | V _{SS} +0.1 | V |
| V _{DD_ADC} | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS}) | -0.3 | 5.5 | V |
| | | Relative to V _{DD} | -0.3 | V _{DD} +0.3 | |
| V _{IN} | SR | Voltage on any GPIO pin with respect to ground (V _{SS}) | -0.3 | 5.5 | V |
| | | Relative to V _{DD} | -0.3 | V _{DD} +0.3 | |

Table 6. Absolute maximum ratings (continued)

| Symbol | | Parameter | Conditions | Value | | Unit |
|---------------|----|---|--|-------|-----|------|
| | | | | Min | Max | |
| I_{INJPAD} | SR | Injected input current on any pin during overload condition | | -10 | 10 | mA |
| I_{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | | -50 | 50 | |
| I_{AVGSEG} | SR | Sum of all the static I/O current within a supply segment | $V_{DD} = 5.0\text{ V} \pm 10\%$, PAD3V5V = 0 | | 70 | mA |
| | | | $V_{DD} = 3.3\text{ V} \pm 10\%$, PAD3V5V = 1 | | 64 | |
| $T_{STORAGE}$ | SR | Storage temperature | | -55 | 150 | °C |

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.5 Recommended operating conditions

Table 7. Recommended operating conditions (3.3 V)

| Symbol | | Parameter | Conditions | Value | | Unit |
|-----------------|----|---|----------------------|--------------|--------------|------|
| | | | | Min | Max | |
| V_{SS} | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| V_{DD}^1 | SR | Voltage on VDD_HV pins with respect to ground (V_{SS}) | | 3.0 | 3.6 | V |
| $V_{SS_LV}^2$ | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS}) | | $V_{SS}-0.1$ | $V_{SS}+0.1$ | V |
| $V_{DD_BV}^3$ | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS}) | | 3.0 | 3.6 | V |
| | | | Relative to V_{DD} | $V_{DD}-0.1$ | $V_{DD}+0.1$ | |
| V_{SS_ADC} | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS}) | | $V_{SS}-0.1$ | $V_{SS}+0.1$ | V |
| $V_{DD_ADC}^4$ | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS}) | | 3.0^5 | 3.6 | V |
| | | | Relative to V_{DD} | $V_{DD}-0.1$ | $V_{DD}+0.1$ | |
| V_{IN} | SR | Voltage on any GPIO pin with respect to ground (V_{SS}) | | $V_{SS}-0.1$ | — | V |
| | | | Relative to V_{DD} | — | $V_{DD}+0.1$ | |

Table 7. Recommended operating conditions (3.3 V) (continued)

| Symbol | | Parameter | Conditions | Value | | Unit |
|---------------------|----|---|---------------------------|-------|------|------|
| | | | | Min | Max | |
| I _{INJPAD} | SR | Injected input current on any pin during overload condition | | -5 | 5 | mA |
| I _{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | | -50 | 50 | |
| TV _{DD} | SR | V _{DD} slope to ensure correct power up ⁶ | | — | 0.25 | V/μs |
| | | | | 3 | — | V/s |
| T _A | SR | Ambient temperature under bias | f _{CPU} < 64 MHz | -40 | 125 | °C |
| T _J | SR | Junction temperature under bias | | -40 | 150 | |

- ¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair
- ² 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
- ³ 100 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
- ⁴ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
- ⁵ Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
- ⁶ Guaranteed by device validation

Table 8. Recommended operating conditions (5.0 V)

| Symbol | | Parameter | Conditions | Value | | Unit |
|----------------------------------|----|---|-----------------------------|----------------------|----------------------|------|
| | | | | Min | Max | |
| V _{SS} | SR | Digital ground on VSS_HV pins | | 0 | 0 | V |
| V _{DD} ¹ | SR | Voltage on VDD_HV pins with respect to ground (V _{SS}) | | 4.5 | 5.5 | V |
| | | | Voltage drop ² | 3.0 | 5.5 | |
| V _{SS_LV} ³ | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS}) | | V _{SS} -0.1 | V _{SS} +0.1 | V |
| V _{DD_BV} ⁴ | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground (V _{SS}) | | 4.5 | 5.5 | V |
| | | | Voltage drop ⁽²⁾ | 3.0 | 5.5 | |
| | | | Relative to V _{DD} | V _{DD} -0.1 | V _{DD} +0.1 | |
| V _{SS_ADC} | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS}) | | V _{SS} -0.1 | V _{SS} +0.1 | V |
| V _{DD_ADC} ⁵ | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS}) | | 4.5 | 5.5 | V |
| | | | Voltage drop ⁽²⁾ | 3.0 | 5.5 | |
| | | | Relative to V _{DD} | V _{DD} -0.1 | V _{DD} +0.1 | |
| V _{IN} | SR | Voltage on any GPIO pin with respect to ground (V _{SS}) | | V _{SS} -0.1 | — | V |
| | | | Relative to V _{DD} | — | V _{DD} +0.1 | |

Table 8. Recommended operating conditions (5.0 V) (continued)

| Symbol | | Parameter | Conditions | Value | | Unit |
|---------------------|----|---|---------------------------|-------|------|------|
| | | | | Min | Max | |
| I _{INJPAD} | SR | Injected input current on any pin during overload condition | | -5 | 5 | mA |
| I _{INJSUM} | SR | Absolute sum of all injected input currents during overload condition | | -50 | 50 | |
| TV _{DD} | SR | V _{DD} slope to ensure correct power up ⁶ | | — | 0.25 | V/μs |
| | | | | 3 | — | V/s |
| T _A | SR | Ambient temperature under bias | f _{CPU} < 60 MHz | -40 | 125 | °C |
| | | | f _{CPU} < 64 MHz | -40 | 105 | |
| T _J | SR | Junction temperature under bias | | -40 | 150 | |

- ¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
- ² Full device operation is guaranteed by design when the voltage drops below 4.5V down to 3.6V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.
- ³ 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
- ⁴ 100 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
- ⁵ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
- ⁶ Guaranteed by device validation

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.6 Thermal characteristics

4.6.1 Package thermal characteristics

Table 9. LQFP thermal characteristics¹

| Symbol | | C | Parameter | Conditions ² | Pin count | Value ³ | | | Unit |
|------------------|----|---|---|-------------------------|-----------|--------------------|-----|------|------|
| | | | | | | Min | Typ | Max | |
| R _{θJA} | CC | D | Thermal resistance, junction-to-ambient natural convection ⁴ | Single-layer board—1s | 100 | | | 64 | °C/W |
| | | | | | 144 | | | 64 | |
| | | | | Four-layer board—2s2p | 100 | | | 50.8 | |
| | | | | | 144 | | | 49.4 | |

- ¹ Thermal characteristics are targets based on simulation that are subject to change per device characterization.
- ² V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C.
- ³ All values need to be confirmed during device validation.
- ⁴ Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

Table 10. 208 MAPBGA thermal characteristics¹

| Symbol | C | Parameter | Conditions | Value | Unit |
|------------------|----|---|-----------------------|-------|------|
| R _{θJA} | CC | Thermal resistance, junction-to-ambient natural convection ² | Single-layer board—1s | TBD | °C/W |
| | | | Four-layer board—2s2p | | |

¹ Thermal characteristics are targets based on simulation that are subject to change per device characterization.

² Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

4.6.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \text{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

R_{θJA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and P_{I/O} (P_D = P_{INT} + P_{I/O}).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

P_{I/O} represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, P_{I/O} < P_{INT} and may be neglected. On the other hand, P_{I/O} may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if P_{I/O} is neglected) is given by:

$$P_D = K / (T_J + 273 \text{ °C}) \quad \text{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273 \text{ °C}) + R_{\theta JA} \times P_D^2 \quad \text{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

4.7 I/O pad electrical characteristics

4.7.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. There are used for improved Nexus debugging capability.

- Input only pads—These pads are associated to ADC channels and 32 kHz slow external crystal oscillator providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

4.7.2 I/O input DC characteristics

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Table 11 provides input DC electrical characteristics as described in Figure 5.

Figure 5. I/O input DC electrical characteristics definition

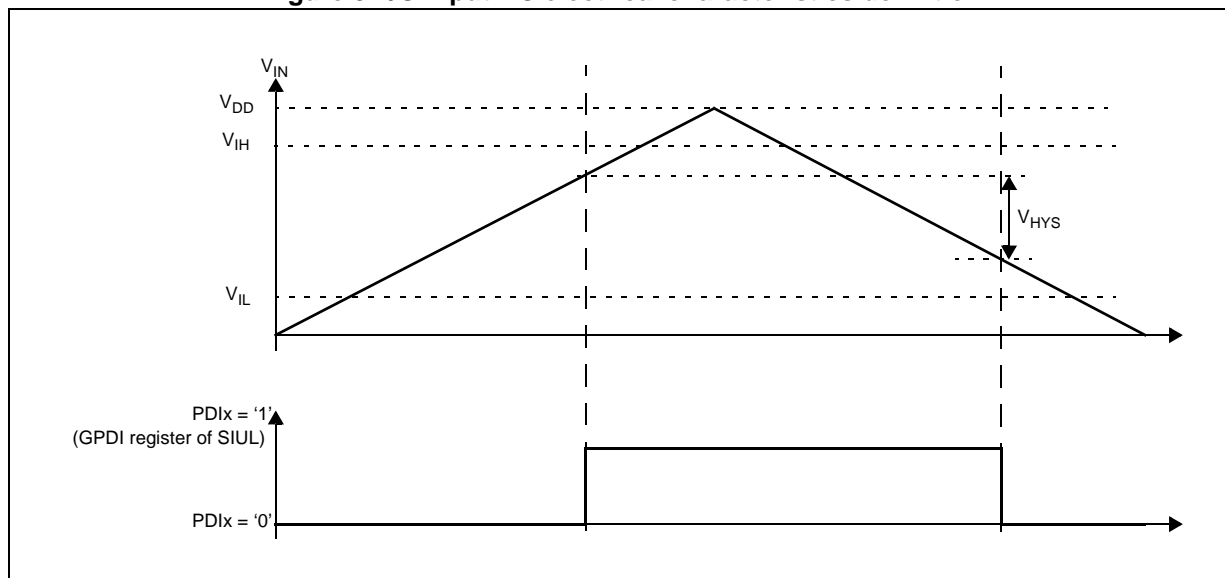


Table 11. I/O input DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit |
|------------------|----|-----------|---|-------------------------|-----|----------------------|------|
| | | | | Min | Typ | Max | |
| V _{IH} | SR | P | Input high level CMOS (Schmitt Trigger) | 0.65V _{DD} | | V _{DD} +0.4 | V |
| V _{IL} | SR | P | Input low level CMOS (Schmitt Trigger) | -0.4 | | 0.35V _{DD} | |
| V _{HYS} | CC | C | Input hysteresis CMOS (Schmitt Trigger) | 0.1V _{DD} | | | |
| I _{LKG} | CC | P | Digital input leakage No injection on adjacent pin | T _A = -40 °C | 2 | — | nA |
| | | | | T _A = 25 °C | 2 | — | |
| | | | | T _A = 105 °C | 12 | 500 | |
| | | | | T _A = 125 °C | 70 | 1000 | |
| W _{FI} | SR | P | Digital input filtered pulse | | | 40 | ns |
| W _{NFI} | SR | P | Digital input not filtered pulse | 1000 | | | ns |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² All values need to be confirmed during device validation.

4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 12 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 13 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 14 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 15 provides output driver characteristics for I/O pads when in FAST configuration.

Table 12. I/O pull-up/pull-down DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|------------------|----|-----------|---------------------------------------|--|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| I _{WPU} | CC | P | Weak pull-up current absolute value | V _{IN} = V _{IL} , V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 10 | | 150 | μA |
| | | | | PAD3V5V = 1 ² | 10 | | 250 | |
| | | | | V _{IN} = V _{IL} , V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | 10 | | 150 | |
| I _{WPD} | CC | P | Weak pull-down current absolute value | V _{IN} = V _{IH} , V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 10 | | 150 | μA |
| | | | | PAD3V5V = 1 | 10 | | 250 | |
| | | | | V _{IN} = V _{IH} , V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | 10 | | 150 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 13. SLOW configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-----------------|----|-----------|--------------------------------------|-----------|---|----------------------|------|--------------------|---|
| | | | | Min | Typ | Max | | | |
| V _{OH} | CC | P | Output high level SLOW configuration | Push Pull | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | | | V |
| | | | | | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | | | |
| | | | | | I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} -0.8 | | | |
| V _{OL} | CC | P | Output low level SLOW configuration | Push Pull | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | | | 0.1V _{DD} | V |
| | | | | | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽²⁾ | | | 0.1V _{DD} | |
| | | | | | I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | | | 0.5 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 14. MEDIUM configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-----------------|----|-----------|--|-----------|--|----------------------|------|--------------------|---|
| | | | | Min | Typ | Max | | | |
| V _{OH} | CC | C | Output high level MEDIUM configuration | Push Pull | I _{OH} = -3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 0.8V _{DD} | | | V |
| | | | | | I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | | | |
| | | | | | I _{OH} = -1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | | | |
| | | | | | I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} -0.8 | | | |
| | | | | | I _{OH} = -100 μA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 0.8V _{DD} | | | |
| V _{OL} | CC | C | Output low level MEDIUM configuration | Push Pull | I _{OL} = 3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 0.2V _{DD} | V |
| | | | | | I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | | | 0.1V _{DD} | |
| | | | | | I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽²⁾ | | | 0.1V _{DD} | |
| | | | | | I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | | | 0.5 | |
| | | | | | I _{OH} = 100 μA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 0.1V _{DD} | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 15. FAST configuration output buffer electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|-----------------|----|-----------|--------------------------------------|-----------|--|----------------------|------|--|---|
| | | | | Min | Typ | Max | | | |
| V _{OH} | CC | P | Output high level FAST configuration | Push Pull | I _{OH} = -14mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8V _{DD} | | | V |
| | | | | | I _{OH} = -7mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ² | 0.8V _{DD} | | | |
| | | | | | I _{OH} = -11mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | V _{DD} -0.8 | | | |

Table 15. FAST configuration output buffer electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|-----------------|----|---|-------------------------|--|-----|-----|--------------------|---|
| | | | | Min | Typ | Max | | |
| V _{OL} | CC | P Output low level FAST configuration | Push Pull | I _{OL} = 14mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | | | 0.1V _{DD} | V |
| | | | | I _{OL} = 7mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽²⁾ | | | 0.1V _{DD} | |
| | | | | I _{OL} = 11mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | | | 0.5 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.7.4 Output pin transition times

Table 16. Output pin transition times

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit | |
|-----------------|----|---|-------------------------|---|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| T _{tr} | CC | D Output transition time output pin ³ SLOW configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 50 | ns |
| | | | C _L = 50 pF | | | | 100 | |
| | | | C _L = 100 pF | | | | 125 | |
| | | | C _L = 25 pF | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | | 50 | |
| | | | C _L = 50 pF | | | | 100 | |
| | | | C _L = 100 pF | | | | 125 | |
| | | | C _L = 100 pF | | | | 125 | |
| T _{tr} | CC | D Output transition time output pin ⁽³⁾ MEDIUM configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 10 | ns |
| | | | C _L = 50 pF | | | | 20 | |
| | | | C _L = 100 pF | | | | 40 | |
| | | | C _L = 25 pF | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | | 12 | |
| | | | C _L = 50 pF | | | | 25 | |
| | | | C _L = 100 pF | | | | 40 | |
| | | | C _L = 100 pF | | | | 40 | |
| T _{tr} | CC | D Output transition time output pin ⁽³⁾ FAST configuration | C _L = 25 pF | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 4 | ns |
| | | | C _L = 50 pF | | | | 6 | |
| | | | C _L = 100 pF | | | | 12 | |
| | | | C _L = 25 pF | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | | 4 | |
| | | | C _L = 50 pF | | | | 7 | |
| | | | C _L = 100 pF | | | | 12 | |
| | | | C _L = 100 pF | | | | 12 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

- ² All values need to be confirmed during device validation.
³ C_L includes device and package capacitances ($C_{PKG} < 5$ pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 17.

Table 18 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 17. I/O supply segment

| Package | Supply segment | | | | | |
|-------------------------|---|-------------|---------------|---------------|------|------------------------|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| 208 MAPBGA ¹ | Equivalent to 144 LQFP segment pad distribution | | | | MCKO | MDO _n /MSEO |
| 144 LQFP | pin20–pin49 | pin51–pin99 | pin100–pin122 | pin 123–pin19 | | |
| 100 LQFP | pin16–pin35 | pin37–pin69 | pin70–pin83 | pin 84–pin15 | | |

¹ 208 MAPBGA available only as development package for Nexus2+

Table 18. I/O consumption

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit | | |
|-----------------------------|----|-----------|---|---|---|---|------|-----|----|
| | | | | Min | Typ | Max | | | |
| I_{DYNSEG} | SR | D | Sum of all the dynamic and static I/O current within a supply segment | $V_{DD} = 5.0$ V \pm 10%, PAD3V5V = 0 | | | 110 | mA | |
| | | | | | $V_{DD} = 3.3$ V \pm 10%, PAD3V5V = 1 | | | | 65 |
| I_{SWTSLW} ³ | CC | D | Dynamic I/O current for SLOW configuration | $C_L = 25$ pF | $V_{DD} = 5.0$ V \pm 10%, PAD3V5V = 0 | | | 20 | mA |
| | | | | | | $V_{DD} = 3.3$ V \pm 10%, PAD3V5V = 1 | | | |
| I_{SWTMED} ⁽³⁾ | CC | D | Dynamic I/O current for MEDIUM configuration | $C_L = 25$ pF | $V_{DD} = 5.0$ V \pm 10%, PAD3V5V = 0 | | | 29 | mA |
| | | | | | | $V_{DD} = 3.3$ V \pm 10%, PAD3V5V = 1 | | | |
| I_{SWTFST} ⁽³⁾ | CC | D | Dynamic I/O current for FAST configuration | $C_L = 25$ pF | $V_{DD} = 5.0$ V \pm 10%, PAD3V5V = 0 | | | 110 | mA |
| | | | | | | $V_{DD} = 3.3$ V \pm 10%, PAD3V5V = 1 | | | |

Table 18. I/O consumption (continued)

| Symbol | C | Parameter | Conditions ¹ | | Value ² | | | Unit | |
|---------------------|----|-----------|---|--|---|-----|-----|------|----|
| | | | | | Min | Typ | Max | | |
| I _{RMSLW} | CC | D | Root medium square I/O current for SLOW configuration | C _L = 25 pF, 2 MHz | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 2.3 | mA |
| | | | | C _L = 25 pF, 4 MHz | | | | 3.2 | |
| | | | | C _L = 100 pF, 2 MHz | | | | 6.6 | |
| | | | | C _L = 25 pF, 2 MHz | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | | 1.6 | |
| | | | | C _L = 25 pF, 4 MHz | | | | 2.3 | |
| | | | | C _L = 100 pF, 2 MHz | | | | 4.7 | |
| I _{RMSMED} | CC | D | Root medium square I/O current for MEDIUM configuration | C _L = 25 pF, 13 MHz | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 6.6 | mA |
| | | | | C _L = 25 pF, 40 MHz | | | | 13.4 | |
| | | | | C _L = 100 pF, 13 MHz | | | | 18.3 | |
| | | | | C _L = 25 pF, 13 MHz | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | | 5 | |
| | | | | C _L = 25 pF, 40 MHz | | | | 8.5 | |
| | | | | C _L = 100 pF, 13 MHz | | | | 11 | |
| I _{RMSFST} | CC | D | Root medium square I/O current for FAST configuration | C _L = 25 pF, 40 MHz | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | 22 | mA |
| | | | | C _L = 25 pF, 64 MHz | | | | 33 | |
| | | | | C _L = 100 pF, 40 MHz | | | | 56 | |
| | | | | C _L = 25 pF, 40 MHz | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | | 14 | |
| | | | | C _L = 25 pF, 64 MHz | | | | 20 | |
| | | | | C _L = 100 pF, 40 MHz | | | | 35 | |
| I _{AVGSEG} | SR | D | Sum of all the static I/O current within a supply segment | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | | | 70 | mA |
| | | | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | | | 65 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² All values need to be confirmed during device validation.

³ Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

4.8 $\overline{\text{nRSTIN}}$ electrical characteristics

The device implements a dedicated bidirectional RESET pin.

Figure 6. Start-up reset requirements

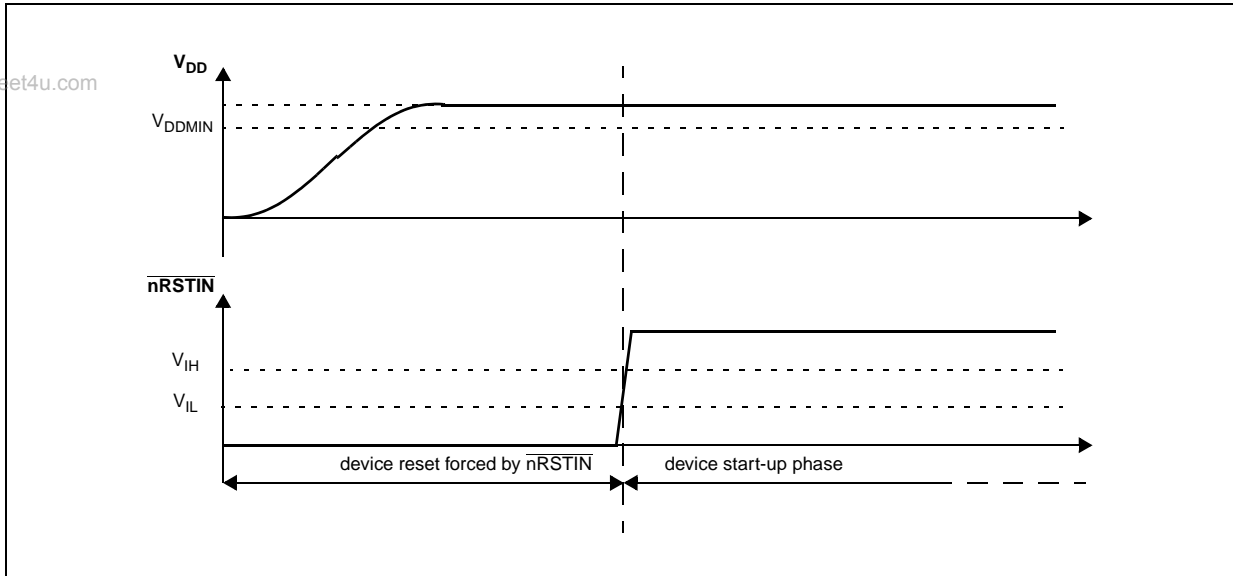


Figure 7. Noise filtering on reset signal

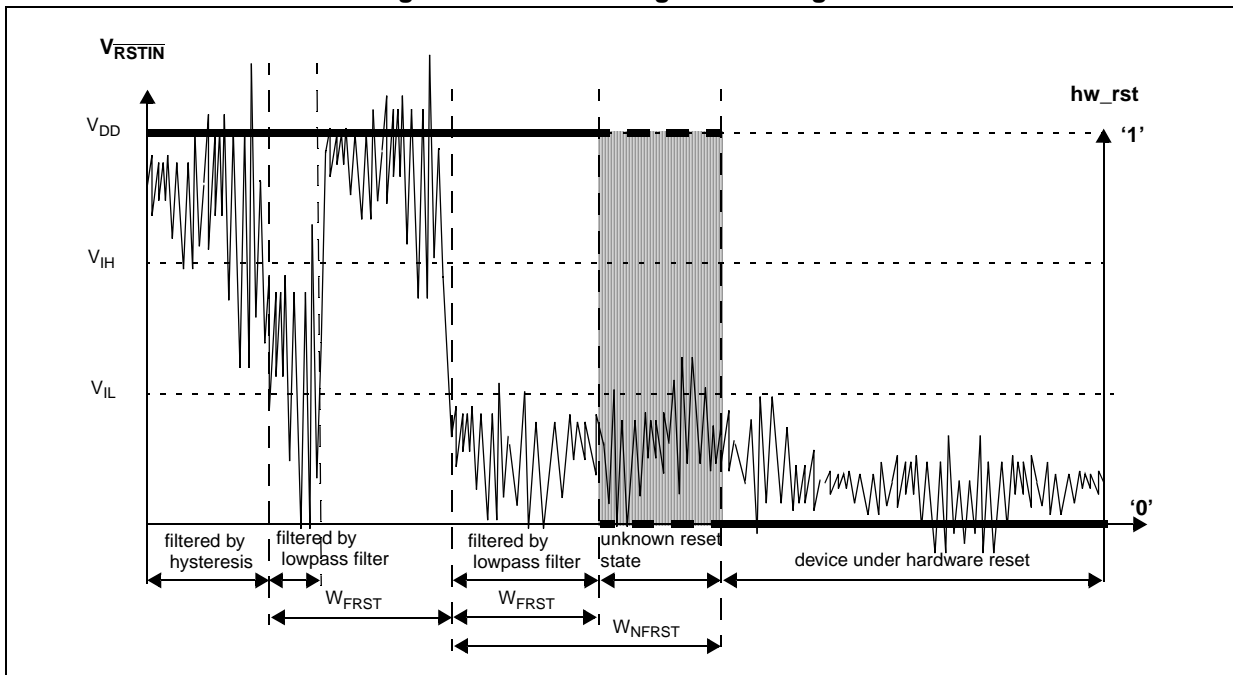


Table 19. Reset electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit |
|--------------------|----|-----------|--|--|-----|----------------------|------|
| | | | | Min | Typ | Max | |
| V _{IH} | SR | P | Input High Level CMOS (Schmitt Trigger) | 0.65V _{DD} | | V _{DD} +0.4 | V |
| V _{IL} | SR | P | Input low Level CMOS (Schmitt Trigger) | -0.4 | | 0.35V _{DD} | V |
| V _{HYS} | CC | C | Input hysteresis CMOS (Schmitt Trigger) | 0.1V _{DD} | | | V |
| V _{OL} | CC | P | Output low level | Push Pull, I _{OL} = 2mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | | 0.1V _{DD} | V |
| | | | | Push Pull, I _{OL} = 1mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ³ | | 0.1V _{DD} | |
| | | | | Push Pull, I _{OL} = 1mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | | 0.5 | |
| T _{tr} | CC | D | Output transition time output pin ⁴ MEDIUM configuration | C _L = 25pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | 10 | ns |
| | | | | C _L = 50pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | 20 | |
| | | | | C _L = 100pF, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | | 40 | |
| | | | | C _L = 25pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | 12 | |
| | | | | C _L = 50pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | 25 | |
| | | | | C _L = 100pF, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | | 40 | |
| W _{FRST} | SR | P | $\overline{\text{nRSTIN}}$ input filtered pulse | | | 40 | ns |
| W _{NFRST} | SR | P | $\overline{\text{nRSTIN}}$ input not filtered pulse | 1000 | | | ns |
| I _{WPUL} | CC | P | Weak pull-up current absolute value | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 | 10 | 150 | μA |
| | | | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 | 10 | 150 | |
| | | | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁵ | 10 | 250 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² All values need to be confirmed during device validation.

³ This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).

⁴ C_L includes device and package capacitance (C_{PKG} < 5 pF).

⁵ The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

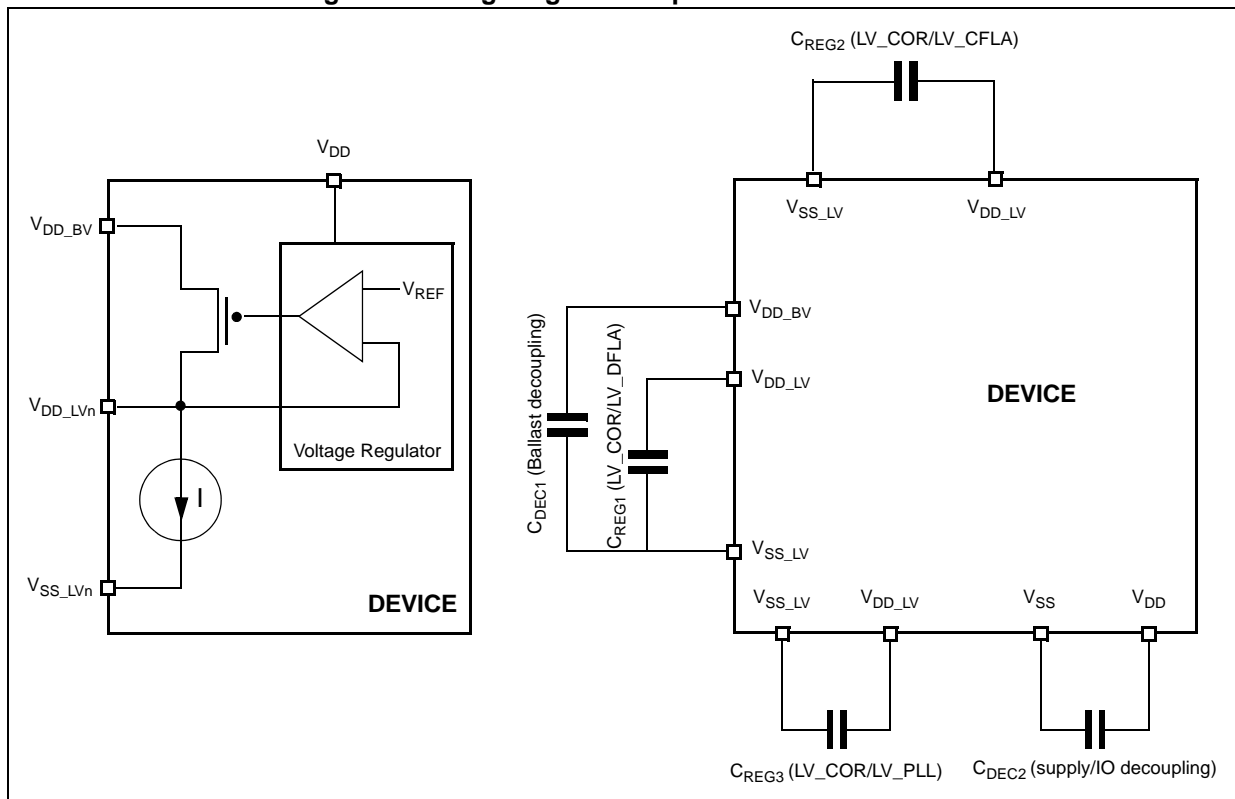
4.9 Power management electrical characteristics

4.9.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV} . The regulator itself is supplied by the common I/O supply V_{DD} . The following supplies are involved:

- HV—High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV—High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD} .
- LV—Low voltage internal power supply for core, FMPLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
 - LV_COR—Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
 - LV_CFLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_DFLA—Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_PLL—Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

Figure 8. Voltage regulator capacitance connection



The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see Section 4.5, “Recommended operating conditions”).

Table 20. Voltage regulator electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit | |
|-----------------|----|-----------|---|---------------------------------------|-----|------------------|------|-----|
| | | | | Min | Typ | Max | | |
| C_{REGn} | SR | — | Internal voltage regulator external capacitance | 200 | | 330 | nF | |
| R_{REG} | SR | — | Stability capacitor equivalent serial resistance | | | 0.2 | W | |
| C_{DEC1} | SR | — | Decoupling capacitance ³ ballast | V_{DD_BV}/V_{SS_LV} pair | 100 | 470 ⁴ | nF | |
| C_{DEC2} | SR | — | Decoupling capacitance regulator supply | V_{DD}/V_{SS} pair | 10 | 100 | nF | |
| V_{MREG} | CC | P | Main regulator output voltage | Before trimming | | 1.32 | V | |
| | | | | After trimming | | 1.28 | | |
| I_{MREG} | SR | — | Main regulator current provided to V_{DD_LV} domain | | | 200 | mA | |
| $I_{MREGINT}$ | CC | D | Main regulator module current consumption | $I_{MREG} = 200$ mA | | 2 | mA | |
| | | | | $I_{MREG} = 0$ mA | | 1 | | |
| V_{LPREG} | CC | P | Low power regulator output voltage | After trimming | | 1.23 | V | |
| I_{LPREG} | SR | — | Low power regulator current provided to V_{DD_LV} domain | | | 15 | mA | |
| $I_{LPREGINT}$ | CC | D | Low power regulator module current consumption | $I_{LPREG} = 15$ mA; $T_A = 55$ °C | | 600 | μA | |
| | | | | $I_{LPREG} = 0$ mA; $T_A = 55$ °C | | 5 | | TBD |
| V_{ULPREG} | CC | P | Ultra low power regulator output voltage | Post trimming | | 1.23 | V | |
| I_{ULPREG} | SR | — | Ultra low power regulator current provided to V_{DD_LV} domain | | | 5 | mA | |
| $I_{ULPREGINT}$ | CC | D | Ultra low power regulator module current consumption | $I_{ULPREG} = 5$ mA; $T_A = 55$ °C | | 100 | μA | |
| | | | | $I_{ULPREG} = 0$ mA; $T_A = 55$ °C | | 2 | | TBD |
| $I_{VREGREF}$ | CC | D | Main LVDs and reference current consumption (low power and main regulator switched off) | $T_A = 55$ °C | | 17 | μA | |
| $I_{VREDLVD12}$ | CC | D | Main LVD current consumption (switch-off during standby) | $T_A = 55$ °C | | 2 | TBD | μA |
| I_{DD_BV} | CC | D | In-rush current on V_{DD_BV} during power-up | | | 400 | mA | |

¹ $V_{DD} = 3.3$ V \pm 10% / 5.0 V \pm 10%, $T_A = -40$ to 125 °C, unless otherwise specified

² All values need to be confirmed during device validation.

- ³ This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
- ⁴ External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

4.9.2 Voltage monitor electrical characteristics

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The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the $5.0\text{ V} \pm 10\%$ range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVD_DIGBKP.

Figure 9. Low voltage monitor vs. reset

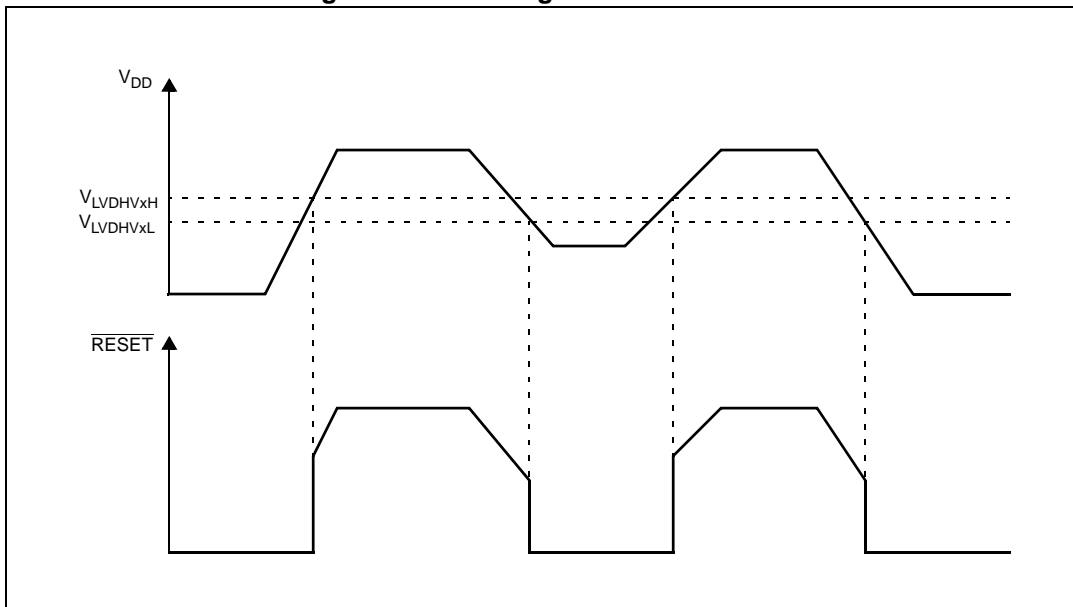


Table 21. Low voltage monitor electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit | |
|------------------------|----|-----------|---|---|------|-----|------|------|
| | | | | Min | Typ | Max | | |
| V _{PORUP} | SR | P | T _A = 25 °C, after trimming | 1.0 | | 5.5 | V | |
| V _{PORH} | CC | P | | Power-on reset threshold | 1.5 | | | 2.6 |
| V _{LVDHV3H} | CC | T | | LVDHV3 low voltage detector high threshold | | | | 2.9 |
| V _{LVDHV3L} | CC | P | | LVDHV3 low voltage detector low threshold | 2.7 | | | |
| V _{LVDHV5H} | CC | T | | LVDHV5 low voltage detector high threshold | | | | 4.4 |
| V _{LVDHV5L} | CC | P | | LVDHV5 low voltage detector low threshold | 3.8 | | | |
| V _{LVDLVCORL} | CC | P | | LVDLVCOR low voltage detector low threshold | 1.07 | | | 1.11 |
| V _{LVDLVBKPL} | CC | P | | LVDLVBKP low voltage detector low threshold | 1.07 | | | 1.11 |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² All values need to be confirmed during device validation.

4.10 Low voltage domain power consumption

Table 22 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 22. Low voltage power domain electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | | |
|---------------------------------|----|-----------|-------------------------|---|-------------------------|-----|------|----|--|
| | | | | Min | Typ | Max | | | |
| I _{DDMAX} | SR | — | Maximum current | | | 150 | mA | | |
| I _{DDRUN} ² | CC | P | RUN mode current | | 80 | | mA | | |
| I _{DDHALT} | CC | P | HALT mode current | | 20 | | mA | | |
| I _{DDSTOP} | CC | P | STOP mode current | Slow internal RC oscillator (128 kHz) running | T _A = 25 °C | 180 | 700 | μA | |
| | | | | | T _A = 55 °C | | TBD | | |
| | | | | | T _A = 85 °C | | | | |
| | | | | | T _A = 105 °C | | | | |
| | | | | | T _A = 125 °C | | | | |
| I _{DDSTBY2} | CC | P | STANDBY2 mode current | Slow internal RC oscillator (128 kHz) running | T _A = 25 °C | 30 | 100 | μA | |
| | | | | | T _A = 55 °C | | TBD | | |
| | | | | | T _A = 85 °C | | | | |
| | | | | | T _A = 105 °C | | | | |
| | | | | | T _A = 125 °C | | | | |

Table 22. Low voltage power domain electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|-----------------------|----|-----------|---|-------------------------|-----|-----|------|
| | | | | Min | Typ | Max | |
| I _{DDSTDBY1} | CC | T | STANDBY1 mode current Slow internal RC oscillator (128 kHz) running | T _A = 25 °C | 20 | 60 | μA |
| | | | | T _A = 55 °C | TBD | | |
| | | | | T _A = 85 °C | | | |
| | | | | T _A = 105 °C | | | |
| | | | | T _A = 125 °C | | | |
| | | D | | | | | |
| | | T | | | | | |
| | | D | | | | | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is **highly** dependent on the application. The given value is thought to be a **worst case value** with all peripherals running, and code fetched from flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

4.11 Flash memory electrical characteristics

4.11.1 Program/Erase characteristics

Table 23 shows the program and erase characteristics.

Table 23. Program and erase specifications

| Symbol | C | Parameter | Value | | | | Unit | |
|--------------------------|----|-----------|---|------------------|--------------------------|------------------|------|----|
| | | | Min | Typ ¹ | Initial max ² | Max ³ | | |
| T _{dwprogram} | CC | C | Double word (64 bits) program time ⁴ | — | 22 | TBD | 500 | μs |
| T _{16Kpperase} | | | 16 KB block pre-program and erase time | — | 300 | 500 | 5000 | ms |
| T _{32Kpperase} | | | 32 KB block pre-program and erase time | — | 400 | 600 | 5000 | ms |
| T _{128Kpperase} | | | 128 KB block pre-program and erase time | — | 800 | 1300 | 7500 | ms |

¹ Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

² Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

³ The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

⁴ Actual hardware programming times. This does not include software overhead.

Table 24. Flash module life

| Symbol | C | Parameter | Conditions | Value | | Unit | |
|-----------|----|-----------|--|--------------------------------|---------|------------------------|--------|
| | | | | Min | Typ | | |
| P/E | CC | C | Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T _J) | — | 100,000 | — | cycles |
| P/E | CC | C | Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T _J) | — | 10,000 | 100,000 ¹ | cycles |
| P/E | CC | C | Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T _J) | — | 1,000 | 100,000 ⁽¹⁾ | cycles |
| Retention | CC | C | Minimum data retention at 85 °C average ambient temperature ² | Blocks with 0–1,000 P/E cycles | 20 | — | years |
| | | | Blocks with 10,000 P/E cycles | 10 | — | years | |
| | | | Blocks with 100,000 P/E cycles | 1–5 ⁽¹⁾ | — | years | |

¹ To be confirmed

² Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 25. Flash read access timing

| Symbol | C | Parameter | Conditions ¹ | Max | Unit | |
|-------------------|----|-----------|-------------------------------------|---------------|------|-----|
| f _{READ} | CC | P | Maximum frequency for Flash reading | 2 wait states | 64 | MHz |
| | | | | 1 wait state | 40 | |
| | | | | 0 wait states | 20 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.11.2 Flash power supply DC characteristics

Table 26 shows the power supply DC characteristics on external supply.

Table 26. Flash power supply DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit | |
|--------------------|----|-----------|--|--|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| I _{FREAD} | CC | D | Sum of the current consumption on V _{DDHV} and V _{DDBV} on read access | Flash module read f _{CPU} = 64 MHz ³ | | | 33 | mA |
| I _{FMOD} | CC | D | Sum of the current consumption on V _{DDHV} and V _{DDBV} on matrix modification (program/erase) | Program/Erase on-going while reading Flash registers f _{CPU} = 64 MHz ⁽³⁾ | | | 33 | mA |
| I _{FLPW} | CC | D | Sum of the current consumption on V _{DDHV} and V _{DDBV} during Flash low-power mode | | | | 900 | µA |

Table 26. Flash power supply DC electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit |
|-------------------|----|-----------|--|--------------------|-----|-----|------|
| | | | | Min | Typ | Max | |
| I _{FPWD} | CC | D | Sum of the current consumption on V _{DDHV} and V _{DDBV} during Flash power-down mode | | | 150 | μA |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² All values need to be confirmed during device validation.

³ f_{CPU} 64 MHz can be achieved only at up to 105 °C

4.11.3 Start-up/Switch-off timings

Table 27. Start-up time/Switch-off time

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|-------------------------|----|-----------|---|-------|-----|-----|------|
| | | | | Min | Typ | Max | |
| T _{FLARSTEXIT} | CC | T | Delay for Flash module to exit reset mode | | | 125 | μs |
| T _{FLALPEXIT} | CC | T | Delay for Flash module to exit low-power mode | | | 0.5 | |
| T _{FLAPDEXIT} | CC | T | Delay for Flash module to exit power-down mode | | | 30 | |
| T _{FLALPENTRY} | CC | T | Delay for Flash module to enter low-power mode | | | 0.5 | |
| T _{FLAPDENTRY} | CC | T | Delay for Flash module to enter power-down mode | | | 1.5 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

4.12 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.12.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and pre-qualification tests in relation with the EMC level requested for his application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
 - Corrupted program counter
 - Unexpected reset
 - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 28. EMI radiated emission measurement^{1,2}

| Symbol | C | Parameter | Conditions | Value | | | Unit | |
|--------------------|----|-----------------------|------------|--|-------------------------------|------|-----------------|------|
| | | | | Min | Typ | Max | | |
| — | SR | Scan range | | 0.150 | | 1000 | MHz | |
| f _{CPU} | SR | Operating frequency | | | 64 | | MHz | |
| V _{DD_LV} | SR | LV operating voltages | | | 1.28 | | V | |
| S _{EMI} | CC | T | Peak level | V _{DD} = 5 V, T _A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f _{OSC} = 8 MHz/f _{CPU} = 64 MHz | No PLL frequency modulation | | 18 | dBμV |
| | | | | | ± 2% PLL frequency modulation | | 14 ³ | dBμV |

¹ EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

² For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

³ All values need to be confirmed during device validation

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 29. ESD absolute maximum ratings^{1 2}

| Symbol | C | Ratings | Conditions | Class | Max value | Unit | |
|-----------------------|----|---------|--|---|-----------|---------------|---|
| V _{ESD(HBM)} | CC | T | Electrostatic discharge voltage (Human Body Model) | T _A = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| V _{ESD(MM)} | CC | T | Electrostatic discharge voltage (Machine Model) | T _A = 25 °C conforming to AEC-Q100-003 | M2 | 200 | |
| V _{ESD(CDM)} | CC | T | Electrostatic discharge voltage (Charged Device Model) | T _A = 25 °C conforming to AEC-Q100-011 | C3A | 500 | |
| | | | | | | 750 (corners) | |

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.12.3.2 Static latch-up (LU)

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Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 30. Latch-up results

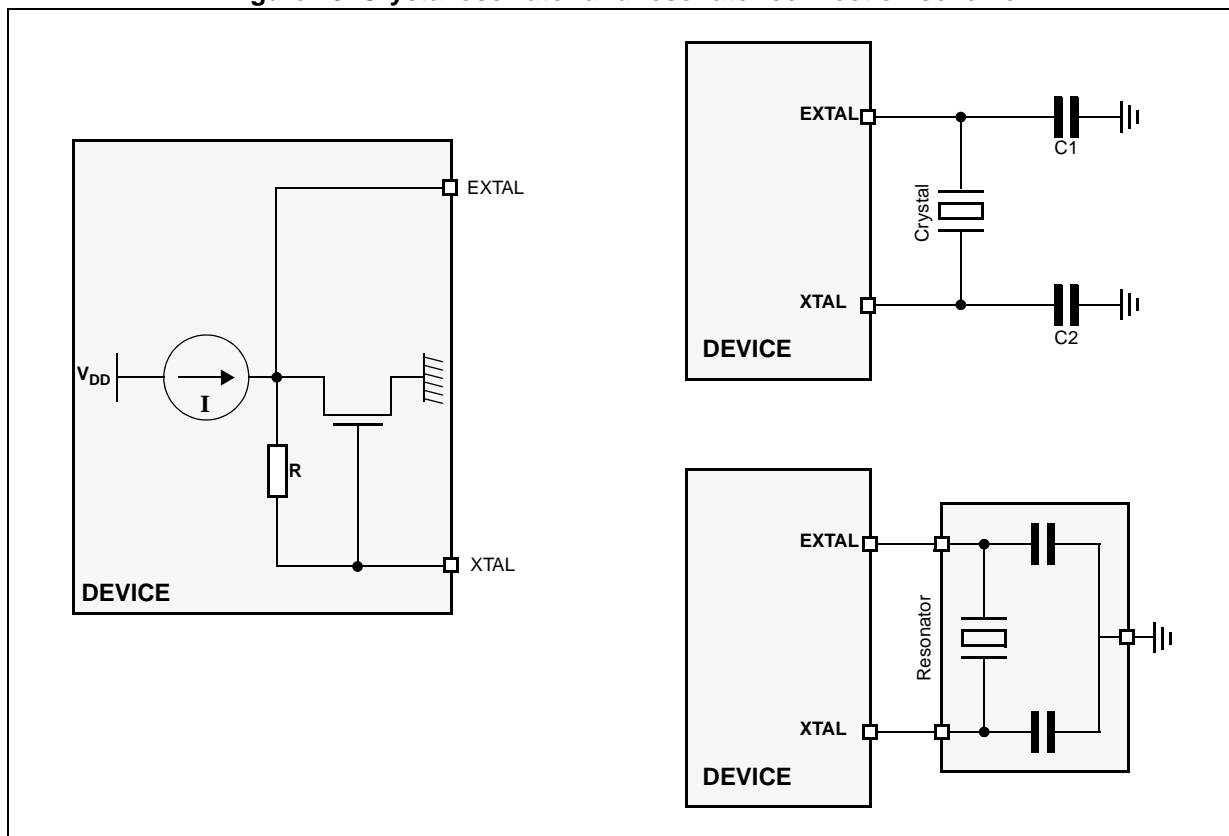
| Symbol | | C | Parameter | Conditions | Class |
|--------|----|---|-----------------------|--|------------|
| LU | CC | T | Static latch-up class | $T_A = 125\text{ }^\circ\text{C}$ conforming to JESD 78 | II level A |

4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 10 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 31 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

Figure 10. Crystal oscillator and resonator connection scheme



NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 31. Crystal description

| Nominal frequency (MHz) | NDK crystal reference | Crystal equivalent series resistance ESR Ω | Crystal motional capacitance (C_m) fF | Crystal motional inductance (L_m) mH | Load on xtalin/xtalout $C1 = C2$ (pF) ¹ | Shunt capacitance between xtalout and xtalin $C0^2$ (pF) |
|-------------------------|-----------------------|---|---|--|--|--|
| 4 | NX8045GB | 300 | 2.68 | 591.0 | 21 | 2.93 |
| 8 | NX5032GA | 300 | 2.46 | 160.7 | 17 | 3.01 |
| 10 | | 150 | 2.93 | 86.6 | 15 | 2.91 |
| 12 | | 120 | 3.11 | 56.5 | 15 | 2.93 |
| 16 | | 120 | 3.90 | 25.3 | 10 | 3.00 |

¹ The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

² The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Figure 11. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

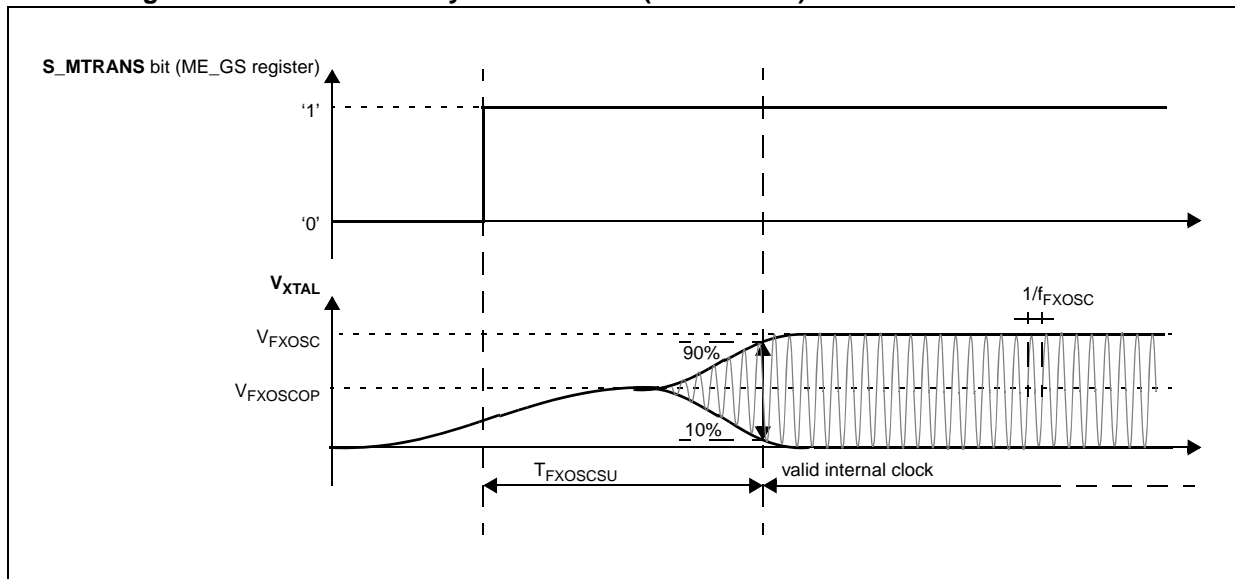


Table 32. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit |
|-------------|----|--|-------------------------|--------------------|-----|------|------|
| | | | | Min | Typ | Max | |
| f_{FXOSC} | SR | Fast external crystal oscillator frequency | | 4.0 | | 16.0 | MHz |

Table 32. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit | |
|---------------------------------|----|-----------|---|--|---------------------|------|----------------------|------|
| | | | | Min | Typ | Max | | |
| g _{mFXOSC} | CC | C | Fast external crystal oscillator transconductance | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0 | 2.2 | | 8.2 | mA/V |
| | CC | P | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0 | 2.0 | | 7.4 | |
| | CC | C | | V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1 | 2.7 | | 9.7 | |
| | CC | C | | V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1 | 2.5 | | 9.2 | |
| V _{FXOSC} | CC | T | Oscillation amplitude at EXTAL | f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0 | 1.3 | | | V |
| | | | | f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1 | 1.3 | | | |
| V _{FXOSCOPI} | CC | P | Oscillation operating point | | | 0.95 | | V |
| I _{FXOSC} ³ | CC | T | Fast external crystal oscillator consumption | | | | 3 | mA |
| T _{FXOSCSU} | CC | T | Fast external crystal oscillator start-up time | f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0 | | | 6 | ms |
| | | | | f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1 | | | 1.8 | |
| V _{IH} | SR | P | Input high level CMOS (Schmitt Trigger) | Oscillator bypass mode | 0.65V _{DD} | | V _{DD} +0.4 | V |
| V _{IL} | SR | P | Input low level CMOS (Schmitt Trigger) | Oscillator bypass mode | -0.4 | | 0.35V _{DD} | V |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

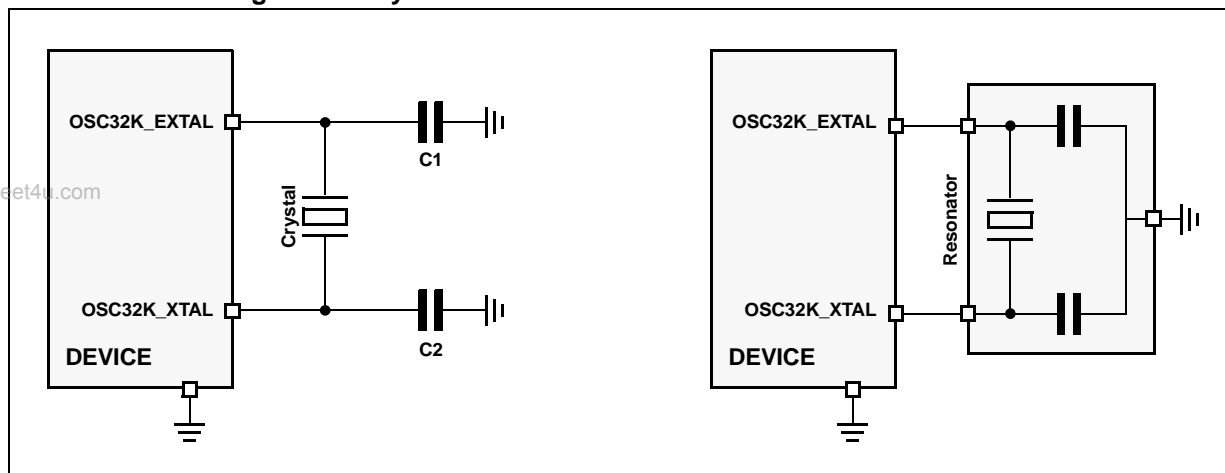
² All values need to be confirmed during device validation.

³ Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

4.14 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

Figure 12. Crystal oscillator and resonator connection scheme



NOTE

OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

Figure 13. Equivalent circuit of a quartz crystal

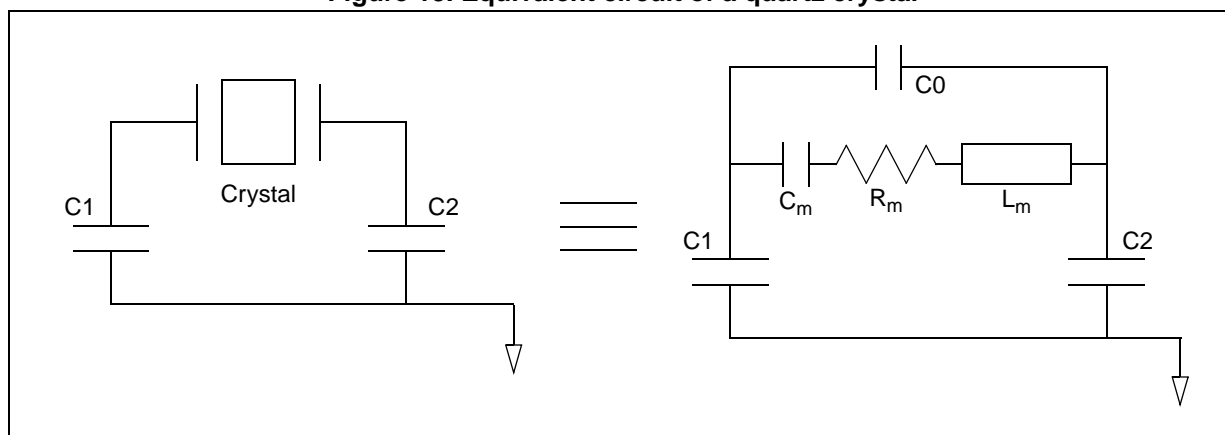


Table 33. Crystal motional characteristics¹

| Symbol | Parameter | Conditions | Value | | | Unit |
|--------------------|--|--|-------|--------|-----|------|
| | | | Min | Typ | Max | |
| L_m | Motional inductance | — | | 11.796 | | KH |
| C_m | Motional capacitance | — | | 2 | | fF |
| C1/C2 | Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground ² | | 18 | | 28 | pF |
| R_m ³ | Motional resistance | AC coupled @ $C_0 = 2.85 \text{ pF}^{(4)}$ | | | 65 | kW |
| | | AC coupled @ $C_0 = 4.9 \text{ pF}^{(4)}$ | | | 50 | |
| | | AC coupled @ $C_0 = 7.0 \text{ pF}^{(4)}$ | | | 35 | |
| | | AC coupled @ $C_0 = 9.0 \text{ pF}^{(4)}$ | | | 30 | |

¹ The crystal used is Epson Toyocom MC306.

- 2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
- 3 Maximum ESR (R_m) of the crystal is 50 k Ω
- 4 C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins

Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics

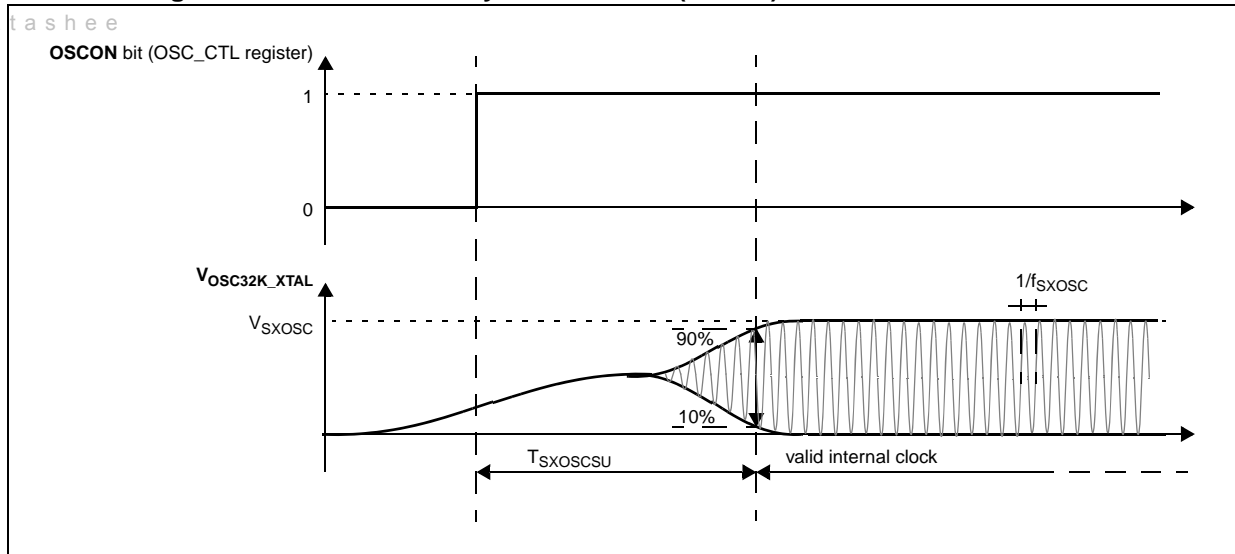


Table 34. Slow external crystal oscillator (32 kHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit |
|-----------------|----|---|--|--------------------|--------|-----|---------------|
| | | | | Min | Typ | Max | |
| f_{SXOSC} | SR | Slow external crystal oscillator frequency | | 32 | 32.768 | 40 | kHz |
| g_{mSXOSC} | CC | Slow external crystal oscillator transconductance | $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ | TBD | | | mA/V |
| | | | $V_{DD} = 5.0 \text{ V} \pm 10\%$ $PAD3V5V = 0$ | TBD | | | |
| | | | $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ | TBD | | | |
| | | | $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ | TBD | | | |
| V_{SXOSC} | CC | Oscillation amplitude | | | 0.6 | | V |
| $I_{SXOSCBIAS}$ | CC | Oscillation bias current | | TBD | | | μA |
| I_{SXOSC} | CC | Slow external crystal oscillator consumption | | | | 8 | μA |
| $T_{SXOSCSU}$ | CC | Slow external crystal oscillator start-up time | | | | 2 | s |

¹ $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to $125 \text{ }^\circ\text{C}$, unless otherwise specified

² All values need to be confirmed during device validation.

4.15 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 35. FMPLL electrical characteristics

| Symbol | | C | Parameter | Conditions ¹ | Value ² | | | Unit |
|---------------------|----|---|---|---|--------------------|-----|-----------------|------|
| | | | | | Min | Typ | Max | |
| f _{PLLIN} | SR | — | FMPLL reference clock ³ | | 4 | | 64 | MHz |
| Δ _{PLLIN} | SR | — | FMPLL reference clock duty cycle ⁽³⁾ | | 40 | | 60 | % |
| f _{PLLOUT} | CC | P | FMPLL output clock frequency | | 16 | | 64 | MHz |
| f _{CPU} | SR | — | System clock frequency | | | | 64 ⁴ | MHz |
| f _{FREE} | CC | P | Free-running frequency | | 20 | | 150 | MHz |
| t _{LOCK} | CC | P | FMPLL lock time | Stable oscillator (f _{PLLIN} = 16 MHz) | | 40 | 100 | μs |
| Δ _{LTJIT} | CC | — | FMPLL long term jitter | f _{PLLIN} = 16 MHz (resonator), f _{PLLCLK} @ 64 MHz, 4000 cycles | | TBD | | ns |
| I _{PLL} | CC | C | FMPLL consumption | T _A = 25 °C | | | 4 | mA |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² All values need to be confirmed during device validation.

³ PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

⁴ f_{CPU} 64 MHz can be achieved only at up to 105 °C

4.16 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 36. Fast internal RC oscillator (16 MHz) electrical characteristics

| Symbol | | C | Parameter | Conditions ¹ | Value ² | | | Unit |
|----------------------------------|----|---|---|---------------------------------|--------------------|-----|-----|------|
| | | | | | Min | Typ | Max | |
| f _{FIRC} | CC | P | Fast internal RC oscillator high frequency | T _A = 25 °C, trimmed | | 16 | | MHz |
| | SR | — | | | 12 | | 20 | |
| I _{FIRCUN} ³ | CC | T | Fast internal RC oscillator high frequency current in running mode | T _A = 25 °C, trimmed | | | 200 | μA |
| I _{FIRCPWD} | CC | D | Fast internal RC oscillator high frequency current in power down mode | T _A = 25 °C | | TBD | 10 | μA |
| | | | | T _A = 55 °C | | TBD | TBD | |

Table 36. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | | Value ² | | | Unit | |
|-----------------------|----|-----------|---|-------------------------|-------------------------------|-----|------|------|----|
| | | | | | Min | Typ | Max | | |
| I _{FIRCSTOP} | CC | T | Fast internal RC oscillator high frequency and system clock current in stop mode | T _A = 25 °C | sysclk = off | | 500 | | μA |
| | | | | | sysclk = 2 MHz | | 600 | | |
| | | | | | sysclk = 4 MHz | | 700 | | |
| | | | | | sysclk = 8 MHz | | 900 | | |
| | | | | | sysclk = 16 MHz | | 1250 | | |
| T _{FIRCSU} | CC | C | Fast internal RC oscillator start-up time | T _A = 55 °C | V _{DD} = 5.0 V ± 10% | 1.1 | 2.0 | μs | |
| | | | | | V _{DD} = 3.3 V ± 10% | TBD | TBD | | |
| | | | | T _A = 125 °C | V _{DD} = 5.0 V ± 10% | | TBD | | |
| | | | | | V _{DD} = 3.3 V ± 10% | | TBD | | |
| Δ _{FIRCPRE} | CC | C | Fast internal RC oscillator precision after software trimming of f _{FIRC} | T _A = 25 °C | | -1 | +1 | % | |
| Δ _{FIRCTRM} | CC | C | Fast internal RC oscillator trimming step | T _A = 25 °C | | | 1.6 | % | |
| Δ _{FIRCVAR} | CC | C | Fast internal RC oscillator variation in temperature and supply with respect to f _{FIRC} at T _A = 55 °C in high-frequency configuration | | | -5 | +5 | % | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

² All values need to be confirmed during device validation.

³ This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 37. Slow internal RC oscillator (128 kHz) electrical characteristics

| Symbol | C | Parameter | Conditions ¹ | | Value ² | | | Unit |
|--------------------------------|----|-----------|---|---|--------------------|-----|-----|------|
| | | | | | Min | Typ | Max | |
| f _{SIRC} | CC | P | Slow internal RC oscillator low frequency | T _A = 25 °C, trimmed | | 128 | | kHz |
| | SR | | | | | 100 | 150 | |
| I _{SIRC} ³ | CC | C | Slow internal RC oscillator low frequency current | T _A = 25 °C, trimmed | | | 5 | μA |
| T _{SIRCSU} | CC | P | Slow internal RC oscillator start-up time | T _A = 25 °C, V _{DD} = 5.0 V ± 10% | TBD | 8 | 12 | μs |

Table 37. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value ² | | | Unit | |
|----------------------------|----|-----------|---|----------------------------------|-----|-----|------|---|
| | | | | Min | Typ | Max | | |
| Δ_{SIRCPRE} | CC | C | Slow internal RC oscillator precision after software trimming of f_{SIRC} | $T_A = 25\text{ }^\circ\text{C}$ | -2 | | +2 | % |
| Δ_{SIRCTrim} | CC | C | Slow internal RC oscillator trimming step | | 2.7 | | | |
| Δ_{SIRCVar} | CC | C | Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at $T_A = 55\text{ }^\circ\text{C}$ in high frequency configuration | High frequency configuration | -10 | | +10 | % |

¹ $V_{\text{DD}} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^\circ\text{C}$, unless otherwise specified.

² All values need to be confirmed during device validation.

³ This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.18 On-chip peripherals

4.18.1 Current consumption

Table 38. On-chip peripherals current consumption

| Symbol | C | Parameter | Conditions | Value | | | Unit |
|------------------------|----|-----------|------------------------------|----------------------------------|-----|-----|--------------------------|
| | | | | Min | Typ | Max | |
| $I_{\text{DD(ADC)}}$ | CC | T | ADC supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | $\mu\text{A}/\text{MHz}$ |
| $I_{\text{DD(CAN)}}$ | CC | T | CAN (FlexCAN) supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | |
| $I_{\text{DD(CTU)}}$ | CC | T | CTU supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | |
| $I_{\text{DD(eMIOS)}}$ | CC | T | eMIOS supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | |
| $I_{\text{DD(FLASH)}}$ | CC | T | Flash supply current | (see Table 26) | | | |
| $I_{\text{DD(I2C)}}$ | CC | T | I2C supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | $\mu\text{A}/\text{MHz}$ |
| $I_{\text{DD(FMPLL)}}$ | CC | T | FMPLL supply current | (see Table 35) | | | |
| $I_{\text{DD(RTC)}}$ | CC | T | RTC supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | $\mu\text{A}/\text{MHz}$ |
| $I_{\text{DD(SCI)}}$ | CC | T | SCI (LINFlex) supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | |
| $I_{\text{DD(SIU)}}$ | CC | T | SIU supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | |
| $I_{\text{DD(SPI)}}$ | CC | T | SPI (DSPI) supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | |
| $I_{\text{DD(SWT)}}$ | CC | T | SWT supply current | $T_A = 25\text{ }^\circ\text{C}$ | TBD | | |
| | | | | | | | |

4.18.2 DSPI characteristics

Table 39. DSPI characteristics

| No. | Symbol | C | Parameter | Value | | | Unit | |
|-----|---------------------------|----|-----------|---|-------------------|---|------------------|-----|
| | | | | Min | Typ | Max | | |
| 1 | t_{SCK} | SR | D | SCK cycle time | 64 | | | ns |
| — | f_{DSPI} | SR | D | DSPI digital controller frequency | | | f_{CPU} | MHz |
| — | Δt_{CSC} | CC | D | Internal delay between pad associated to SCK and pad associated to CSn in master mode | | | 120 ¹ | ns |
| 2 | t_{CSCext} ² | CC | D | CS to SCK delay | Master mode | $t_{CSCext} = t_{CSC} + \Delta t_{CSC}$ | | ns |
| | | | | | Slave mode | 32 | | |
| 3 | t_{ASCext} ³ | CC | D | After SCK delay | Master mode | $t_{ASCext} = t_{ASC} + \Delta t_{CSC}$ | | ns |
| | | | | | Slave mode | $1/f_{DSPI} + 5$ ns | | ns |
| 4 | t_{SDC} | CC | D | SCK duty cycle | Master mode | | $t_{SCK}/2$ | ns |
| | | | | | Slave mode | $t_{SCK}/2$ | | |
| 5 | t_A | SR | D | Slave access time | 27 | | | ns |
| 6 | t_{DI} | SR | D | Slave SOUT disable time | 0 | | | ns |
| 7 | — | | | | | | | |
| 8 | — | | | | | | | |
| 9 | t_{SUI} | SR | D | Data setup time for inputs | Master (MTFE = 0) | 35 | | ns |
| | | | | | Slave | 5 | | |
| | | | | | Master (MTFE = 1) | 35 | | |
| 10 | t_{HI} | SR | D | Data hold time for inputs | Master (MTFE = 0) | 0 | | ns |
| | | | | | Slave | 2 ⁴ | | |
| | | | | | Master (MTFE = 1) | 0 | | |
| 11 | t_{SUO} ⁵ | CC | D | Data valid after SCK edge | Master (MTFE = 0) | | 32 | ns |
| | | | | | Slave | | 34 | |
| | | | | | Master (MTFE = 1) | | 32 | |
| 12 | t_{HO} ⁽⁵⁾ | CC | D | Data hold time for outputs | Master (MTFE = 0) | 2 | | ns |
| | | | | | Slave | 5.5 | | |
| | | | | | Master (MTFE = 1) | 2 | | |

¹ Maximum is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM pad.

² The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext} .

³ The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext} .

⁴ This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

⁵ SCK and SOUT configured as MEDIUM pad

Figure 15. DSPI classic SPI timing – master, CPHA = 0

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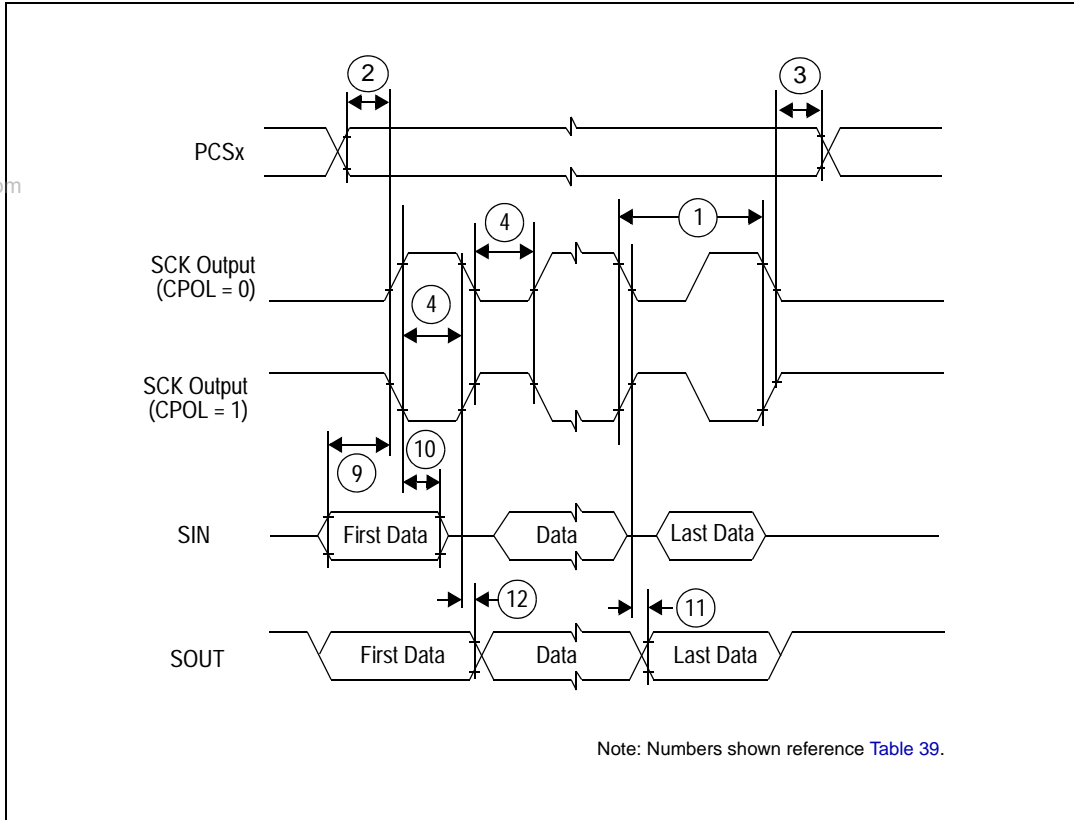


Figure 16. DSPI classic SPI timing – master, CPHA = 1

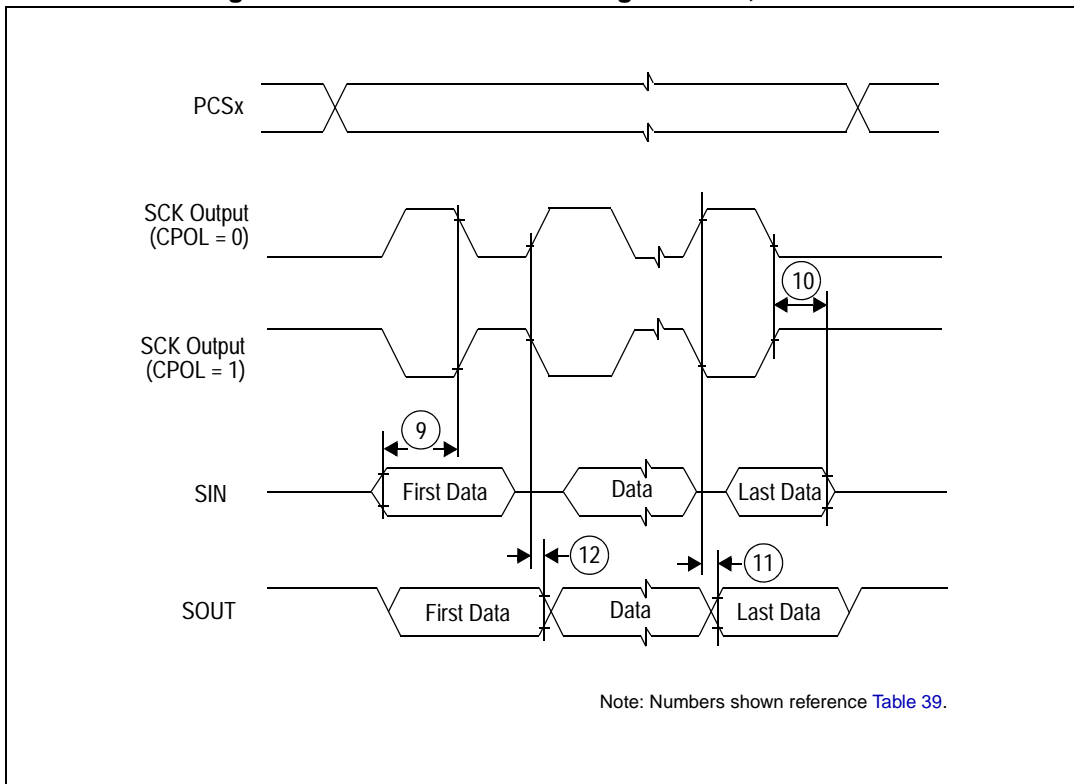


Figure 17. DSPI classic SPI timing – slave, CPHA = 0

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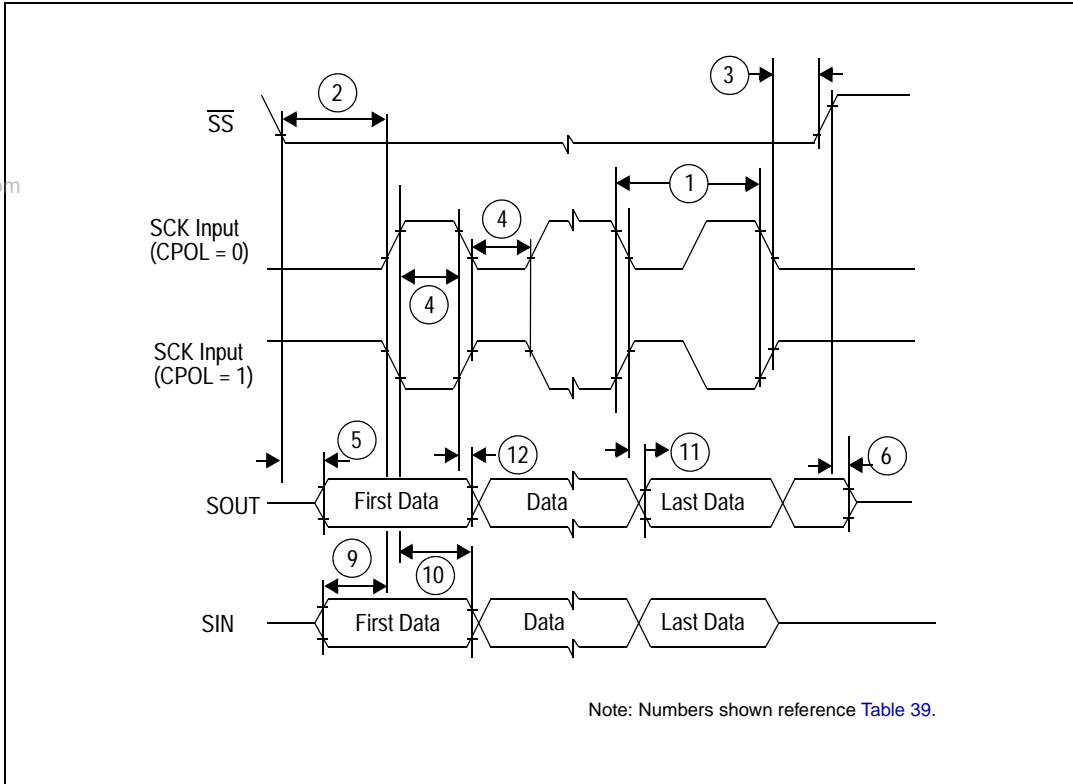


Figure 18. DSPI classic SPI timing – slave, CPHA = 1

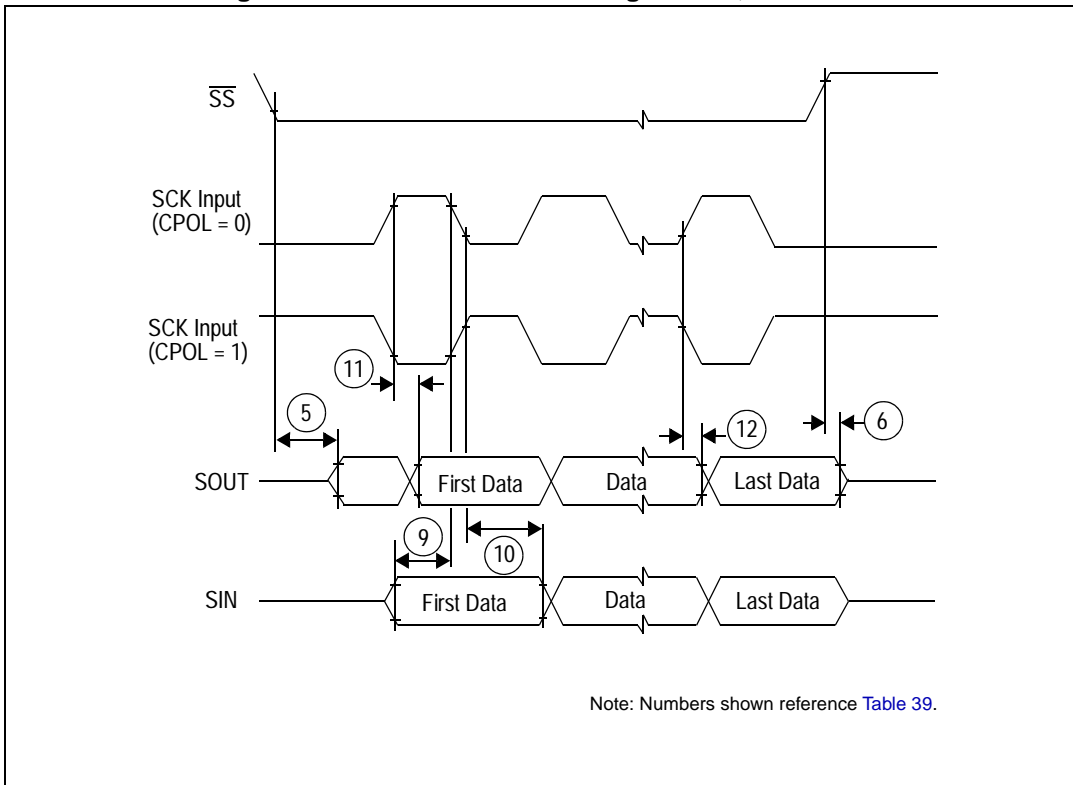


Figure 19. DSPI modified transfer format timing – master, CPHA = 0

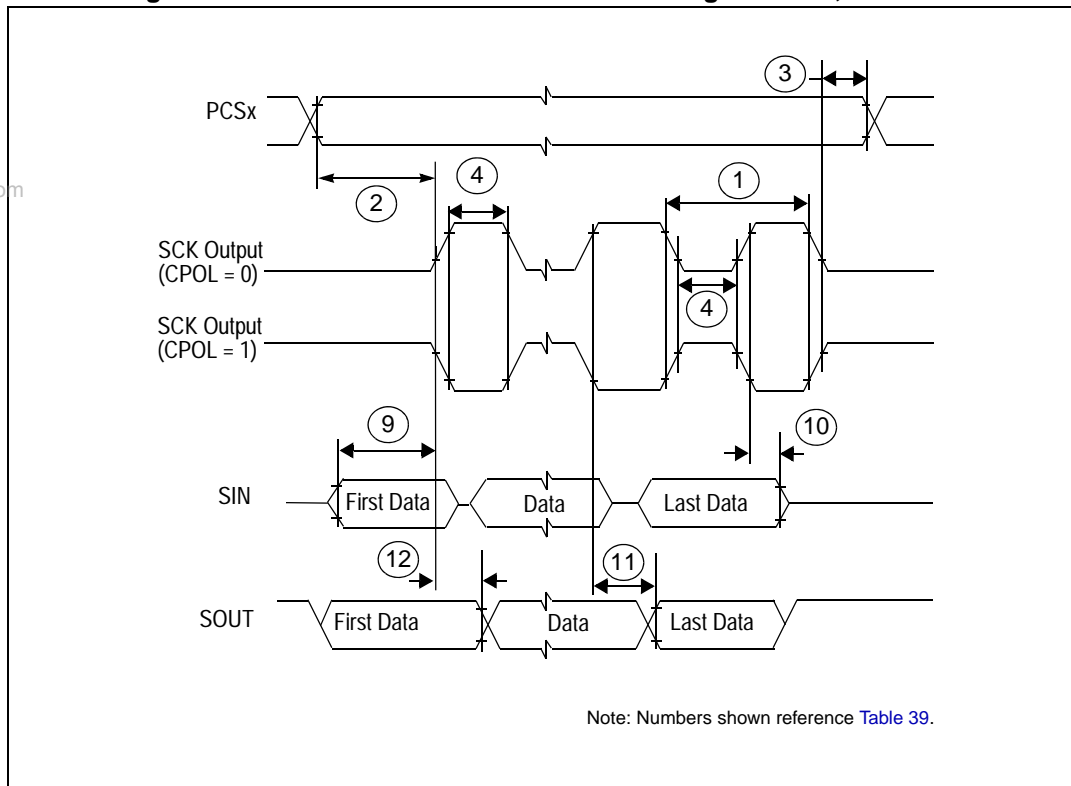


Figure 20. DSPI modified transfer format timing – master, CPHA = 1

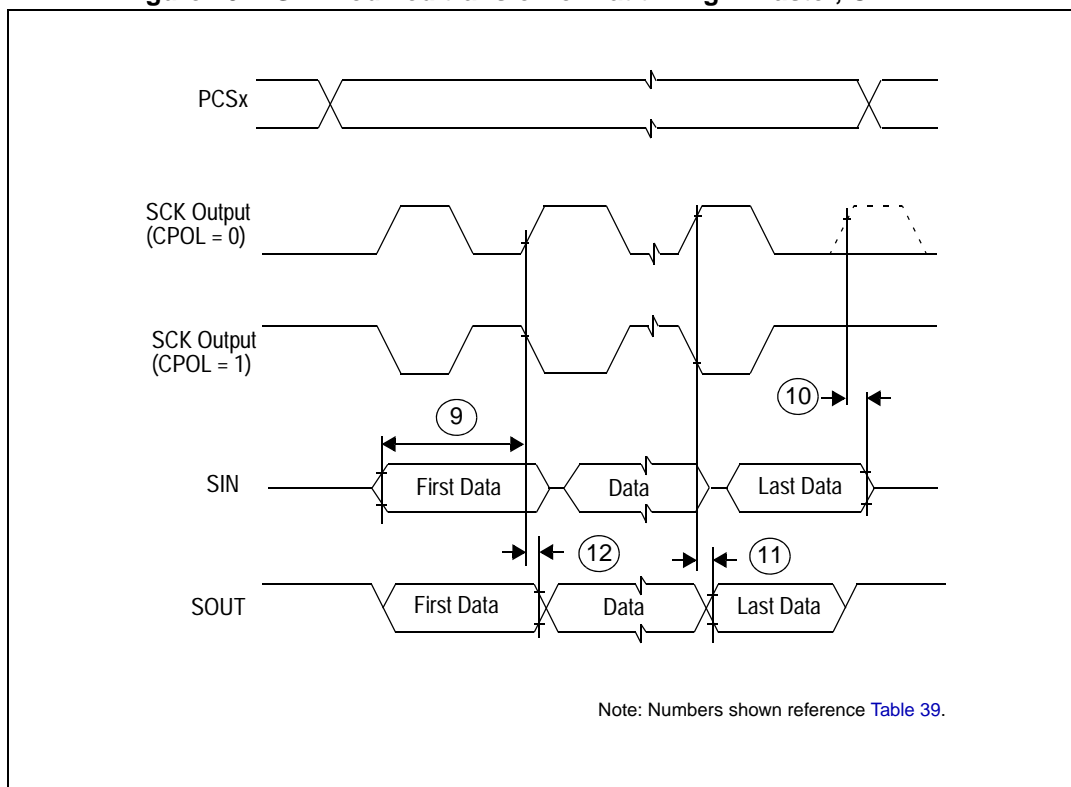


Figure 21. DSPI modified transfer format timing – slave, CPHA = 0

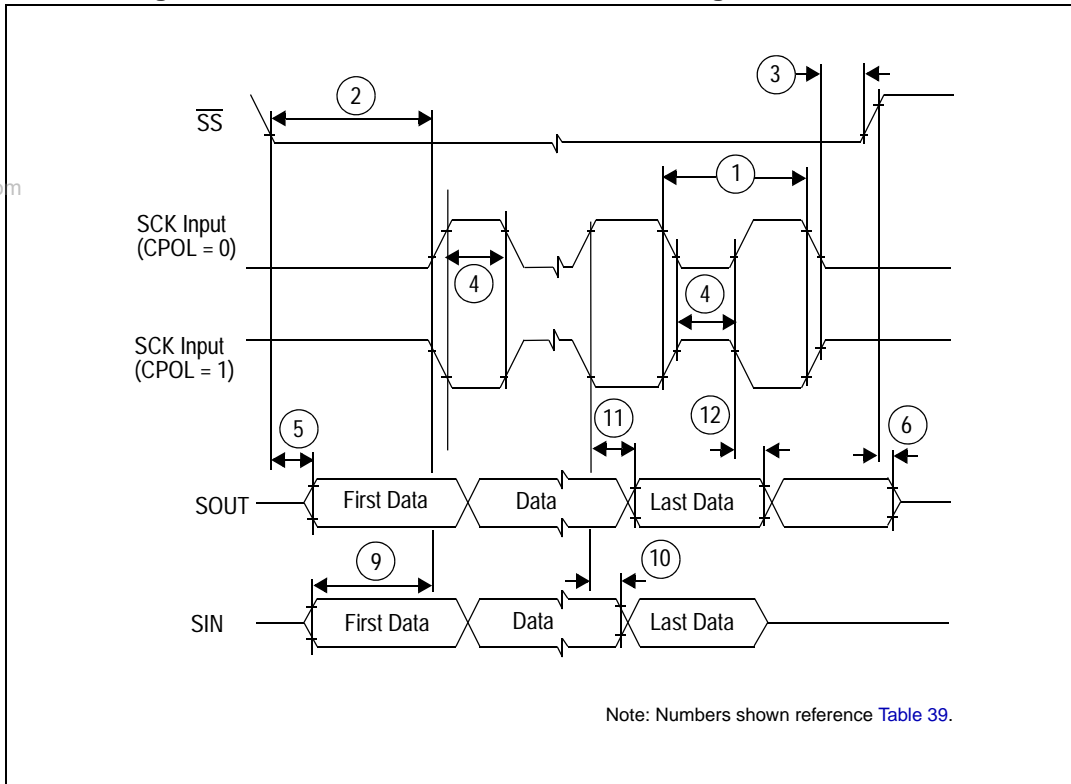


Figure 22. DSPI modified transfer format timing – slave, CPHA = 1

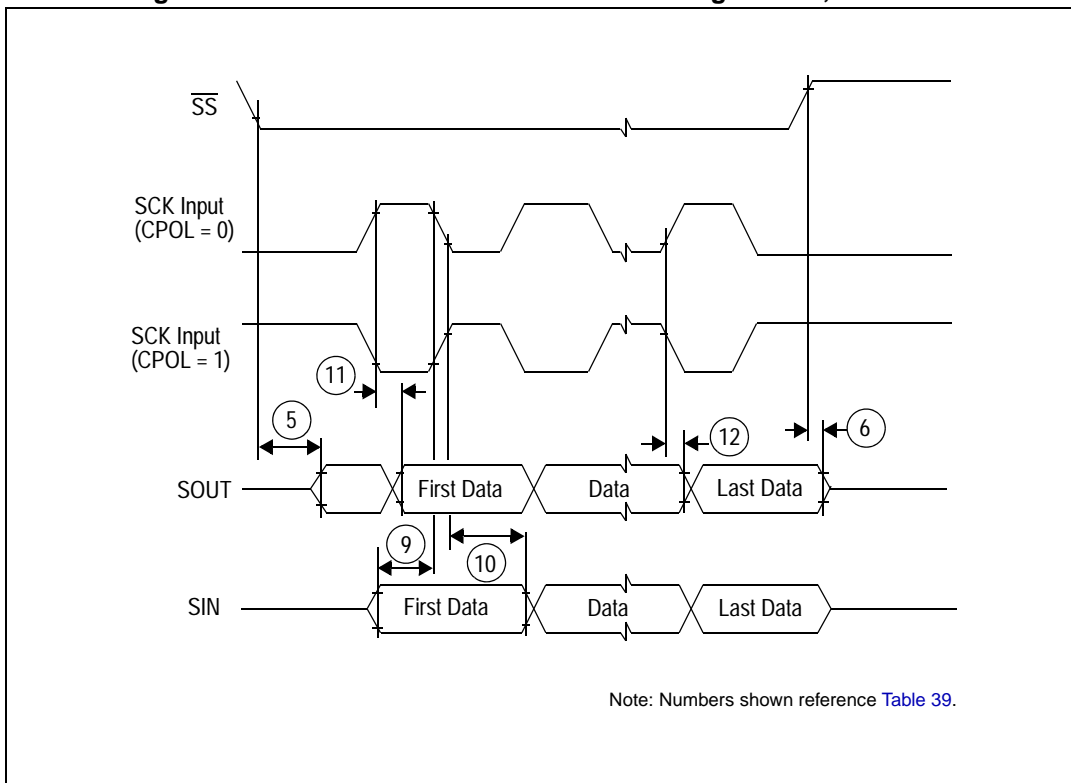
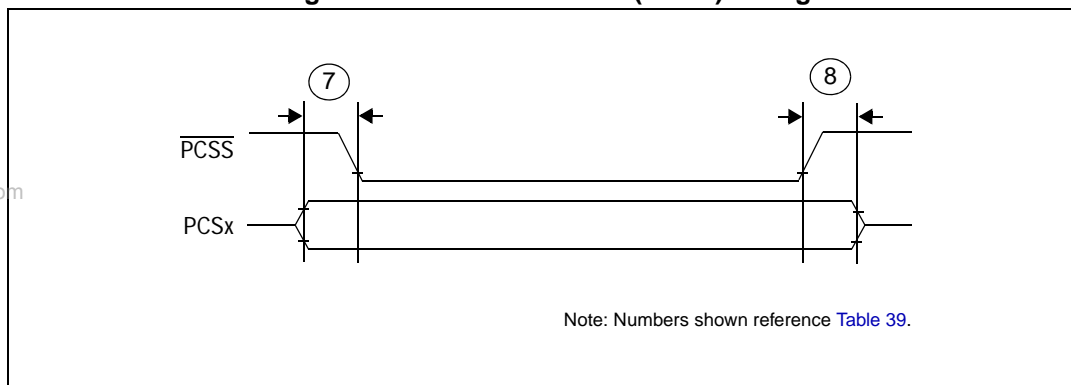


Figure 23. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

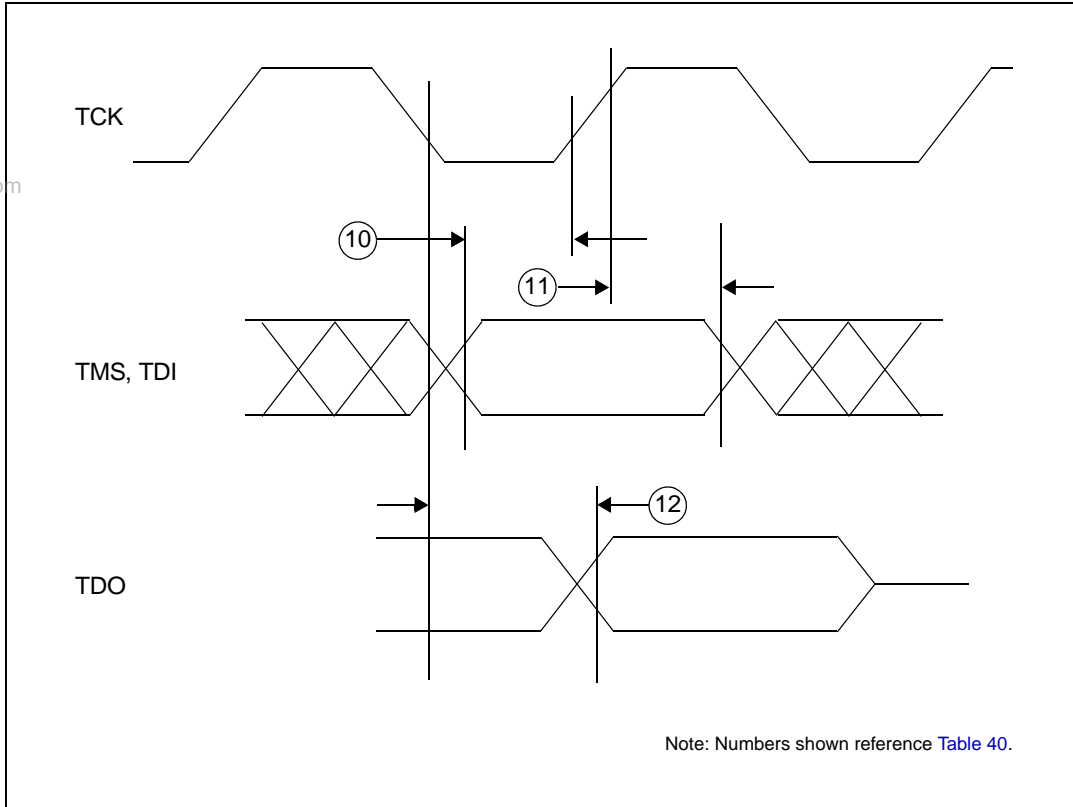


4.18.3 Nexus characteristics

Table 40. Nexus characteristics

| No. | Symbol | C | Parameter | Value | | | Unit |
|-----|----------------------|----|-----------|-------------------------------|-----|-----|------|
| | | | | Min | Typ | Max | |
| 1 | $t_{\text{T CYC}}$ | CC | D | TCK cycle time | 64 | | ns |
| 2 | $t_{\text{M CYC}}$ | CC | D | MCKO cycle time | 32 | | ns |
| 3 | $t_{\text{M DOV}}$ | CC | D | MCKO low to MDO data valid | | | 8 |
| 4 | $t_{\text{M SEOV}}$ | CC | D | MCKO low to MSEO_b data valid | | | 8 |
| 5 | $t_{\text{E VTOV}}$ | CC | D | MCKO low to EVTO data valid | | | 8 |
| 10 | $t_{\text{N TDIS}}$ | CC | D | TDI data setup time | 15 | | ns |
| | $t_{\text{N TMSS}}$ | CC | D | TMS data setup time | 15 | | ns |
| 11 | $t_{\text{N TDIH}}$ | CC | D | TDI data hold time | 5 | | ns |
| | $t_{\text{N TM SH}}$ | CC | D | TMS data hold time | 5 | | ns |
| 12 | $t_{\text{T DOV}}$ | CC | D | TCK low to TDO data valid | 35 | | ns |
| 13 | $t_{\text{T DOI}}$ | CC | D | TCK low to TDO data invalid | 6 | | ns |

Figure 24. Nexus TDI, TMS, TDO timing

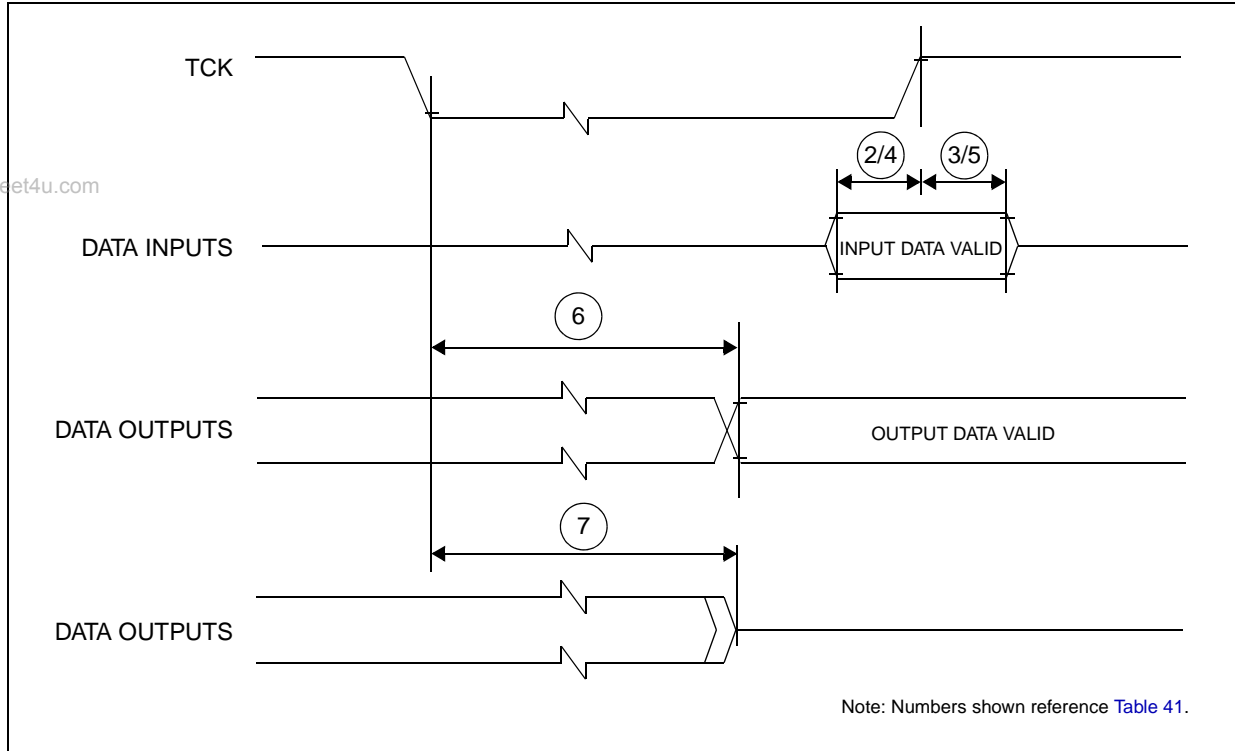


4.18.4 JTAG characteristics

Table 41. JTAG characteristics

| No. | Symbol | C | Parameter | Value | | | Unit | |
|-----|------------|----|-----------|------------------------|-----|-----|------|----|
| | | | | Min | Typ | Max | | |
| 1 | t_{JCYC} | CC | D | TCK cycle time | 64 | | | ns |
| 2 | t_{TDIS} | CC | D | TDI setup time | 15 | | | ns |
| 3 | t_{TDIH} | CC | D | TDI hold time | 5 | | | ns |
| 4 | t_{TMSS} | CC | D | TMS setup time | 15 | | | ns |
| 5 | t_{TMSh} | CC | D | TMS hold time | 5 | | | ns |
| 6 | t_{TDOV} | CC | D | TCK low to TDO valid | | | 33 | ns |
| 7 | t_{TDOI} | CC | D | TCK low to TDO invalid | 6 | | | ns |

Figure 25. Timing diagram – JTAG boundary scan

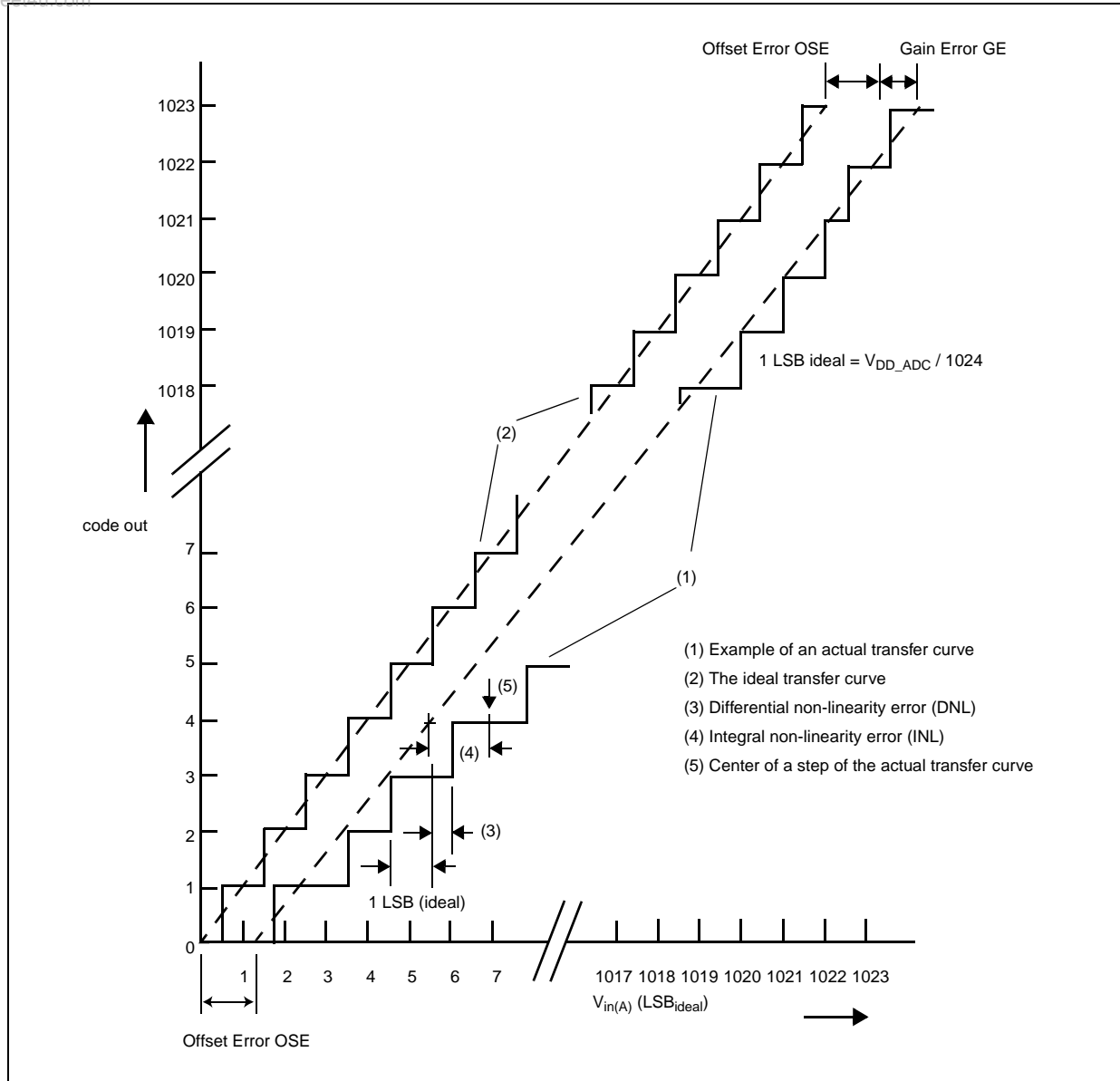


4.18.5 ADC electrical characteristics

4.18.5.1 Introduction

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 26. ADC characteristic and error definitions



4.18.5.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 k Ω is obtained ($R_{EQ} = 1 / (f_c * C_S)$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} \text{LSB}$$

Equation 4 generates a constraint for external network design, in particular on a resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 27. Input equivalent circuit (precise channels)

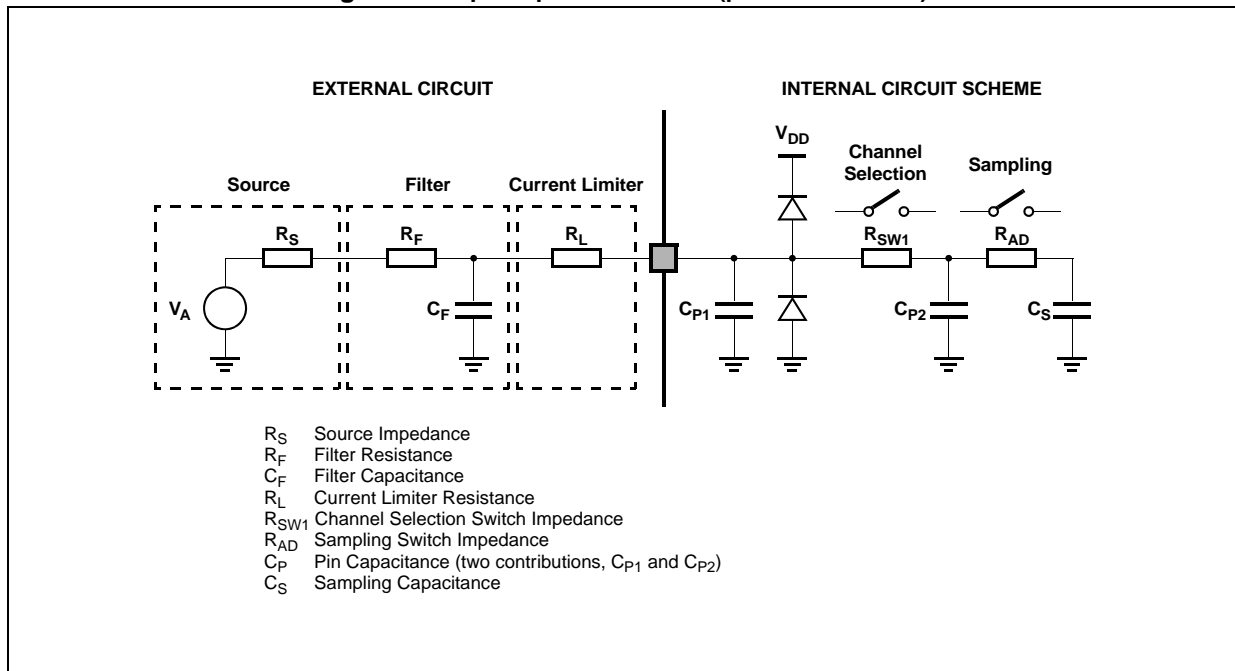
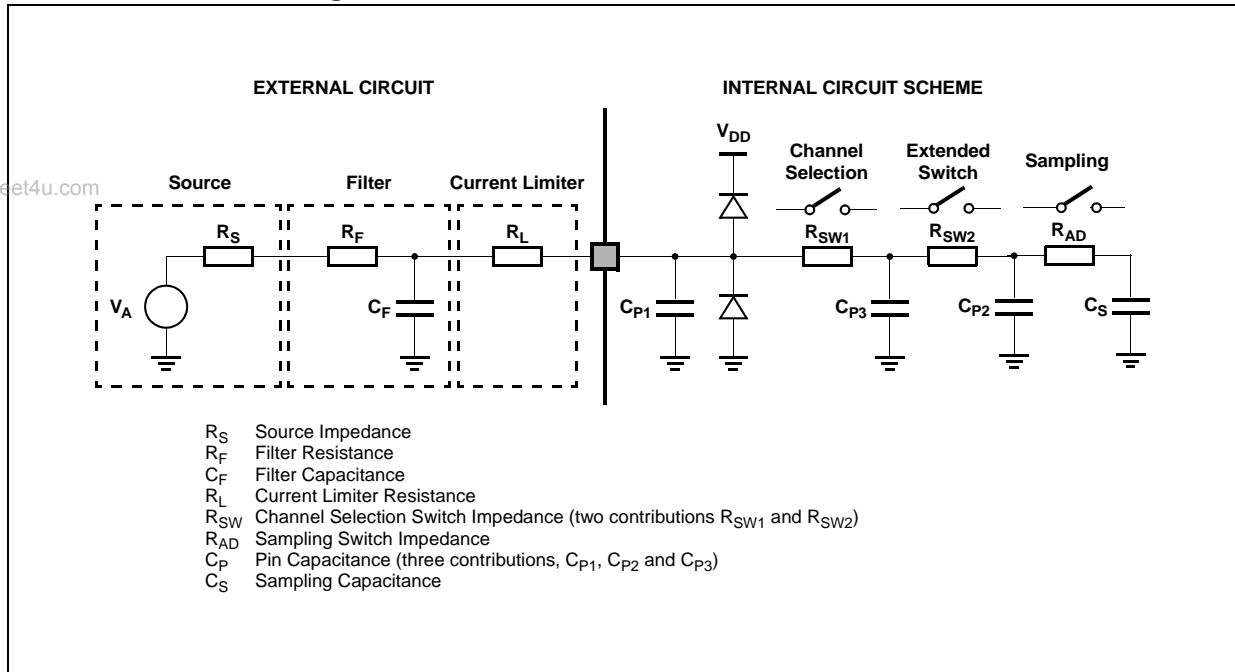
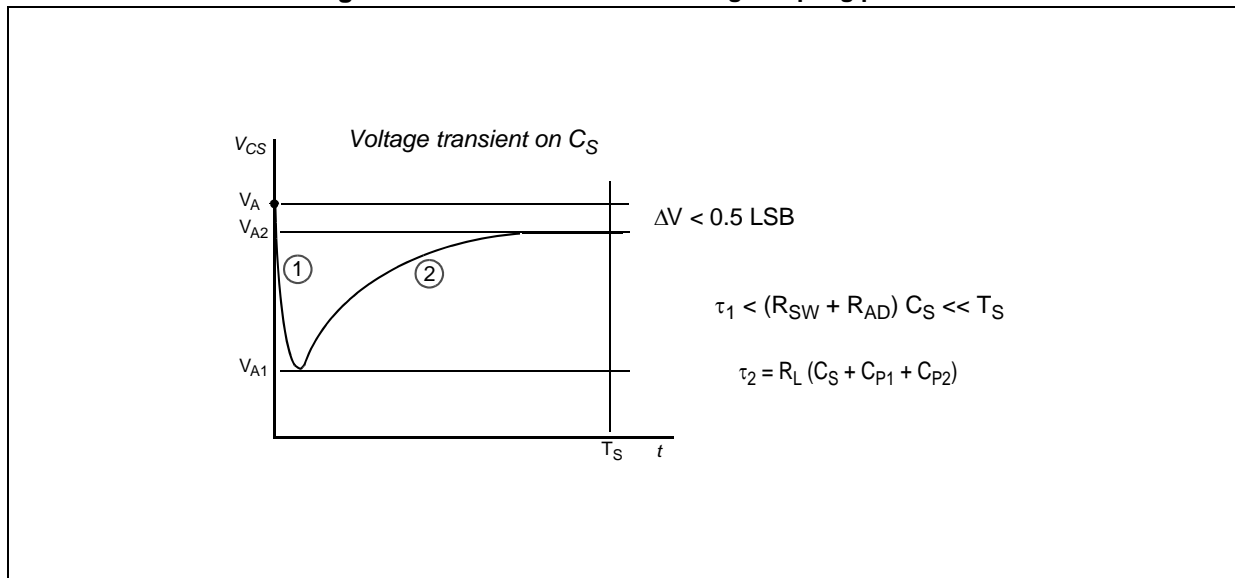


Figure 28. Input equivalent circuit (extended channels)



A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F , C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit in Figure 27): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 29. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S , a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < T_S$$

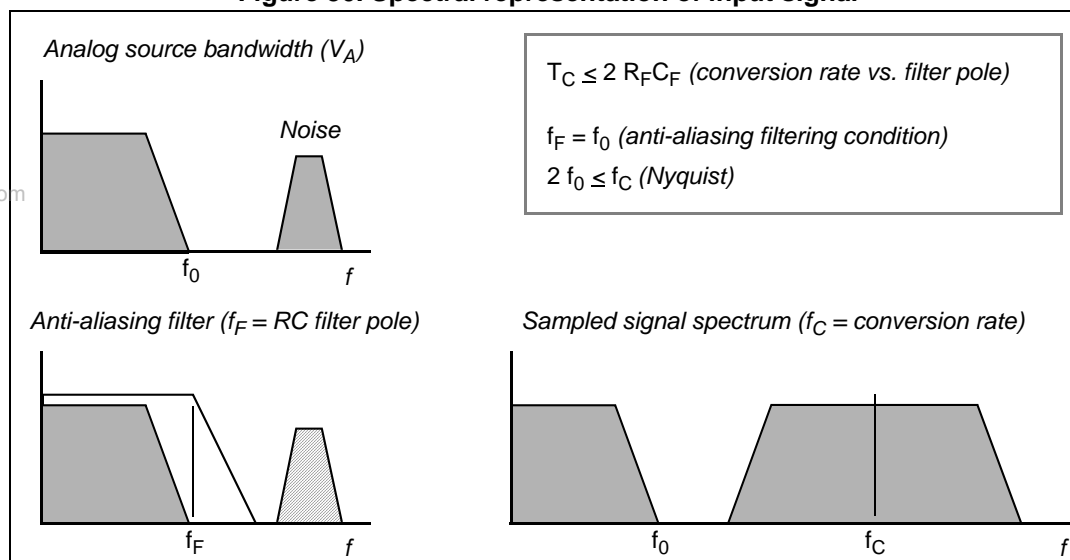
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 30. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S , so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S ; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S :

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S} \quad \text{Eqn. 11}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

$$C_F > 2048 \cdot C_S \quad \text{Eqn. 12}$$

4.18.5.3 ADC electrical characteristics

Table 42. ADC input leakage current

| Symbol | C | Parameter | Conditions | Value | | | Unit | | |
|------------------|----|-----------|-----------------------|-------------------------|--------------------------------------|-----|------|-----|----|
| | | | | Min | Typ | Max | | | |
| I _{LKG} | CC | C | Input leakage current | T _A = -40 °C | No current injection on adjacent pin | | 1 | | nA |
| | | | | T _A = 25 °C | | | 1 | | |
| | | | | T _A = 105 °C | | | 8 | 200 | |
| | | | | T _A = 125 °C | | | 45 | 400 | |

Table 43. ADC conversion characteristics

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit |
|----------------------|----|-----------|--|--|-------|--------------------------|------|
| | | | | Min | Typ | Max | |
| V _{SS_ADC} | SR | — | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS}) ² | -0.1 | | 0.1 | V |
| V _{DD_ADC} | SR | — | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS}) | V _{DD} -0.1 | | V _{DD} +0.1 | V |
| V _{AINx} | SR | — | Analog input voltage ³ | V _{SS_ADC} -0.1 | | V _{DD_ADC} +0.1 | V |
| f _{ADC} | SR | — | ADC analog frequency | 6 | | 32 + 4% | MHz |
| Δ _{ADC_SYS} | SR | — | ADC digital clock duty cycle (ipg_clk) | ADCLKSEL = 1 ⁴ | 45 | 55 | % |
| t _{ADC_PU} | SR | — | ADC power up delay | | | 1.5 | μs |
| t _{ADC_S} | CC | T | Sample time ⁵ | f _{ADC} = 32 MHz, ADC_conf_sample_input = 17 | 0.5 | | μs |
| | | | | f _{ADC} = 6 MHz, INPSAMP = 255 | | | |
| t _{ADC_C} | CC | P | Conversion time ⁶ | f _{ADC} = 32 MHz, ADC_conf_comp = 2 | 0.625 | | μs |
| C _S | CC | D | ADC input sampling capacitance | | | 3 | pF |
| C _{P1} | CC | D | ADC input pin capacitance 1 | | | 3 | pF |
| C _{P2} | CC | D | ADC input pin capacitance 2 | | | 1 | pF |
| C _{P3} | CC | D | ADC input pin capacitance 3 | | | 1 | pF |

Table 43. ADC conversion characteristics (continued)

| Symbol | C | Parameter | Conditions ¹ | Value | | | Unit | |
|------------------|----|-----------|---|-------------------------------|-----|-----|------|-----|
| | | | | Min | Typ | Max | | |
| R _{SW1} | CC | D | Internal resistance of analog source | | | 3 | kΩ | |
| R _{SW2} | CC | D | Internal resistance of analog source | | | 2 | kΩ | |
| R _{AD} | CC | D | Internal resistance of analog source | | | 0.1 | kΩ | |
| I _{INJ} | SR | — | Input current Injection Current injection on one ADC input, different from the converted one | V _{DD} = 3.3 V ± 10% | –5 | 5 | mA | |
| | | | | V _{DD} = 5.0 V ± 10% | –5 | 5 | | |
| INL | CC | T | Absolute value for integral non-linearity | No overload | | 0.5 | 1.5 | LSB |
| DNL | CC | T | Absolute differential non-linearity | No overload | | 0.5 | 1.0 | LSB |
| OFS | CC | T | Absolute offset error | | | 0.5 | | LSB |
| GNE | CC | T | Absolute gain error | | | 0.6 | | LSB |
| TUE _p | CC | P | Total unadjusted error ⁷ for precise channels, input only pins | Without current injection | –2 | 0.6 | 2 | LSB |
| | | T | | With current injection | –3 | | 3 | |
| TUE _x | CC | T | Total unadjusted error ⁽⁷⁾ for extended channel | Without current injection | –3 | 1 | 3 | LSB |
| | | T | | With current injection | –4 | | 4 | |

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

² Analog and digital V_{SS} **must** be common (to be tied together externally).

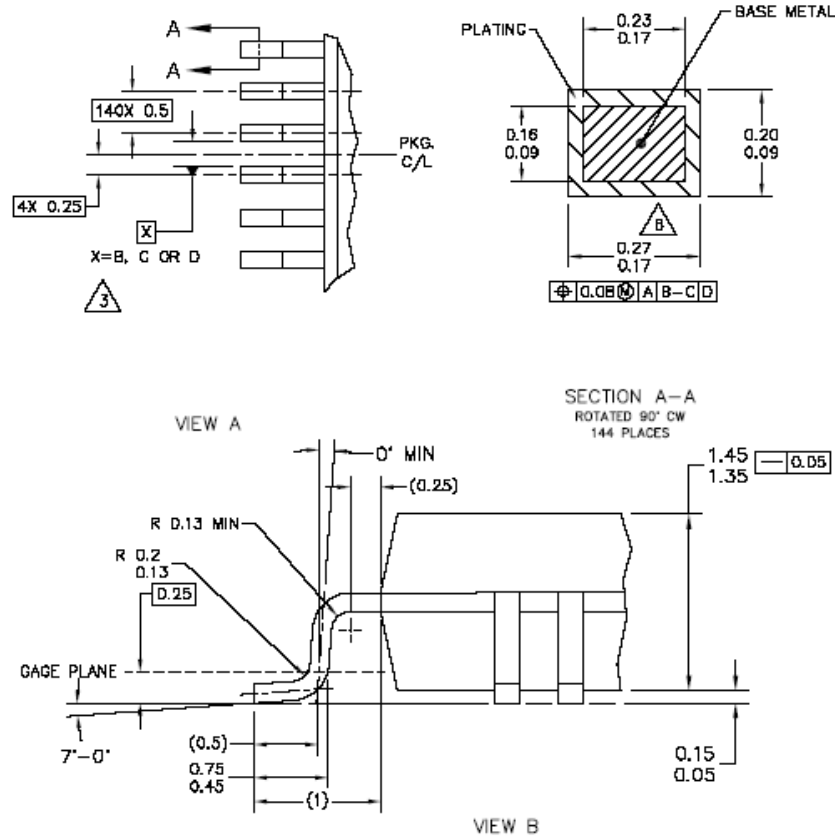
³ V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

⁴ Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

⁵ During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

⁶ This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

⁷ Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.



| | | | |
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| TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK | DOCUMENT NO: 9BASS2J177W | REV: F | |
| | CASE NUMBER: 91B-03 | 20 MAY 2005 | |
| | STANDARD: NON-JEDEC | | |

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 mm.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 32. 144 LQFP package mechanical drawing (2 of 2)

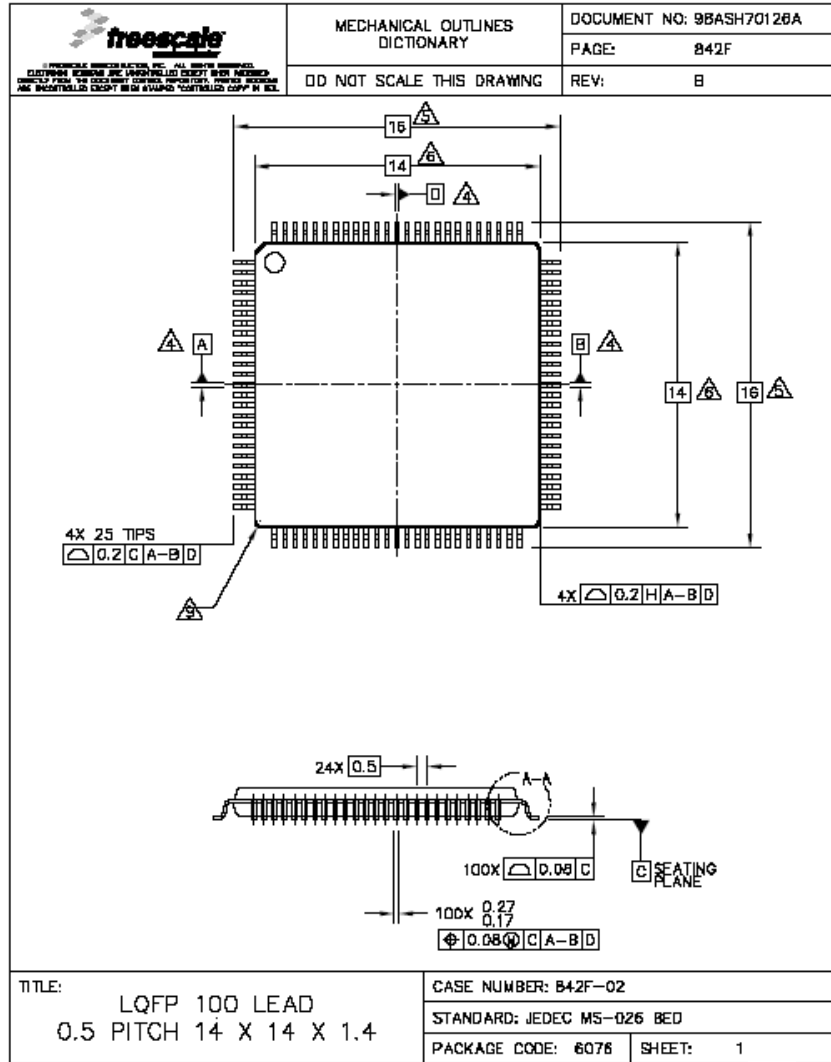


Figure 33. 100 LQFP package mechanical drawing (1 of 4)

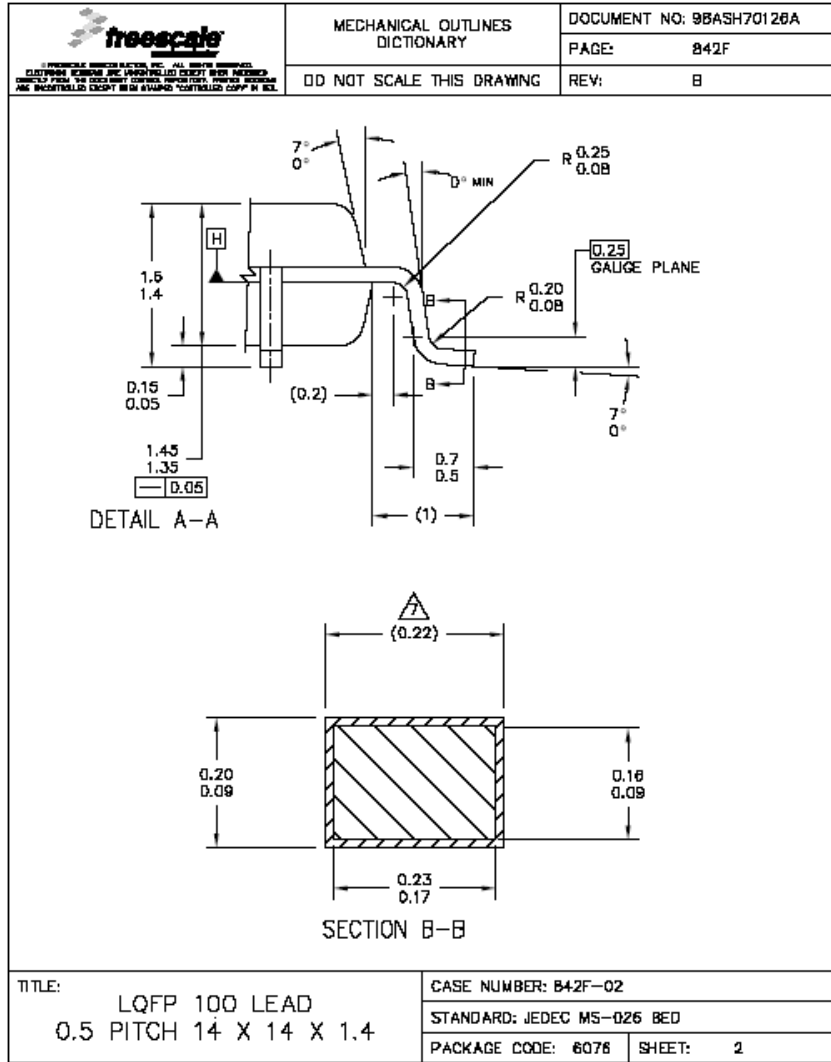


Figure 34. 100 LQFP package mechanical drawing (2 of 4)


| | | |
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| | DO NOT SCALE THIS DRAWING | PAGE: 842F REV: B |
| <p>1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.</p> <p>2. CONTROLLING DIMENSION: MILLIMETER</p> <p>3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.</p> <p>4. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.</p> <p>5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM C.</p> <p>6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.</p> <p>7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07.</p> <p>8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.</p> <p>9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.</p> | | |
| TITLE: LQFP 100 LEAD 0.5 PITCH 14 X 14 X 1.4 | | CASE NUMBER: B42F-02 STANDARD: JEDEC MS-026 BED PACKAGE CODE: 6076 SHEET: 3 |

Figure 35. 100 LQFP package mechanical drawing (3 of 4)


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|---|------------|---|----------------------------|--------------------------|--|
| | | | | PAGE: 842F | |
| | | | | REV: B | |
| LTR | ORIGINATOR | REVISIONS | DRAFTER | DATE | |
| B | FE WONG | UPDATED TO FREESCALE FORMAT. PACKAGE CODE WAS 8264. | F. WONG | APR 05, 05 | |
| Empty space for drawing content | | | | | |
| TITLE: | | | CASE NUMBER: B42F-02 | | |
| LQFP 100 LEAD | | | STANDARD: JEDEC MS-026 BEO | | |
| 0.5 PITCH 14 X 14 X 1.4 | | | PACKAGE CODE: 6076 | SHEET: 4 OF 4 | |

Figure 36. 100 LQFP package mechanical drawing (4 of 4)

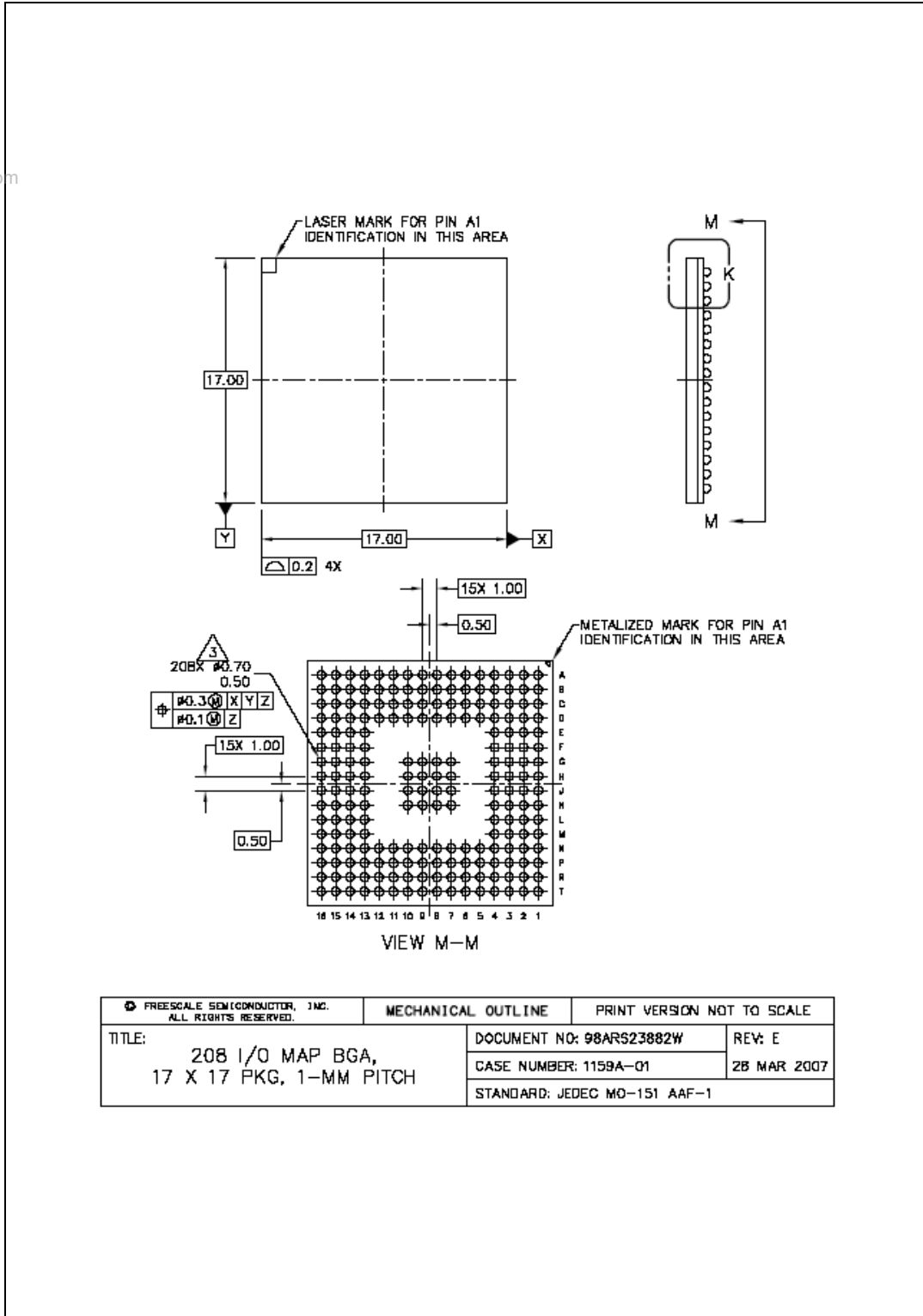
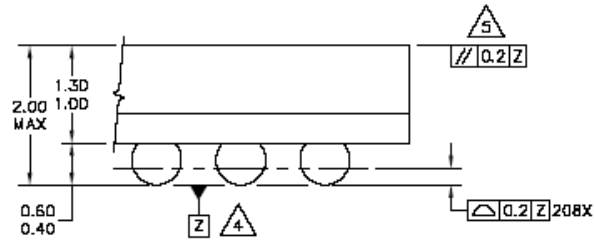


Figure 37. 208 MAPBGA package mechanical drawing (1 of 2)



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODE SUMMARY:
MAP BGA: 5253
MAP BGA PGE DIE: 5371

| | | | |
|---|--------------------|------------------------------|-------------|
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| TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1-MM PITCH | | DOCUMENT NO: 9BARS23BB2W | REV: E |
| | | CASE NUMBER: 1159A-01 | 28 MAR 2007 |
| | | STANDARD: JEDEC MO-151 AAF-1 | |

Figure 38. 208 MAPBGA package mechanical drawing (2 of 2)

6 Ordering information

Table 44. Orderable Part Number Summary

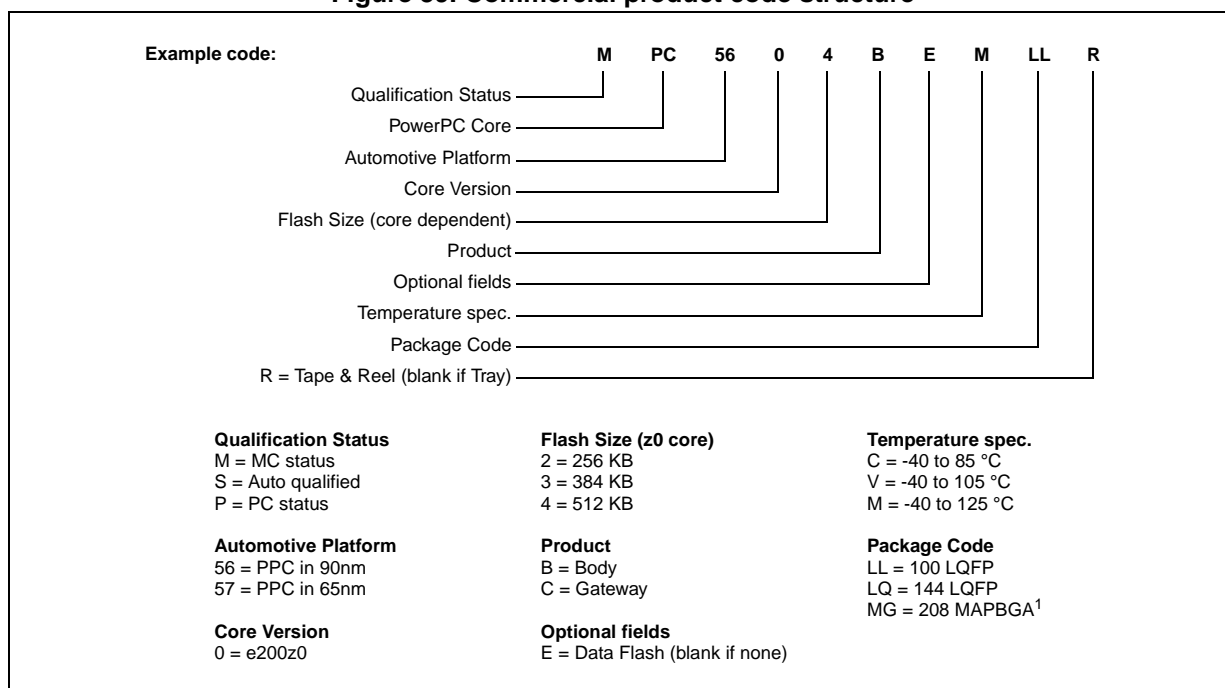
| Orderable Part Number | CPU | Code Flash / SRAM (Kbytes) | Package | Operating temp. (°C) | Speed (MHz) | Data Flash | Voltage | Packing |
|-----------------------|---------|----------------------------|----------|----------------------|-------------|------------|---------|-------------|
| MPC5602BEMLL | e200z0h | 256 / 24 | 100 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5602BEMLLR | | | | | | | | Tape & Reel |
| MPC5602BEMLQ | e200z0h | 256 / 24 | 144 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5602BEMLQR | | | | | | | | Tape & Reel |
| MPC5602CEMLL | e200z0h | 256 / 32 | 100 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5602CEMLLR | | | | | | | | Tape & Reel |
| MPC5603BEMLL | e200z0h | 384 / 28 | 100 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5603BEMLLR | | | | | | | | Tape & Reel |
| MPC5603BEMLQ | e200z0h | 384 / 28 | 144 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5603BEMLQR | | | | | | | | Tape & Reel |
| MPC5603CEMLL | e200z0h | 384 / 40 | 100 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5603CEMLLR | | | | | | | | Tape & Reel |
| MPC5602BEVLL | e200z0h | 256 / 24 | 100 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5602BEVLLR | | | | | | | | Tape & Reel |
| MPC5602BEVLQ | e200z0h | 256 / 24 | 144 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5602BEVLQR | | | | | | | | Tape & Reel |
| MPC5602CEVLL | e200z0h | 256 / 32 | 100 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5602CEVLLR | | | | | | | | Tape & Reel |
| MPC5603BEVLL | e200z0h | 384 / 28 | 100 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5603BEVLLR | | | | | | | | Tape & Reel |
| MPC5603BEVLQ | e200z0h | 384 / 28 | 144 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5603BEVLQR | | | | | | | | Tape & Reel |
| MPC5603CEVLL | e200z0h | 384 / 40 | 100 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5603CEVLLR | | | | | | | | Tape & Reel |
| MPC5604BEMLL | e200z0h | 512 / 32 | 100 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5604BEMLLR | | | | | | | | Tape & Reel |
| MPC5604BEMLQ | e200z0h | 512 / 32 | 144 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5604BEMLQR | | | | | | | | Tape & Reel |
| MPC5604BEVLL | e200z0h | 512 / 32 | 100 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5604BEVLLR | | | | | | | | Tape & Reel |

Table 44. Orderable Part Number Summary (continued)

| Orderable Part Number | CPU | Code Flash / SRAM (Kbytes) | Package | Operating temp. (°C) | Speed (MHz) | Data Flash | Voltage | Packing |
|-----------------------|---------|----------------------------|--------------------------|----------------------|-------------|------------|---------|-------------|
| MPC5604BEVLQ | e200z0h | 512 / 32 | 144 LQFP | -40 to 105 | 64 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5604BEVLQR | | | | | | | | Tape & Reel |
| MPC5604CEMLL | e200z0h | 512 / 48 | 100 LQFP | -40 to 125 | 60 | 4 x 16 KB | 3.3/5 V | Tray |
| MPC5604CEMLLR | | | | | | | | Tape & Reel |
| MPC5604BEMMG | e200z0h | 512 / 48 | 208 MAP BGA ¹ | -40 to 125 | 64 | 4 x 16 KB | 3.3/5 V | Tray |

¹ 208 MAPBGA available only as development package for Nexus2+

Figure 39. Commercial product code structure



¹ 208 MAPBGA available only as development package for Nexus2+

7 Document revision history

Table 45 summarizes revisions to this document.

Table 45. Revision history

| Revision | Date | Substantive changes |
|----------|------------|---------------------|
| 1 | 4-Apr-2008 | Initial release |

Table 45. Revision history (continued)

| Revision | Date | Substantive changes |
|----------|-------------|---|
| 1.1 | 15-Apr-2008 | <p>Added the following information missing in Rev. 1:</p> <ul style="list-style-type: none"> • Table headings in the “Device summary” table • Heading for the 208 MAPBGA column in the “System pin descriptions” and “Functional port pin descriptions” tables |
| 2 | 06-Mar-2009 | <p>Made minor editing and formatting changes to improve readability</p> <p>Harmonized oscillator naming throughout document</p> <p>Features:</p> <ul style="list-style-type: none"> —Replaced 32 KB with 48 KB as max SRAM size —Updated description of INTC —Changed max number of GPIO pins from 121 to 123 <p>Updated Section 1.1, “Introduction”</p> <p>Updated Table 2</p> <p>Added Section 2, “Device blocks”</p> <p>Section 3, “Package pinouts”: Removed signal descriptions (these are found in the device reference manual)</p> <p>Updated Figure 2:</p> <ul style="list-style-type: none"> —Replaced VPP with VSS_HV on pin 18 —Added MA[1] as AF3 for PC[10] (pin 28) —Added MA[0] as AF2 for PC[3] (pin 116) —Changed description for pin 120 to PH[10] / GPIO[122] / TMS —Changed description for pin 127 to PH[9] / GPIO[121] / TCK —Replaced NMI[0] with NMI on pin 11 <p>Updated Figure 3:</p> <ul style="list-style-type: none"> —Replaced VPP with VSS_HV on pin 14 —Added MA[1] as AF3 for PC[10] (pin 22) —Added MA[0] as AF2 for PC[3] (pin 77) —Changed description for pin 81 to PH[10] / GPIO[122] / TMS —Changed description for pin 88 to PH[9] / GPIO[121] / TCK —Removed E1UC[19] from pin 76 —Replaced [11] with WKUP[11] for PB[3] (pin 1) —Replaced NMI[0] with NMI on pin 7 <p>Updated Figure 4:</p> <ul style="list-style-type: none"> —Changed description for ball B8 from TCK to PH[9] —Changed description for ball B9 from TMS to PH[10] —Updated descriptions for balls R9 and T9 <p>Added Section 4.2, “Parameter Classification” and tagged parameters in tables where appropriate</p> <p>Added Section 4.3, “NVUSRO register”</p> <p>Updated Table 7</p> <p>Section 4.5, “Recommended operating conditions”: Added note on RAM data retention to end of section</p> <p>Updated Table 8 and Table 9</p> <p>Added Section 4.6.1, “Package thermal characteristics”</p> <p>Updated Section 4.6.2, “Power considerations”</p> <p>Updated Figure 5</p> <p>Updated Table 12, Table 13, Table 14, Table 15 and Table 16</p> |

Table 45. Revision history (continued)

| Revision | Date | Substantive changes |
|----------|-------------|--|
| 2 | 06-Mar-2009 | Updated Table 12 , Table 13 , Table 14 , Table 15 and Table 16 Added Section 4.7.4 , "Output pin transition times" Updated Table 19 Updated Figure 6 Updated Table 20 Section 4.9.1 , "Voltage regulator electrical characteristics": Amended description of LV_PLL Figure 8 : Exchanged position of symbols C _{DEC1} and C _{DEC2} Updated Table 21 |

Appendix A Abbreviations

[Table 40](#) lists abbreviations used but not defined elsewhere in this document.

Table 40. Abbreviations

| Abbreviation | Meaning |
|--------------|---|
| CMOS | Complementary metal–oxide–semiconductor |
| CPHA | Clock phase |
| CPOL | Clock polarity |
| CS | Peripheral chip select |
| EVTO | Event out |
| LED | Light emitting diode |
| MCKO | Message clock out |
| MDO | Message data out |
| MSEO | Message start/end out |
| MTFE | Modified timing format enable |
| SCK | Serial communications clock |
| SOUT | Serial data out |
| TBD | To be defined |
| TCK | Test clock input |
| TDI | Test data input |
| TDO | Test data output |
| TMS | Test mode select |

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