Section 22 Electrical Specifications

22.1 Absolute Maximum Ratings

Table 22-1 lists the absolute maximum ratings.

Table 22-1 Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	–0.3 to +7.0	V
Flash memory programming voltage		FV_{PP}	–0.3 to +13.0	V
Programming voltage		V_{PP}	–0.3 to +13.5	V
Input voltage	Pins other than Ports 7, MD_1,	V_{in}	–0.3 to V_{CC} + 0.3	V
	Port 7	V_{in}	–0.3 to AV_{CC} + 0.3	V
	MD_1	V_{in}	F-ZTAT version: –0.3 to +13.0 Other versions: –0.3 to V_{CC} + 0.3	V
Analog supply voltage		AV_{CC}	–0.3 to +7.0	V
Analog input voltage		V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature		T_{opr}	Regular specifications: –20 to +75	°C
			Wide-range specifications: –40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Note: Exceeding the absolute maximum ratings shown in table 20-1 can permanently destroy the chip.*

* FV_{PP} must not exceed 13 V and V_{PP} must not exceed 13.5 V, including peak overshoot. In the F-ZTAT version, MD_1 must not exceed 13 V, including peak overshoot.

22.2 Electrical Characteristics

22.2.1 DC Characteristics

Table 22-2 lists the DC characteristics of the 5-V version. Table 22-3 lists the DC characteristics of 4-V version. Table 22-4 lists the DC characteristics of the 3-V version. Table 22-5 gives the allowable current output values of the 5-V and 4-V versions. Table 22-6 gives the allowable current output values of the 3-V version. Bus drive characteristics common to 5 V, 4 V and 3 V versions are listed in table 22-7.

Table 22-2 DC Characteristics (5-V Version)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%*1, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$P6_7$ to $P6_0$*4, $\overline{IRQ_2}$ to $\overline{IRQ_0}$*5, $\overline{IRQ_7}$ to $\overline{IRQ_3}$,	(1)	V_T^-	1.0	—	—	V	
			VT+	—	—	Vcc × 0.7		
		0.4	V+ – VT–	0.4	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0, EXTAL, $\overline{NMI}$	(2)	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	SCL, SDA			V_{CC} × 0.7	—	V_{CC} + 0.3		
	$P7_7$ to $P7_0$			2.0	—	AV_{CC} + 0.3		
	All input pins other than (1) and (2) above			2.0	—	V_{CC} + 0.3		
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0	(3)	V_{IL}	–0.3	—	0.5	V	
	SCL, SDA			–0.3	—	1.0		
	All input pins other than (1) and (3) above			–0.3	—	0.8		
Output high voltage	All output pins*6		V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
				3.5	—	—	V	I_{OH} = –1.0m

Table 22-2 DC Characteristics (5-V Version) (cont)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%*1, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Output low voltage	All output pins*6		V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	$P1_7$ to $P1_0$, $P2_7$ to $P2_0$			—	—	1.0		I_{OL} = 10.0 mA
Input leakage current	$\overline{RES}$, $\overline{STBY}$		$\lvert I_{in} \rvert$	—	—	10.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V
	$\overline{NMI}$, MD_1, MD_0			—	—	1.0		
	$P7_7$ to $P7_0$			—	—	1.0		Vin = 0.5 V to AV_{CC} – 0.5 V
Leakage current in three-state (off state)	Ports 1 to 6, 8, 9,		$\lvert I_{TSI} \rvert$	—	—	1.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 3		$-I_P$	30	—	250	µA	Vin = 0 V
	Ports 6			60	—	500		
Input capacitance	$\overline{STBY}$ (F-ZTAT version)	(4)	C_{in}	—	—	120	pF	Vin = 0 V, f = 1MHz, Ta = 25°C
	$\overline{RES}$, $\overline{STBY}$ (except F-ZTAT version)			—	—	60		
	$\overline{NMI}$, MD_1			—	—	50		
	$P9_7$, $P8_6$			—	—	20		
	All input pins other than (4)			—	—	15		
Current dissipation*2	Normal operation		I_{CC}	—	27	45	mA	f = 12 MHz
				—	36	60		f = 16 MHz
	Sleep mode			—	18	30		f = 12 MHz
				—	24	40		f = 16 MHz
	Standby modes*3			—	0.01	5.0	µA	Ta ≤ 50°C
				—	—	20.0		50°C < Ta

Table 22-2 DC Characteristics (5-V Version) (cont)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%[*1], V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog supply current	During A/D conversion	AI_{CC}	—	2.0	5.0	mA	
	During A/D and D/A conversion		—	2.0	5.0		
	A/D and D/A conversion idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 5.5 V
Analog supply voltage[*1]		AV_{CC}	4.5	—	5.5	V	During operation
			2.0	—	5.5		While idle or when not in use
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Even when the A/D and D/A converters are not used, connect AV_{CC} to power supply V_{CC} and keep the applied voltage between 2.0 V and 5.5 V.
2. Current dissipation values assume that $V_{IH\ min}$ = V_{CC} – 0.5 V, $V_{IL\ max}$ = 0.5 V, all output pins are in the no-load state, and all input pull-up transistors are off.
3. For these values it is assumed that V_{RAM} • V_{CC} < 4.5 V and $V_{IH\ min}$ = V_{CC} × 0.9, $V_{IL\ max}$ = 0.3 V.
4. $P6_7$ to $P6_0$ include supporting module inputs multiplexed with them.
5. $\overline{IRQ_2}$ includes $\overline{ADTRG}$ multiplexed with it.
6. Applies when IICE = 0. The output low level is determined separately when the bus drive function is selected.

Table 22-3 DC Characteristics (4-V Version)

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$P6_7$ to $P6_0$*4, $\overline{IRQ}_2$ to $\overline{IRQ}_0$*5, $\overline{IRQ}_7$ to $\overline{IRQ}_3$	(1)	V_T^-	1.0	—	—	V	V_{CC} = 4.5 V to 5.5 V
			V_T^+	—	—	V_{CC} × 0.7		
			$V_T^+ - V_T^-$	0.4	—	—		
			V_T^-	0.8	—	—		V_{CC} = 4.0 V to 4.5 V
			V_T^+	—	—	V_{CC} × 0.7		
			$V_T^+ - V_T^-$	0.3	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0, EXTAL, $\overline{NMI}$	(2)	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	SCL, SDA			V_{CC} × 0.7	—	V_{CC} + 0.3		
	$P7_7$ to $P7_0$			2.0	—	AV_{CC} + 0.3		
	All input pins other than (1) and (2) above			2.0	—	V_{CC} + 0.3		
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0	(3)	V_{IL}	–0.3	—	0.5	V	
	SCL, SDA			–0.3	—	1.0		V_{CC} = 4.5 V to 5.5 V
				–0.3	—	0.8		V_{CC} = 4.0 V to 4.5 V
	All input pins other than (1) and (3) above			–0.3	—	0.8		V_{CC} = 4.5 V to 5.5 V Vcc
				–0.3	—	0.6		V_{CC} = 4.0 V to 4.5 V
Output high voltage	All output pins *6		V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
				3.5	—	—		I_{OH} = –1.0 mA, V_{CC} = 4.5 V to

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
							5.5 V
			2.8	—	—		I_{OH} = –1.0 mA, V_{CC} = 4.0 V to 4.5 V
Output low voltage	All output pins *6	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	$P1_7$ to $P1_0$, $P2_7$ to $P2_0$		—	—	1.0		I_{OL} = 10.0 mA
Input leakage current	$\overline{RES}$, $\overline{STBY}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V
	$\overline{NMI}$, MD_1, MD_0		—	—	1.0		
	$P7_7$ to $P7_0$		—	—	1.0		Vin = 0.5 V to AV_{CC} – 0.5 V
Leakage current in three-state(off state)	Ports 1 to 6, 8, 9,	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V,
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	250	µA	Vin = 0 V, VCC = 4.5 V to 5.5 V
	Ports 6		60	—	500		
	Ports 1 to 3		20	—	200		Vin = 0 V, VCC = 4.0 V to 4.5 V
	Ports 6		40	—	400		
Input capacitance	$\overline{STBY}$ (F-ZTAT (4) version)	C_{in}	—	—	120	pF	Vin = 0 V, f = 1MHz, Ta = 25°C
	$\overline{RES}$, $\overline{STBY}$ (except F-ZTAT version)		—	—	60		
	$\overline{NMI}$, MD_1		—	—	50		
	$P9_7$, $P8_6$		—	—	20		
	All input pins other than (4) above		—	—	15		

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*2	Normal operation	I_{CC}	—	27	45	mA	f = 12 MHz
			—	36	60		f = 16 MHz, V_{CC} = 4.5 V to 5.5 V
	Sleep mode		—	18	30		f = 12 MHz
			—	24	40		f = 16 MHz, V_{CC} = 4.5 V to 5.5 V
	Standby modes*3		—	0.01	5.0	µA	Ta ≤ 50°C
			—	—	20.0		50°C < Ta
Analog supply current	During A/D conversion	AI_{CC}	—	2.0	5.0	mA	
	During A/D and D/A conversion		—	2.0	5.0		
	A/D and D/A conversion idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 5.5 V
Analog supply voltage*1		AV_{CC}	4.0	—	5.5	V	During operation
			2.0	—	5.5		While idle or when not in use
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Even when the A/D and D/A converters are not used, connect AV_{CC} to power supply V_{CC} and keep the applied voltage between 2.0 V and 5.5 V.

2. Current dissipation values assume that $V_{IH\,min} = V_{CC} - 0.5$ V, $V_{IL\,max} = 0.5$ V, all output pins are in the no-load state, and all input pull-up transistors are off.
3. For these values it is assumed that $V_{RAM} \bullet V_{CC} < 4.0$ V and $V_{IH\,min} = V_{CC} \times 0.9$, $V_{IL\,max} = 0.3$ V.
4. $P6_7$ to $P6_0$ include supporting module inputs multiplexed with them.
5. IRQ_2 includes $\overline{ADTRG}$ multiplexed with it.
6. Applies when IICE = 0. The output low level is determined separately when the bus drive function is selected.

Table 22-4 DC Characteristics (3-V Version)

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V*1, $V_{SS} = AV_{SS}$ = 0 V, Ta = –20°C to +75°C

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$P6_7$ to $P6_0$*4, $\overline{IRQ}$ 2 to $\overline{IRQ0}$*5, $\overline{IRQ_7}$ to $\overline{IRQ_3}$	(1)	V_T^-	$V_{cc} \times 0.15$	—	—	V	
			V_T^+	—	—	VCC × 0.7		
			$V_T^+ - V_T^-$	0.2	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0, EXTAL, $\overline{NMI}$	(2)	V_{IH}	$V_{cc} \times 0.9$	—	V_{cc} + 0.3	V	
	SCL, SDA			$V_{cc} \times 0.7$	—	V_{cc} + 0.3		
	$P7_7$ to $P7_0$			$V_{cc} \times 0.7$	—	AV_{cc} + 0.3		
	All input pins other than (1) and (2) above			$V_{cc} \times 0.7$	—	V_{cc} + 0.3		
Input low voltage*4	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0	(3)	V_{IL}	–0.3	—	$V_{cc} \times 0.1$	V	
	SCL, SDA			–0.3	—	V_{cc} × 0.15		
	All input pins other than (1) and (3) above			–0.3	—	V_{cc} × 0.15		
Output high voltage	All output pins*6		V_{OH}	V_{cc} – 0.5	—	—	V	I_{OH} = –200 µA
				VCC – 1.0	—	—		I_{OH} = –1 mA
Output low voltage	All output pins*6		V_{OL}	—	—	0.4	V	I_{OL} = 0.8 mA
	P17 to P10, $P2_7$ to $P2_0$			—	—	0.4		I_{OL} = 1.6 mA
Input leakage	$\overline{RES}$, $\overline{STBY}$		| I_{in} |	—	—	10.0	µA	Vin = 0.5 V to V_{cc} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
current							
	$\overline{NMI}$, MD_1, MD_0		—	—	1.0		
	$P7_7$ to $P7_0$		—	—	1.0		Vin = 0.5 V to AV_{CC} – 0.5 V
Leakage current in three-state(off state)	Ports 1 to 6, 8, 9	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V,
Input pull-up MOS current	Ports 1 to 3	$-I_p$	3	—	120	µA	Vin = 0 V, V_{CC} = 2.7 V to 3.6 V
	6		30	—	250		
Input capacitance	$\overline{STBY}$ (F-ZTAT (4) version)	C_{in}	—	—	120	pF	Vin = 0 V, f = 1MHz, Ta = 25°C
	$\overline{RES}$, $\overline{STBY}$ (except F-ZTAT version)		—	—	60		
	$\overline{NMI}$, MD_1		—	—	50		
	$P9_7$, $P8_6$		—	—	20		
	All input pins other than (4) above		—	—	15		
Current dissipation[*2]	Normal operation	I_{CC}	—	7	—	mA	f = 6 MHz, V_{CC} = 2.7 V to 3.6 V
			—	12	22		f = 10 MHz, V_{CC} = 2.7 V to 3.6 V
			—	25	—		f = 10 MHz, V_{CC} = 4.0 V to5.5 V
	Sleep mode		—	5	—		f = 6 MHz, V_{CC} = 2.7 V to 3.6 V
			—	9	16		f = 10 MHz, V_{CC} = 2.7 V to 3.6 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
			—	18	—		f = 10 MHz, V_{CC} = 4.0 V to 5.5 V
	Standby modes[3]		—	0.01	5.0	µA	Ta ≤ 50°C
			—	—	20.0		50°C < Ta
Analog supply current	During A/D conversion	AI_{CC}	—	2.0	5.0	mA	
	During A/D and D/A conversion		—	2.0	5.0		
	A/D and D/A conversion idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 5.5 V
Analog supply voltage[1]		AV_{CC}	2.7	—	5.5	V	During operation
			2.0	—	5.5		While idle or when not in use
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Even when the A/D and D/A converters are not used, connect AV_{CC} to power supply V_{CC} and keep the applied voltage between 2.0 V and 5.5 V.
2. Current dissipation values assume that $V_{IH\,min} = V_{CC} - 0.5$ V, $V_{IL\,max} = 0.5$ V, all output pins are in the no-load state, and all input pull-up transistors are off.
3. For these values it is assumed that $V_{RAM} \bullet V_{CC} < 2.7$ V and $V_{IH\,min} = V_{CC} \times 0.9$, $V_{IL\,max} = 0.3$ V.
4. $P6_7$ to $P6_0$ include supporting module inputs multiplexed with them.
5. IRQ_2 includes $\overline{ADTRG}$ multiplexed with it.
6. Applies when IICE = 0. The output low level is determined separately when the bus drive function is selected.

Table 22-5 Allowable Output Current Values (5-V and 4-V Versions)

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	SCL, SDA (bus drive selection)	I_{OL}	—	—	20	mA
	Ports 1 and 2		—	—	10	
	Other output pins		—	—	2	
Allowable output low (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	80	mA
	Total of all output		—	—	120	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output high current (total)	Total of all output	$\Sigma-I_{OH}$	—	—	40	mA

Table 22-6 Allowable Output Current Values (3-V Version)

Conditions: V_{CC} = 2.7 to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	SCL, SDA (bus drive selection)	I_{OL}	—	—	10	mA
	Ports 1 and 2		—	—	2	
	Other output pins		—	—	1	
Allowable output low (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	40	mA
	Total of all output		—	—	60	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output high current (total)	Total of all output	$\Sigma-I_{OH}$	—	—	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current values in tables 22-5 and 22-6. In particular, when driving a darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 22-1 and 22-2.

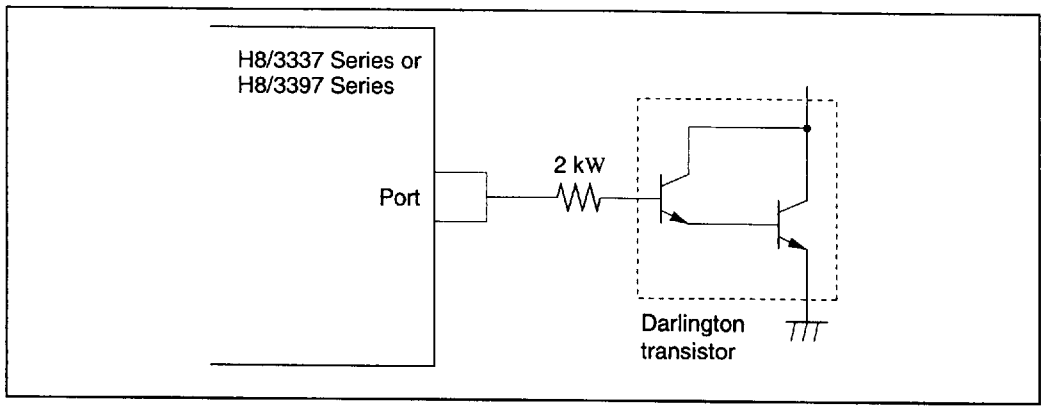


Figure 22-1 Example of Circuit for Driving a Darlington Transistor (5-V Version)

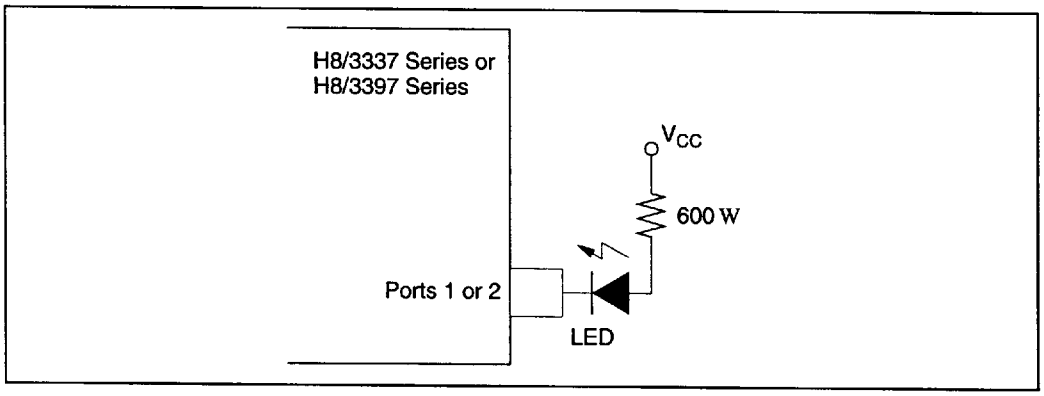


Figure 22-2 Example of Circuit for Driving an LED (5-V Version)

Table 22-7 Bus Drive Characteristics

Conditions: V_{SS} = 0 V, Ta = –20 to 75°C

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Output low voltage	SCL, SDA (bus drive selection)	V_{OL}	—	—	0.5	V	V_{CC} = 5 V ±10% I_{OL} = 16 mA
			—	—	0.5		V_{CC} = 2.7 V to 5.5 V I_{OL} = 8 mA

22.2.2 AC Characteristics

The AC characteristics are listed in following tables. Bus timing parameters are given in table 22-8, control signal timing parameters in table 22-9, timing parameters of the on-chip supporting modules in table 22-10, I^2C bus timing parameters in table 22-11, and external clock output delay timing parameters in table 22-12.

Table 22-8 Bus Timing

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

		Condition C		Condition B		Condition A			
		10 MHz		12 MHz		16 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Clock cycle time	t_{cyc}	100	500	83.3	500	62.5	500	ns	Fig. 22-4
Clock pulse width low	t_{CL}	30	–	30	–	20	–	ns	
Clock pulse width high	t_{CH}	30	–	30	–	20	–	ns	
Clock rise time	t_{Cr}	–	20	–	10	–	10	ns	
Clock fall time	t_{Cf}	–	20	–	10	–	10	ns	
Address delay time	t_{AD}	–	50	–	35	–	30	ns	
Address hold time	t_{AH}	20	–	15	–	10	–	ns	
Address strobe delay time	t_{ASD}	–	50	–	35	–	30	ns	
Write strobe delay time	t_{WSD}	–	50	–	35	–	30	ns	
Strobe delay time	t_{SD}	–	50	–	35	–	30	ns	
Write strobe pulse width*1	t_{WSW}	110	–	90	–	60	–	ns	
Address setup time 1*1	t_{AS1}	15	–	10	–	10	–	ns	
Address setup time 2*1	t_{AS2}	65	–	50	–	40	–	ns	
Read data setup time	t_{RDS}	35	–	20	–	20	–	ns	
Read data hold time*1	t_{RDH}	0	–	0	–	0	–	ns	
Read data access time*1	t_{ACC}	–	170	–	160	–	110	ns	
Write data delay time	t_{WDD}	–	80/75*2	–	65/60*2	–	60	ns	
Write data setup time	t_{WDS}	0/5*2	–	0/5*2	–	0/5*2	–	ns	
Write data hold time	t_{WDH}	20	–	20	–	20	–	ns	
Wait setup time	t_{WTS}	40	–	35	–	30	–	ns	Fig. 22-5
Wait hold time	t_{WTH}	10	–	10	–	10	–	ns	

Note: *1 Values at maximum operating frequency
*2 H8/3337YF-ZTAT version/other products

Table 22-9 Control Signal Timing

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

		Condition C 10 MHz		Condition B 12 MHz		Condition A 16 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RES}$ setup time	t_{RESS}	300	–	200	–	200	–	ns	Fig. 22-6
$\overline{RES}$ pulse width	t_{RESW}	10	–	10	–	10	–	t_{cyc}	
$\overline{NMI}$ setup time ($\overline{NMI}$, IRQ_0 to IRQ_7)	t_{NMIS}	300	–	150	–	150	–	ns	Fig. 22-7
$\overline{NMI}$ hold time ($\overline{NMI}$, IRQ_0 to IRQ_7)	t_{NMIH}	10	–	10	–	10	–	ns	
Interrupt pulse width for recovery from software standby mode ($\overline{NMI}$, IRQ_0 to IRQ_2, IRQ_6)	t_{NMIW}	300	–	200	–	200	–	ns	
Crystal oscillator settling time (reset)	t_{OSC1}	20	–	20	–	20	–	ms	Fig. 22-8
Crystal oscillator settling time (software standby)	t_{OSC2}	8	–	8	–	8	–	ms	Fig. 22-9

- Measurement Conditions for AC Characteristics

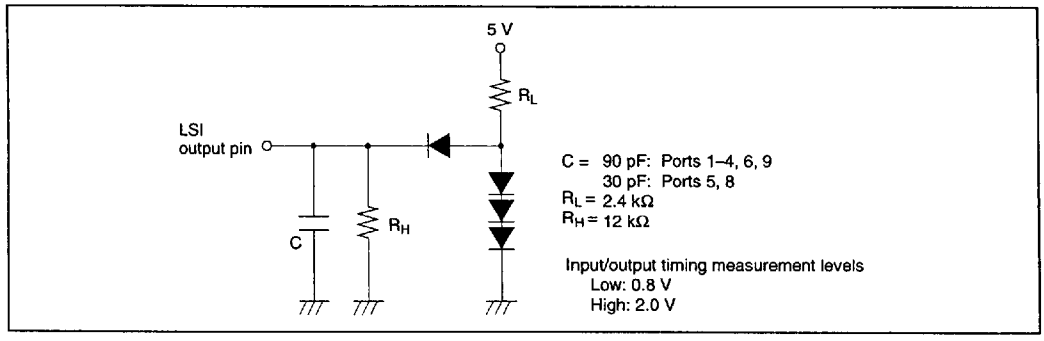


Figure 22-3 Output Load Circuit

Table 22-10 Timing Conditions of On-Chip Supporting Modules

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

			Condition C		Condition B		Condition A			
			10 MHz		12 MHz		16 MHz			
Item		Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
FRT	Timer output delay time	t_{FTOD}	–	150	–	100	–	100	ns	Fig. 22-10
	Timer input setup time	t_{FTIS}	80	–	50	–	50	–	ns	
	Timer clock input setup time	t_{FTCS}	80	–	50	–	50	–	ns	Fig. 22-11
	Timer clock pulse width	t_{FTCWH} t_{FTCWL}	1.5	–	1.5	–	1.5	–	t_{cyc}	
TMR	Timer output delay time	t_{TMOD}	–	150	–	100	–	100	ns	Fig. 22-12
	Timer reset input setup time	t_{TMRS}	80	–	50	–	50	–	ns	Fig. 22-14
	Timer clock input setup time	t_{TMCS}	80	–	50	–	50	–	ns	Fig. 22-13
	Timer clock pulse width (single edge)	t_{TMCWH}	1.5	–	1.5	–	1.5	–	t_{cyc}	
	Timer clock pulse width (both edges)	t_{TMCWL}	2.5	–	2.5	–	2.5	–	t_{cyc}	
PWM	Timer output delay time	t_{PWOD}	–	150	–	100	–	100	ns	Fig. 22-15
SCI	Input clock cycle (Async)	t_{Scyc}	4	–	4	–	4	–	t_{cyc}	Fig. 22-16
	(Sync)	t_{Scyc}	6	–	6	–	6	–	t_{cyc}	
	Transmit data delay time (Sync)	t_{TXD}	–	200	–	100	–	100	ns	
	Receive data setup time (Sync)	t_{RXS}	150	–	100	–	100	–	ns	
	Receive data hold time (Sync)	t_{RXH}	150	–	100	–	100	–	ns	
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	Fig. 22-17
Ports	Output data delay time	t_{PWD}	–	150	–	100	–	100	ns	Fig. 22-18
	Input data setup time	t_{PRS}	80	–	50	–	50	–	ns	
	Input data hold time	t_{PRH}	80	–	50	–	50	–	ns	

Table 22-10 Timing Conditions of On-Chip Supporting Modules (cont)

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

			Condition C		Condition B		Condition A			
			10 MHz		12 MHz		16 MHz			
Item		Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
HIF read cycle	$\overline{CS}$/HA_0 setup time	t_{HAR}	10	–	10	–	10	–	ns	Fig. 22-19
	$\overline{CS}$/HA_0 hold time	t_{HRA}	10	–	10	–	10	–	ns	
	$\overline{IOR}$ pulse width	t_{HRPW}	220	–	120	–	120	–	ns	
	HDB delay time	t_{HRD}	–	200	–	100	–	100	ns	
	HDB hold time	t_{HRF}	0	40	0	25	0	25	ns	
	HIRQ delay time	t_{HIRQ}	–	200	–	120	–	120	ns	
HIF write cycle	$\overline{CS}$/HA_0 setup time	t_{HAW}	10	–	10	–	10	–	ns	Fig. 22-20
	$\overline{CS}$/HA_0 hold time	t_{HWA}	10	–	10	–	10	–	ns	
	$\overline{IOW}$ pulse width	t_{HWPW}	100	–	60	–	60	–	ns	
	HDB setup time High-speed GATE A_{20} not used	t_{HDW}	50	–	30	–	30	–	ns	
	High-speed GATE A_{20} uesd		85	–	55	–	45	–		
	HDB hold time	t_{HWD}	25	–	15	–	15	–	ns	
	GA_{20} delay time	t_{HGA}	–	180	–	90	–	90	ns	

Table 22-11 I^2C Bus Timing

Conditions: V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, Ta = –20°C to +75°C

Item	Symbol	Rating			Unit	Test Condition	Note
		Min	Typ	Max			
SCL clock cycle time	t_{SCL}	$12t_{cyc}$	—	—	ns		Figure 22-21
SCL clock high pulse width	t_{SCLH}	$3t_{cyc}$	—	—	ns		
SCL clock low pulse width	t_{SCLL}	$5t_{cyc}$	—	—	ns		
SCL, SDA rise time	t_{Sr}	—	—	1000	ns	Normal mode 100 kbit/s (max)	
		$20 + 0.1C_b$	—	300		High-speed mode 400 kbit/s (max)	
SCL, SDA fall time	t_{Sf}	—	—	300	ns	Normal mode 100 kbit/s (max)	
		$20 + 0.1C_b$	—	300		High-speed mode 400 kbit/s (max)	
SDA bus free time	t_{BUF}	$7t_{cyc} - 300$	—	—	ns		
SCL start condition hold time	t_{STAH}	$3t_{cyc}$	—	—	ns		
SCL resend start condition hold time	t_{STAS}	$3t_{cyc}$	—	—	ns		
SDA stop condition setup time	t_{STOS}	$3t_{cyc}$	—	—	ns		
SDA data setup time	t_{SDAS}	$1t_{cyc} + 10$	—	—	ns		
SDA data hold time	t_{SDAH}	0	—	—	ns		
SDA load capacitance	C_b	—	—	400	pF		

Table 22-12 External clock output delay Timing

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V,
$V_{SS} = AV_{SS}$ = 0V, Ta = – 40°C to +85°C

Item	Symbol	Min	Max	Unit	Notes
External clock output delay time	t_{DEXT}	500	—	µs	fig-22-22

Note: * t_{DEXT} includes to $\overline{RES}$ pulse width t_{RESW} (10 t_{cyc}).

22.2.3 A/D Converter Characteristics

Table 22-13 lists the characteristics of the on-chip A/D converter.

Table 22-13 A/D Converter Characteristics

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, $V_{SS} = AV_{SS}$ = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = – 40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, $V_{SS} = AV_{SS}$ = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = – 40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, $V_{SS} = AV_{SS}$ = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

	Condition C			Condition B			Condition A			
	10 MHz			12 MHz			16 MHz			
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion (single mode)*	—	—	13.4	—	—	11.2	—	—	8.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal source impedance	—	—	5	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	±6.0	—	—	±3.0	—	—	±3.0	LSB
Offset error	—	—	±4.0	—	—	±3.5	—	—	±3.5	LSB
Full-scale error	—	—	±4.0	—	—	±3.5	—	—	±3.5	LSB
Quantizing error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±4.0	—	—	±4.0	LSB

Note: * Values at maximum operating frequency

22.2.4 D/A Converter Characteristics (H8/3337 Series Only)

Table 22-14 lists the characteristics of the on-chip D/A converter.

Table 22-14 D/A Converter Characteristics

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = – 40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C (regular specifications), Ta = – 40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

	Condition C			Condition B			Condition A				
	10 MHz			12 MHz			16 MHz				
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Resolution	8	8	8	8	8	8	8	8	8	Bits	
Conversion time (settling time)	—	—	10.0	—	—	10.0			10.0	µs	30 pF load capacitance
Absolute accuracy	—	±2.0	±3.0	—	±1.0	±1.5	—	±1.0	±1.5	LSB	2 MΩ load resistance
	—	—	±2.0	—	—	±1.0	—	—	±1.0	LSB	4 MΩ load resistance

22.3 MCU Operational Timing

This section provides the following timing charts:

22.3.1 Bus Timing

(1) Basic Bus Cycle (without Wait States) in Expanded Modes

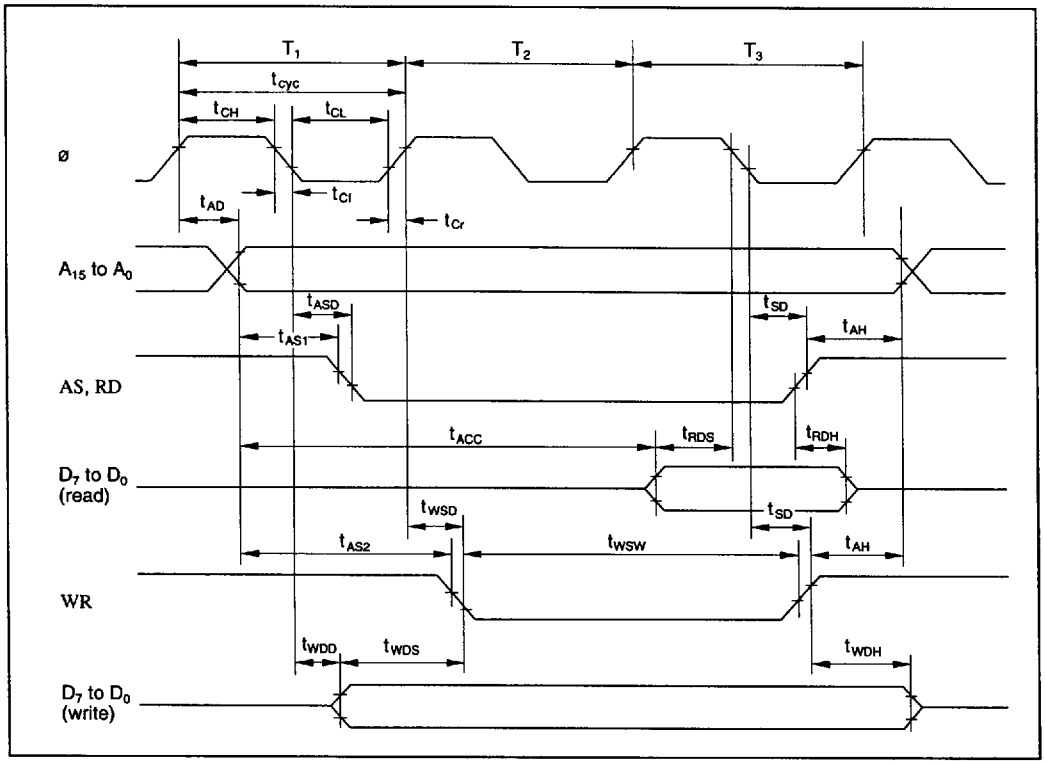


Figure 22-4 Basic Bus Cycle (without Wait States) in Expanded Modes

(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

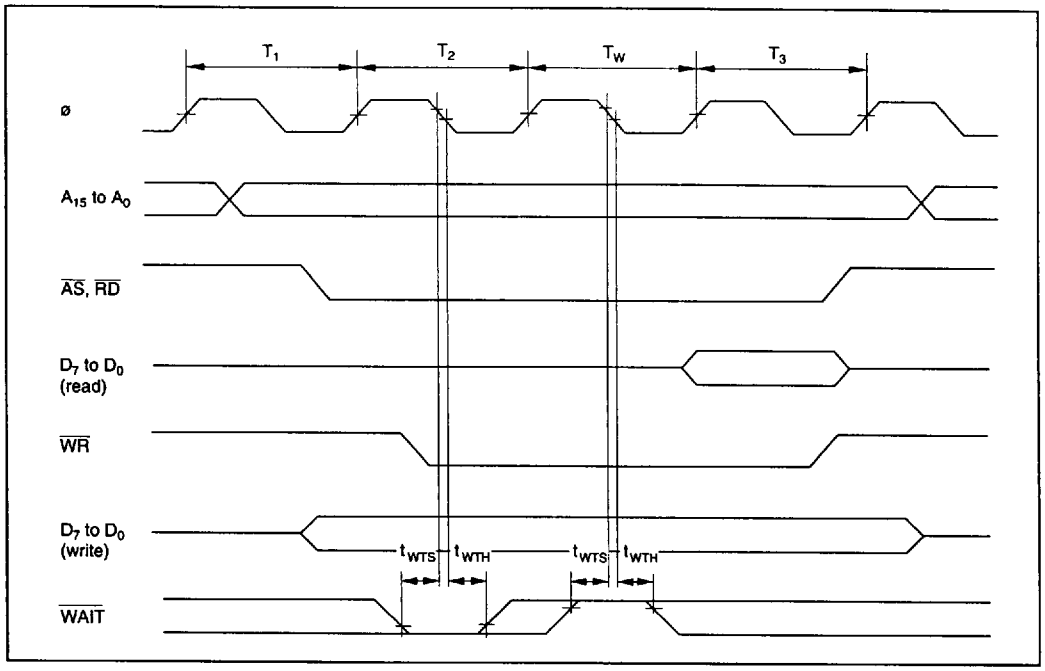


Figure 22-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes (Modes 1 and 2)

22.3.2 Control Signal Timing

(1) Reset Input Timing

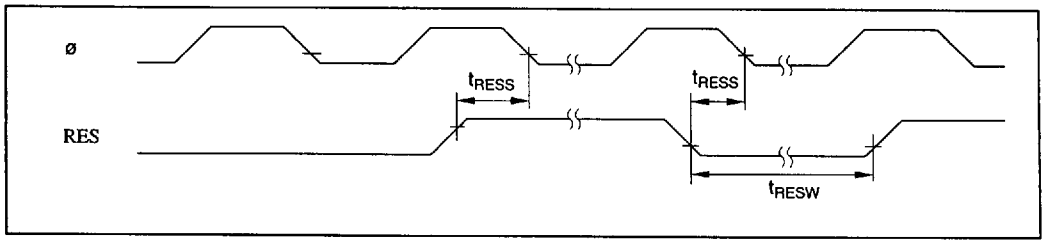


Figure 22-6 Reset Input Timing

(2) Interrupt Input Timing

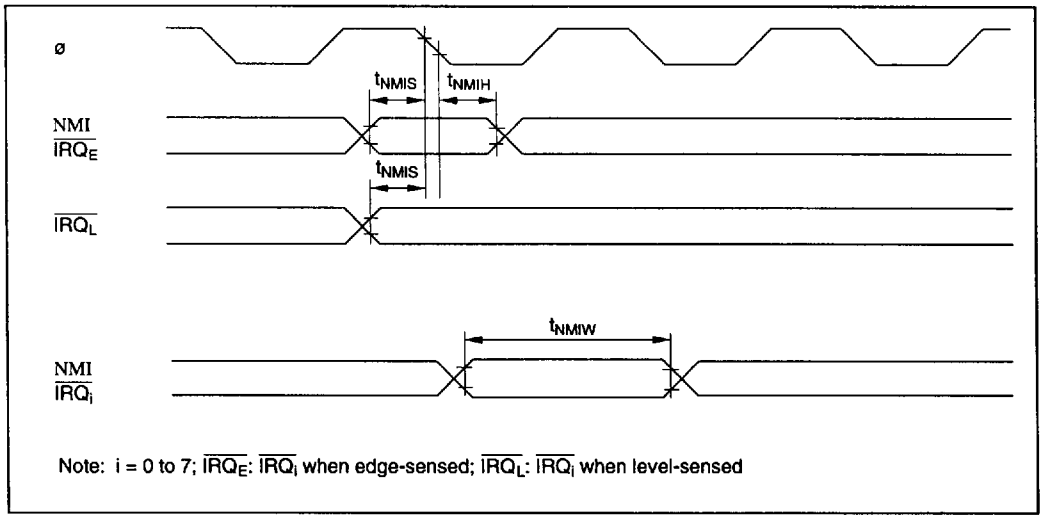


Figure 22-7 Interrupt Input Timing

(3) Clock Settling Timing

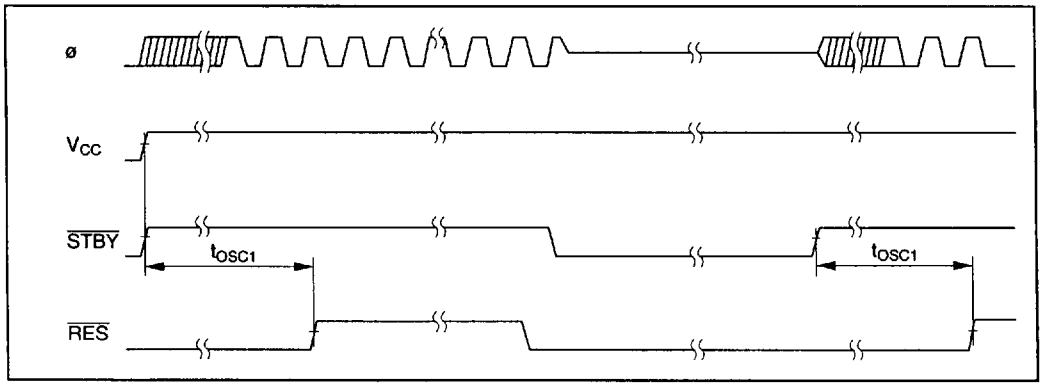


Figure 22-8 Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

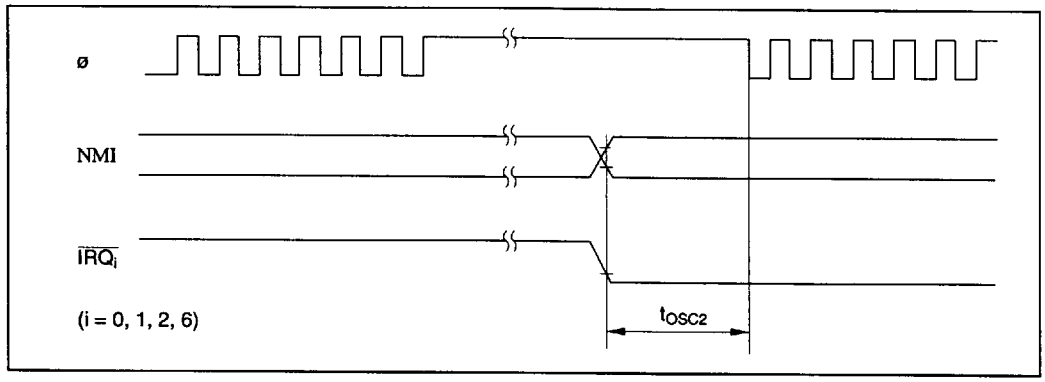


Figure 22-9 Clock Settling Timing for Recovery from Software Standby Mode

22.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

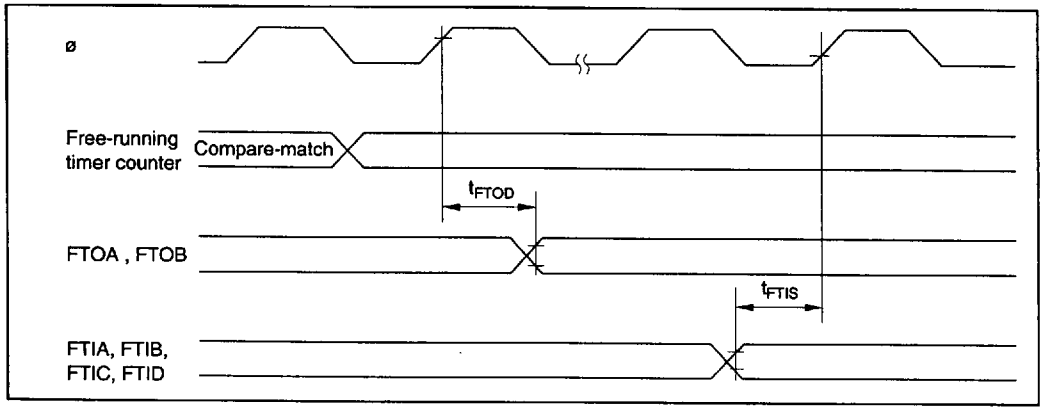


Figure 22-10 Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

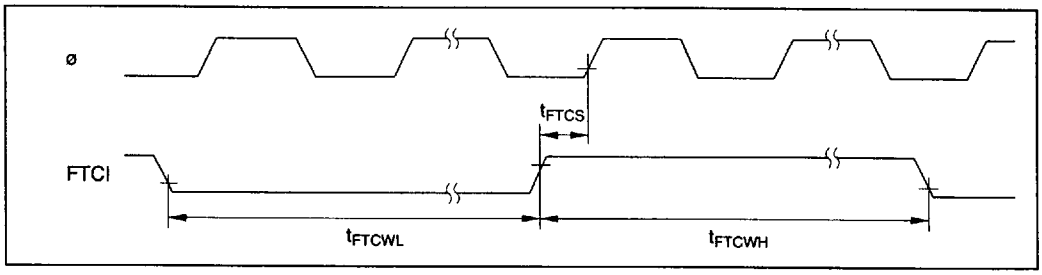


Figure 22-11 External Clock Input Timing for Free-Running Timer

22.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

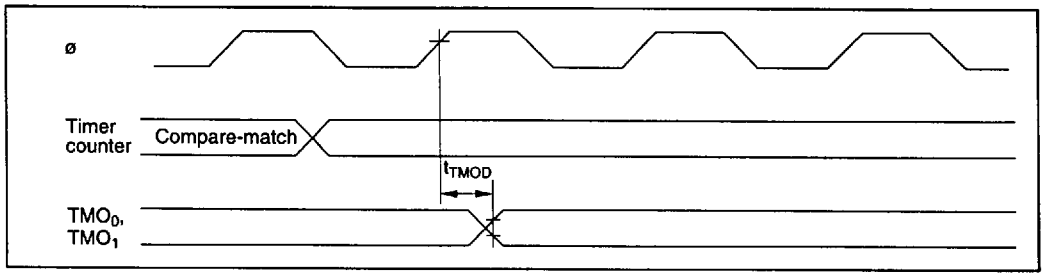


Figure 22-12 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

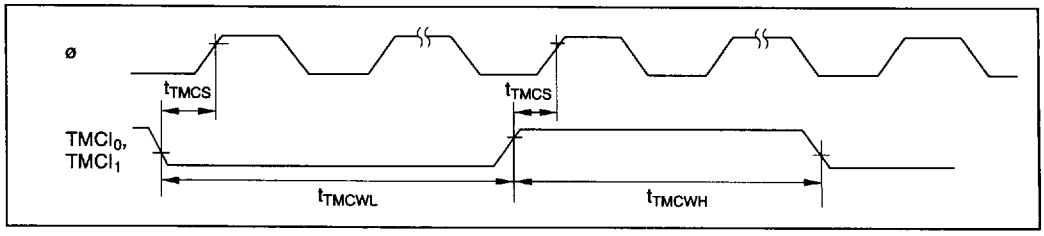


Figure 22-13 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

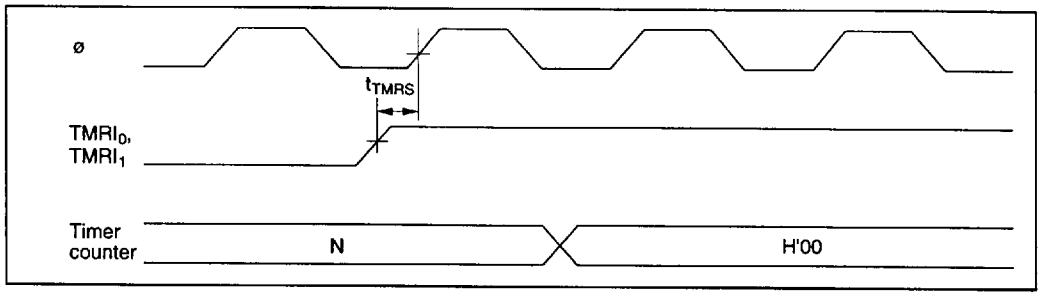


Figure 22-14 8-Bit Timer Reset Input Timing

22.3.5 Pulse Width Modulation Timer Timing

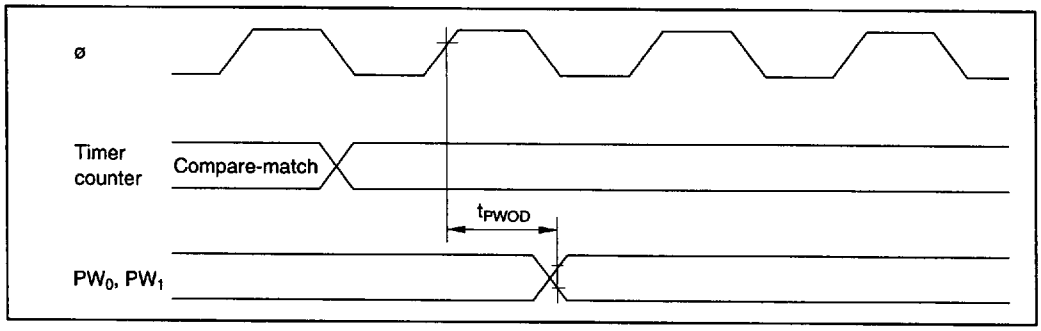


Figure 22-15 PWM Timer Output Timing

22.3.6 Serial Communication Interface Timing

(1) SCI Input/Output Timing

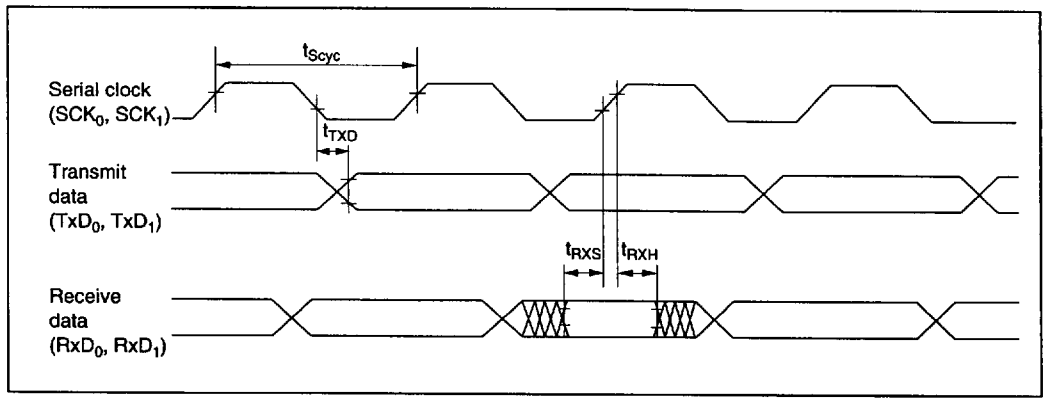


Figure 22-16 SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

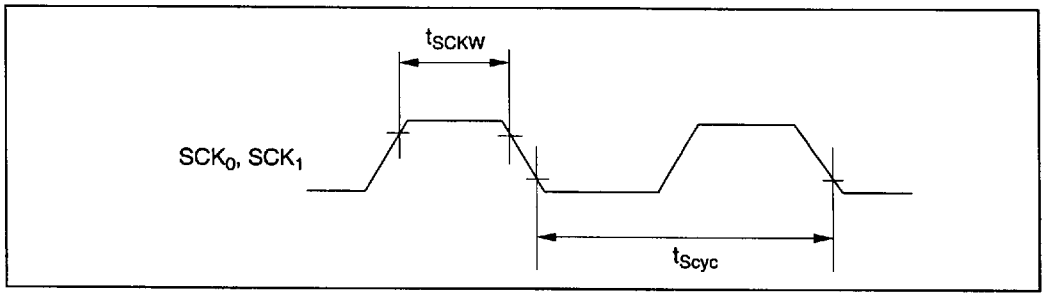


Figure 22-17 SCI Input Clock Timing

22.3.7 I/O Port Timing

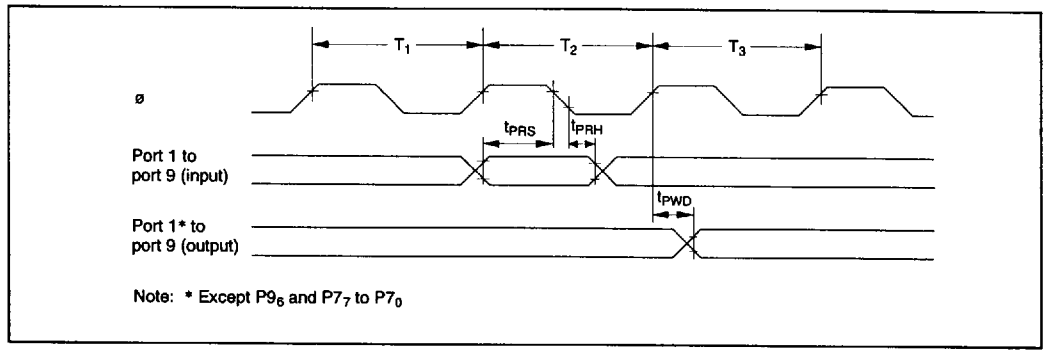


Figure 22-18 I/O Port Input/Output Timing

22.3.8 Host Interface Timing (H8/3337 Series Only)

(1) Host Interface Read Timing

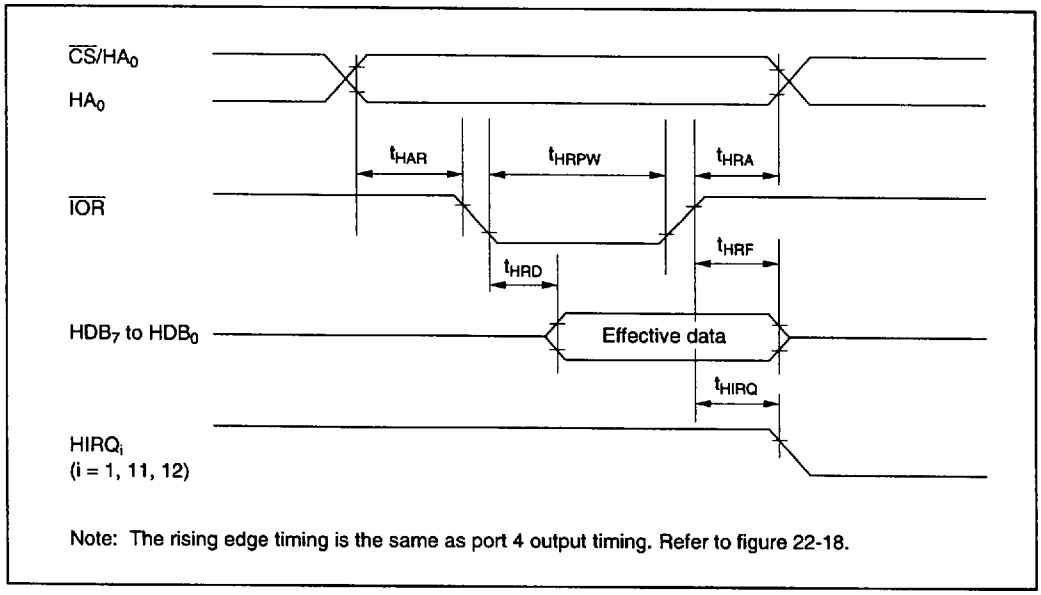


Figure 22-19 Host Interface Read Timing

(2) Host Interface Write Timing

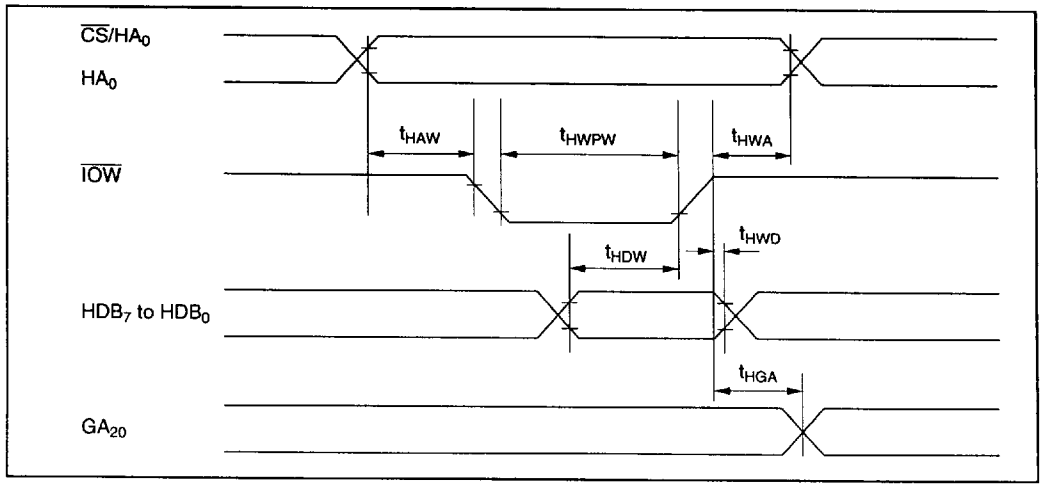
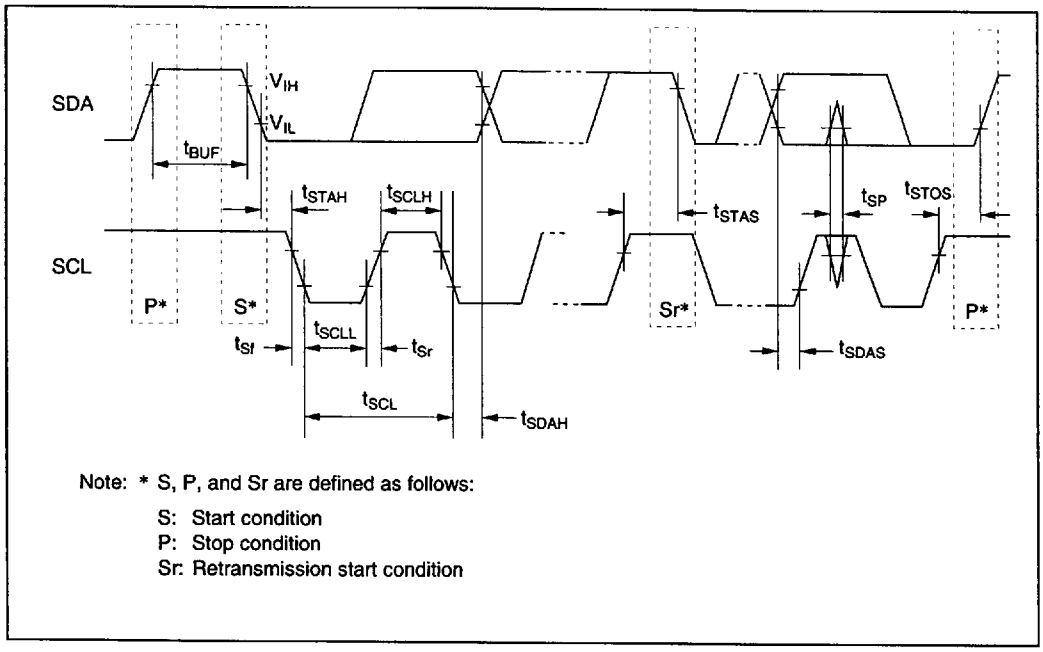


Figure 22-20 Host Interface Write Timing

22.3.9 I^2C Bus Timing (Option) (H8/3337 Series Only)

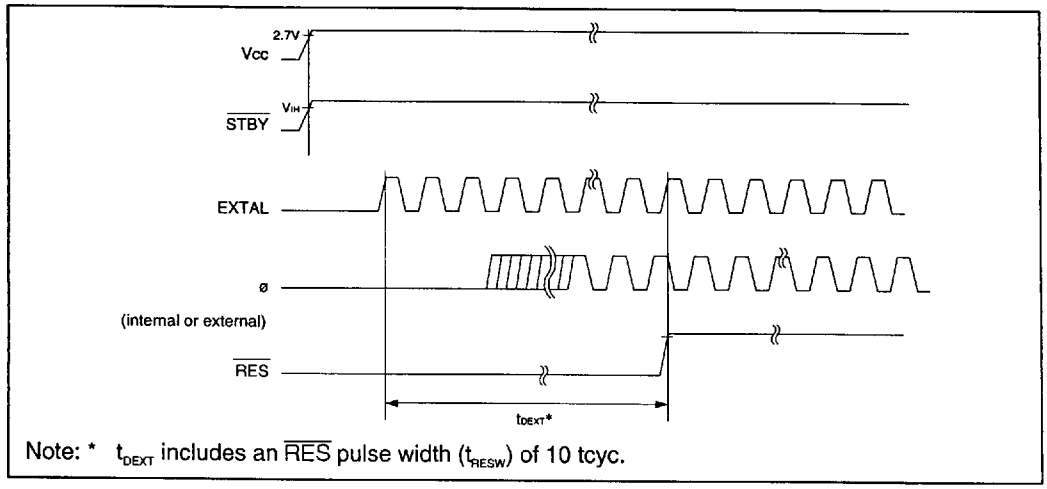


Note: * S, P, and Sr are defined as follows:

S: Start condition
P: Stop condition
Sr: Retransmission start condition

Figure 22-21 I^2C Interface Input/Output Timing

22.3.10 External Clock Output Timing



Note: * t_{DEXT} includes an $\overline{RES}$ pulse width (t_{RESW}) of 10 tcyc.

Figure 22-22 External clock output delay Timing