T-49-19-08

DALLAS SEMICONDUCTOR

PRELIMINARY

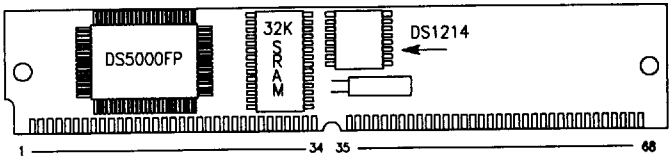
Micro SipStik™ with Embedded Bus DS2259

Time Micro SipStik™ with Embedded Bus DS2259T

FEATURES

- Sipstik version of DS5000 or DS5000T
- Provides access to Embedded Address/ Data Bus
- Frees up port pins for I/O use
- Direct interface to byte wide memories
- Supplied with 8K or 32 KBytes of NVSRAM for Program/Data
- 15 address lines - addresses up to 32K bytes externally
- Compatible with DS2250
- DS2259T: Permanently powered clock/ calendar
- 64-position SIMM connection scheme

PACKAGE OUTLINE



ORDERING INFORMATION

DS2259 XX–XX MICRO SIPSTIK
DS2259T XX–XX TIME MICRO SIPSTIK

Speed Grade

8	8 MHz
12	12 MHz
16	16 MHz

Program/Data RAM

8	8 Kbytes
32	32 Kbytes

DESCRIPTION

The DS2259 and DS2259T are the functional equivalents of the DS2250 and DS2250T, respectively, with the additional feature that the both devices are supplied with the Embedded Address/Data bus available for interface to external devices. The Embedded Bus is non-multiplexed and includes 15 address and 8 data lines, as well as chip enable and read/write control signals. In addition, all of the 40 pins of the DS2250 and the DS2250T are available. As a result, all of the 8051 compatible I/O ports are available for I/O. The DS2259(T) plug into the SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles.

T-49-19-08

PIN DESCRIPTION

Table 1 summarizes the pin assignments for both the DS2259 and DS2259T by pin function. All inverted signal names are denoted with a asterisk (*) as a suffix to the signal name (e.g. INT0*). This convention is followed throughout this data sheet.

TABLE 1: PIN ASSIGNMENTS

PIN	SIGNAL	DESCRIPTION	TYPE
40	V_{CC}	System V_{CC}	-
20	GND	Ground	-
19	XTAL2	Crystal Input 2	Input
18	XTAL1	Crystal Input 1	"
29	PSEN*	Program Store Enable	Output; active low
30	ALE	Address Latch Enable	Output; active high
31	EA*	External Access Enable	Input; active low
9	RST	Reset	Input; active high
32	P0.7/AD7	Port 0 bit 7/Addr.-Data7	Bidirectional I/O; open drain/ Bidirectional address-data
33	P0.6/AD6	Port 0 bit 6/Addr.-Data6	" " " "
34	P0.5/AD5	Port 0 bit 5/Addr.-Data5	" " " "
35	P0.4/AD4	Port 0 bit 4/Addr.-Data4	" " " "
36	P0.3/AD3	Port 0 bit 3/Addr.-Data3	" " " "
37	P0.2/AD2	Port 0 bit 2/Addr.-Data2	" " " "
38	P0.1/AD1	Port 0 bit 1/Addr.-Data1	" " " "
39	P0.0/AD0	Port 0 bit 0/Addr.-Data0	" " " "
8	P1.7	Port 1 bit 7	Bidirectional I/O
7	P1.6	Port 1 bit 6	" "
6	P1.5	Port 1 bit 5	" "
5	P1.4	Port 1 bit 4	" "
4	P1.3	Port 1 bit 3	" "
3	P1.2	Port 1 bit 2	" "
2	P1.1	Port 1 bit 1	" "
1	P1.0	Port 1 bit 0	" "
28	P2.7	Port 2 bit 7/A15	Bidirectional I/O/Output
27	P2.6	Port 2 bit 6/A14	" " "
26	P2.5	Port 2 bit 5/A13	" " "
25	P2.4	Port 2 bit 4/A12	" " "

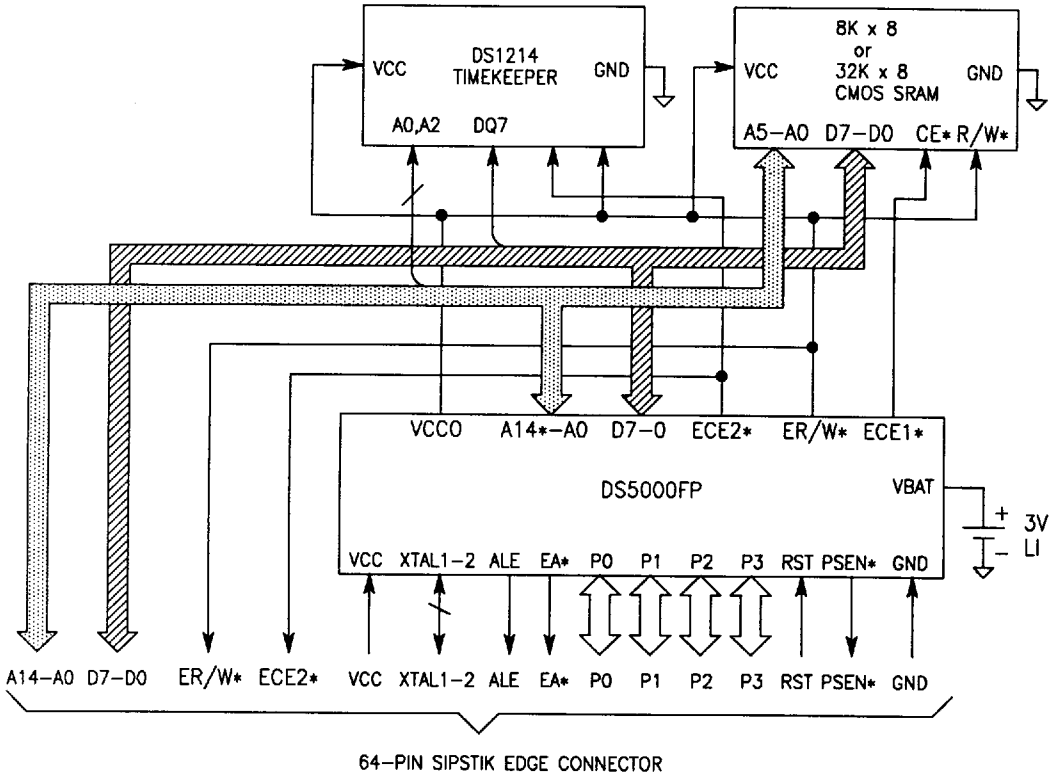
T-49-19-08

24	P2.3	Port 2 bit 3/A11	"	"	
23	P2.2	Port 2 bit 2/A10	"	"	
22	P2.1	Port 2 bit 1/A9	"	"	"
21	P2.0	Port 2 bit 0/A8	"	"	"
17	P3.7 / RD*	Port 3 bit 7 / Read Enable	Bidirectional I/O/Output		
16	P3.6 / WR*	Port 3 bit 6 / Write Enable	"	"	"
15	P3.5 / T1	Port 3 bit 5 / Timer Ctr. Input 1	"	"	"
14	P3.4 / T0	Port 3 bit 4 / Timer Ctr. Input 0	"	"	"
13	P3.3 / INT1*	Port 3 bit 3 / Ext. Int. Input 1	"	"	"
12	P3.2 / INT0*	Port 3 bit 2 / Ext. Int. Input 0	"	"	"
11	P3.1 / TXD	Port 3 bit 1 / Xmit Data Output	"	"	"
10	P3.0 / RXD	Port 3 bit 0 / Rcv. Data Input	"	"	"
55	EA14	Embedded Address line 14	Output		
54	EA13	Embedded Address line 13	"		
53	EA12	Embedded Address line 12	"		
52	EA11	Embedded Address line 11	"		
51	EA10	Embedded Address line 10	"		
50	EA9	Embedded Address line 9	"		
49	EA8	Embedded Address line 8	"		
48	EA7	Embedded Address line 7	"		
47	EA6	Embedded Address line 6	"		
46	EA5	Embedded Address line 5	"		
45	EA4	Embedded Address line 4	"		
44	EA3	Embedded Address line 3	"		
43	EA2	Embedded Address line 2	"		
42	EA1	Embedded Address line 1	"		
41	EA0	Embedded Address line 0	"		
63	ED7	Embedded Data line 7	Bidirectional data		
62	ED6	Embedded Data line 6	"	"	
61	ED5	Embedded Data line 5	"	"	
60	ED4	Embedded Data line 4	"	"	
59	ED3	Embedded Data line 3	"	"	
58	ED2	Embedded Data line 2	"	"	
57	ED1	Embedded Data line 1	"	"	
56	ED0	Embedded Data line 0	"	"	
65	ECE2*	Embedded Chip Enable 2	Output		
64	ER/W*	Embedded Bus Read/Write	"		

BLOCK DIAGRAM

Figure 1 is a block diagram of the DS2259(T). The DS2259 contains a DS5000FP Soft Microcontroller, an 8K x 8 or 32K x 8 static RAM, and a lithium cell for data retention. Togther, these components for all of the functionallity of a DS5000 or DS2250. In the DS2259T version, a DS1214 Timekeeper is added to give the system the basic functionallity of a DS5000T or DS2250T.

FIGURE 1: DS2259(T) BLOCK DIAGRAM



The embedded address and data bus from the DS2259(T) can be used to connect to a variety of external devices. Pins A14-A0 address up to 32 KBytes of memory space which is transferred over pins ED0-ED7 (bidirectional data bus) under the control of ECE2*. Transfers over this bus can be performed using MOVX instructions when the ECE2 bit is enabled in the MCON register. The ER/W* signal is also brought out to indicate a read or write operation. The ECE1* signal is not routed to the edge connector, and is therefore not directly accessible for external devices. Instead, this signal is used to control the on-board NVSRAM. The timing characteristics of the embedded address/data bus and its associated control signals (ECE1*, ECE2* and ER/W*) are given at the back of this data sheet.

MEMORY ORGANIZATION

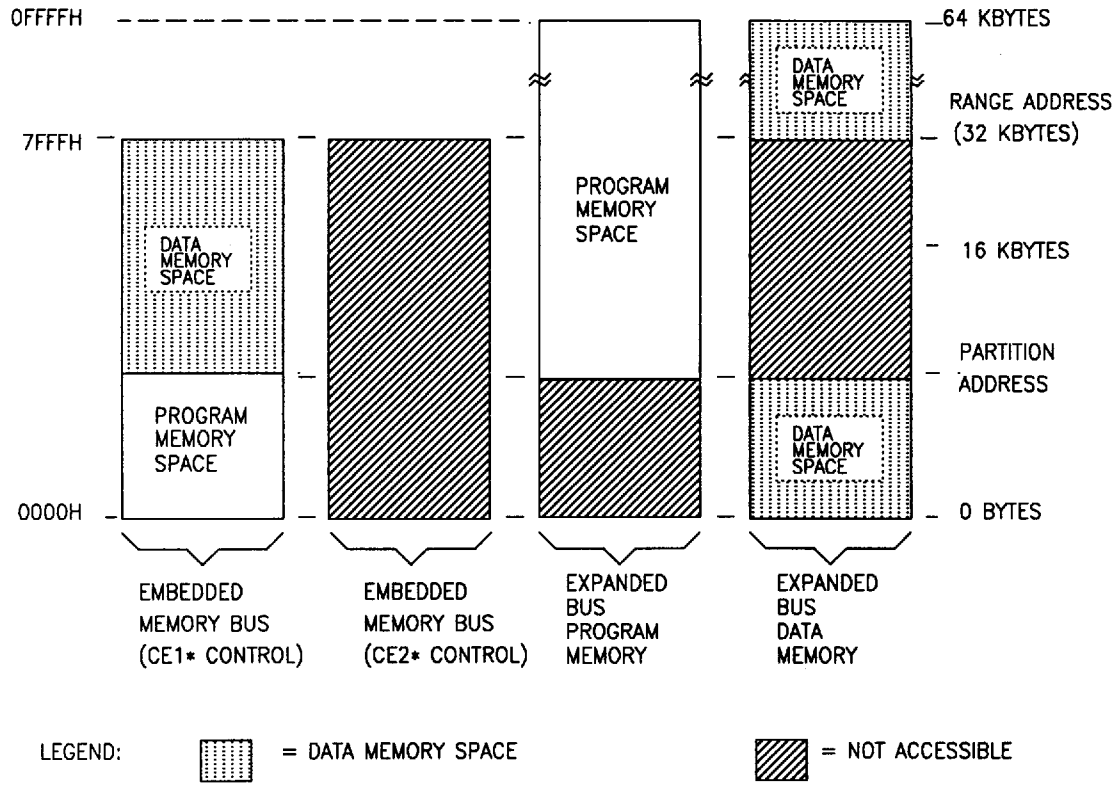
The following is a description of how the memory spaces on the Embedded Address/Data bus may be utilized by the designer. This discussion assumes that the reader is familiar with the programming model of the DS5000, which is described in detail in Section 4 of the DS5000 User's Guide.

The memory on the DS2259(T) is organized as two separately accessed 32K byte memory maps. Each of the maps are enabled by one of the two separate chip enable signals from the microcontroller die: CE1* and CE2*. These chip enable signals operate under the control of the application software via the ECE2 bit in the MCON Special Function register.

Figure 2 illustrates the mapping within the embedded RAM which results when the ECE2 bit is cleared to 0. In this case, only the Program/Data RAM which is under the control of the CE1* signal is accessible and it is mapped in an identical fashion to a 8 or 32K byte version of a DS5000. The Partition Address and the Range Address (as defined in the MCON register) determine the mapping of Program and Data Memory space within the CE1* controlled embedded RAM area. Any program memory access from location 0000H up to (but not including) the Partition Address location will be mapped to the corresponding locations within the embedded Program/Data RAM. Program accesses at or above the Partition and/or Range addresses will be executed via the Expanded Address/Data bus in place of Ports 0 and 2, as long as the Security Lock bit is cleared to 0. If the Security Lock bit is set to a 1, then no external Program Memory accesses are possible. Any data memory access (using a MOVX instruction) from the Partition Address location up to (but not including) the Range address location will be mapped to the corresponding locations within the embedded Program/Data RAM. Any Data Memory access outside of the area between these two addresses will be executed on the Expanded Bus.

T-49-19-08

FIGURE 2: PROGRAM/DATA MEMORY MAPPING: ECE2=0

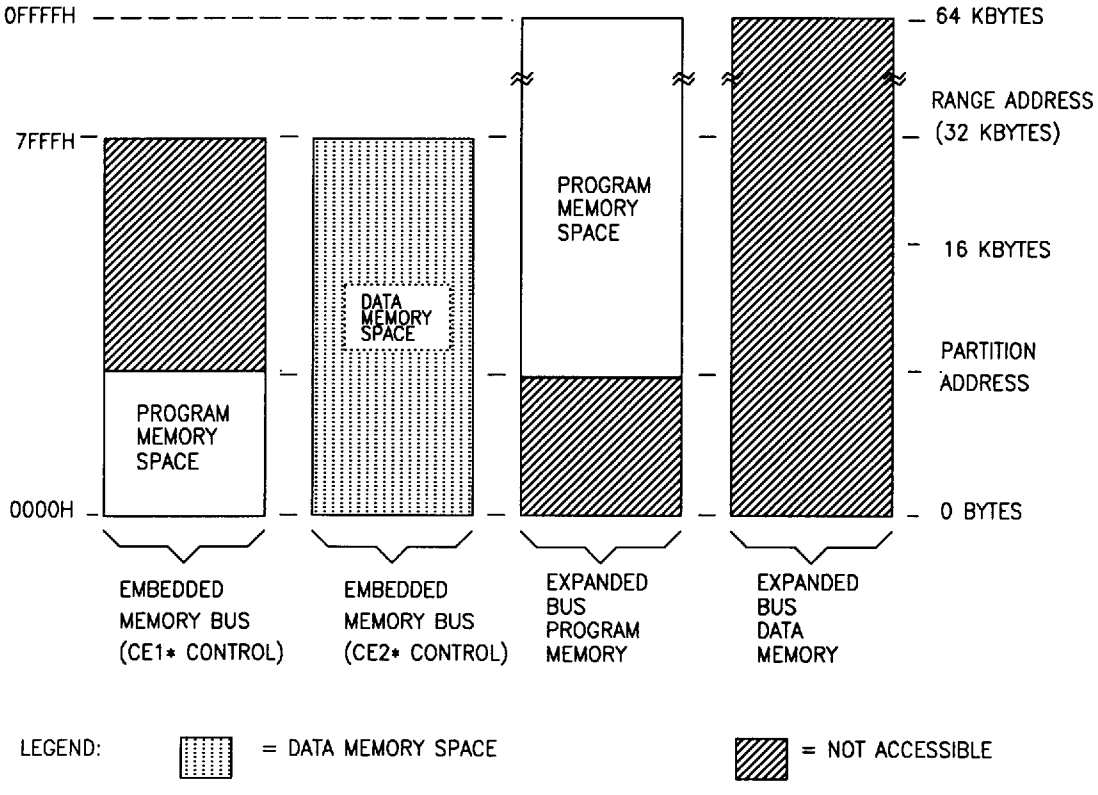


When ECE2 is set to 1 by the application software, Program Memory accesses to the embedded RAM will still cause only CE1* to be activated. However, any Data Memory access by a MOVX instruction to the embedded RAM will cause CE2* to be activated instead of CE1*. As a result, external devices under the control of the CE2* signal can only be used for data memory accesses.

The amount of external space accessed with ECE2 set is dependent on the setting of the Range Address. If the Range Address is set for 8K bytes, then external devices mapped from 0000H to 1FFFH are accessible via MOVX instructions on the Embedded Bus. Any MOVX accesses performed from 2000H to 7FFFH will not be performed on either the Embedded Bus or on the Expanded Bus (in place Ports 0 and 2). If it is desired to perfom data memory accesses on the Expanded Bus at 2000H or above, then the ECE2 bit must be reset to 0.

In the case of the Range Address set to 32K bytes, external devices mapped from 0000H to 7FFFH (32K bytes) may be accessed. As long as ECE2 remains set to 1, it is not possible to access any data memory space above 7FFFH. If the ECE2 bit is reset to 0, then data memory accesses may be performed on the Expanded Bus from 8000H to FFFFH. The case of a 32K byte Range Address with ECE2 set to 1 is illustrated in Figure 3.

FIGURE 3: PROGRAM/DATA MEMORY MAPPING: ECE2=1



DS2259T CLOCK/CALENDAR

The DS2259T incorporates a permanently powered Embedded Clock/Calendar (ECC) that is identical in function to the DS1215 Timekeeper. The real-time clock is also memory-mapped on the internal Embedded RAM address/data bus. As a result, it may be accessed by software as if it were Embedded Data RAM using the "MOVX" set of instructions. Accesses to the ECC take place with no effect on I/O port pins. Detailed operation of the ECC may be found in the DS5000T data sheet.

For the DS2259T the ECC is accessed via the CE2* control line from the microcontroller. The CE2* signal to the card edge connector is routed through the ECC so that the CE* signal to any external device is conditioned by control logic within the ECC itself. Access to the external device by the application software can proceed as normal until communication with the ECC is desired. The application software may then select the ECC by performing the 64-bit pattern recognition CE2* read cycle sequence. Reads and writes can then proceed as described for the DS5000T.

POWER MANAGEMENT

In the absence of V_{CC}, lithium power provides backup to the on board SRAM. When V_{CC} drops, the on board CE2* and EA14 are kept high to prevent accidental memory or timekeeper access. The CE2* and EA14 signals which are routed to the connector are not backed in this manner. When V_{CC} drops, these signal will follow.

ABSOLUTE MAXIMUM RATINGS *

T-49-19-08

Voltage on any pin relative to ground	-0.3 to 7.0V
Operating Temperature	0 deg. to 70 deg. C
Storage Temperature	-40 deg. C to +70 deg. C
Soldering Temperature on the leads	260 deg. C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The DS5000FP adheres to all of the published AC and DC specifications for the DS5000. The following are additional AC timing characteristics which apply only to the DS5000FP. In the following specifications 1 T_{CLK} machine cycle = 12 oscillator cycles.

T-49-19-08

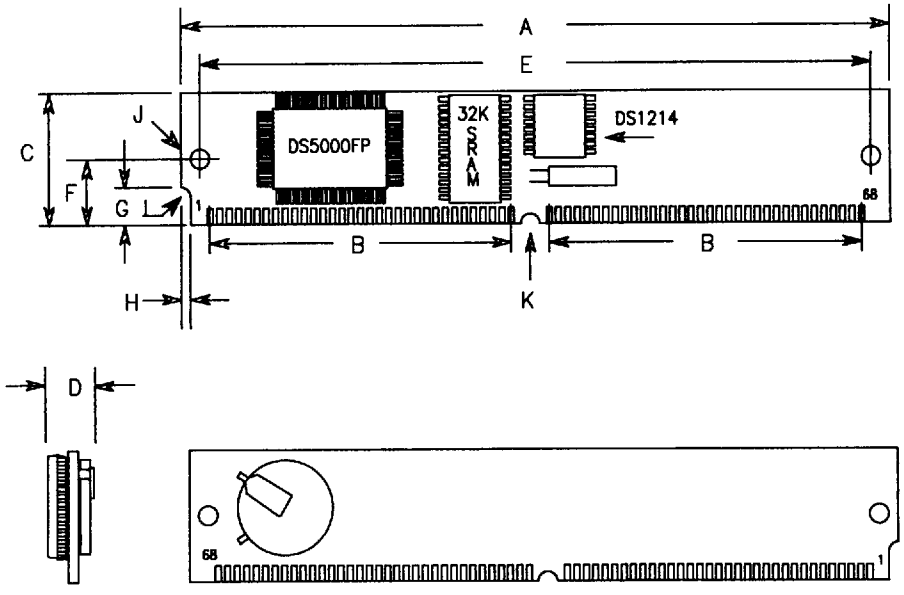
EMBEDDED ADDRESS/DATA BUS TIMING A.C. CHARACTERISTICS

(T_A = 0° to 70° C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN.	MAX.	UNITS
56	Delay to Embedded Address Valid from ECE1* low during opcode fetch	t_{CE1LPA}		20	ns
57	ECE1* or ECE2* Pulse Width	t_{CEPW}	4TCLK-15		ns
58	Embedded Address Hold after ECE1* high during opcode fetch	t_{CE1HPA}	2TCLK-20		ns
59	Embedded Data setup to ECE1* high during opcode fetch	t_{OVCE1H}	1TCLK+40		ns
60	Embedded Data hold after ECE1* high during opcode fetch	t_{CE1HOV}	10		ns
61	Embedded Address Hold after ECE1* or ECE2* high during MOVX	t_{CEHDA}	4TCLK-30		ns
62	Delay from Embedded Address Valid to ECE1* or ECE2* low during MOVX	t_{CELDA}	4TCLK-25		ns
63	Embedded Data setup to ECE1* or ECE2* high during MOVX (read)	t_{DACEH}	1TCLK+40		ns
64	Embedded Data hold after ECE1* or ECE2* high during MOVX (read)	t_{CEHDV}	10		ns
65	Embedded Address Valid to ER/W* active during MOVX (write)	t_{AVRWL}	3TCLK-35		ns
66	Delay from ER/W* low to Valid Data Out during MOVX (write)	t_{RWLDV}	20		ns
67	Valid Data Out hold time from ECE1* or ECE2* high	t_{CEHDV}	1TCLK-15		ns
68	Valid Data Out hold time from ER/W* high	t_{RWHDV}	0		ns
69	Write pulse width (ER/W* low time)	t_{RWLPW}	6TCLK-20		ns

T-49-19-08

DS2259 (T)
Micro Sipstik



DIM.	INCHES	MM
A	4.050	102.87
B	1.650	41.91
C	0.840	21.34
D	0.350	8.89
E	3.784	96.11
F	0.400	10.16
G	0.250	6.35
H	0.080	2.03
I	R .062	R 1.57
J	D 0.125	D 3.18