ANALOG DEVICES

Dual Boostrapped 12 V MOSFET Driver with Output Disable

Preliminary Technical Data   ADP3418

FEATURES
All-In-One Synchronous Buck Driver
Bootstrapped High-Side Drive
One PWM Signal Generates Both Drives
Anticross-Conduction Protection Circuitry
Output Disable Control Turns Off both MOSFETs to
    Float Output per Intel VRM 10 Specification

APPLICATIONS
Multiphase Desktop CPU Supplies
Single-Supply Synchronous Buck Converters

GENERAL DESCRIPTION
The ADP3418 is a dual high-voltage MOSFET driver optimized for driving two N-channel MOSFETs which are the two switches in a non-isolated synchronous buck power converter. Each of the drivers is capable of driving a 3000 pF load with a 20 ns propagation delay and a 30 ns transition time. One of the drivers can be bootstrapped, and is designed to handle the high-voltage slew rate associated with floating high-side gate drivers. The ADP3418 includes overlapping drive protection (ODP) to prevent shoot-through current in the external MOSFETs. The $\overline{OD}$ pin shuts off both the high-side and the low-side MOSFETs to prevent rapid output capacitor discharge during system shutdown.

The ADP3418 is specified over the commercial temperature range of 0°C to 85°C and is available in a thermally-enhanced 8-lead SOIC package.
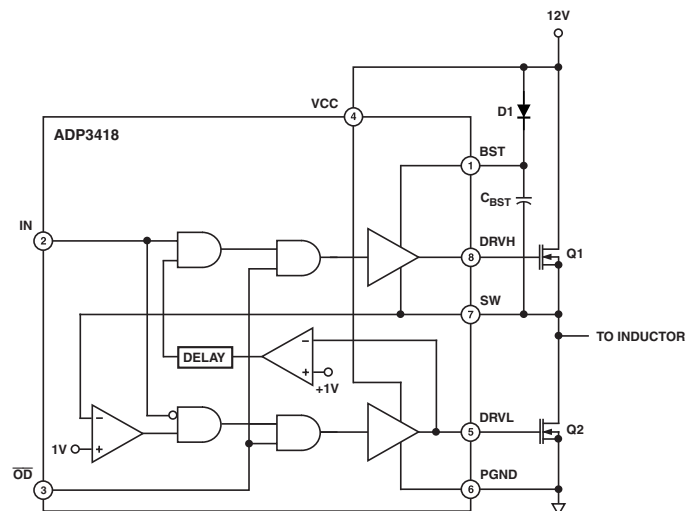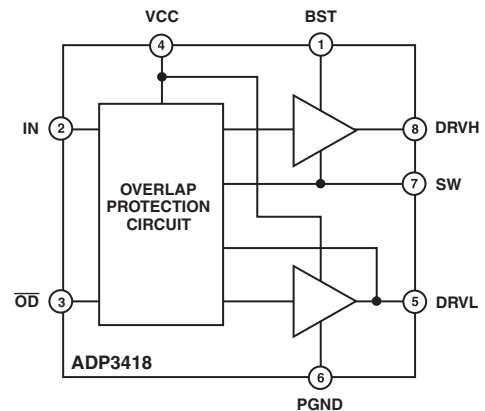
FUNCTIONAL BLOCK DIAGRAM

Figure 1. General Application Circuit.

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ADP3418–SPECIFICATIONS[1] (VCC = 12 V, BST = 4 V to 26 V, T_A = 0°C to +85°C, unless otherwise noted)

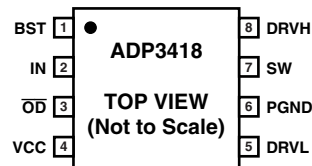| Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY						
Supply Voltage Range	V_{CC}		4.15		13.2	V
Supply Current	I_{SYS}	BST = 12 V, IN = 0 V		5	7	mA
$\overline{OD}$ INPUT						
Input Voltage High			2.0			V
Input Voltage Low					0.8	V
Input Current			-1		+1	μA
Propagation Delay Time[2]	$tpdl_{\overline{OD}}$	See Figure 2		15	30	ns
	$tpdh_{\overline{OD}}$	See Figure 2		15	30	ns
PWM INPUT						
Input Voltage High			2.0			V
Input Voltage Low					0.8	V
Input Current			-1		+1	μA
HIGH-SIDE DRIVER						
Output Resistance, Sourcing Current		$V_{BST} - V_{SW}$ =12 V		1.75	3.0	Ω
Output Resistance, Sinking Current		$V_{BST} - V_{SW}$ =12 V		1.0	2.5	Ω
Transition Times[2]	t_{rDRVH}	See Figure 3, $V_{BST} - V_{SW}$ =12 V, C_{LOAD} =3 nF		45	55	ns
	t_{fDRVH}	See Figure 3, $V_{BST} - V_{SW}$ =12 V, C_{LOAD} = 3 nF		20	30	ns
Propagation Delay[2,3]	$t_{pdhDRVH}$	See Figure 3, $V_{BST} - V_{SW}$ =12 V		45	65	ns
	$t_{pdlDRVH}$	$V_{BST} - V_{SW}$ =12 V		15	35	ns
LOW-SIDE DRIVER						
Output Resistance, Sourcing Current				1.75	3.0	Ω
Output Resistance, Sinking Current				1.0	2.5	Ω
Transition Times[2]	t_{rDRVL}	See Figure 3, C_{LOAD} = 3 nF		25	35	ns
	t_{fDRVL}	See Figure 3, C_{LOAD} = 3 nF		21	30	ns
Propagation Delay[2,3]	$t_{pdhDRVL}$	See Figure 3		30	60	ns
	$t_{pdlDRVL}$	See Figure 3		10	20	ns

NOTES
[1] All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
[2] AC specifications are guaranteed by characterization, but not production tested.
[3] For propagation delays, "tpdh" refers to the specified signal going high; "tpdl" refers to it going low.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

VCC .... −0.3 V to 15 V
BST .... −0.3 V to 30 V
BST to SW .... −0.3 V to 15 V
S W ....−5 V to 25 V
All Other Inputs and Outputs ......−0.3 V to VCC + 0.3 V
Operating Ambient Temperature Range ..... 0°C to +85°C
Operating Junction Temperature Range ... 0°C to +125°C
Storage Temperature Range ....−65°C to +150°C
θ_{JA} .... 123°C/W
Lead Temperature (Soldering, 10 sec) .... +300°C
Vapor Phase (60 sec) ....+215°C
Infrared (15 sec) ....+220°C
*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to PGND

PIN CONFIGURATION
R-8

```
           ┌───────────┐
  BST  1 ──┤ ●         ├── 8  DRVH
   IN  2 ──┤  ADP3418  ├── 7  SW
   OD  3 ──┤ TOP VIEW  ├── 6  PGND
  VCC  4 ──┤(Not to Scale)├── 5  DRVL
           └───────────┘
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ORDERING GUIDE

Model	Temperature Range	Package
ADP3418JR	0°C to +85°C	R-8 (SO-8)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3418 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

REV. PrC

PIN FUNCTION DESCRIPTIONS

| Pin	Name	Function
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between BST and SW pins holds this bootstrapped voltage for the high-side MOSFET as it is switched. The capacitor should be chosen between 100 nF and 1 μF.
2	IN	Logic-level Input. This pin has primary control of the drive outputs.
3	$\overline{\text{OD}}$	Output Disable. When low, this pin disables normal operation, forcing DRVH and DRVL low.
4	VCC	Input Supply. This pin should be bypassed to PGND with ~1 μF ceramic capacitor.
5	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) MOSFET.
6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
7	SW	This pin is connected to the buck-switching node, close to the upper MOSFET's source. It is the floating return for the upper MOSFET drive signal. It is also used to monitor the switched voltage to prevent turn-on of the lower MOSFET until the voltage is below ~1 V. Thus, according to operating conditions, the high-low transition delay is determined at this pin.
8	DRVH	Buck Drive. Output drive for the upper (buck) MOSFET.
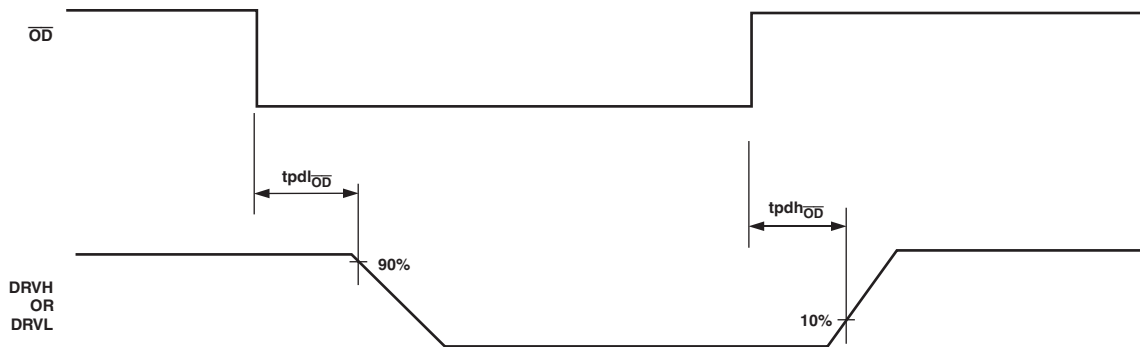
Figure 2. Output Disable Timing Diagram
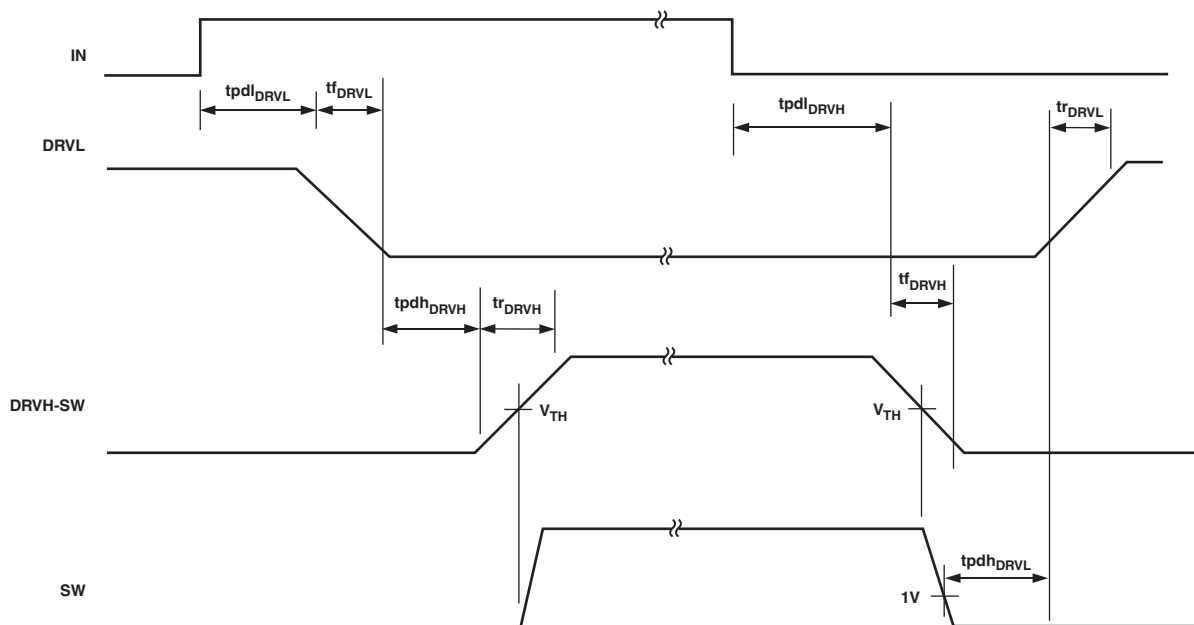
Figure 3. Nonoverlap Timing Diagram (Timing Is Referenced to the 90% and 10% Points Unless Otherwise Noted)

ADP3418

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC
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