

CAT25C256

256K-Bit Serial CMOS E²PROM

FEATURES

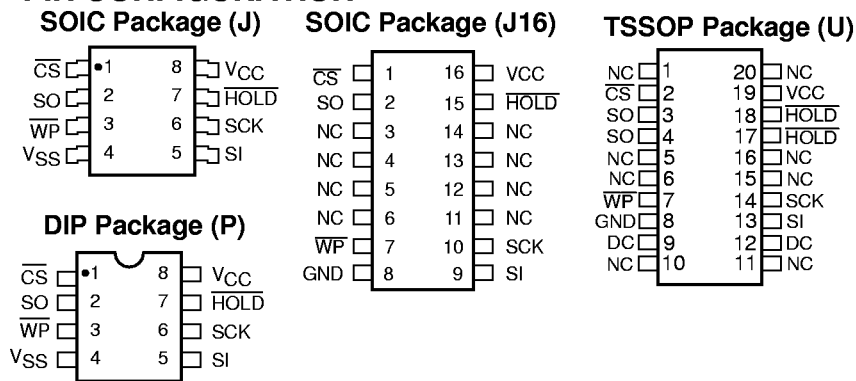
- 10 MHz SPI Compatible
- 1.8 to 6.0 Volt Operation
- Hardware Protection
- Zero Standby Current
- Low Power CMOS Technology
- SPI Modes (0,0 & 1,1)
- Commercial, Industrial and Automotive Temperature Ranges
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Self-Timed Write Cycle
- 8-Pin DIP/SOIC, 16-Pin SOIC and 20-Pin TSSOP
- 64-Byte Page Write Buffer
- Block Write Protection-1/4, 1/2 or all of array
– Programmable Hardware Write Protection

DESCRIPTION

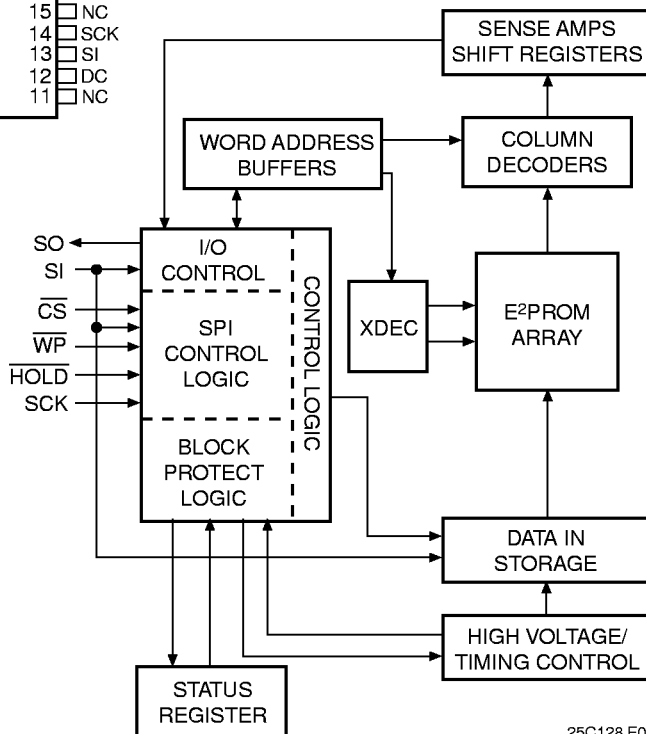
The CAT25C256 is a 256K-Bit SPI Serial CMOS E²PROM internally organized as 8Kx8/16Kx8 bits. Catalyst's advanced CMOS Technology substantially reduces device power requirements. The CAT25C256 features a 256-byte page write buffer. The device operates via the SPI bus serial interface and is enabled through a Chip Select (\overline{CS}). In addition to the Chip Select, the clock input (SCK), data in (SI) and data out (SO) are

required to access the device. The \overline{HOLD} pin may be used to suspend any serial communication without resetting the serial sequence. The CAT25C256 is designed with software and hardware write protection features including Block Lock protection. The device is available in 8-pin DIP, 8-pin SOIC, 16-pin SOIC and 20-pin TSSOP packages.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN FUNCTIONS

Pin Name	Function
SO	Serial Data Output
SCK	Serial Clock
\overline{WP}	Write Protect
V _{CC}	+1.8V to +6.0V Power Supply
V _{SS}	Ground
\overline{CS}	Chip Select
SI	Serial Data Input
\overline{HOLD}	Suspends Serial Input
NC	No Connect

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground ⁽¹⁾	-2.0V to +V _{CC} +2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (T _a = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N _{END} ⁽³⁾	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽³⁾	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽³⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽³⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

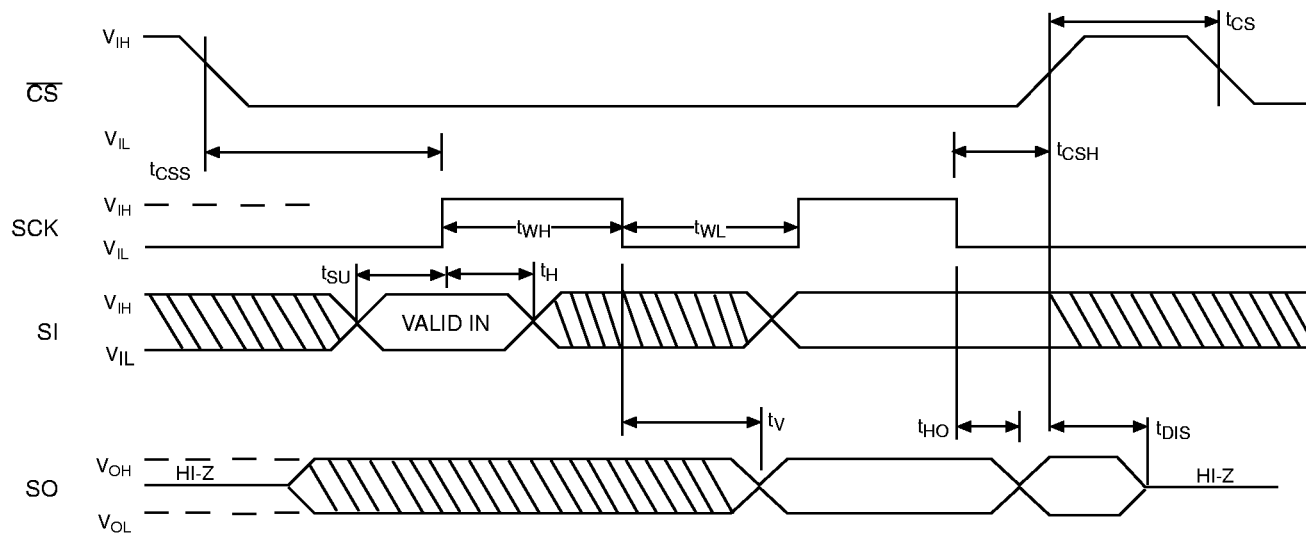
V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _{CC1}	Power Supply Current (Operating Write)			5	mA	V _{CC} = 5V @ 10MHz SO=open; CS=V _{SS}
I _{CC2}	Power Supply Current (Operating Read)			1	mA	V _{CC} = 5.5V F _{CLK} = 10MHz
I _{SB}	Power Supply Current (Standby)			0	μA	$\overline{CS} = V_{CC}$ V _{IN} = V _{SS} or V _{CC}
I _{LI}	Input Leakage Current			2	μA	
I _{LO}	Output Leakage Current			3	μA	V _{OUT} = 0V to V _{CC} , CS = 0V
V _{IL} ⁽³⁾	Input Low Voltage	-1		V _{CC} × 0.3	V	
V _{IH} ⁽³⁾	Input High Voltage	V _{CC} × 0.7		V _{CC} + 0.5	V	
V _{OL1}	Output Low Voltage			0.4	V	4.5V ≤ V _{CC} < 5.5V I _{OL} = 3.0mA I _{OH} = -1.6mA
V _{OH1}	Output High Voltage	V _{CC} - 0.8			V	
V _{OL2}	Output Low Voltage			0.2	V	1.8V ≤ V _{CC} < 2.7V I _{OL} = 150μA I _{OH} = -100μA
V _{OH2}	Output High Voltage	V _{CC} - 0.2			V	

Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

Figure 1. Synchronous Data Timing



A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		V _{CC} = 1.8V-6V		V _{CC} = 4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t_{SU}	Data Setup Time	50		20		ns	C _L = 50pF
t_H	Data Hold Time	50		25		ns	
t_{WH}	SCK High Time	250		40		ns	
t_{WL}	SCK Low Time	250		40		ns	
f_{SCK}	Clock Frequency	DC	1	DC	10	MHz	
t_{LZ}	\overline{HOLD} to Output Low Z		50		50	ns	
$t_{RI}^{(1)}$	Input Rise Time		2		2	μs	
$t_{FI}^{(1)}$	Input Fall Time		2		2	μs	
t_{HD}	\overline{HOLD} Setup Time	250		250		ns	
t_{CD}	\overline{HOLD} HOLD Time	250		250		ns	
t_{WC}	Write Cycle Time		10		5	ms	
t_V	Output Valid from Clock Low		250		80	ns	
t_{HO}	Output HOLD Time	0		0		ns	
t_{DIS}	Output Disable Time		250		75	ns	
t_{HZ}	\overline{HOLD} to Output High Z		150		50	ns	
t_{CS}	\overline{CS} High Time	1000		250		ns	
t_{CSS}	\overline{CS} Setup Time	1000		250		ns	
t_{CSh}	\overline{CS} HOLD Time	1000		250		ns	

NOTE:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

FUNCTIONAL DESCRIPTION

The CAT25C256 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT25C256 to interface directly with many of today's popular microcontrollers. The CAT25C256 contains an 8-bit instruction register.

After the device is selected with \overline{CS} going low, the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed. The instruction set and the operation codes are detailed in the instruction set table.

PIN DESCRIPTION

SI: Serial Input

SI is the serial data input pin. This pin is used to input all opcodes, byte addresses, and data to be written to the 25C256. Input data is latched on the rising edge of the serial clock.

SO: Serial Output

SO is the serial data output pin. This pin is used to transfer data out of the 25C256. During a read cycle, data is shifted out on the falling edge of the serial clock.

SCK: Serial Clock

SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the 25C256. Opcodes, byte addresses, or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK.

\overline{CS} : Chip Select

\overline{CS} is the Chip select pin. \overline{CS} low enables the CAT25C256 and \overline{CS} high disables the CAT25C256. \overline{CS} high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway). The CAT25C256 draws ZERO current in the Standby mode. A low to high transition on \overline{CS} is required prior to any sequence being initiated. A low to high transition on \overline{CS} after a valid write sequence is what initiates an internal write cycle.

\overline{WP} : Write Protect

\overline{WP} is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When \overline{WP} is tied low and the WPEN bit in the status register is set to "1", all write operations to the status register are inhibited. \overline{WP} going low while \overline{CS} is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, \overline{WP} going low will have no effect on any write operation to the status register. The \overline{WP} pin function is blocked when the WPEN bit is set to 0.

\overline{HOLD} : Hold

\overline{HOLD} is the HOLD pin. The \overline{HOLD} pin is used to pause transmission to the CAT25C256 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause, \overline{HOLD} must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, \overline{HOLD} is brought high, while SCK is low. (\overline{HOLD} should be held high any time this function is not being used.) \overline{HOLD} may be tied high directly to V_{cc} or tied to V_{cc} through a resistor.

INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000110	Enable Write Operations
WRDI	0000100	Disable Write Operations
RDSR	0000101	Read Status Register
WRSR	0000001	Write Status Register
READ	0000011	Read Data from Memory
WRITE	0000010	Write Data to Memory

STATUS REGISTER

The Status Register indicates the status of the device.

The $\overline{\text{RDY}}$ (Ready) bit indicates whether the CAT25C256 is busy with a write operation. When set to 1 a write cycle is in progress and when set to 0 the device indicates it is ready. This bit is read only.

The WEL (Write Enable) bit indicates the status of the write enable latch. When set to 1, the device is in a Write Enable state and when set to 0 the device is in a Write Disable state. The WEL bit is a read only bit. It can be set by the WREN instruction and can be reset by the WRDI instruction.

The BPO and BP1 (Block Protect) bits indicate which blocks are currently protected. These bits are set by the user issuing the WRSR instruction. The user is allowed to protect quarter of the memory, half of the memory or the entire memory by setting these bits. Once protected

the user may only read from the protected portion of the array. These bits are non-volatile.

The WPEN (Write Protect Enable) is an enable bit for the $\overline{\text{WP}}$ pin. The WPEN bit and $\overline{\text{WP}}$ in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{\text{WP}}$ is low and WPEN bit is set to high. When the chip is hardware write protected, only writes are disabled to the non-volatile bits (WPEN, BP0 and BP1) in the status register as well as the block protected section in the memory array. Hardware write protection is disabled when either $\overline{\text{WP}}$ pin is high or the WPEN bit is low.

STATUS REGISTER

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	$\overline{\text{RDY}}$

BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	BPO		
0	0	None	No Protection
0	1	3000-3FFF	Quarter Array Protection
1	0	2000-3FFF	Half Array Protection
1	1	0000-3FFF	Full Array Protection

WRITE PROTECT ENABLE OPERATION

WPEN	$\overline{\text{WP}}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

DEVICE OPERATION

Write Enable and Disable

The CAT25C256 contains a write enable latch. This latch must be set before any write operation. The device powers up in a write disable state when V_{CC} is applied. WREN instruction will enable writes (set the latch) to the device. WRDI instruction will disable writes (reset the latch) to the device. Disabling writes will protect the device against inadvertent writes.

READ Sequence

The part is selected by pulling \overline{CS} low. The 8-bit read instruction is transmitted to the CAT25C256, followed by the 16-bit address (the three Most Significant Bits are don't care for 25C64 and two most significant bits are don't care for 25C128).

After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address (1FFFh for 25C64 and 3FFFh for 25C128) is reached, the address counter rolls over to 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by pulling the \overline{CS} high. To read the status register, RDSR instruction should be sent. The contents of the status register are shifted out on the SO line. The status register may be read at any time even during a write cycle.

Figure 2. WREN Instruction Timing

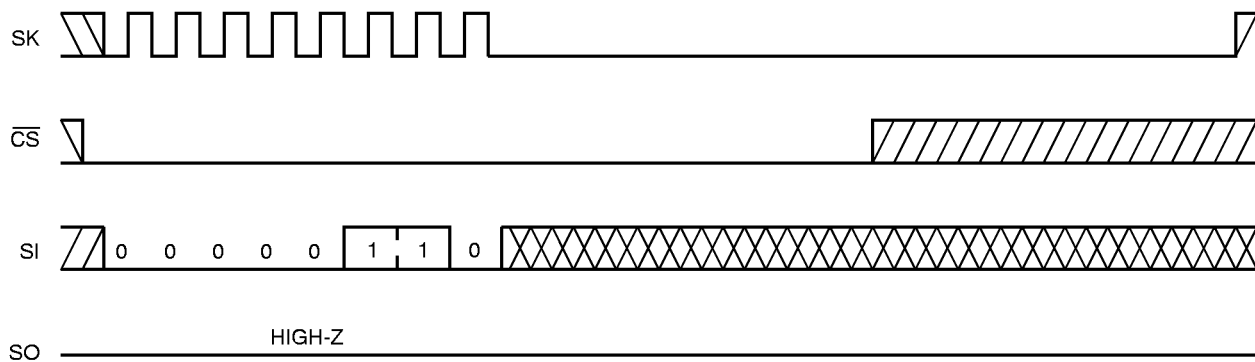
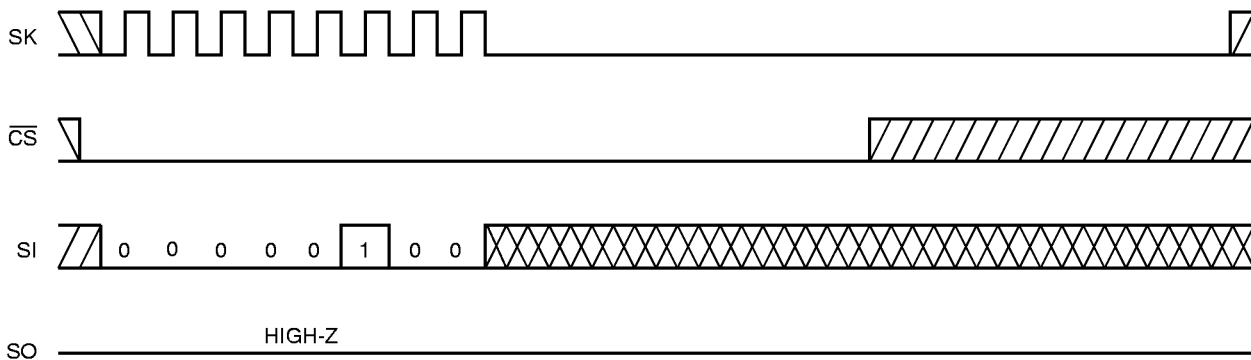


Figure 3. WRDI Instruction Timing



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WRITE Sequence

The CAT25C256 powers up in a Write Disable state. Prior to any write instructions, the WREN instruction must be sent to CAT25C256. The device goes into Write enable state by pulling the \overline{CS} low and then clocking the WREN instruction into CAT25C256. The \overline{CS} must be brought high after the WREN instruction to enable writes to the device. If the write operation is initiated immediately after the WREN instruction without \overline{CS} being brought high, the data will not be written to the array because the write enable latch will not have been properly set. Also, for a successful write operation the

must be outside the protected address field location selected by the Block protection level.

Byte Write

Once the device is in a Write Enable state, the user may proceed with a write sequence by setting the \overline{CS} low, issuing a write instruction via the SI line, followed by the 16-bit address (the three Most Significant Bits are don't care for 25C64 and two most significant bits are don't care for 25C128), and then the data to be written. Programming will start after the \overline{CS} is brought high. The low to high transition of the \overline{CS} pin must occur during the SCK low time, immediately after the clocking the least significant bit of the data bit.

Figure 4. Read Instruction Timing

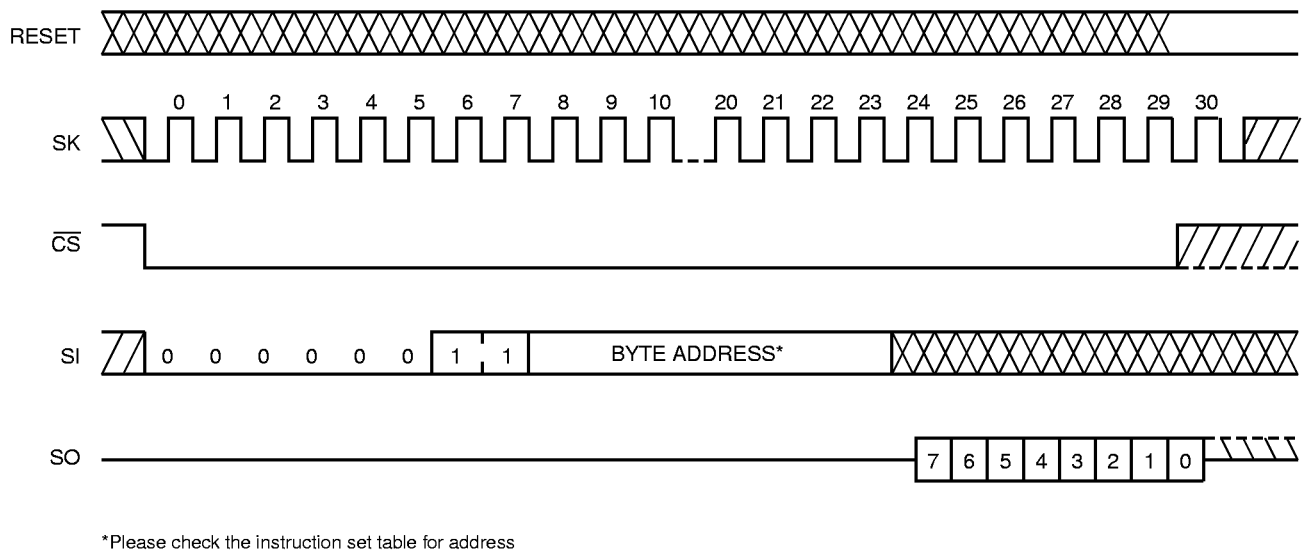
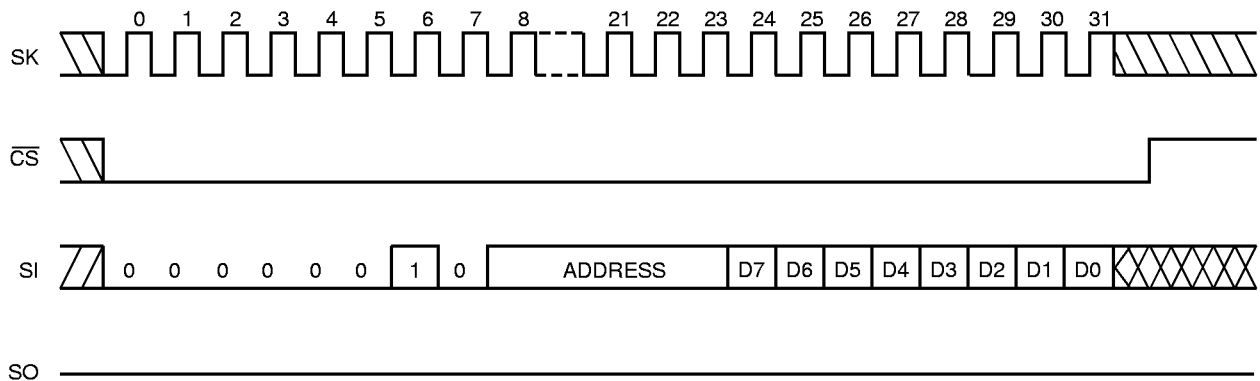


Figure 5. Write Instruction Timing



address of the memory location(s) to be programmed

During an internal write cycle, all commands will be ignored except the RDSR (Read Status Register) instruction.

The Status Register can be read to determine if the write cycle is still in progress. If Bit 0 of the Status Register is set at 1, write cycle is in progress. If Bit 0 is set at 0, the device is ready for the next instruction

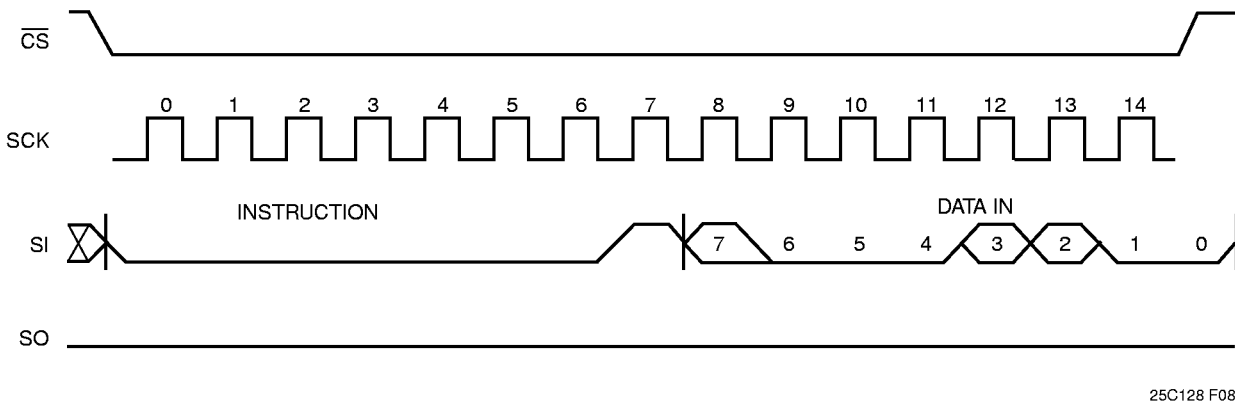
Page Write

The CAT25C256 features page write capability. The host may continue to write up to 64 bytes of data to the CAT25C256. The only restriction is that the 64 bytes must reside on the same page. If the address counter

reaches the end of the page and clock continues, the counter will “roll over” to the first address of the page and overwrite any data that may have been written. After each byte of data received, five lower order address bits are internally incremented by one; the high order bits of address will remain constant. The CAT25C256 is automatically returned to the write disable state at the completion of the write cycle.

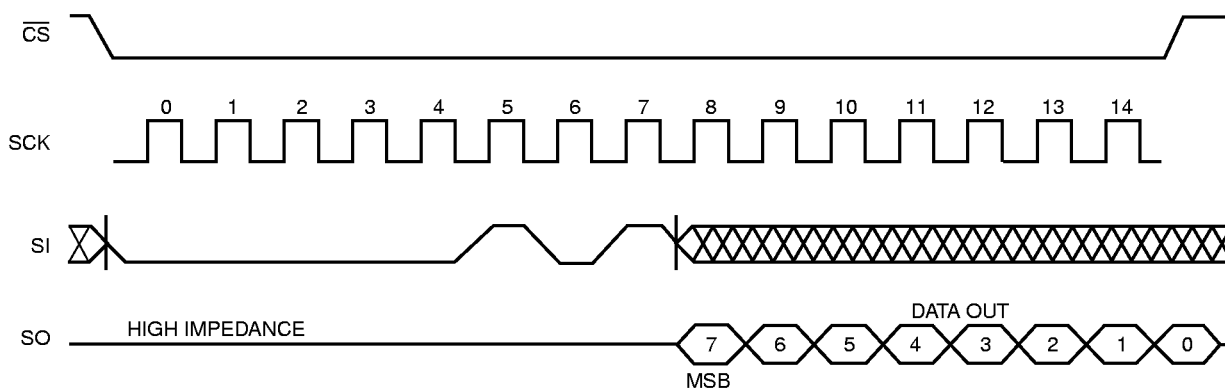
To write to the status register, the WRSR instruction should be sent. Only Bit 2, Bit 3 and Bit 7 of the status register can be written using the WRSR instruction.

Figure 6. WRSR Timing



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Figure 7. RDSR Timing



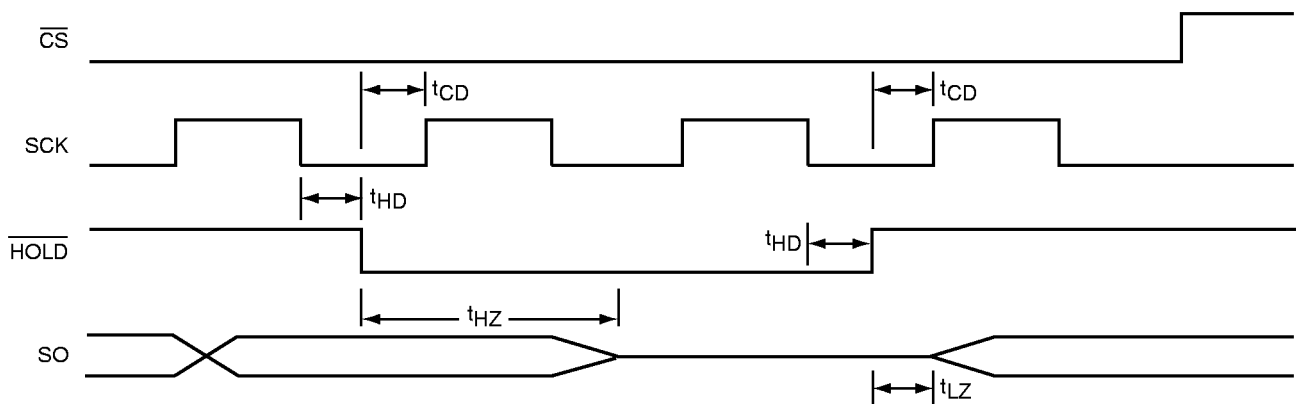
25C128 F09

DESIGN CONSIDERATIONS

The CAT25C256 powers up in a Write disable state and is in a low power standby mode. A WREN instruction must be issued to perform any writes to the device. After a successful byte/page write or status register write the CAT25C256 goes into a write disable mode. \overline{CS} must be set high after the proper number of clock cycles to start an internal write cycle. Access to the array during an internal write cycle is ignored and programming is continued. On power up, SO in a high impedance. Also, on power up \overline{CS} should be brought low to enter a ready state and receive an instruction.

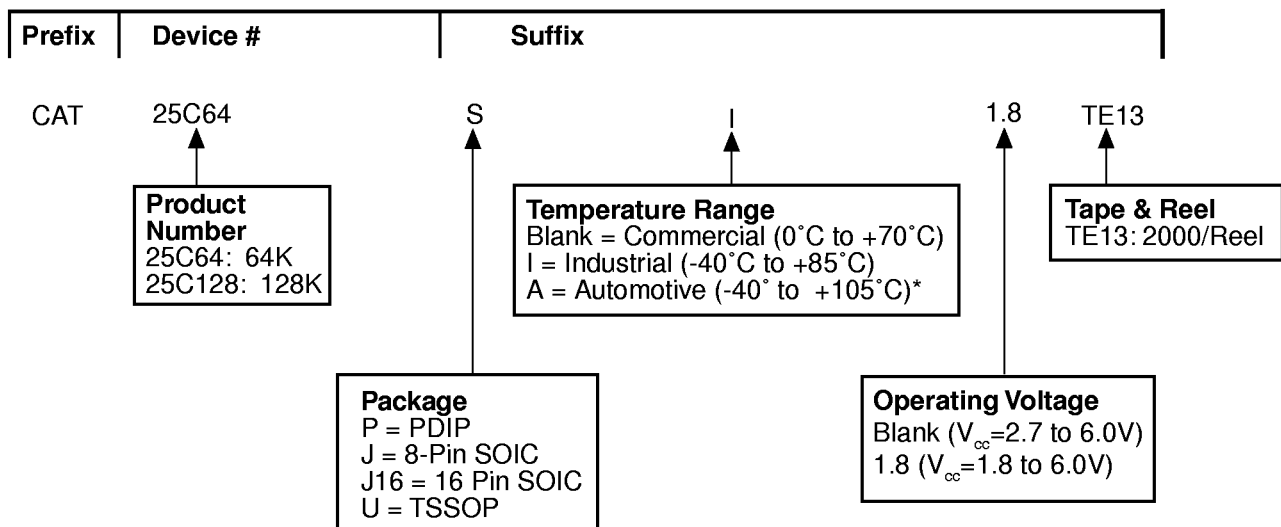
If an invalid Op code is received, no data will be shifted into the CAT25C256, and the serial output pin (SO) will remain in a high impedance state until the falling edge of \overline{CS} is detected again. This will reinitialize the serial communication.

Figure 8. \overline{HOLD} Timing



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ORDERING INFORMATION



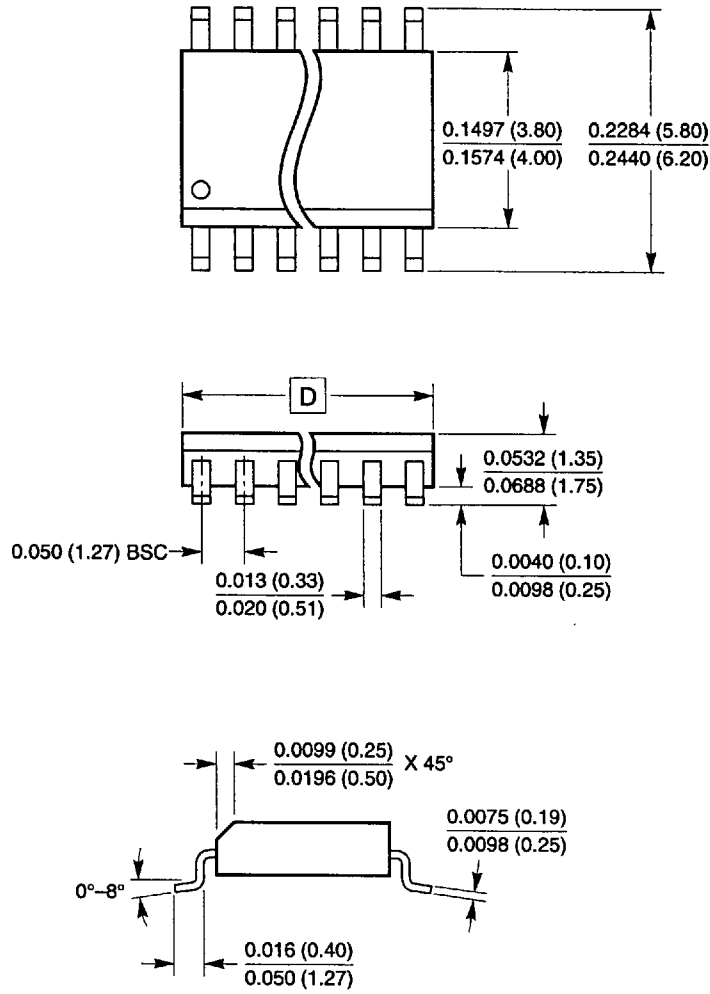
* -40°C to +125°C is available upon request

Notes:

(1) The device used in the above example is a 25C256SI-1.8TE7 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel)



8 AND 14-LEAD 150 MIL WIDE SOIC (J)



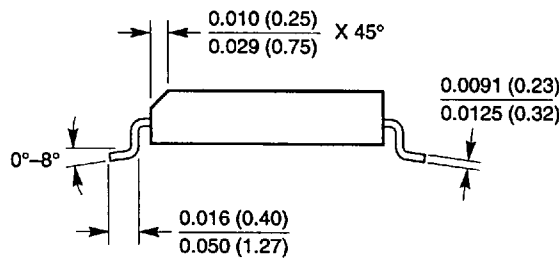
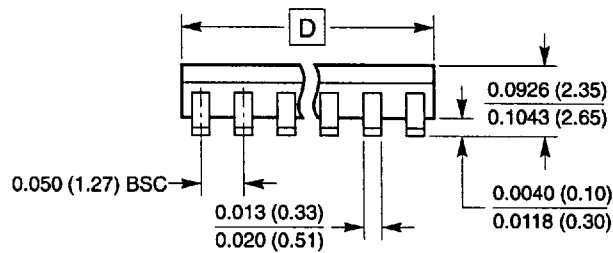
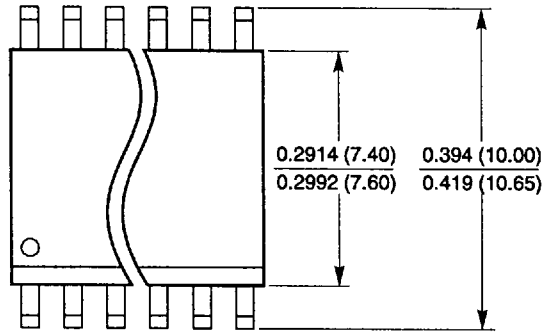
Dimension D		
Pkg	Min	Max
8L	0.1890(4.80)	0.1968(5.00)
14L	0.3367(8.55)	0.3444(8.75)

Notes:

1. Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.



16-28-LEAD 300 MIL WIDE SOIC (J)



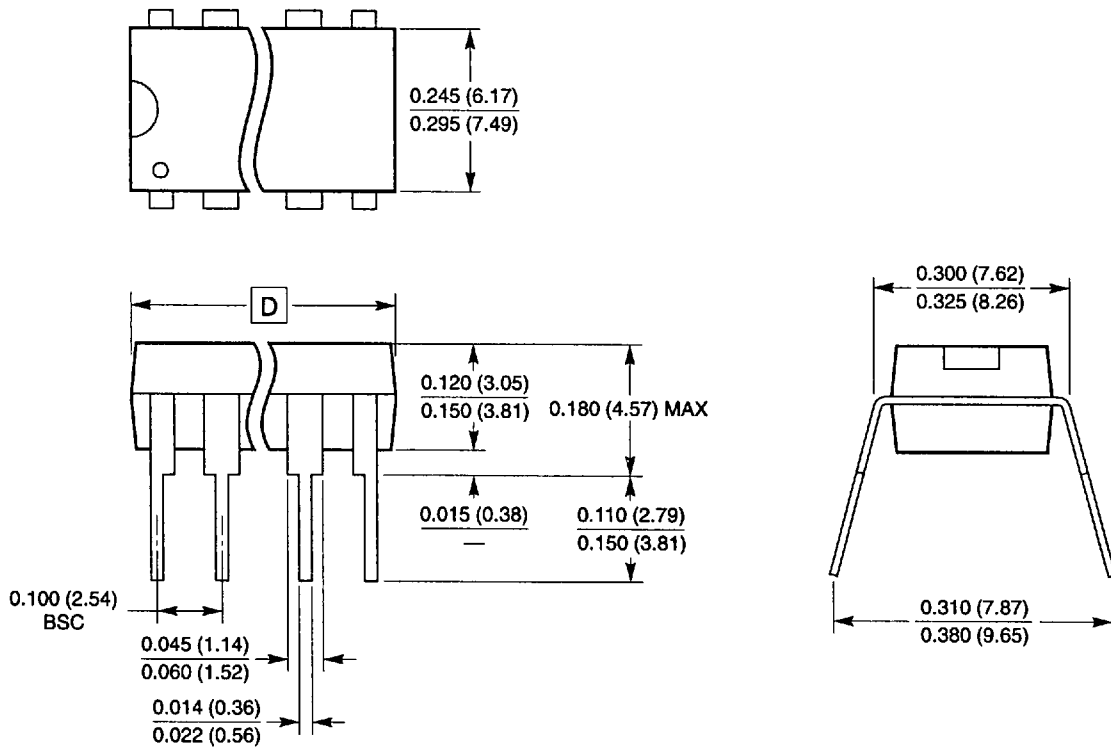
Dimension D		
Pkg	Min	Max
16L	0.3977 (10.10)	0.4133 (10.50)
18L	0.4469 (11.35)	0.4625 (11.75)
20L	0.4961 (12.60)	0.5118 (13.00)
24L	0.5985 (15.20)	0.6141 (15.60)
28L	0.6969 (17.70)	0.7125 (18.10)

Notes:

1. Complies with JEDEC publication 95 MS-013 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.



8-22-LEAD 300 MIL WIDE PLASTIC DIP (P)



Dimension D		
Pkg	Min	Max
8L	0.355 (9.02)	0.385 (9.70)
14L	0.645 (16.38)	0.685 (17.40)
16L	0.745 (21.45)	0.785 (19.94)
18L	0.845 (21.46)	0.885 (22.48)
20L	0.945 (24.00)	0.985 (25.02)
22L	1.045 (26.54)	1.085 (27.56)

Notes:

1. Complies with JEDEC Publication 95 MS001 dimensions; however, some of the dimensions may be more stringent
2. All linear dimensions are in inches and parenthetically in millimeters.