NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6950

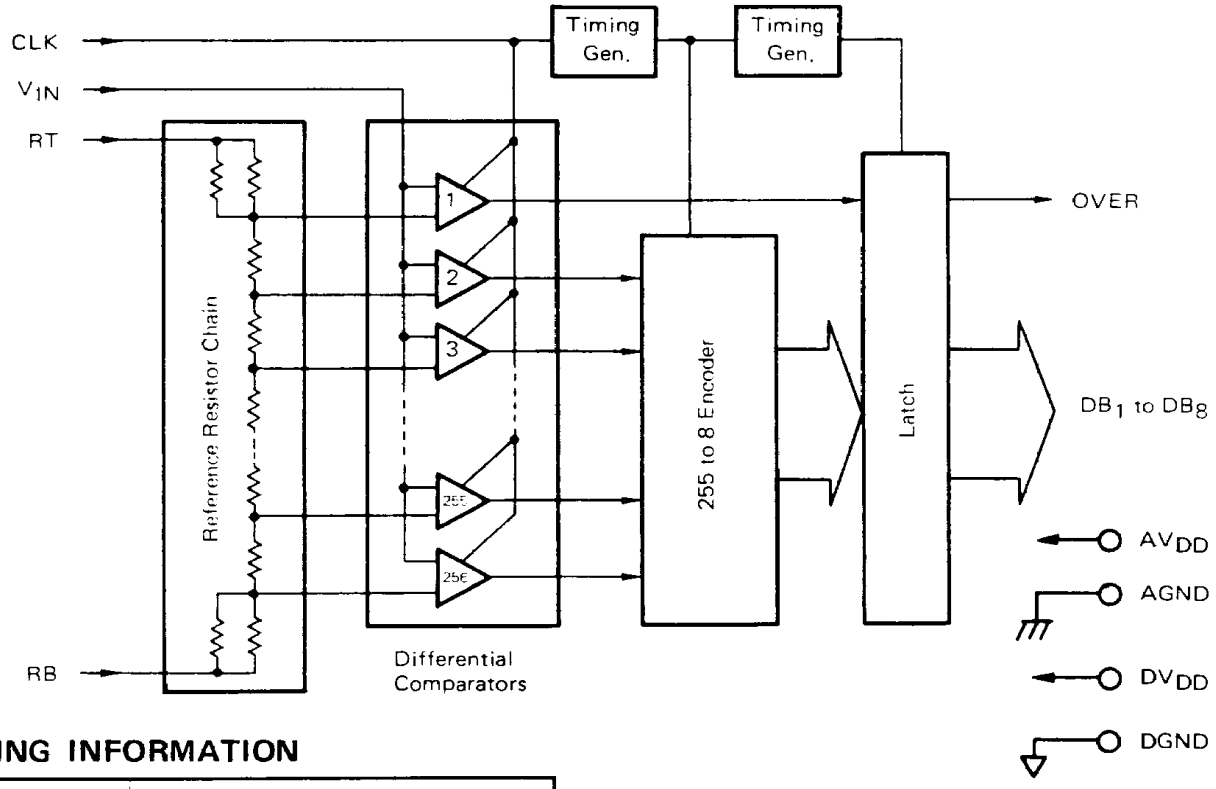
8 bit A/D Converter for Video Signal Processing
CMOS LSI

The μPD6950 is an 8 bit A/D converter designed for use in video applications. The high-speed CMOS processing technology and full-parallel conversion technics adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 15 Msps can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and high-speed facsimile.

FEATURES

- Resolution : 8 bits
- Conversion rate : 15 Msps
- Linearity : ±1.5 LSB MAX.
- Reference voltage : 3.5 V TYP.
- Power supply voltage : +5 V single
- Low power consumption (400 mW TYP.)
- TTL compatible (Digital output)
- 24 pin plastic DIP

BLOCK DIAGRAM



ORDERING INFORMATION

Ordering Name	Package
μPD6950C	24 pin plastic DIP (600 mil)

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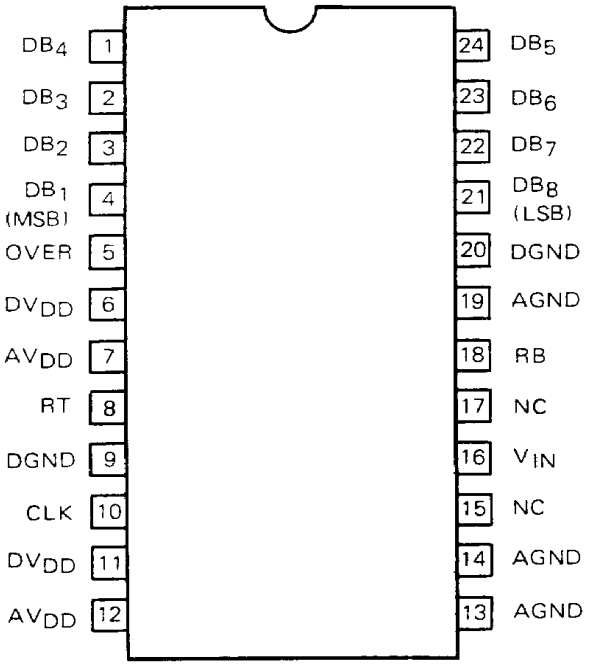
The ★ mark outside the columns denotes major points where revisions or additions are made in this edition.

CONNECTION DIAGRAM (Top View)



1	DB_4	Digital output (4th)
2	DB_3	Digital output (3rd)
3	DB_2	Digital output (2nd)
4	DB_1	Digital output (MSB)
5	OVER	Over range
6	DV_{DD}	Digital power supply
7	AV_{DD}	Analog power supply
8	RT	Reference voltage (high voltage side)
9	DGND	Digital GND
10	CLK	Sampling clock input
11	DV_{DD}	Digital power supply
12	AV_{DD}	Analog power supply
13	AGND	Analog GND
14	AGND	Analog GND
15	NC	No connection
16	V_{IN}	Analog input
17	NC	No connection
18	RB	Reference voltage (Low level side)
19	AGND	Analog GND
20	DGND	Digital GND
21	DB_8	Digital input (LSB)
22	DB_7	Digital input (7th)
23	DB_6	Digital input (6th)
24	DB_5	Digital input (5th)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power supply voltage	−0.3 to +7.0	V
Input terminal voltage	−0.3 to V_{DD}+0.3	V
Output terminal voltage	−0.3 to V_{DD}+0.3	V
Reference GND voltage	−0.3 to +0.3	V
Analog power supply voltage	DV_{DD}−0.3 to DV_{DD}+0.3	V
Analog GND voltage	DGND−0.3 to DGND+0.3	V
Operating temperature range	−20 to +75	°C
Storage temperature range	−40 to +125	°C

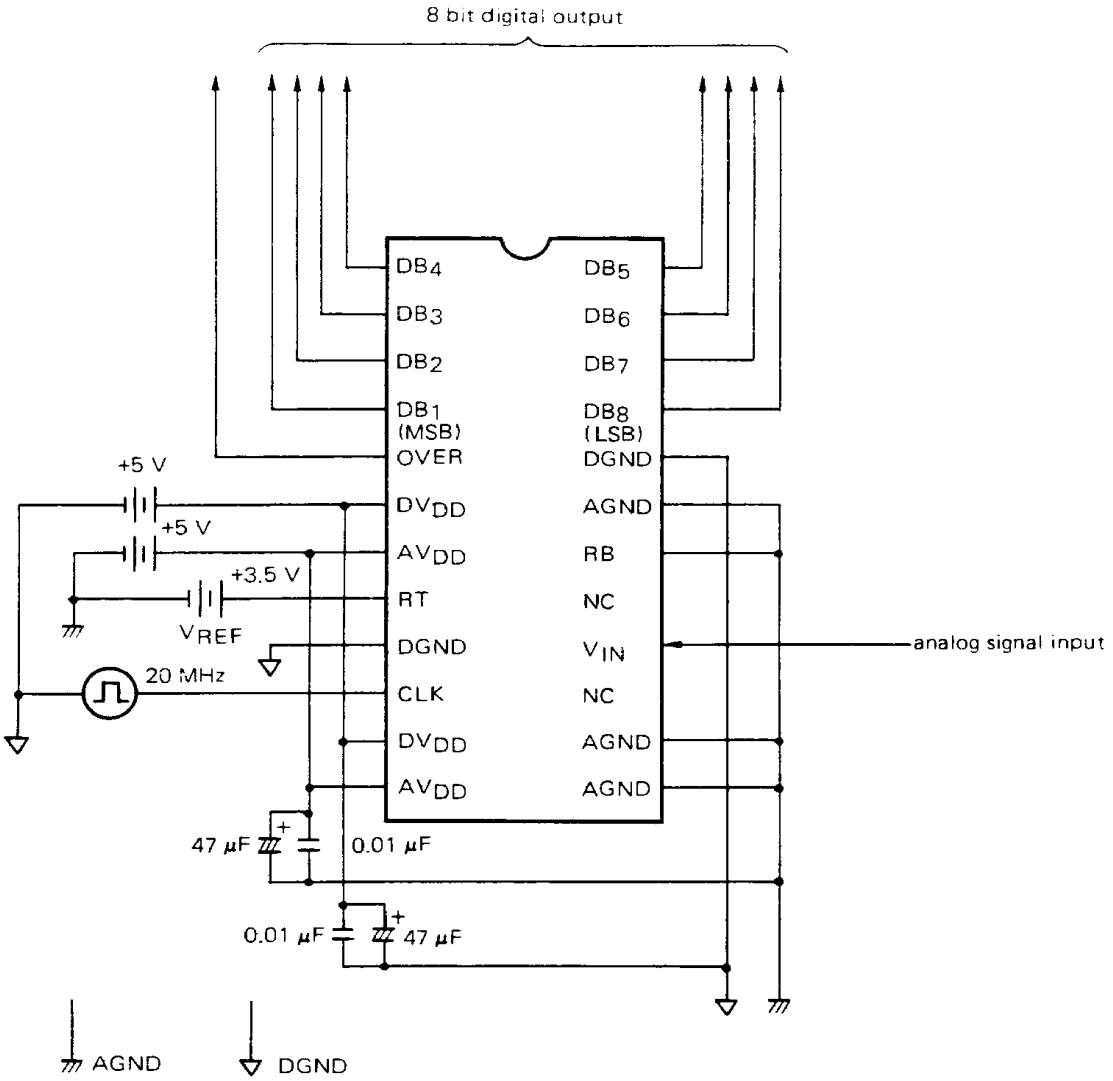
RECOMMENDED OPERATING CONDITION (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	AV_{DD}, DV_{DD}	4.5	5.0	5.5	V	AGND=DGND=0 V
Reference voltage	V_{RT}	2.5	3.5	V_{DD}−1	V	$V_{REF}=V_{RT}-V_{RB}$, V_{RB}=0 V
Sampling clock	f_{samp}	0.01		15	MHz	
Sampling clock low level pulse width	t_{PWL}	25			ns	
Sampling clock high level pulse width	t_{PWH}	25			ns	
CLK input high level	V_{IH}	2.7			V	
CLK input low level	V_{IL}			0.4	V	
Analog input voltage	V_{AIN}	0		V_{REF}	V	

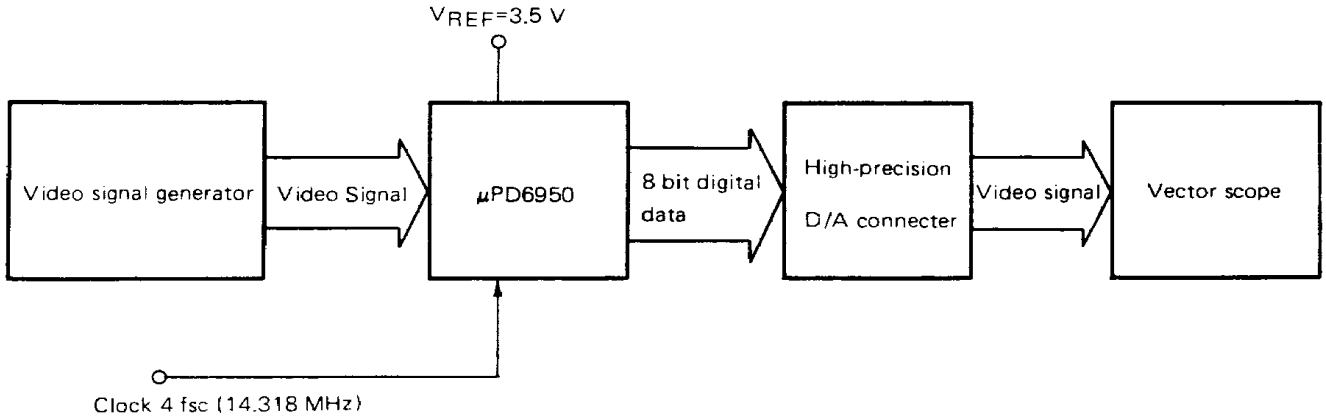
ELECTRICAL CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = AV_{DD} = DV_{DD} = 5 V ±0.25 V, f_{samp} = 15 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply current	I_{DD}		80	110	mA	$I_{DD}=AI_{DD}+DI_{DD}$, $AV_{DD}=DV_{DD}$=5.0 V
Resolution	RES		8		bit	
Non-linearity	NL			±1.5	LSB	$AV_{DD}+DV_{DD}$=5.0±0.25 V, V_{REF}=3.5 V, T_a=0 to 60 °C
Differential gain	DG		3	5	%	40 IRE Ramp Signal, V_{REF}=3.5 V, T_a=0 to 60 °C, f_{samp}=14.318 MHz
Differential phase	DP		3	5	deg	40 IRE Ramp Signal, V_{REF}=3.5 V, T_a=0 to 60 °C, f_{samp}=14.318 MHz
Data output delay time	t_D	20	30	40	ns	CLK ↑→ DB_1 to 6, OVER
Data output high level voltage	V_{OH}	2.8			V	I_{OH}=−1.0 mA
Data output low level voltage	V_{OL}			0.4	V	I_{OL}=1.8 mA
Reference resistance	R_{REF}		1.5		kΩ	Between RT and RB
Analog input resistance	R_{IN}		1		MΩ	
Analog input capacitance	C_{IN}		80		pF	

TEST CIRCUIT

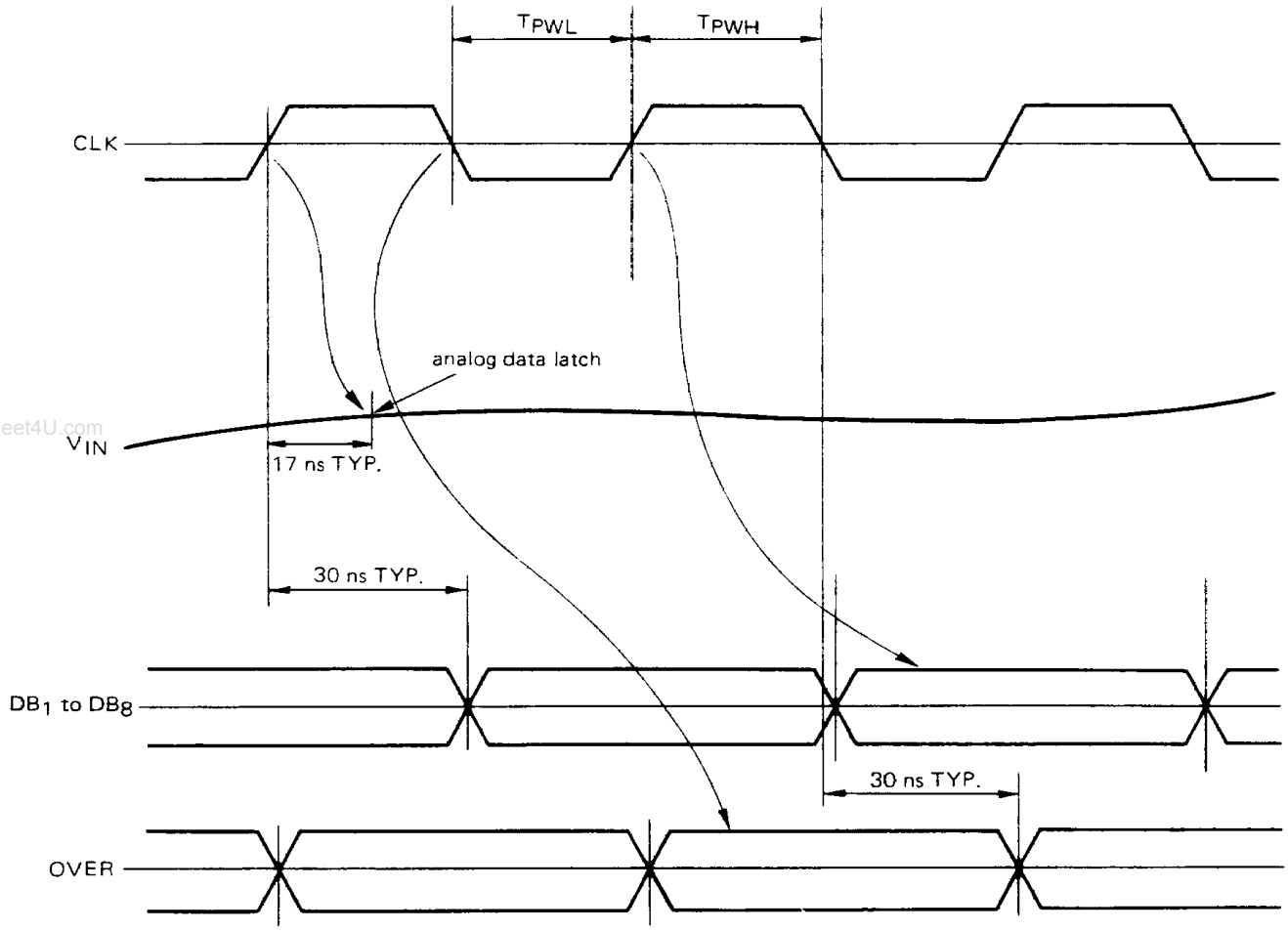


DG AND DP MEASUREMENT BLOCK DIAGRAM



The video signal from the video signal generator is 40 IRE Ramp signal.

TIMING CHART



PIN DESCRIPTIONS

DGND (Pins 9, 20) Digital system ground

AGND (Pins 13, 14, 19) Analog system ground

DV_{DD} (Pins 6, 11) Digital system power supply (+5 V)

AV_{DD} (Pins 7, 12) Analog system power supply (+5 V)

The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

★ Insert by-pass capacitors of about 0.01 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible to the μPD6950 pins. Supply the digital system power from the analog power line through the low path filter to prevent from luch up.

RT (Pin 8) Reference voltage input pin (high voltage side)

RB (Pin 18) Reference voltage input pin (low voltage side)

These pins are the reference voltage V_{REF} input pins.

Normally, these pins are used at RT = 3.5 V and RB = AGND.

V_{IN} (Pin 16) Analog input pin

The input analog signal applied to this pin is latched synchronized with the rising edge of the sampling clock and is subsequently obtained as an 8 bit digital signal from pins DB_1 thru DB_8.

Note: Since the electrostatic resistivity of the analog input pin is a little lower than other pins to achieve the required input characteristics, this input should be handled with extra care.

DB_1 to DB_8 (Pins 1 thru 4, and 21 thru 24) Digital data output pins

DB_1 to DB_8 are the 8 bit digital data output pins. The code format is binary, and the output voltage level is TTL compatible.

The analog signal applied to the analog input pin is latched at the rising edge of the sampling clock, converted to digital data, and then obtained as the output at the next rising edge of the sampling clock.

analog input	digital output								
	OVER	DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6	DB_7	DB_8 (LSB)
0 V (RB) to 1/2 LSB	0	0	0	0	0	0	0	0	0
1/2 LSB to (1+1/2) LSB	0	0	0	0	0	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(254+1/2) LSB to (255+1/2) LSB	0	1	1	1	1	1	1	1	1
(255+1/2) LSB to 3.5 V (RT)	1	1	1	1	1	1	1	1	1
3.5 V (RT) to V_{DD}	1	1	1	1	1	1	1	1	1

$$LSB = \frac{RT - RB}{256}$$

OVER (Pin 5) Over range output pin

This output signal indicates analog signal overflow. A high level output is generated if the input voltage level of the analog input V_{IN} exceeds (255+1/2) LSB where LSB is $(V_{RT}-V_{RB})/256$. The output signal is obtained ★ at the falling edge of the sampling clock.

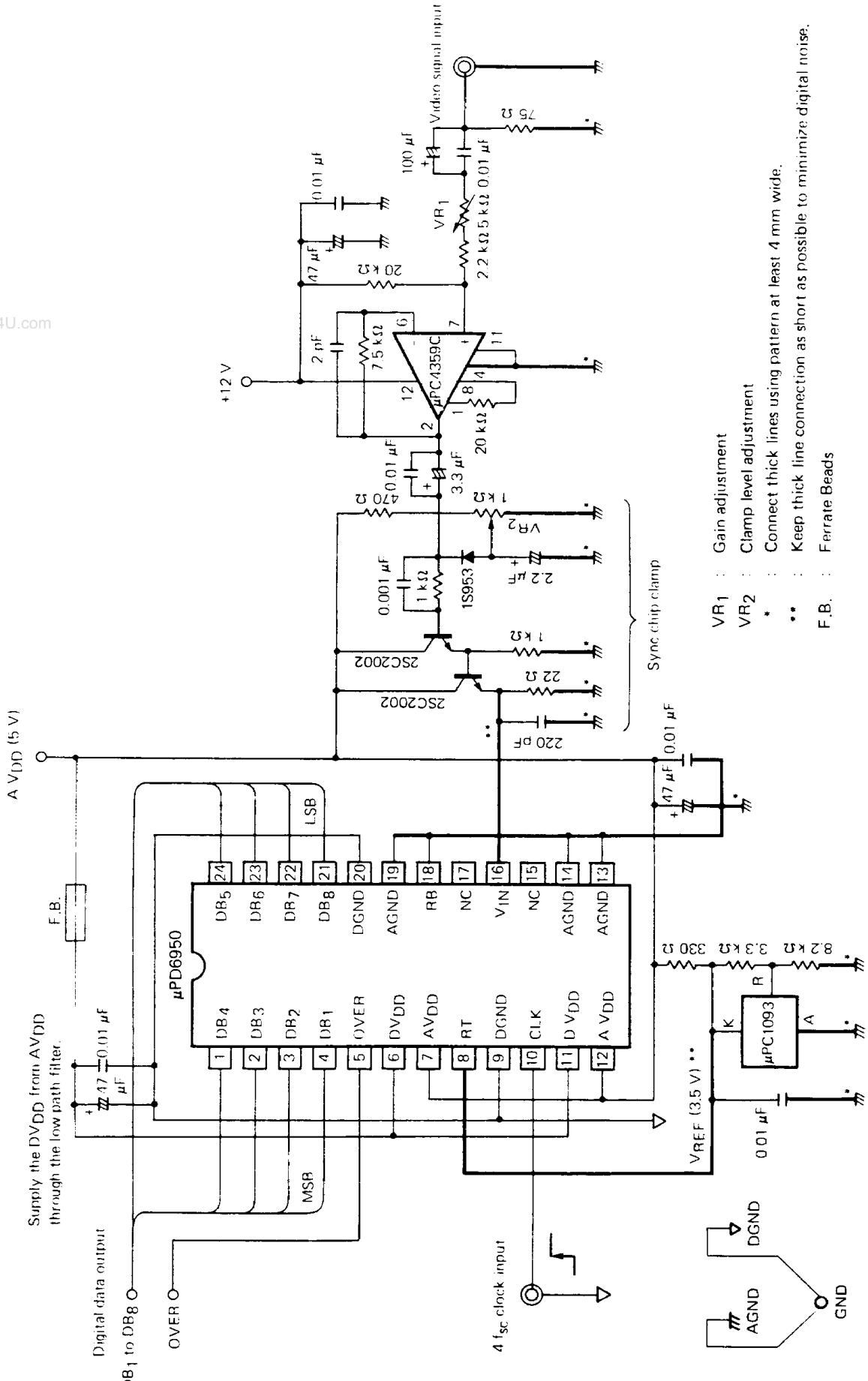
CLK (Pin 10) Sampling clock input pin

The analog signal is latched by the falling edge of the clock signal applied to the A/D converter sampling clock input pin. The complete sequence of events involved in A/D conversion (comparison, encoding, latching, data ★ output) is synchronized with this clock signal. The maximum clock frequency is 15 MHz.

NC (Pins 15, 17) No connection pins

These pins may be connected to analog ground.

APPLICATION CIRCUIT



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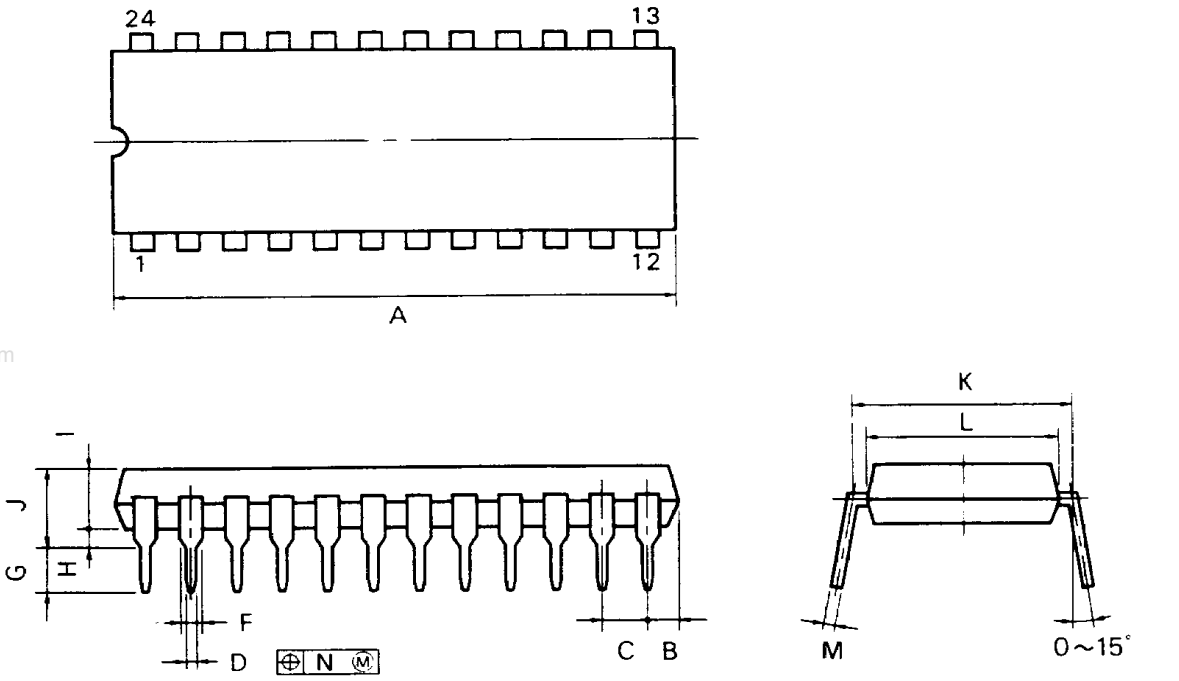
NEC reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

PACKAGE DIMENSIONS (Unit: mm)

24PIN PLASTIC DIP (600 mil)



P24C-100-600

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	33.02 MAX.	1.300 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01

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