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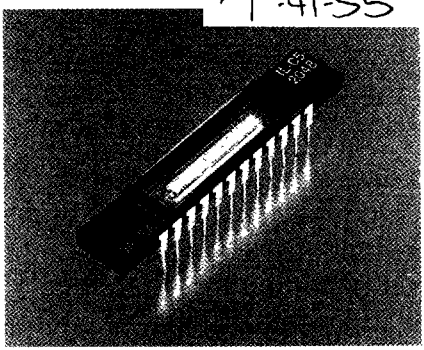
IL-C5/C7 TURBOSENSOR™

IL-C5 -2048, -4096, IL-C7-3456 Linear Image Sensor Arrays

T-41-55

FEATURES

- **TURBOSENSOR™ Ultra High Speed Technology**
- **4096, 3456 or 2048 Elements**
- **Exposure Control**
- **60 MHz Effective Data Rate**
- **Linear Response Photoelements**
- **7μm (H) x 7μm (V) Pixel Size**
- **Dual Output Architecture for Improved Throughput**



DESCRIPTION

DALSA's IL-C5 series linear CCD image sensors use TURBOSENSOR™ technology to provide very high data rates of 30 MHz per output for an effective output rate of 60 MHz. The IL-C5 has a pitch of 7μm, which doubles the resolution within the same optical aperture used by sensors with 14μm pitch, such as the IL-C4 series. The IL-Cx sensors are ideally suited for high speed, high resolution applications, and employ buried channel CCD shift registers to maximize output speed and reduce noise.

The dynamic range of the photoelements exceeds 6,000:1 and provides an output which is linear for all light levels. Exposure control is incorporated to allow integration times shorter than the readout times. Both IL-C5 array sizes are functionally equivalent and are pin-for-pin compatible. IL-C7 pinout specifications are available from DALSA.

APPLICATIONS

The IL-C5 series is ideally suited for applications requiring maximum speed and high resolution. The IL-C5-4096 provides over 800 points-per-inch resolution across five inches.

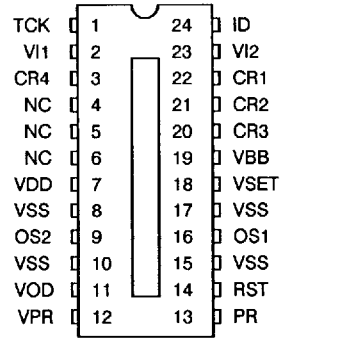
DALSA also offers the CL-Cx line scan cameras which utilize the IL-C5 sensors for:

- **High Performance Document Scanning**
- **Inspection**
- **Bar Code Scanning**
- **Gauging and Measurement**

For mechanical information regarding package size and tolerance, refer to package #50-01-24005 in **Optical and Mechanical Considerations of Sensors** on pp. 101-104 of this databook.

IL-C5 PIN FUNCTIONAL DESCRIPTION

PIN	SYMBOL	NAME
1	TCK	Transfer Clock
2	VI1	White Reference Input 1
3	CR4	Readout Clock, Phase 4
4-6	NC	No Connection
7	VDD	Amplifier Supply Voltage
8, 10, 15, 17	VSS	Ground Reference
9	OS2	Output Signal 2, Even Pixels
11	VOD	Output Drain Bias Voltage
12	VPR	Pixel Reset Bias
13	PR	Pixel Reset Clock
14	RST	Output Reset Clock
16	OS1	Output Signal 1, Odd Pixels
18	VSET	Output Node Set Voltage
19	VBB	Substrate Bias Voltage
20	CR3	Readout Clock, Phase 3
21	CR2	Readout Clock, Phase 2
22	CR1	Readout Clock, Phase 1
23	VI2	White Reference Input 2
24	ID	White Reference Diode Input



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NOTE: Documentation and Pinout apply to IL-C5 REV B Sensors only.

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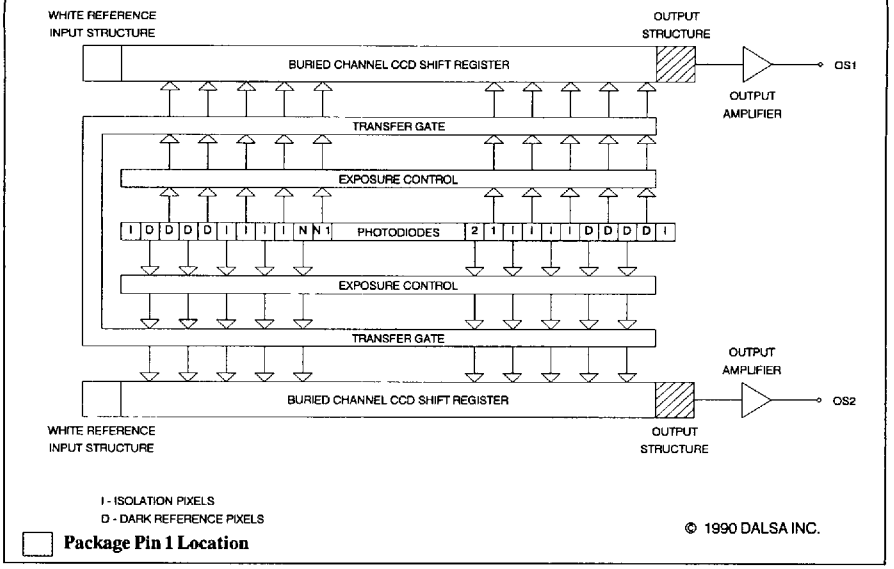
IL-C5 IMAGE SENSOR BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PHOTOELEMENTS

The linear array consists of a line of 4096, 3456, or 2048 photoelements, each with a photosensitive area of 49 square micrometers and center to center spacing of 7 micrometers.

The array of photoelements is enclosed by 4 isolation pixels and 4 dark reference pixels on each end of the array. The dark reference pixels can be used for clamping purposes.

The TURBOSENSOR™ photoelement offers ultra high speed operation and responds linearly with respect to input light intensity. An electronic shutter exists for exposure control and antiblooming.

TRANSFER GATE

This gate controls the flow of light generated signal charge from the photoelements into the CCD shift registers. Electrons from the photoelement are transferred when a high potential (equal to the high clock voltage) is applied to the transfer gate. A single input to the device (TCK) controls the transfer gate for both the even and odd pixels.

CCD SHIFT REGISTERS

There are two buried channel CCD signal transport shift registers, one on each side of the line of photoelements. Buried channel shift registers are used to maximize speed, improve charge transfer efficiency, and reduce noise. Alternate signal charge packets are transferred to the transport CCD shift registers and serially shifted towards the output signal amplifiers.

WHITE REFERENCE

A white reference signal is created in the last CCD register to be read out. The white reference signal is controlled by the signals VI1, VI2 and ID. The reference is created when ID is pulsed low and is read out in the pixel cell after the last dark reference pixel.

OUTPUT STRUCTURE

The signal charge packets from the transport shift registers are transferred serially, over the SET gate, to a floating sensing diffusion. As the signal charge is received, the corresponding potential on the diffusion is applied to the input of a two stage low noise amplifier structure, producing an output signal voltage (OS1 or OS2). The floating sensing diffusion is cleared of signal charge by the reset gate, driven by the reset clock (RST) in preparation for the subsequent signal charge packet.

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RECOMMENDED DC OPERATION

SIGNAL NAMES

The signal names assigned to the package pins describe both the function of the pin as well as the sense of input signals. DC (unclocked) bias and supply voltages are designated with signal names beginning with "V". Clocked signals begin with any other letter and are representative of the function of the pin.

SUPPLY VOLTAGES

VDD provides operating current to the on chip output amplifier and hence should be well regulated. The substrate, or bulk bias voltage, VBB, is negative with respect to ground in some applications. This low current bias should be well regulated. Since protection diodes are provided between many clock lines and the substrate, no clocks can be permitted to go below VBB. A negative VBB can reduce charge injection.

OUTPUT BIAS

A high impedance DC gate bias, VSET, controls transfer of signal charge onto the output sensing diffusion. This voltage should be adjusted externally to optimize output structure operation. If VSET is not optimized, single bright pixels (or a white reference pixel) will appear to "bleed" into adjacent pixels and could be mistaken for very poor CTE or crosstalk.

The shift register output drain voltage, VOD, is a bias provided to the output structure to discharge signal electrons after sensing. This voltage can be fixed at VDD but should be well filtered to reduce noise.

WHITE REFERENCE BIAS

The white reference pixel output can be adjusted to provide an output swing proportional to the difference of the voltages VI2 - VI1 with VI2 > VI1 in order to create the white reference pixel output. Increasing the difference VI2 - VI1 will result in a larger white reference pixel.

To disable the white reference output, or to create a dark reference, VI2 should be less than or equal to the VI1 voltage (VI1 = VI2 = 0). The majority of applications disable this feature.

PHOTOELEMENT BIAS

VPR is a high impedance DC bias that is used to reset the photoelements when exposure control is used. If VPR is too high a loss of low light level sensitivity will occur. If VPR is too low the photodetectors will appear to saturate even under dark conditions.

IL-C5 DC OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS at Tp = 25°C. (See notes)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Amplifier supply voltage	10.0	15.0	16.0	V
VBB	Substrate voltage	-3.0	-0.5	0.0	V
VOD	Shift register drain voltage	8.0	15.0	16.0	V
VSET (IL-C5)	Set Voltage	1.0	3.0	12.0	V
VSET (IL-C7)	Set Voltage	1.0	5.5	12.0	V
VPR	Pixel Reset Bias	5.0	10.0	18.0	V
VI1	White Reference Input 1	0.0	2.0	12.0	V
VI2	White Reference Input 2	0.0	5.0	12.0	V

NOTES:

(1) Voltages with respect to ground (VSS).

(2) Tp is defined as the package temperature.

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RECOMMENDED CLOCK OPERATION

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PHOTOELEMENTS

Signal charge electrons are photogenerated during the exposure period, which is set by the time between the high to low transition of the Pixel Reset Clock (PR) and the following high to low transition of the transfer pulse (TCK). Signal charge is integrating when PR and TCK are low. Exposure control is achieved by adjusting the duration of the high level of the pixel reset clock. Antiblooming can be achieved by returning the PR clock to a positive potential for its low period. The typical level of antiblooming occurs with a low potential of PR of approximately 4 volts. When TCK is pulsed high the pixel data is transferred into the first phase (CR1) of the CCD readout shift register.

TRANSPORT CLOCKS

Four phase transport clocks (CR1-CR4) are required for the IL-C5. Two phase is used for the IL-C7. All transport clocks can be operated at 50% duty cycle continuously. CR1 and CR3 are complementary, non-overlapping as are CR2 and CR4. The clock high voltages can be set by the user for the specific application. In general, higher clock voltages will provide better CTE and higher operating speeds; however, power dissipation on the device will increase due to an increase in C dV/dt current to the clocks. Power dissipation must be considered for the larger arrays, especially the 4096 element device. Rise times on the clock should typically be 1/6th of the period.

TRANSFER CLOCK

The transfer clock (TCK) controls the transfer of signal from the pixel into the CCD shift register. The high voltage on this clock line should be equal to the high voltage on the transport clocks. The TCK low voltage can be brought as far negative as VBB. TCK should occur once per frame, and only after the previous frame has been readout.

OUTPUT CONTROL CLOCKS

One output structure clock (RST) is required to clear the output node after sensing. This clock should go to a high voltage equal to the transport clock (CR) high voltages, and to a low of VSS. During RST high, the outputs (OS1 and OS2) will go to a reset level as shown in the clock diagrams.

OUTPUT SIGNALS

The output signals OS1 and OS2 provide video data for the odd and even pixels, respectively. The frequency of OS1 and OS2 is equal to the frequency of the RST clock. It is recommended to buffer the output signals to provide current gain. The AC output signal rides on a DC offset. It is recommended that AC coupling be used after the buffer.

IL-C5 CLOCK CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS at Tp = 25°C.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VH(CR)	Transport clock HIGH	7.0	12.0	16.0	V
VL(CR)	Transport clock LOW	0.0	0.0	0.5	V
VH(TCK)	Transfer clock HIGH	7.0	12.0	16.0	V
VL(TCK)	Transfer clock LOW	0.0	0.0	0.5	V
VH(ID)	Input Diode clock HIGH	7.0	12.0	16.0	V
VL(ID)	Input Diode clock LOW	0.0	0.0	0.5	V
VH(RST)	Reset clock HIGH	7.0	12.0	16.0	V
VL(RST)	Reset clock LOW	0.0	0.0	0.5	V
VH(PR)	Pixel reset clock HIGH	7.0	12.0	16.0	V
VL(PR)	Pixel reset clock LOW	VBB	0.0	12.0	V
f(RST)	Reset freq.(per output rate)		15	30	MHz
f(DATA)	Data freq. (effective data rate)		30	60	MHz

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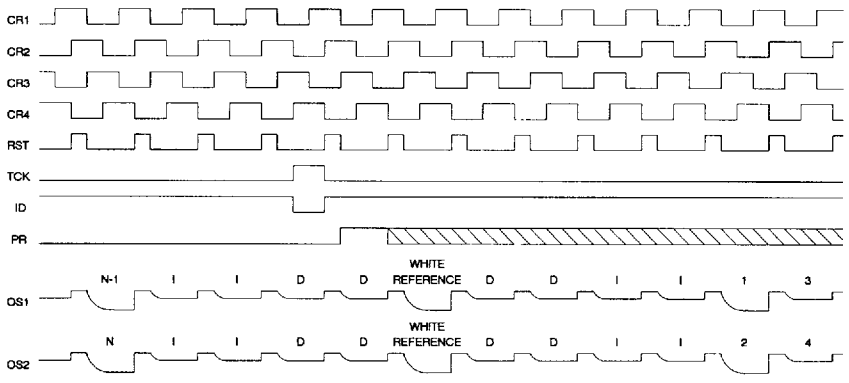
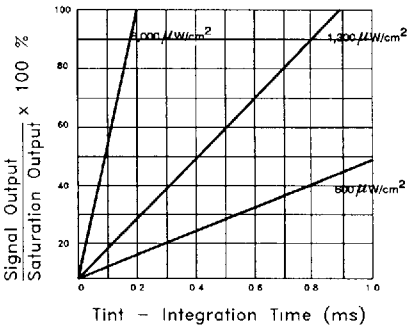
IL-C5 OVERALL CLOCKING



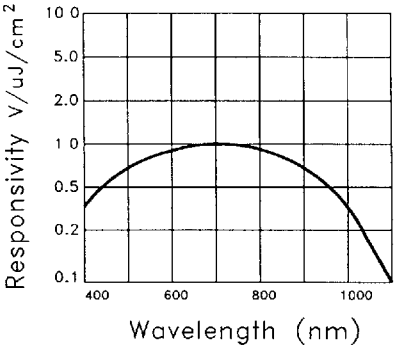
I - ISOLATION PIXELS
D - DARK PIXELS
N - NUMBER OF PHOTOELEMENTS IN ARRAY

NOTES 1) TIMING IS SHOWN FOR A FULL CYCLE OF N/2 + 8 CR1 PULSES BETWEEN TCK PULSES
2) PR IS USED TO CONTROL INTEGRATION TIME AND IS DETERMINED BY THE TIME BETWEEN THE FALLING EDGE OF PR AND THE NEXT TCK PULSE
Consult DALSA for IL-C7 timing

IL-C5 PERFORMANCE MEASUREMENTS



Output vs. Integration Time



Spectral Response

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IL-C5 PERFORMANCE CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C. (See notes).				
Dynamic range[1]		6,000:1		
Noise Equivalent Exposure (NEE)		200		pJ/cm^2
Saturation Equivalent Exposure (SEE)[2]		1200		nJ/cm^2
Responsivity[2]		0.8		V/μJ/cm^2
Saturation Output Amplitude (V_{SAT})[3]		960		mV
V_{NOISE}[4]				
Peak-Peak		0.8		mV
RMS		0.16		mV
FPN (exposure control disabled)		2.0		mV
FPN (exposure control enabled)		10.0		mV
PRNU (exposure control disabled)[5]		5		% V_{SAT}
PRNU (exposure control enabled)[5]		15		% V_{SAT}
CTE[6]	0.9999	0.99999	0.999999	
White Reference Amplitude[3]		250		mV
DC Output Offset		9.5		V
DC Balance		100		mV
Output Gain Mismatch		10		% V_{SAT}
Storage Temperature (T_P)[7]	−70		+125	°C
Operating Temperature (T_P)[7]	−60		+90	°C

Notes:

1. Ratio of VSAT to RMS Noise with reset noise eliminated through correlated double sampling (CDS).
2. Responsivity at peak Quantum Efficiency (near 700 nm).
3. Output amplitude with respect to dark reference level.
4. Amplifier noise measured with reset noise eliminated through correlated double sampling (CDS)
5. PRNU is measured at approximately 50% VSAT and is the difference between the active pixels with the lowest and highest outputs, expressed as a percentage of VSAT.
6. CTE is the measurement for a one stage transfer, measured at f_{RST} = 3.75 MHz.
7. TP is package temperature.
8. Specifications for IL-C7 series sensors available.

Test Conditions:

1. All tests are done at f_{RST} = 3.75 MHz, or f_{DATA} = 7.5 MHz.
2. Light Source QTH lamp with WBHM, unless otherwise noted
3. VDD, VOD = 15 V; VBB = 0 V; Clock high voltage 12 V, low voltage 0 V, (includes CRx, Clx, CSx, TCK, RST as applicable); VSET as required for maximum VSAT and CTE

IL-C5 ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C.				
Output impedance		200		Ω
Amplifier supply current		20		mA
DC Bias Currents (VOD, VSET, VBB)			1	mA
Amplifier power dissipation	225	300	550	mW
Resistance to VBB				
Transport clock (CR1, CR2, CR3, CR4)			5	
Transfer clock (TCK)		5		MΩ
Reset, Set gate		5		MΩ
Capacitance to VBB				
Transport clock (CR1, CR2)[1]		250		pF
Transfer clock (TCK)[1]			25	
Reset (RST), Set (VSET) gate		12		pF

Notes:

1. Capacitance given for 2048 element array. For 4096 element array apply the following factors: 1.9.

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Optical and Mechanical Considerations of Sensors

Optical and Mechanical Considerations of DALSA CCD Image Sensors

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This applications note provides packaging information for the sensors listed in this databook. Please refer to the tables on the following pages for the critical dimensions of each image sensor series. For more information on a particular image sensor, please refer to the specific datasheet.

FIGURE 1. DIMENSIONS OF PACKAGE # 50-01-24005

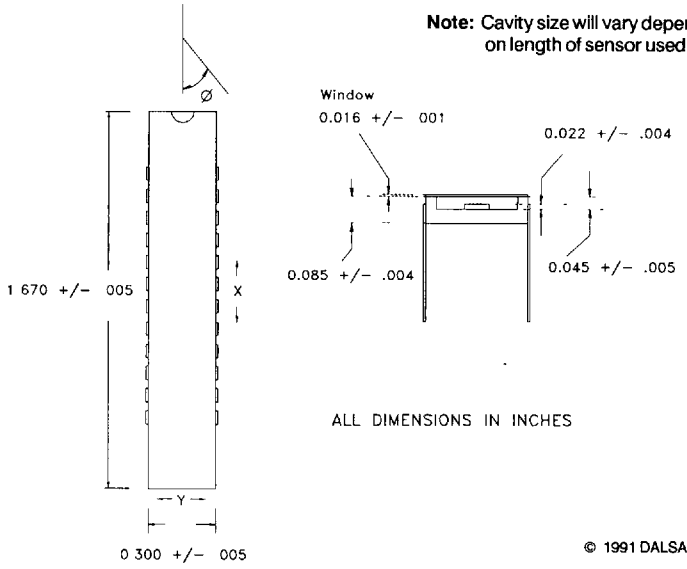

TABLE 1. PACKAGE # 50-01-24005 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-24005	IL-C3-0128	0.55 ± .09	0.15 ± .02	$0^{o} \pm 3.0^{o}$
50-01-24005	IL-C3-0256	0.55 ± .08	0.15 ± .02	$0^{o} \pm 2.5^{o}$
50-01-24005	IL-C3-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C9-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C4-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C4-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C5-2048	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C5-4096	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C6-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-E1-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-E1-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-E1-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-F2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-F2-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-F2-2048	0.55 ± .04	0 15 ± .02	$0^{o} \pm 1.0^{o}$

Note: X = center imaging area to center pin 1 along package Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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FIGURE 2. DIMENSIONS OF PACKAGE # 50-01-40003

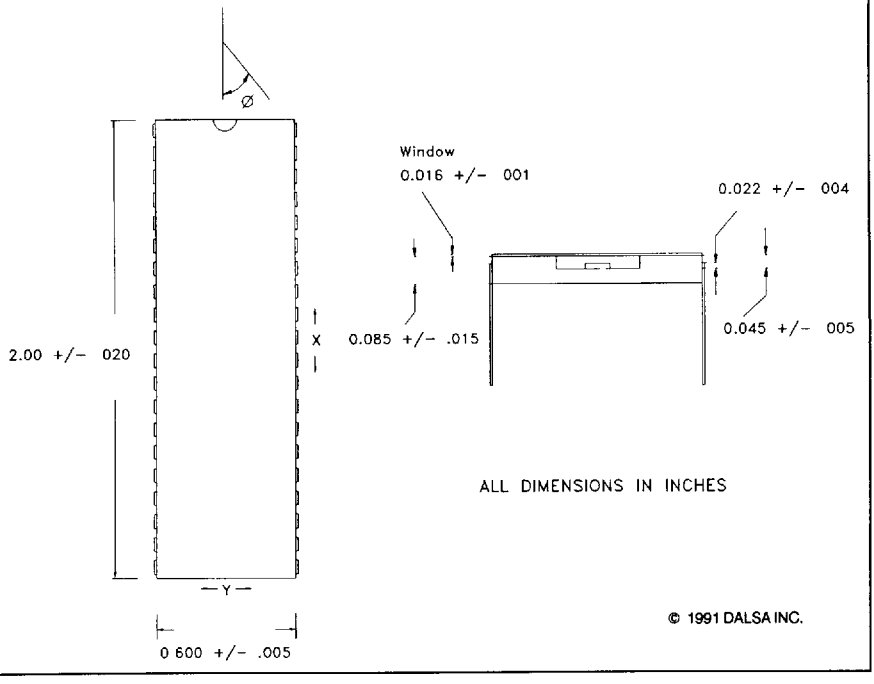

TABLE 2. PACKAGE # 50-01-40003 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40003	IT-C5-2048	0.95 ± 0.1	0.3 ± 0.05	$0^{\circ} \pm 2.5^{\circ}$
50-01-40003	IT-C5-4096	0.95 ± 0.08	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-E1-1536	0.95 ± 0.08	0.3 ± 0 05	$0^{\circ} \pm 2.0^{\circ}$
50-01-40003	IT-E1-2048	0.95 ± 0.06	0.3 ± 0.05	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-F2-2048	0.95 ± 0.06	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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FIGURE 3. DIMENSIONS OF PACKAGE # 50-01-24002

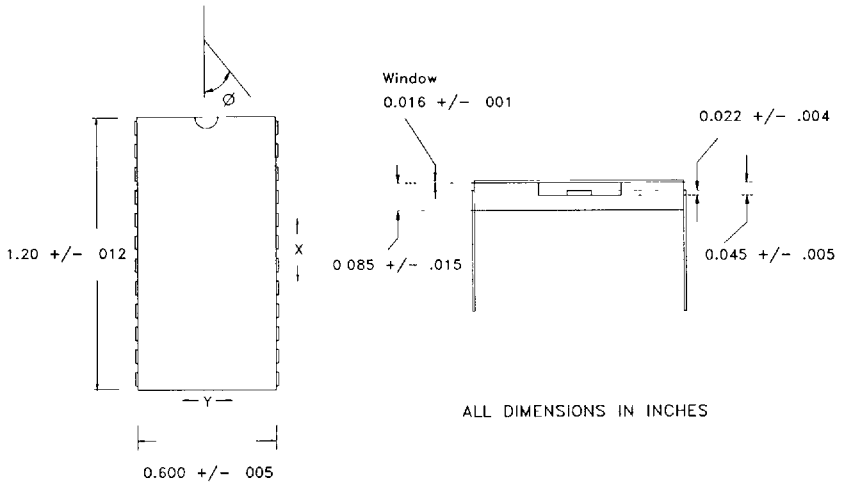

TABLE 3. PACKAGE # 50-01-40002 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40002	IA-D1-0032	0.56 ± 0.12	0.3 ± 0.05	$0^{o} \pm 5.0^{o}$
50-01-40002	IA-D1-0064	0.57 ± 0.09	0.3 ± 0.04	$0^{o} \pm 4.0^{o}$
50-01-40002	IA-D1-0128	0.59 ± 0.12	0.3 ± 0.03	$0^{o} \pm 2.5^{o}$
50-01-40002	IA-D1-0256	0.71 ± 0.10	0.3 ± 0.03	$0^{o} \pm 1.5^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation

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FIGURE 4. DIMENSIONS OF PACKAGE # 50-01-28004

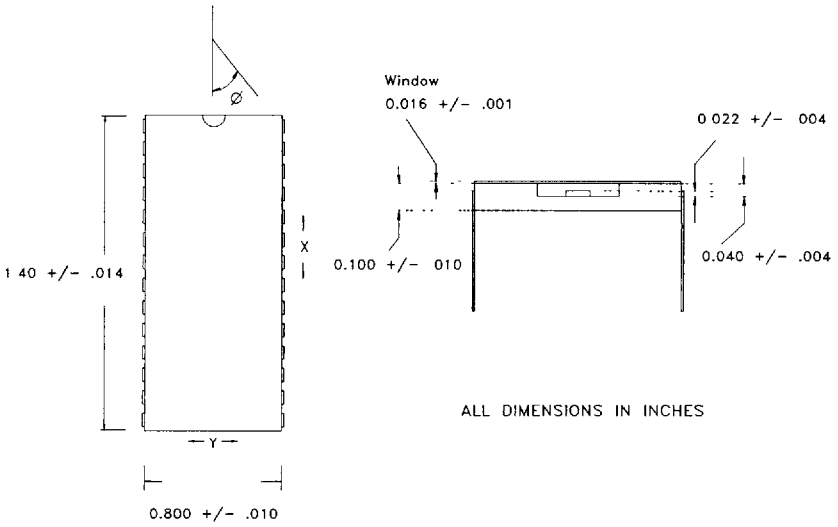

TABLE 4. PACKAGE # 50-01-28004 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-28004	IA-D2-0512	0.65 ± 0.08	0.4 ± 0.04	$0^{o} \pm 3.0^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation