HM6289 Series

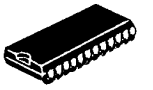
16384-Word × 4-Bit High Speed CMOS Static RAM (with $\overline{OE}$)

The Hitachi HM6289 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. Low power version retains the data with battery back up.

HM6289 Series

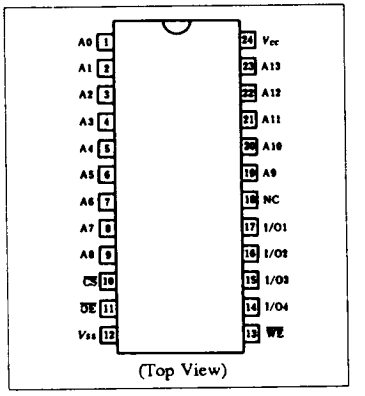


(CP-24D)

Features

- High speed
  - Access time: 25/35 ns (max)
- High density 24-pin SOJ package
- Low power
  - Active mode: 300 mW (typ)
  - Standby mode: 100 µW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

Pin Arrangement



(Top View)

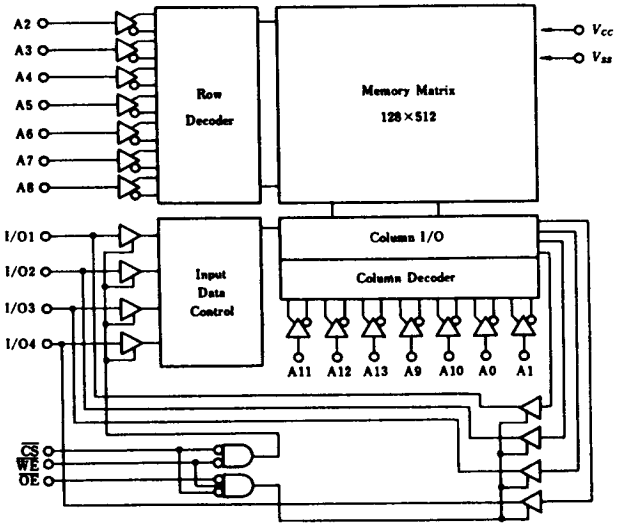
Ordering Information

Type No.	Access Time	Package
HM6289JP-25	25 ns	300-mil
HM6289JP-35	35 ns	24-pin
HM6289LJP-25	25 ns	SOJ
HM6289LJP-35	35 ns	(CP-24D)

Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



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Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O pin	Ref. Cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	Icc	Dout	Read cycle (1)–(3)
L	H	L	Write	Icc	Din	Write cycle (1)–(2)
L	L	L	Write	Icc	Din	Write cycle (3)–(6)

Note: ×; H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{in}	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	–55 to +125	°C
Storage temperature range under bias	T_{bias}	–10 to +85	°C

Note: *1. Vin min = –2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	Vcc = Max Vin = 0V to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0 V to Vcc
Operating Vcc current	Icc	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. cycle
Standby Vcc current (1)	I_{SB1}*2	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V
	I_{SB1}*3	—	0.02	0.1	mA	0V ≤ Vin ≤ 0.2 V or Vcc – 0.2 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. P-version
*3. LP-version

Capacitance (Ta = 25°C, f = 1MHz)

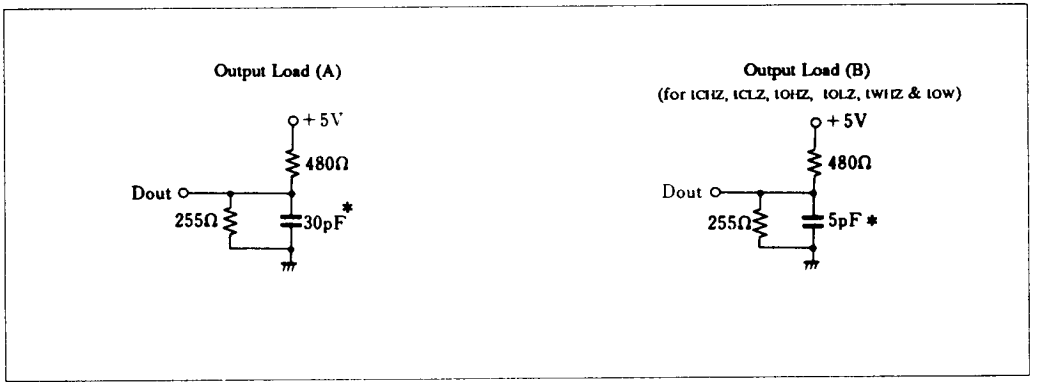
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	V I/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures



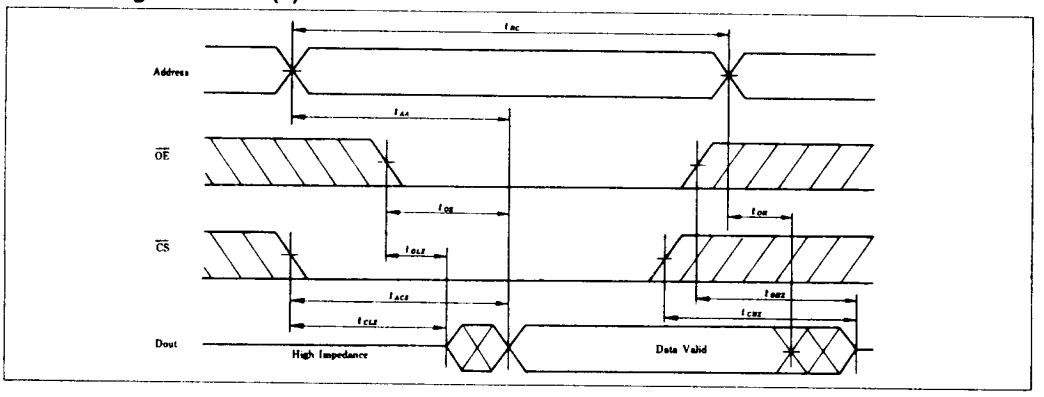
Note: * Including scope & jig.

Read Cycle

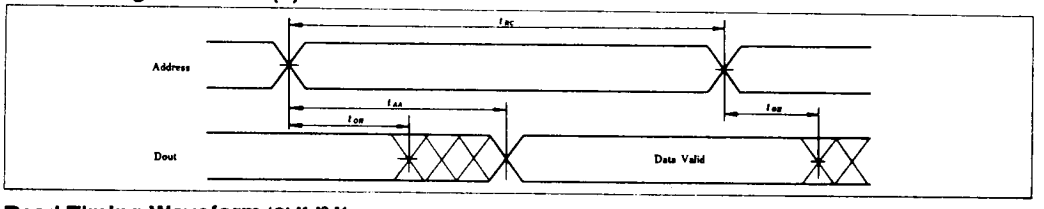
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	12	0	20	ns
Chis disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Note: *1. Output transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

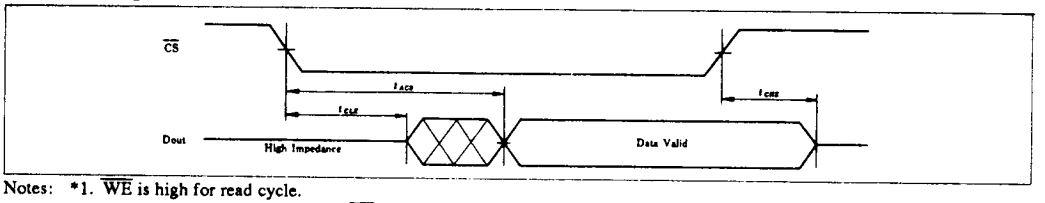
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1,*2,*4



Read Timing Waveform (3) *1,*3,*4



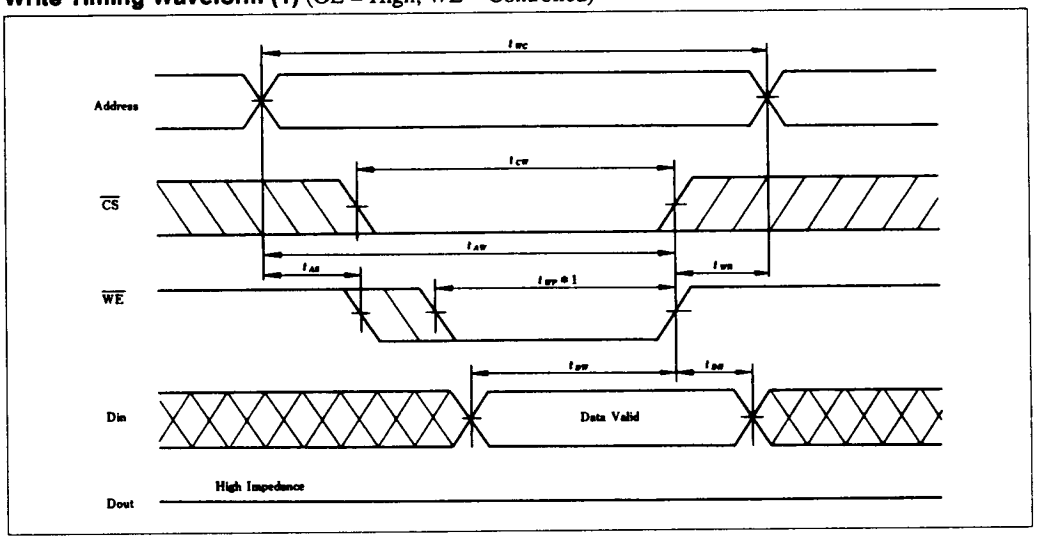
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

Write Cycle

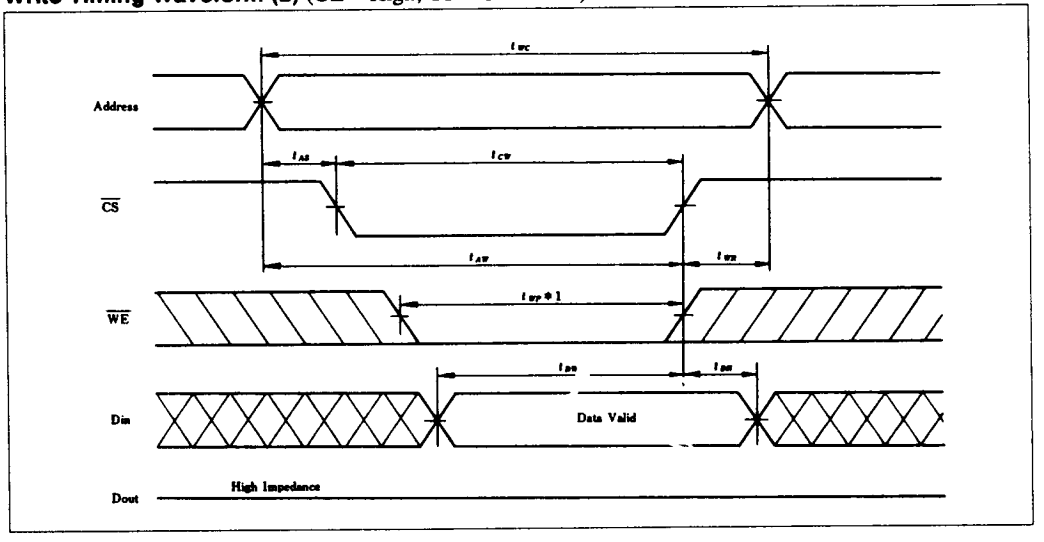
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Write cycle time	tWC	25	—	35	—	ns
Chip selection to end of write	tCW	20	—	30	—	ns
Address valid to end of write	tAW	20	—	30	—	ns
Address setup time	tAS	0	—	0	—	ns
Write pulse width	tWP	20	—	30	—	ns
Write recovery time	tWR	0	—	0	—	ns
Output disable to output in high-Z*1	tOHZ	0	10	0	10	ns
Write to output in high-Z*1	tWHZ	0	8	0	10	ns
Data to write time overlap	tDW	12	—	20	—	ns
Data hold from write time	tDH	0	—	0	—	ns
Output active from end of write*1	tOW	5	—	5	—	ns

Note: *1. Output transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

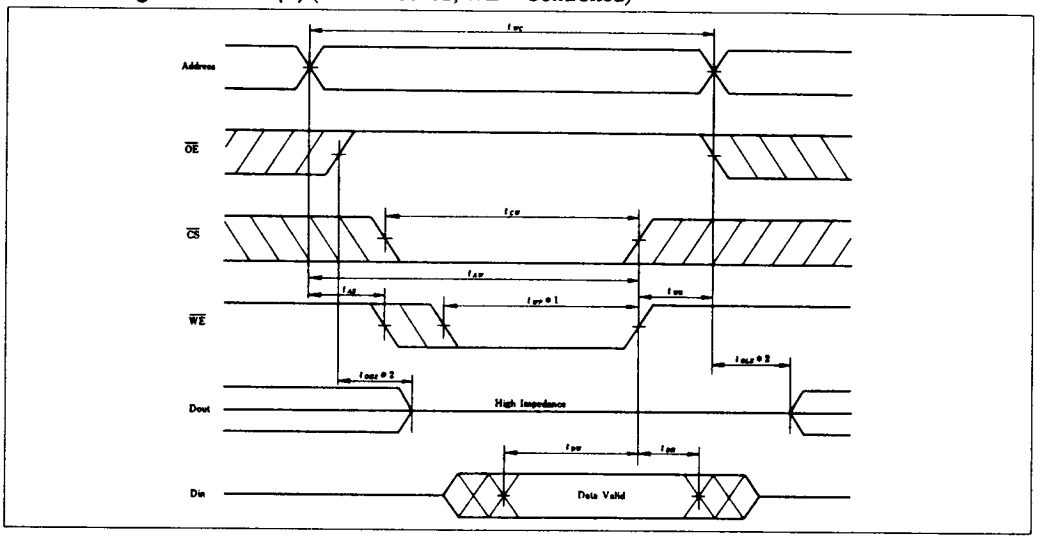
Write Timing Waveform (1) ($\overline{OE}$ = High, $\overline{WE}$ = Controlled)



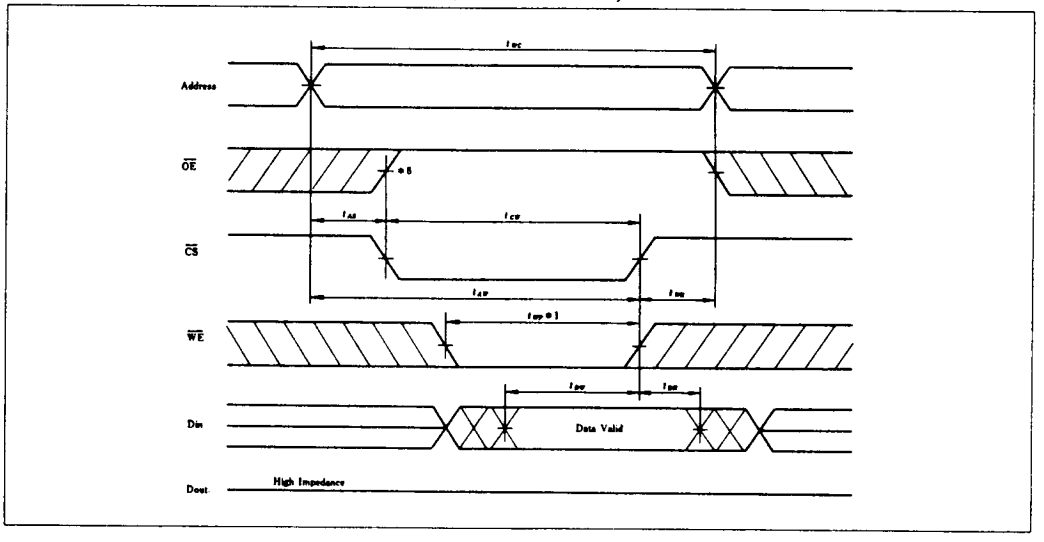
Write Timing Waveform (2) ($\overline{OE}$ = High, $\overline{CS}$ = Controlled)



Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ = Controlled)



Write Timing Waveform (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ = Controlled)



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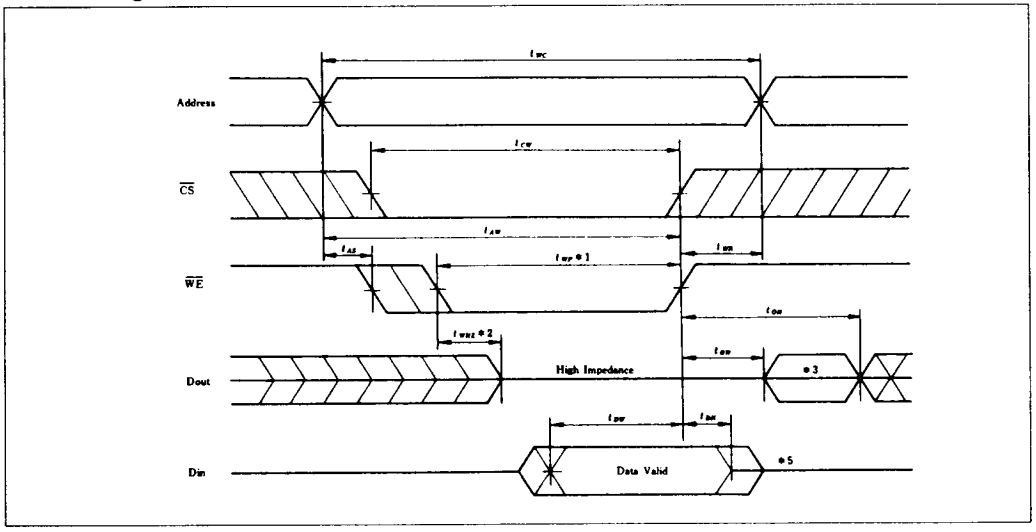
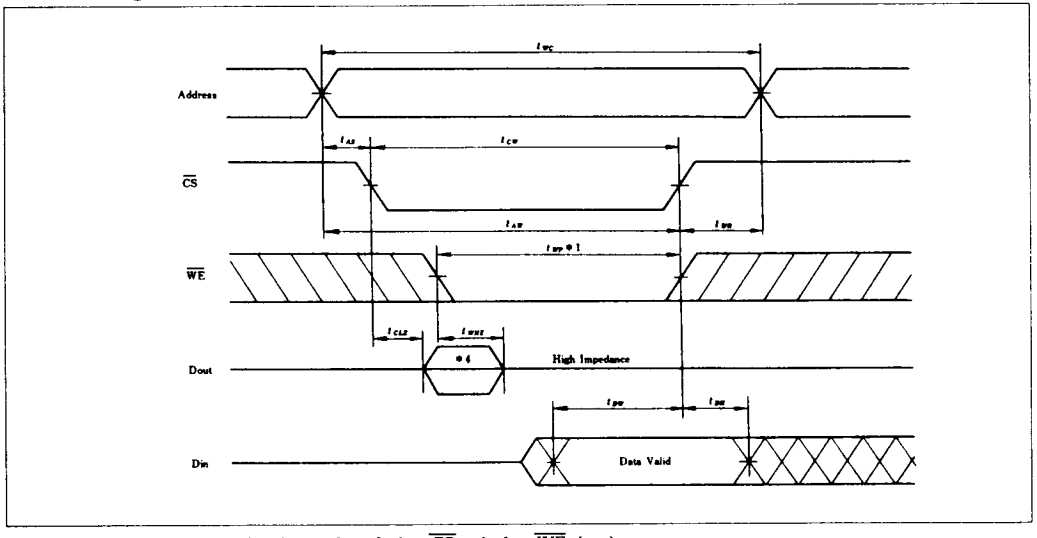
Write Timing Waveform (5) ($\overline{OE}$ = Low, $\overline{WE}$ = Controlled)



Write Timing Waveform (6) ($\overline{OE}$ = Low, $\overline{CS}$ = Controlled)



Notes: *1 A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (tWP)
*2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tOW. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle, if tWR is long enough.
*7. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

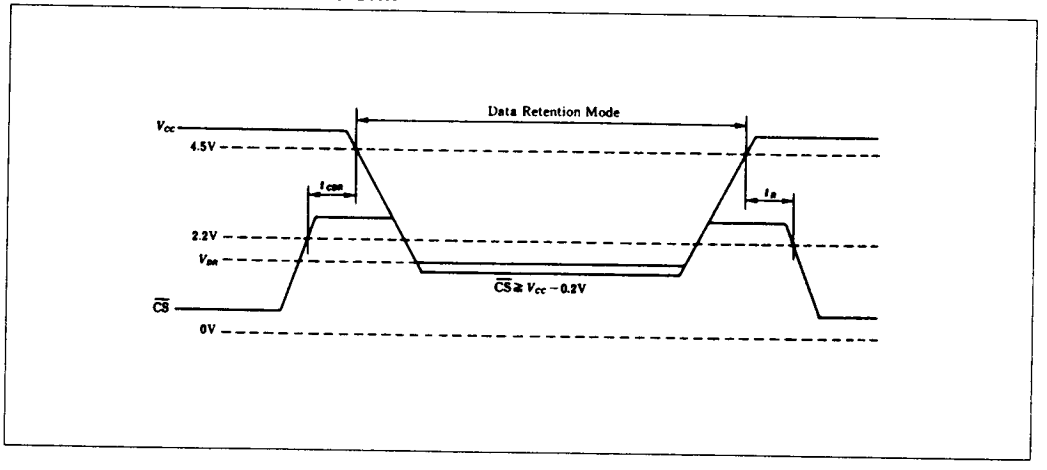
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

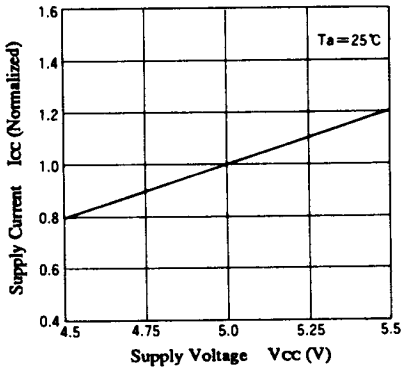
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V,
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Note: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

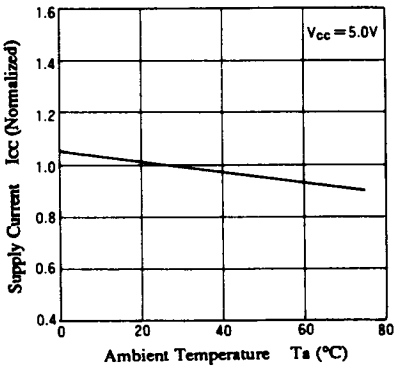
Low Vcc Data Retention Waveform



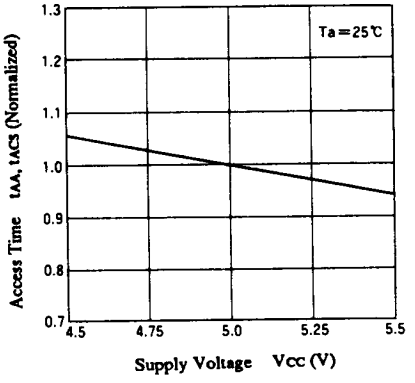
Supply Current vs. Supply Voltage



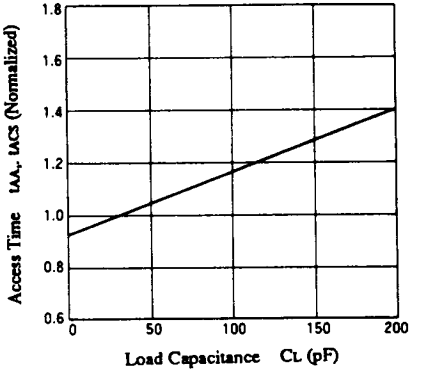
Supply Current vs. Ambient Temperature



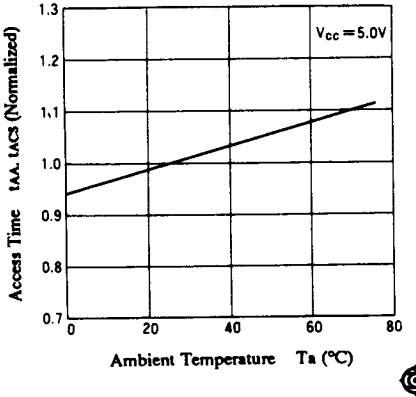
Access Time vs. Supply Voltage



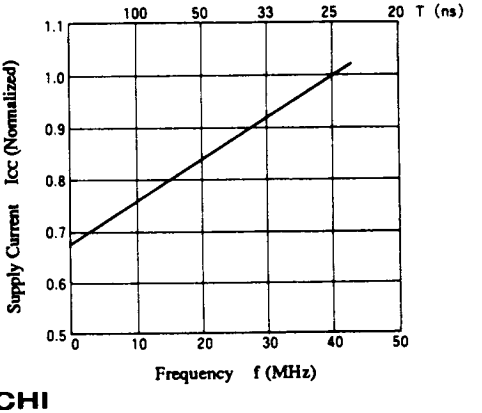
Access Time vs. Load Capacitance



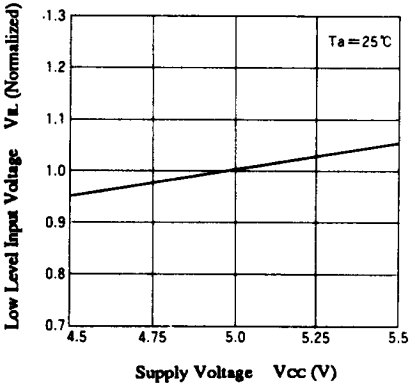
Access Time vs. Ambient Temperature



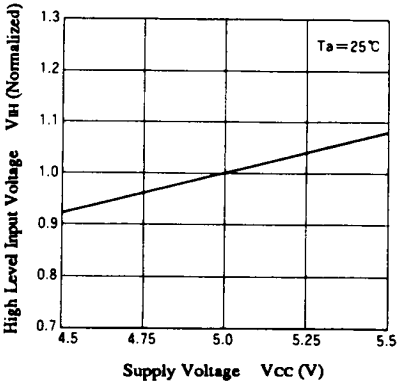
Supply Current vs. Frequency



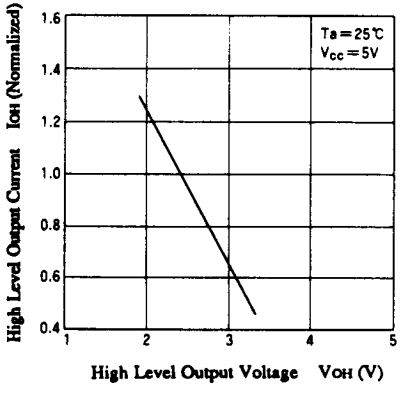
Low Level Input Voltage vs. Supply Voltage



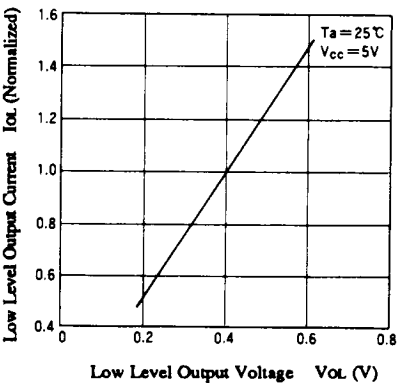
High Level Input Voltage vs. Supply Voltage



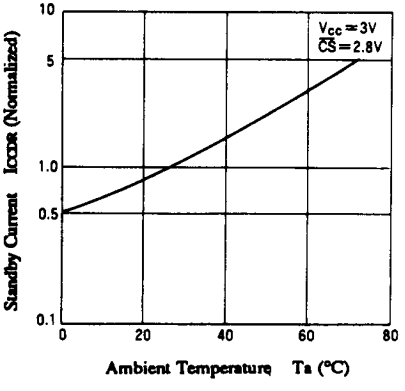
Output Current vs. Output Voltage (1)



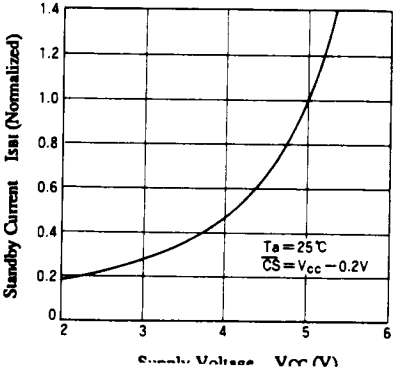
Output Current vs. Output Voltage (2)



Standby Current vs. Ambient Temperature



Standby Current vs. Supply Voltage



Standby Current vs. Input Voltage