Integrated Device Technology, Inc.

2 x 16K x 16 CMOS STATIC RAM MODULE

IDT7MB4009

FEATURES:

- High Density 512K CMOS static RAM Module
- Cost effective surface mount components mounted on an epoxy laminate (FR-4) substrate
- Packaged in a 44 pin, 600 mil wide DIP (Dual In-line Package)
- Fast access time: 15ns (max.)
- Common data and address pins for both banks of RAM resulting in increased density
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL compatible

DESCRIPTION:

The IDT7MB4009 is a 2 x 16K x 16 high-speed static RAM module constructed on an epoxy laminate surface using 8 16K x 4 static RAMs packaged in surface mount packages. Extremely fast speeds can be obtained by using RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology.

The IDT7MB4009 is organized as two separate banks of 16K x 16 RAM with common address and data pins to minimize the module size. The IDT7MB4009 is packaged in a 44 pin, 600 mil wide DIP, packing 512K of fast memory in 1.8 square inches.

The IDT7MB4009 is available with access time as fast as 15ns, with maximum power consumption of 4.2W.

All inputs and outputs of the IDT7MB4009 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

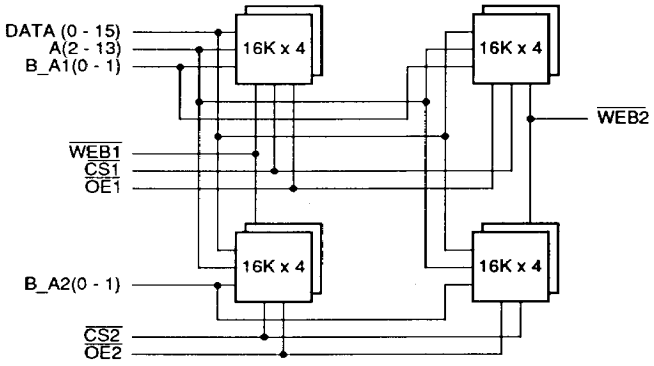
PIN CONFIGURATION(1)

GND	1	44	Vcc
D(0)	2	43	B_A1(0)
D(1)	3	42	B_A1(1)
D(2)	4	41	B_A2(0)
D(3)	5	40	B_A2(1)
D(4)	6	39	WEB2
D(5)	7	38	A(2)
D(6)	8	37	A(3)
D(7)	9	36	A(4)
D(8)	10	35	A(5)
GND	11	34	A(6)
$\overline{CS1}$	12	33	$\overline{CS2}$
$\overline{OE1}$	13	32	$\overline{OE2}$
D(9)	14	31	Vcc
D(10)	15	30	A(7)
D(11)	16	29	A(8)
D(12)	17	28	A(9)
WEB1	18	27	A(10)
D(13)	19	26	A(11)
D(14)	20	25	A(12)
D(15)	21	24	A(13)
Vcc	22	23	GND

2707 drw 01

NOTE:
1. For module dimensions, please refer to module drawing M13 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2707 drw 02

PIN NAMES

A (2-13)	Address Input
B_A1 (0-1)	Burst address, Bank 1
B_A2 (0-1)	Burst address, Bank 2
D (0-15)	Data Inputs/Outputs
$\overline{WEB1}$	Write Enable, Upper
$\overline{WEB2}$	Write Enable, Lower
$\overline{CS1}$, 2	Chip Select - Bank 1, 2
$\overline{OE1}$, 2	Output Enable - Bank 1, 2
GND	Ground
Vcc	Power Supply

2707 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	50	mA

2707 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2707 tbl 03

NOTE:
1. V_{IL} = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2707 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB4009 Min.	IDT7MB4009 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V
I_{CC1}	Operating Current	f = 0, $\overline{CS} \le V_{IL}$ V_{CC} = Max., Outputs Open	—	620	mA
I_{CC2}	Dynamic Operating Current	f = f_{MAX}, $\overline{CS} \le V_{IL}$, V_{CC} = Max., Outputs Open	—	760	mA
I_{SB}	Standby Supply Current	f = f_{MAX}, $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open	—	440	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \ge V_{IH}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $\le$ 0.2V	—	120	mA

2707 tbl 05

8

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Loads	See Figures 1 and 2

2707 tbl 07

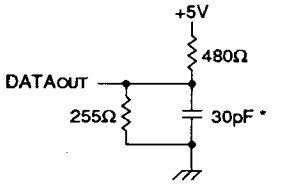
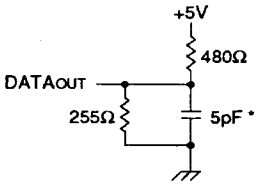


Figure 1. Output Load



2707 drw 03

Figure 2. Output Load (for tCLZ, tOLZ, tCHZ, tOHZ, tOW and tWHZ)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

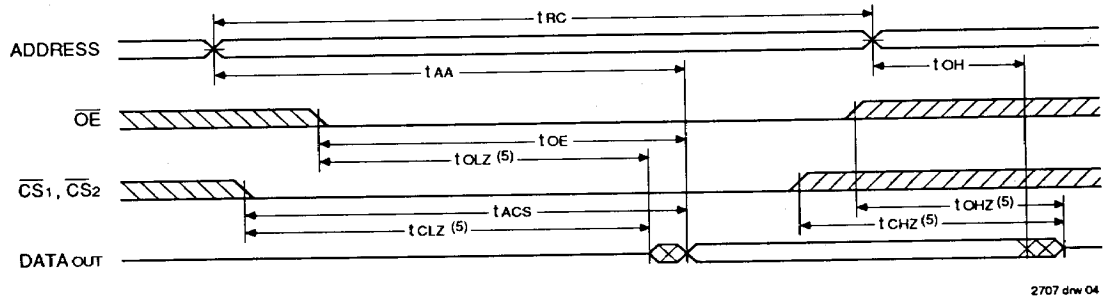
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB4009S15 Min.	7MB4009S15 Max.	7MB4009S20 Min.	7MB4009S20 Max.	7MB4009S25 Min.	7MB4009S25 Max.	Unit
Read Cycle								
tRC	Read Cycle Time	15	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	ns
tCLZ (1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	12	—	15	—	15	ns
tOLZ (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
tCHZ (1)	Chip Select to Output in High Z	—	8	—	10	—	12	ns
tOHZ (1)	Output Disable to Output in High Z	—	8	—	10	—	15	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU (1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD (1)	Chip Deselect to Power Down Time	—	15	—	20	—	25	ns
Write Cycle								
tWC	Write Cycle Time	13	—	18	—	20	—	ns
tCW	Chip Select to End of Write	13	—	18	—	20	—	ns
tAW	Address Valid to End of Write	13	—	18	—	21	—	ns
tAS	Address Set Up Time	0	—	0	—	1	—	ns
tWP	Write Pulse Width	12	—	17	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ (1)	Write Enable to Output in High Z	—	6	—	7	—	8	ns
tDW	Data to Write Time Overlap	8	—	10	—	13	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW (1)	Output Active from End of Write	5	—	5	—	5	—	ns

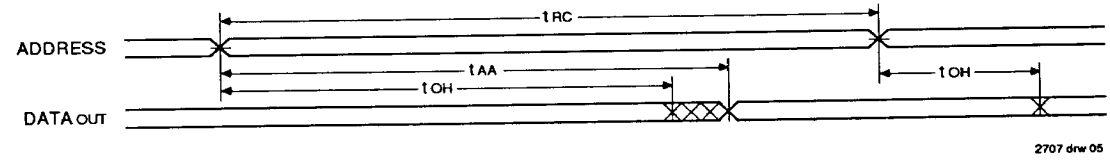
2707 tbl 06

NOTE:
1. This parameter is guaranteed by design, but not tested.

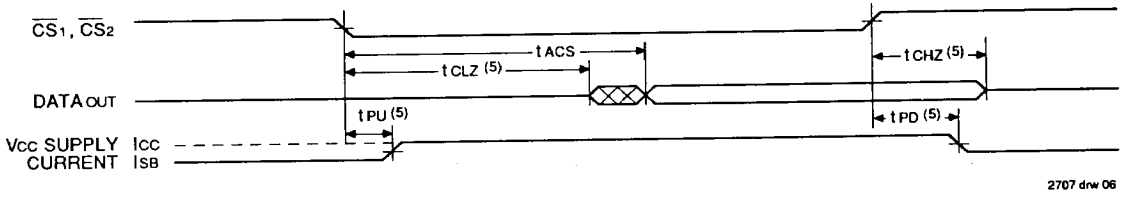
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



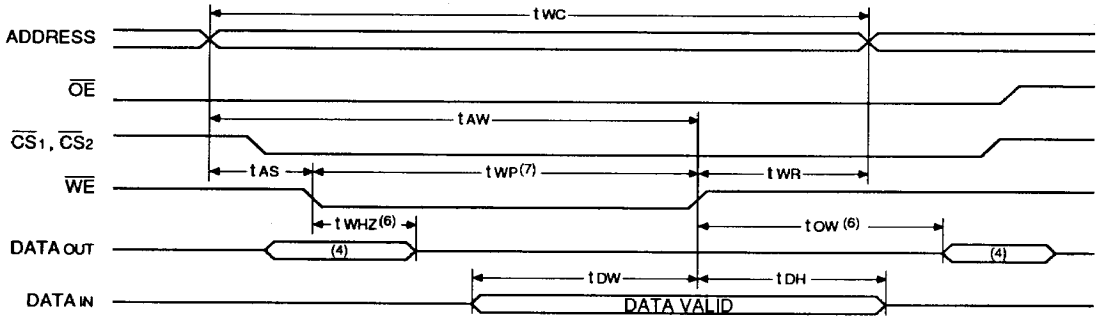
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, $\overline{CS_2}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS_1}$ and/or $\overline{CS_2}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

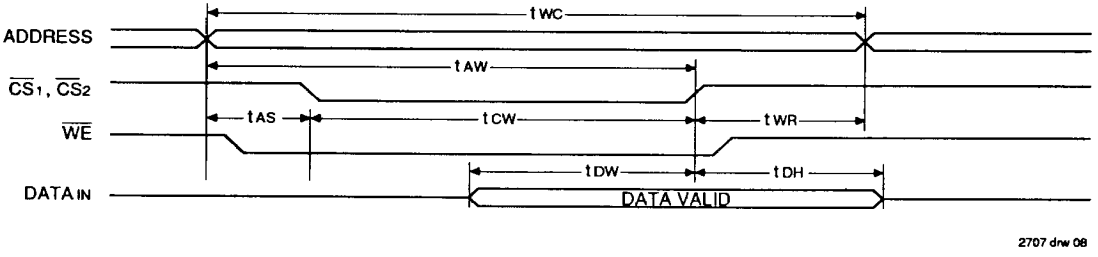
8

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2707 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5, 8)



2707 drw 08

NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, a low $\overline{CS_2}$ and a low $\overline{WE}$.
3. t_{WP} is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a WE controlled write cycle, the write pulse width must be the greater of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE}$ = V_{IL}.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(1)}$	Input Capacitance (Address)	V_{IN} = 0V	40	pF
$C_{IN(1)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

2707 tbl 08

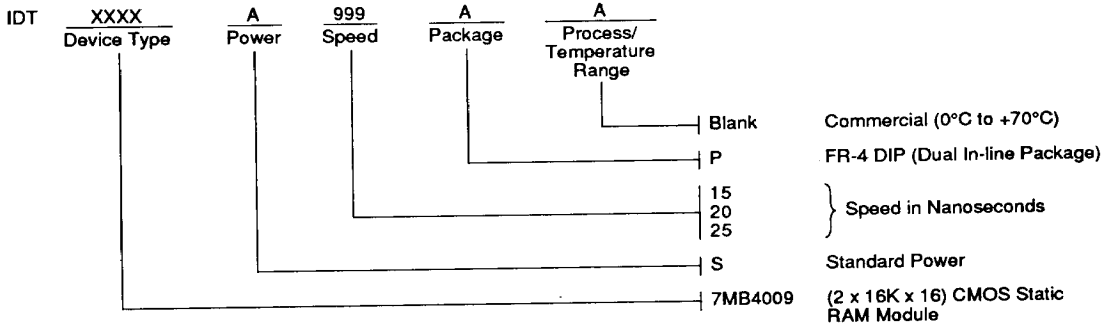
NOTE:
1. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE1}$	$\overline{OE2}$	$\overline{WEB1}$	$\overline{WEB2}$	Output	Power
Standby	H	H	X	X	X	X	High Z	Standby
Read	L	H	L	X	H	H	D_{OUT} BANK (1)	Active
Read	L	H	H	X	H	H	High Z	Active
Read	H	L	X	L	H	H	D_{OUT} BANK (2)	Active
Read	H	L	X	H	H	H	High Z	Active
Write	L	H	X	X	L	H	D_{IN} BANK (1) D (0-7)	Active
Write	L	H	X	X	H	L	D_{IN} BANK (1) D (8-15)	Active
Write	H	L	X	X	L	H	D_{IN} BANK (2) D (0-7)	Active
Write	H	L	X	X	H	L	D_{IN} BANK (2) D (8-15)	Active
Write	L	H	X	X	L	L	D_{IN} BANK (1) D (0-15)	Active
Write	H	L	X	X	L	L	D_{IN} BANK (2) D (0-15)	Active

2707 tbl 09

ORDERING INFORMATION



2707 drw 09

8