# Ultra Low Power 1-Bit 32 kHz RTC

## Features

- Supply current typically 800 nA at 3 V
- 50 ns access time with 50 pF load capacitance
- Fully operational from 2.0 V to 5.5 V
- No busy states or danger of a clock update while accessing
- Serial communication on one line of a standard parallel data bus or over a conventional 3 wire serial interface
- Interface compatible with both Intel and Motorola
- Seconds, minutes, hours, day of month, month, year, week day and week number in BCD format
- Leap year and week number correction
- Time set lock mode to prevent unauthorized setting of the current time or date
- Oscillator stability 0.3 ppm / volt
- No external capacitor needed
- Frequency measurement and test modes
- Temperature range - 40 to +85 °C
- Packages DIP8 and SO8

## Description

The V3021 is a low power CMOS real time clock. Data is transmitted serially as 4 address bits and 8 data bits, over one line of a standard parallel data bus. The device is accessed by chip select ($\overline{CS}$) with read and write control timing provided by either $\overline{RD}$ and $\overline{WR}$ pulse (Intel CPU) or $\overline{DS}$ with advanced R/$\overline{W}$ (Motorola CPU). Data can also be transmitted over a conventional 3 wire serial interface having CLK, data I/O and strobe. The V3021 has no busy states and there is no danger of a clock update while accessing. Supply current is typically 800 nA at $V_{DD}$ = 3.0 V. Battery operation is supported by complete functionality down to 2.0 V. The oscillator stability is typically 0.3 ppm/V.

## Applications

- Utility meters
- Battery operated and portable equipment
- Consumer electronics
- White/brown goods
- Pay phones
- Cash registers
- Personal computers
- Programmable controller systems
- Data loggers
- Automotive electronics

## Typical Operating Configuration

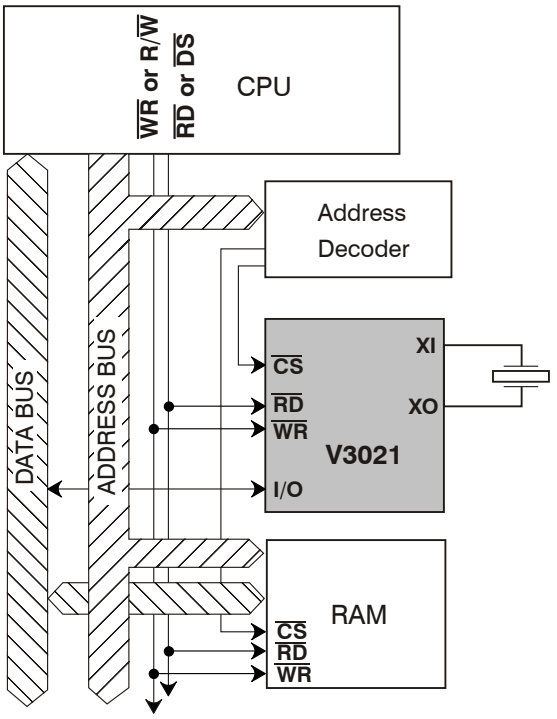



Fig. 1

## Pin Assignment

DIP8 / SO8

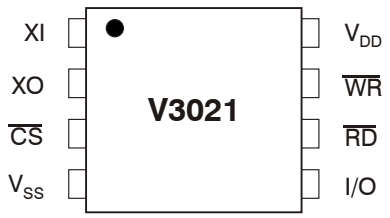



Fig. 2

## Absolute Maximum Ratings

| Parameter | Symbol | Conditions |
|---|---|---|
| Maximum voltage at $V_{DD}$ | $V_{DDmax}$ | $V_{SS}$ + 7.0 V |
| Minimum voltage at $V_{DD}$ | $V_{DDmin}$ | $V_{SS}$ - 0.3 V |
| Maximum voltage at any signal pin | $V_{max}$ | $V_{DD}$ + 0.3 V |
| Minimum voltage at any signal pin | $V_{min}$ | $V_{SS}$ - 0.3 V |
| Maximum storage temperature | $T_{STOmax}$ | +150 °C |
| Minimum storage temperature | $T_{STOmin}$ | -65 °C |
| Electrostatic discharge maximum to MIL-STD-883C method 3015 | $V_{Smax}$ | 1000 V |
| Maximum soldering conditions | $T_{Smax}$ | 250 °C x 10 s |

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

## Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, it is advised that normal precautions be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

## Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Operating temperature | $T_A$ | -40 | | +85 | °C |
| Logic supply voltage | $V_{DD}$ | 2.0 | 5.0 | 5.5 | V |
| Supply voltage dv/dt (power-up & power-down) | | | | 6 | V/ms |
| Decoupling capacitor | | | 100 | | nF |
| **Crystal Characteristics** | | | | | |
| Frequency[1)] | f | | 32.768 | | kHz |
| Load capacitance | $C_L$ | 7 | 8.2 | 30 | pF |
| Series resistance | $R_S$ | | 35 | 50 | kW |

[1)] See Fig. 3

Table 2

## Electrical Characteristics

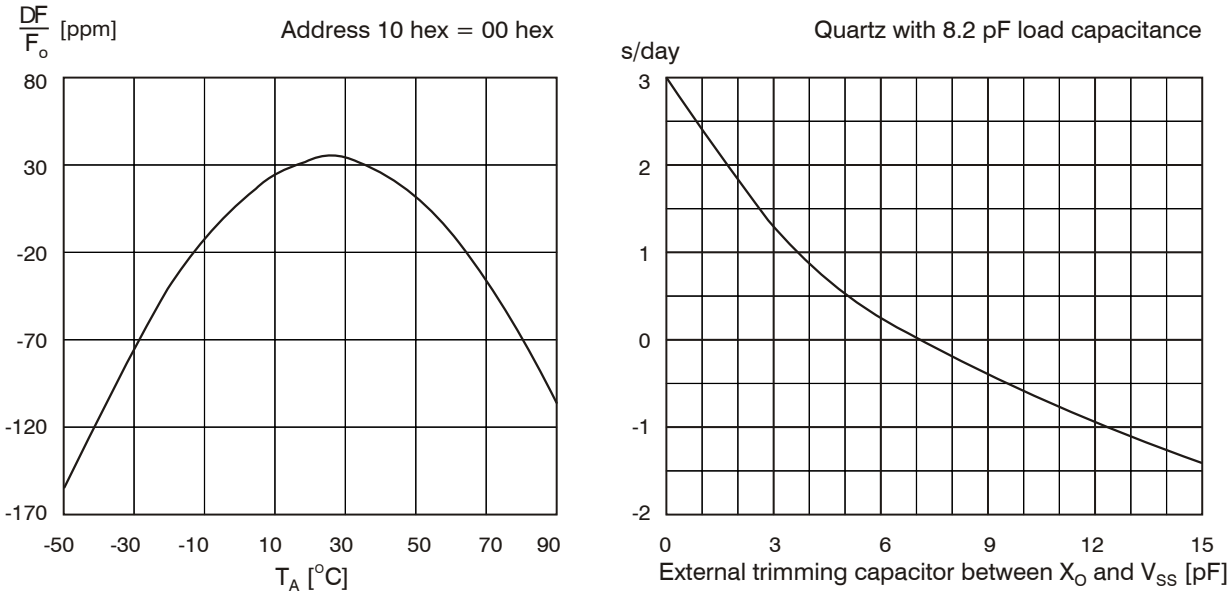
$V_{DD}$ = 5.0V ± 10%, $V_{SS}$ = 0 V and $T_A$ = - 40 to 85 °C, unless otherwise specified

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Total static supply | $I_{SS}$ | all outputs open, all inputs at $V_{DD}$ $V_{DD}$ = 3.0 V, address 0 = 0 | | 0.8 | 1.8 | mA |
| Total static supply | $I_{SS}$ | all outputs open, all inputs at $V_{DD}$, $V_{DD}$ = 5 V, address 0 = 0 | | 1.3 | 10 | mA |
| | | $T_A$ = +25°C | | | 3 | mA |
| Dynamic current | $I_{SS}$ | I/O to $V_{SS}$ through 1 MW $\overline{RD}$ = $V_{SS}$, $\overline{WR}$ = $V_{DD}$, $\overline{CS}$ = 4 MHz address 0 = 0, read all 0 | | | 300 | mA |
| **Input / Output** | | | | | | |
| Input logic low | $V_{IL}$ | | | | 1.0 | V |
| Input logic high | $V_{IH}$ | | 3.5 | | | V |
| Output logic low | $V_{OL}$ | $I_{OL}$ = 4 mA | | | 0.4 | V |
| Output logic high | $V_{OH}$ | $I_{OH}$ = 4 mA | 2.4 | | | V |
| Input leakage | $I_{IN}$ | 0.0 < $V_{IN}$ < 5.0 V | | 0.1 | 1 | mA |
| Output tri-state leakage on I/O pin | $I_{TS}$ | $\overline{CS}$ high, and address 0, bit 0, low | | 0.1 | 1 | mA |
| **Oscillator** | | | | | | |
| Starting voltage | $V_{STA}$ | | 1.8 | | | V |
| Input capacitance on XI | $C_{IN}$ | $T_A$ = +25 °C | | 13 | | pF |
| Output capacitance on XO | $C_{OUT}$ | $T_A$ = +25 °C | | 9 | | pF |
| Start-up time | $T_{STA}$ | | | 1 | | s |
| Frequency stability | Df/f | 2.0 £ $V_{DD}$ £ 5.5V , $T_A$ = +25 °C | | 0.3 | 0.5 | ppm/V |
| **Frequency Measurement Mode** | | | | | | |
| Current source on I/O pin pulsed on/off @ 256 Hz | $I_{ONF}$ | $\overline{CS}$ high, addr.0, bit 0, high $V_{I/O}$ = 1 V | 10 | 25 | 60 | mA |

Table 3

The V3021 will run slightly too fast, in order to allow the user to adjust the frequency, depending on the mean operating temperature. This is made since the crystal adjustment can only work by lowering the frequency with an added capacitor between XO and $V_{SS}$. The printed circuit capacitance has also to be taken in consideration. The V3021 in DIL8 package, running with an 8.2 pF crystal at room temperature, will be adjusted to better than ± 1 s/day with a 6.8 pF capacitor.

### Typical Frequency on I/O Pin

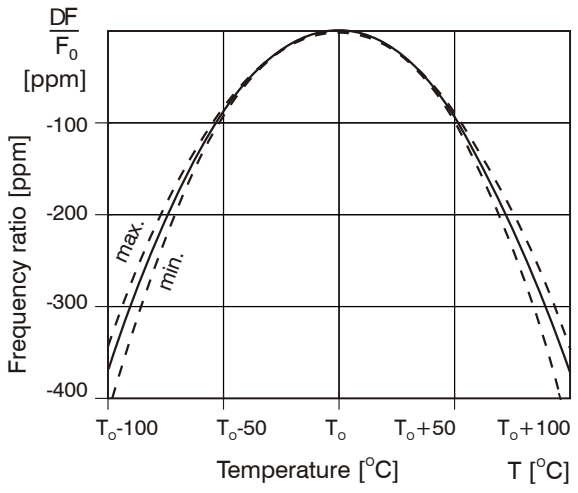



Typical drift for ideal 32'768 Hz quartz

**Note :** The trimming capacitor value must not exceed 15 pF. Greater values may disturb the oscillator function.

Fig. 3

### Quartz Characteristics




$$\frac{DF}{F_o} = -0.038 \frac{ppm}{^oC^2} (T - T_o)^2 \pm 10\%$$

$DF/F_o$ = the ratio of the change in frequency to the nominal value expressed in ppm (It can be thought of as the frequency deviation at any temperature.)

$T$ = the temperature of interest in °C

$T_o$ = the turnover temperature (25 ± 5 °C)

To determine the clock error (accuracy) at a given temperature, add the frequency tolerance at 25°C to the value obtained from the formula above.

Fig. 4

## Timing Characteristics

$V_{SS}$ = 0 V, and $T_A$ = - 40 to +85 °C, unless otherwise specified

| Parameter | Symbol | Test Conditions | Min. | Max. | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ ³ 2 V | | $V_{DD}$ = 5.0V ± 10% | | | |
| Chip select duration | $t_{CS}$ | Write cycle | 200 | | 50 | | | ns |
| RAM access time[1] | $t_{ACC}$ | $C_{LOAD}$ = 50 pF | | 180 | | 50 | 60 | ns |
| Time between two transfers | $t_W$ | | 500 | | 100 | | | ns |
| Rise time[2] | $t_R$ | | 10 | 200 | 10 | | 200 | ns |
| Fall time[2] | $t_F$ | | 10 | 200 | 10 | | 200 | ns |
| Data valid to Hi-impedance[3] | $t_{DF}$ | | 10 | 100 | 15 | 30 | 40 | ns |
| Write data settle time[4] | $t_{DW}$ | | 60 | | 50 | | | ns |
| Data hold time[5] | $t_{DH}$ | | 80 | | 25 | | | ns |
| Advance write time | $t_{ADW}$ | | 25 | | 10 | | | ns |
| Write pulse time[6] | $t_{WC}$ | | 200 | | 50 | | | ns |

Table 4

[1] $t_{ACC}$ starts from $\overline{RD}$ or $\overline{CS}$, whichever activates last
Typically, $t_{ACC}$ = 5 + 0.9 $C_{EXT}$ in ns; where $C_{EXT}$ (external parasitic capacitance) is in pF

[2] $\overline{CS}$, $\overline{RD}$, $\overline{DS}$, $\overline{WR}$ and R/$\overline{W}$ rise and fall times are specified by $t_R$ and $t_F$

[3] $t_{DF}$ starts from $\overline{RD}$ or $\overline{CS}$, whichever deactivates first

[4] $t_{DW}$ ends at $\overline{WR}$ or $\overline{CS}$, whichever deactivates first

[5] $t_{DH}$ starts from $\overline{WR}$ or $\overline{CS}$, whichever deactivates first

[6] $t_{WC}$ starts from $\overline{WR}$ or $\overline{CS}$, whichever activates last and ends at $\overline{WR}$ or $\overline{CS}$, whichever deactivates first

## Timing Waveforms

### Read Timing for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola ($\overline{DS}$ (or $\overline{RD}$ pin tied to $\overline{CS}$) and R/$\overline{W}$)

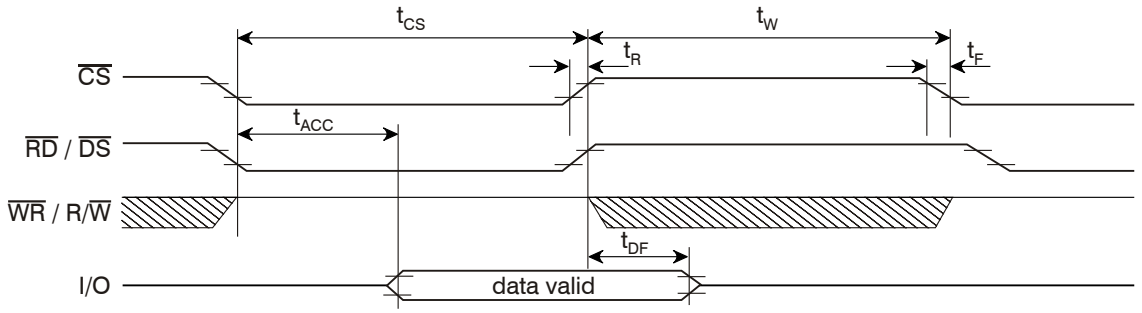



Fig. 5a

### Write Timing for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)

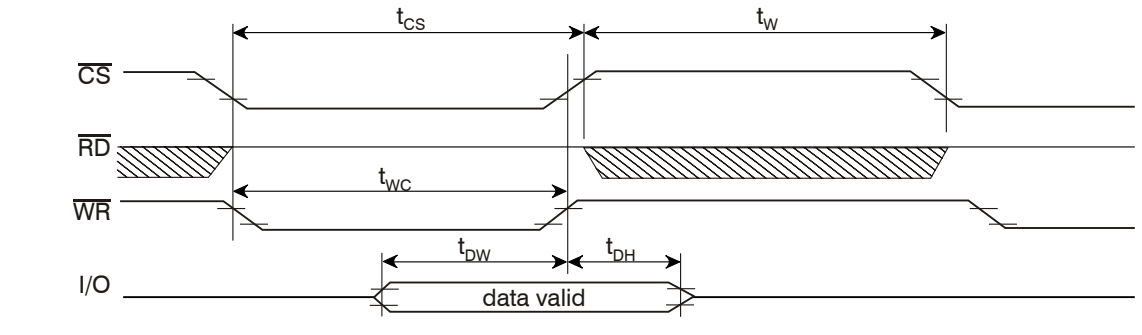



Fig. 5b

**Write Timing for Motorola ($\overline{DS}$ (or $\overline{RD}$ pin tied to $\overline{CS}$) and R/$\overline{W}$)**

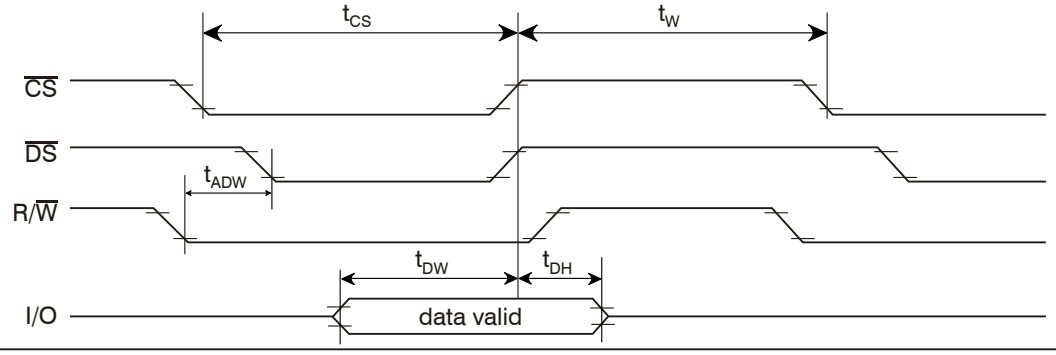



Fig. 5c

## Communication Cycles

**Read Data Cycle for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)**

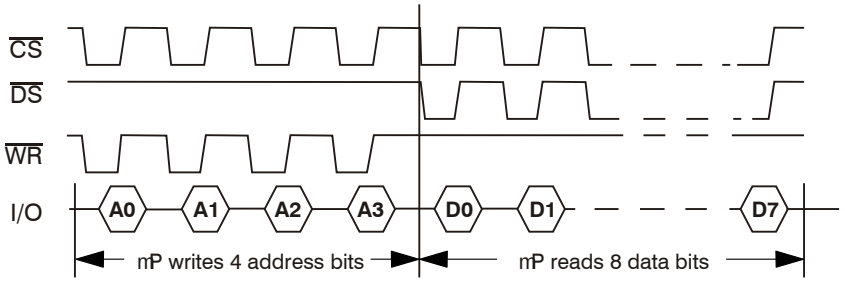



Fig. 6a

**Read Data Cycle for Motorola ($\overline{DS}$ (or $\overline{RD}$ Pin Tied to $\overline{CS}$) and R/$\overline{W}$)**

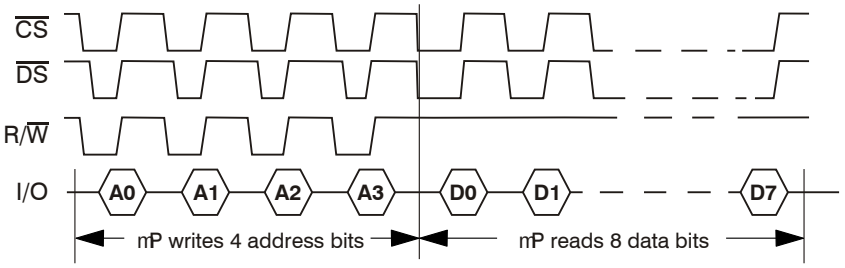



Fig. 6b

**Write Data Cycle for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)**

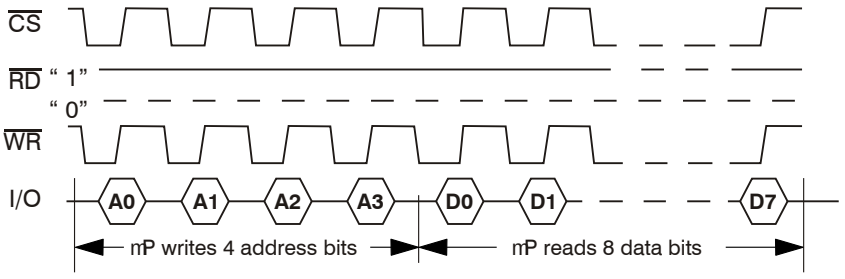



Fig. 6c

**Write Data Cycle for Motorola ($\overline{DS}$ (or $\overline{RD}$ Pin Tied to $\overline{CS}$) and R/$\overline{W}$)**

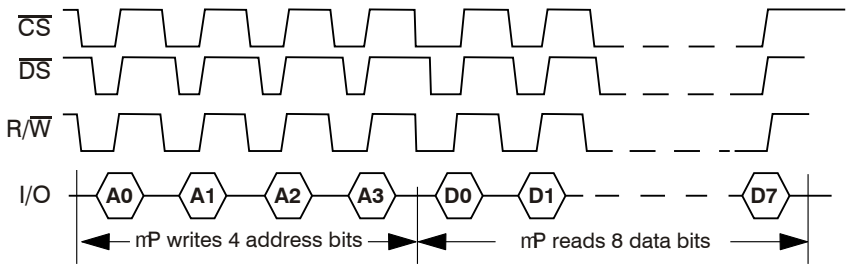



Fig. 6d

**Address Command Cycle for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse)**

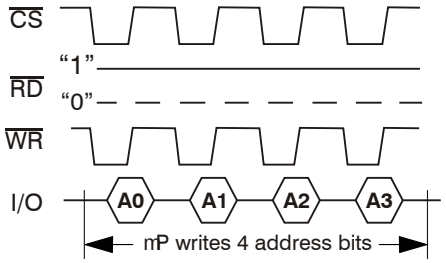



Fig. 6e

**Address Command Cycle for Motorola ($\overline{DS}$ (or $\overline{RD}$ Pin Tied to $\overline{CS}$) and R/$\overline{W}$)**

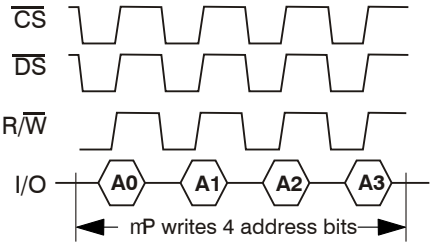



Fig. 6f

## Block Diagram

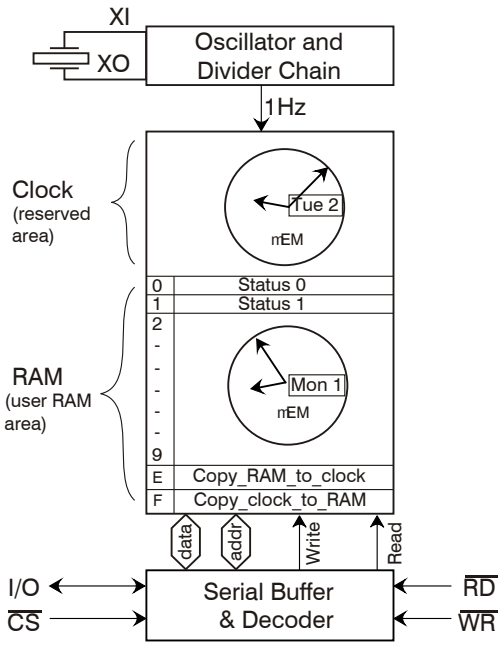



Fig. 7

## Pin Description

| Pin | Name | Function |
|---|---|---|
| 1 | XI | 32 kHz crystal input |
| 2 | XO | 32 kHz crystal output |
| 3 | $\overline{CS}$ | Chip select input |
| 4 | $V_{SS}$ | Ground supply |
| 5 | I/O | Data input and output |
| 6 | $\overline{RD}$ | Intel $\overline{RD}$, Motorola $\overline{DS}$ (or tie to $\overline{CS}$) |
| 7 | $\overline{WR}$ | Intel $\overline{WR}$, Motorola R/$\overline{W}$ |
| 8 | $V_{DD}$ | Positive supply |

Table 5

## Functional Description

### Serial Communication

The V3021 resides on the parallel data and address buses as a standard peripheral (see Fig. 13 and 14). Address decoding provides an active low chip select ($\overline{CS}$) to the device. For Intel compatible bus timing the control signals $\overline{RD}$ and $\overline{WR}$ pulse and $\overline{CS}$ are used for a single bit read or write (see Fig. 5a and 5b). Two options exist for Motorola compatible bus timing. The first is to use the control signals $\overline{DS}$ with R/$\overline{W}$ and $\overline{CS}$, the second is to tie the $\overline{RD}$ input to $\overline{CS}$ and use the control signals R/$\overline{W}$ and $\overline{CS}$ (see Fig. 5a and 5c). Data transfer is accomplished through a single input / output line (I/O). Any data bus line can be chosen. A conventional 3 wire serial interface can also be used to communicate with the V3021 (see Fig. 15).

### Communication Cycles

The V3021 has 3 serial communication cycles. These are :

1) Read data cycle
2) Write data cycle
3) Address command cycle

A communication cycle always begins by writing the 4 address bits, A0 to A3. A microprocessor read from the V3021 cannot begin a communication cycle. Read and write data cycles are similar and consist of 4 address bits and 8 data bits. The 4 address bits, A0 to A3, define the RAM location and the 8 data bits, D0 and D7, provide the relevant information. An address command cycle consists of only 4 address bits.

### Read Data Cycle

A read data cycle commences by writing the 4 RAM address bits (A3, A2, A1 and A0) to the V3021. The LSB, A0, is transmitted first (see Fig. 6a and 6b). Eight microprocessor reads from the V3021 will read the RAM data at this address, beginning with the LSB, D0. The read data cycle finishes on reading the 8th data bit, D7.

### Write Data Cycle

A write data cycle commences by writing the 4 RAM address bits (A3, A2, A1 and A0) to the V3021. The LSB, A0, is transmitted first (see Fig. 6c and 6d). Eight microprocessor writes to the V3021 will write the new RAM data. The LSB, D0, is loaded first. The write data cycle finishes on writing the 8th data bit, D7.

### Address Command Cycle

An address command cycle consists of just 4 address bits. The LSB, A0, is transmitted first (see Fig. 6e and 6f). On writing the fourth address bit, A3, the address will be decoded. If the address bits are recognized as one of the command codes E hex or F hex (see Table 6), then the communication cycle is terminated and the corresponding command is executed. Subsequent microprocessor writes to the V3021 begin another communication cycle with the first bit being interpreted as the address LSB, A0.

### Clock Configuration

The V3021 has a reserved clock area and a user RAM area (see Fig. 7). The clock is not directly accessible, it is used for internal time keeping and contains the current time and date. The contents of the RAM is shown in Table 6, it contains a data space and an address command space. The data space is directly accessible. Addresses 0 and 1 contain status information ( see Tables 7a and 7b), addresses 2 to 5, time data, and addresses 6 and 9, date data. The address command space is used to issue commands to the V3021.

RAM Map

| Address Dec | Address Hex | Parameter | BCD range |
|---|---|---|---|
| **Data Space** | | | |
| 0 | 0 | Status 0 | |
| 1 | 1 | Status 1 | |
| 2 | 2 | Seconds | 00-59 |
| 3 | 3 | Minutes | 00-59 |
| 4 | 4 | Hours | 00-23 |
| 5 | 5 | Day of month | 01-31 |
| 6 | 6 | Month | 01-12 |
| 7 | 7 | Year | 00-99 |
| 8 | 8 | Week day | 01-07 |
| 9 | 9 | Week number | 00-52 |
| **Address Command Space** | | | |
| 14 | E | Copy_RAM_to_clock | |
| 15 | F | Copy_clock_to_RAM | |

Table 6

### Commands

Two commands are available (see Table 6). The Copy_RAM_to_clock command is used to set the current time and date in the clock and the Copy_clock_to_RAM command to copy the current time and date from the clock to the RAM. The Copy_RAM_to_clock command, address data E hex, causes the clock time and date to be overwritten by the time and date stored in the RAM at addresses 2 to 9. Address 1 is also cleared (see section “Time and Date Status Bits”). Prior to using this command, the desired time and date must be loaded into the RAM using write data cycles and the time set lock bit, address 0, bit 7, must be clear (see section “ Time Set Lock”).

## Status Information

The RAM addresses 0 and 1 contain status and control data for the V3021. The function of each bit (0 and 7) within address locations 0 and 1 is shown in Tables 7a and 7b respectively.

Status Word

**Status 0 - address 0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

0 - inactive
1 - active

Read / Write bits

- Frequency Measurement Mode
- Reserved
- Test Mode 0
- Test Mode 1
- Time Set Lock
- Reserved
- Reserved
- Reserved

Table 7a

**Status 1 - address 1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

0 - No change from last Copy_clock_to_RAM
1 - Change from last Copy_clock_to_RAM

Read ONLY bits

- Seconds
- Minutes
- Hours
- Day of month
- Month
- Year
- Week day
- Week number

Table 7b

## Reset and Initialization

Upon microprocessor recovery from a system reset, the V3021 must be initialized by software in order to guarantee that it is expecting a communication cycle (i.e the internal serial buffer is waiting for the address bit A0). Software can initialize the V3021 to expect a communication cycle by executing 8 microprocessor reads (see Fig. 8).

Initializing Access to the V3021

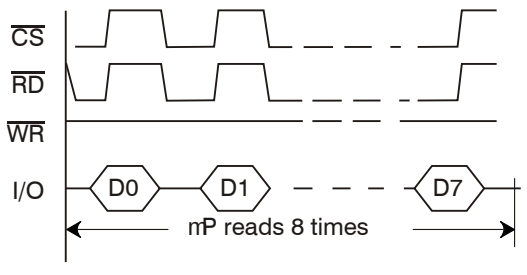



Fig. 8

On first startup or whenever power has failed ($V_{DD}$ < 2.0 V) the status register 0 and the clock must be initialized by software. Having initialized the interface to expect the address bit A0, write 0 to status register 0, then set the clock (see section “Clock and Calendar”).

## Time and Date Status Bits

There are time and date status bits at address 1 in the RAM. Upon executing a Copy_clock_to_RAM command, the time and date status bits in the RAM show which time and date parameters changed since the last time this command was used. A logic 1 in the seconds status bit (address 1, bit 0) in the RAM indicates that the seconds location in the RAM (address 2) changed since the last Copy_clock_to_RAM command and thus needs to be read. The seconds location must change before any other time or date location can change. If the seconds status bit is clear, then no time or date location changed since the last Copy_clock_to_RAM command and so the RAM need not to be read by software.

Table 7b shows the seconds, minutes, hours, day of the month, month, year, week day, and week number status bit locations. They are set or cleared similar to the seconds location. It should be noted that if the minutes status bit is clear, then the seconds bit may be set, but all other status bits are clear. Similarly with hours, the bits representing the units less than hours may have been set, but the bits for the higher units will be clear. This rule holds true for the week day or day of month locations also.

The time and date status bits can be used to drive software routines which need to be executed every

- second,
- minute,
- hour,
- day of month / week day,
- month,
- year,

or - week.

In this application it is necessary to poll the V3021 at least once every time interval used as it does not generate an interrupt. Upon executing a Copy_RAM_to_clock command, the time and date status bits in the RAM are cleared.

## Time Set Lock

The time set lock control bit is located at address 0, bit 4 (see Table 7a). When set by software, the bit disables the Copy_RAM_to_clock command (see section “Commands”.) A set bit prevents unauthorized overwriting of the current time and date in the clock. Clearing the time set lock bit by software will re-enable the Copy_RAM_to_clock command. On first startup or whenever power has failed ($V_{DD}$ < 2.0 V), the time set lock bit must be setup by software.

Reading the Current Time and Date

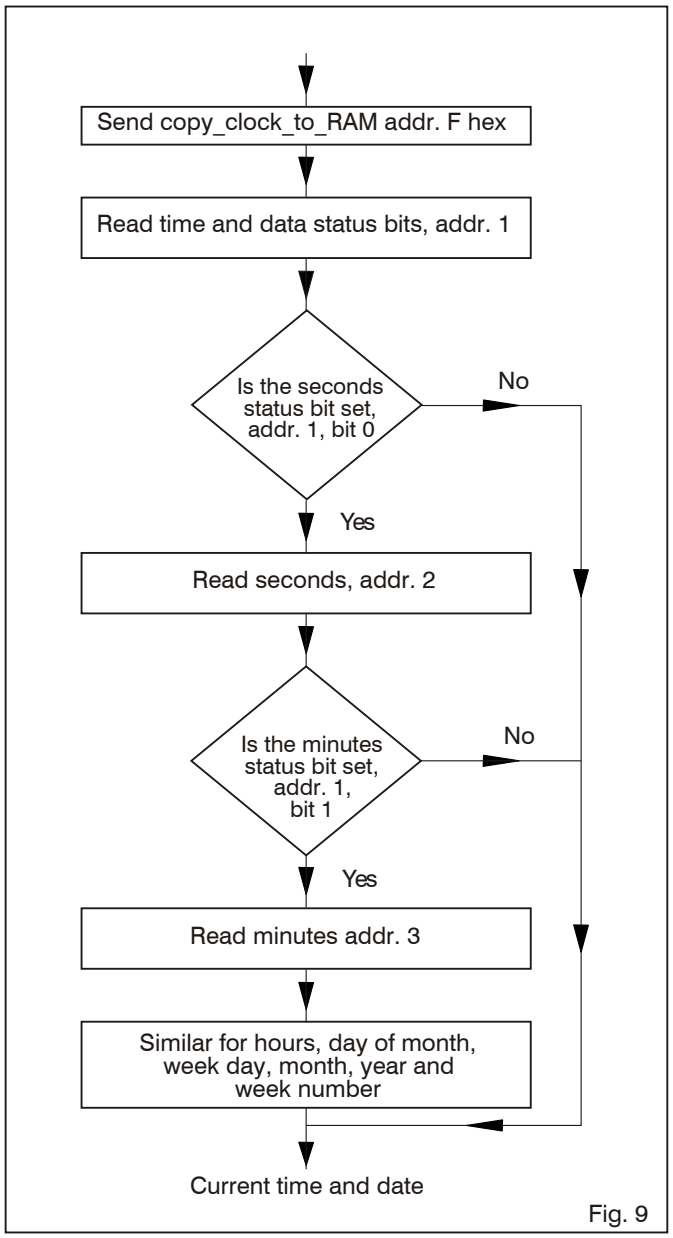



Fig. 9

## Clock and Calendar

The time and date addresses in the RAM (see Table 6) provide access to the seconds, minutes, hours, day of month, month, year, week day, and week number. These parameters have the ranges indicated on Table 6 and are in BCD format. If a parameter is found to be out of range, it will be cleared on its being next incremented. The V3021 incorporates leap year correction and week number calculation. The week number changes only at the incrementation of the day number from 7 to 1. If week 52 day 7 falls on the 25th, 26th or 27th of December, then the week number will change to 0 otherwise it will be week 1. Week days are numbered from 1 to 7 with Monday as 1.

Reading of the current time and date must be preceded by a Copy_clock_to_RAM command. The time and date status bits will indicate which time and date addresses changed since the last time the command was used (see Fig. 9). The time and date from the last Copy_clock_to_RAM command is held unchanged in the RAM, except when power ($V_{DD}$) has failed totally. To change the current time and date in the clock, the desired time and date must first be written to the RAM, the time set lock bit cleared, and then a Copy_RAM_to_clock command sent (see Fig. 10). The time set lock bit can be used to prevent unauthorized setting of the clock.

Setting the Current Time and Date

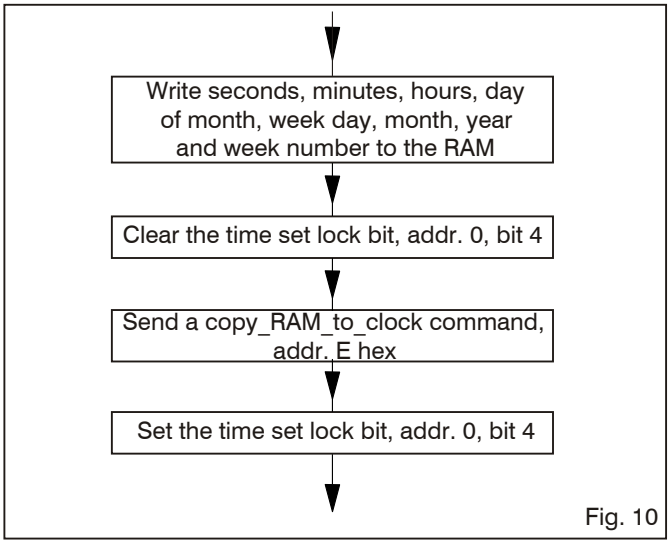



Fig. 10

## Frequency Measurement

Setting bit 0 at address 0 will put a pulsed current source (25 mA) onto the I/O pin, when the device is not chip selected (i.e. CS input high). The current source will be pulsed on/off at 256 Hz. The period for ± 0 ppm time keeping is 3.90625 ms. To measure the frequency signal on pin I/O, the data bus must be high impedance. The best way to ensure this is to hold the microprocessor and peripherals in reset mode while measuring the frequency. The clarity of the signal measured at pin I/O will depend on both the probe input impedance (typically 1 MW) and the magnitude of the leakage current from other devices driving the line connected to pin I/O. If the signal measured is unclear, put a 200 kW resistor from pin I/O to $V_{SS}$. It should be noted that the magnitude of the current source (25 mA) is not sufficient to drive the data bus line in case of any other device driving the line, but it is sufficient to take the line to a high logic level when the data bus is in high impedance.

Use a crystal of nominal $C_L$ = 8.2 pF as specified in the section "Operating Conditions". The MX series from Microcrystal is recommended. The accuracy of the time keeping is dependent upon the frequency tolerance and the load capacitance of the crystal. 11.57 ppm correspond to one second a day.

### Test

From the various test features added to the V3021 some may be activated by the user. Table 7a shows the test mode bits. Table 8 shows the 3 available test modes and how they can be activated. Test mode 0 is activated by setting bit 2, address 0, and causes all time keeping to be accelerated by 32. Test mode 1 is activated by setting bit 3, address 0, and causes all the time and date locations, address 2 to address 9, to be incremented in parallel at 1 Hz with no carry over (independent of each other). The third test mode combines the previous two resulting in parallel incrementing at 32 Hz.

### Test Modes

| Addr. 0 bit 3 | Addr. 0 bit 2 | Function |
|---|---|---|
| 0 | 0 | Normal operation |
| 0 | 1 | All time keeping accelerated by 32 |
| 1 | 0 | Parallel increment of all time data at 1 Hz with no carry over |
| 1 | 1 | Parallel increment of all time data at 32 Hz with no carry over |

Table 8

An external signal generator can be used to drive the divider chain of the V3021. Fig. 11a and 11b show how to connect the signal generator. The speed can be increased by increasing the signal generator frequency to a maximum of 128 kHz. An external signal generator and test modes can be combined.

To leave test both test bits (address 0, bits 2 and 3) must be cleared by software. Test corrupts the current time and date and so the time and date should be reloaded after a test session.

Signal Generator Connection

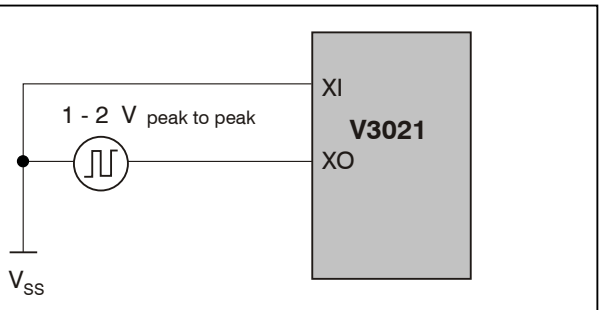



Fig. 11a

**Note :** The peak value of the signal provided by the signal generator should not exceed 2 V on XO.

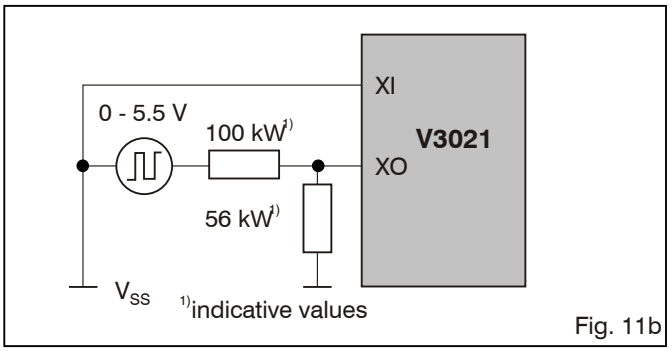



Fig. 11b

**Note :** The peak value of the signal provided by the signal generator should not exceed 2 V on XO.

### Crystal Layout

In order to ensure proper oscillator operation we recommend the following standard practices:
- Keep traces as short as possible.
- Use a guard ring around the crystal.

Fig. 12 shows the recommended layout.

Oscillator Layout

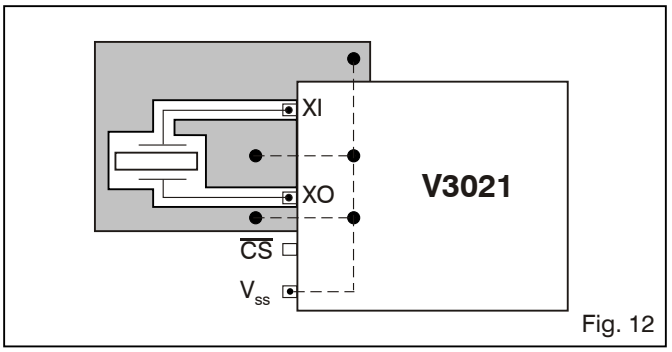



Fig. 12

### Access Considerations

The section “Communication Cycles” describes the serial data sequences necessary to complete a communication cycle. In common with all serial peripherals, the serial data sequences are not re-entrant, thus a high priority interrupt, or another software task, should not attempt to access the V3021 if it is already in the middle of a cycle. A semaphore (software flag) on access would allow the V3021 to be shared with other software tasks or interrupt routines. There is no time limit on the duration of a communication cycle and thus interrupt routines (which do not use the V3021) can be fully executed in mid cycle without any consequences for the V3021.

## Typical Applications

### V3021 Interfaced with Intel CPU ($\overline{RD}$/$\overline{WR}$ Pulse)

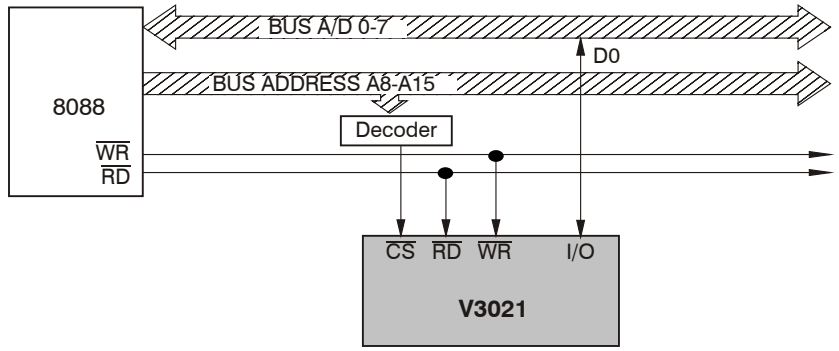



Fig. 13

### V3021 Interfaced with Motorola CPU (Advanced R/$\overline{W}$)

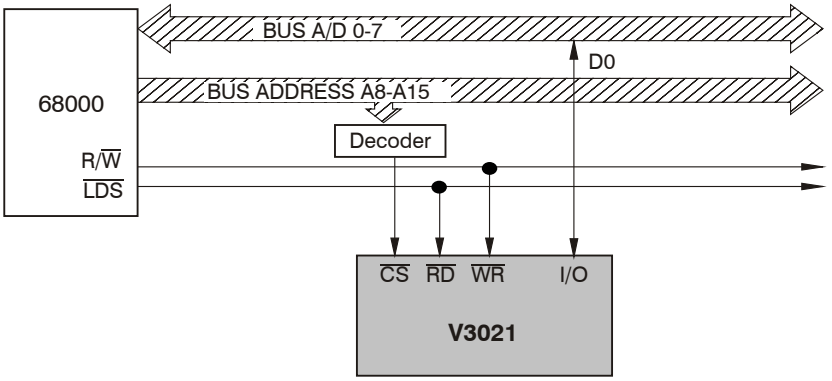
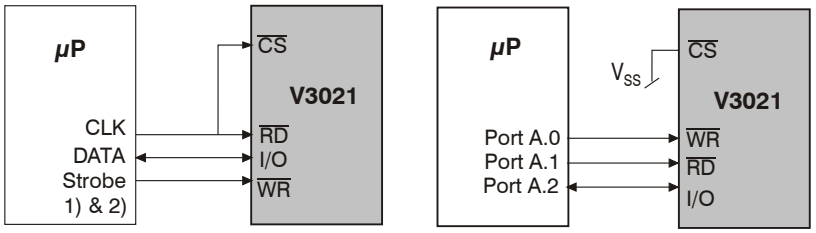



Fig. 14

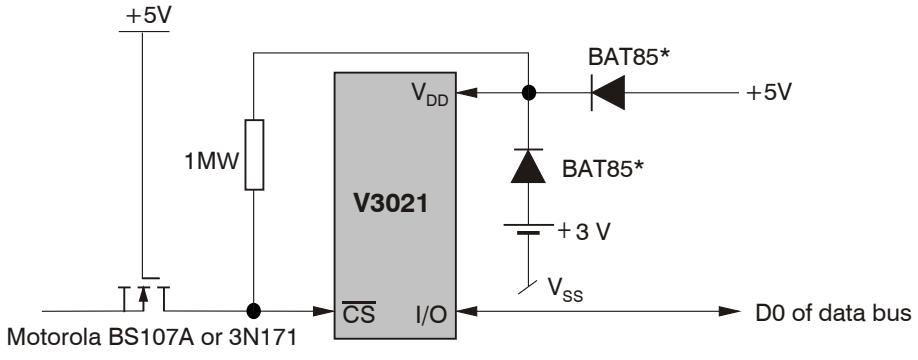
### 3 Wire Serial Interface




1) With strobe low bits are written to the V3021, and with strobe high bits are read from the V3021
2) For serial ports with byte transfer only, an address command cycle should be combined with every data cycle to give 8 address bits and 8 data bits. For example to read the current minutes, write address data F + 3 (1111 + 0011) and then read 8 data bits.

Fig. 15

### Battery Switch Over Circuit




* Use Schottky barrier diodes. The BAT85 has a typical $V_F$ of 250 mV at an $i_F$ of 1 mA.
The reverse current is typically 200 nA at a $V_R$ of 5 V. The reverse recovery time is 5 ns. For surface mount applications use the Philips BAT17 in SOT-23 or other.

Fig. 16

## Ordering Information

The V 3021 is available in the following package :

| | |
|---|---|
| DIP8 plastic package | V3021 8P |
| SO8 plastic package | V3021 8S |

When ordering, please specify the complete part number.