μPB10474
1,024 x 4-Bit
10K ECL RAM

Description

The μPB10474 is a very high-speed 10K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Three versions with access times of 8 ns, 10 ns and 15 ns maximum are available in hermetic, 400-mil, 24-pin cerdip packaging.

Features

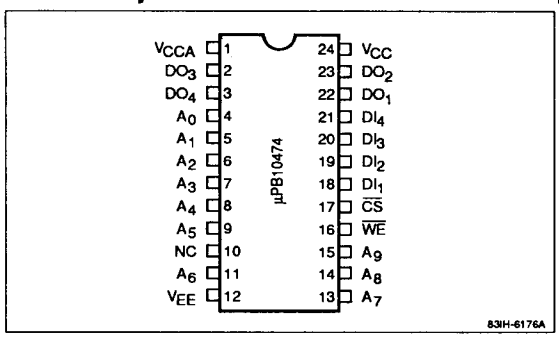
- 1,024-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10474D-8	8 ns	24-pin cerdip
D-10	10 ns	
D-15	15 ns	

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

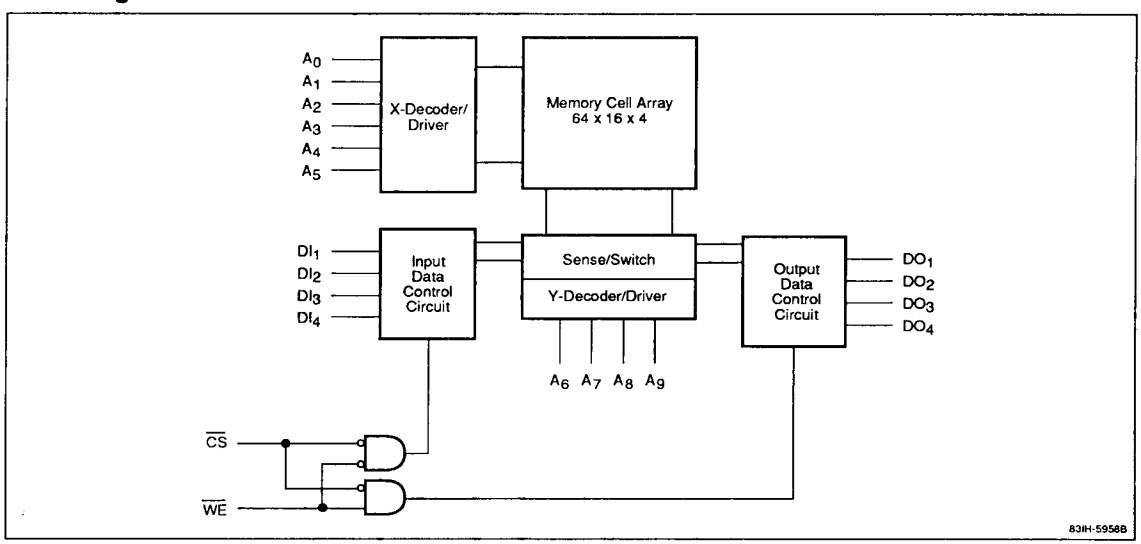
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V

Parameter	Symbol	μPB10474-8			μPB10474-10			μPB10474-15			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Read Operation												
Chip select access time	t_{ACS}			5			6			8	ns	
Chip select recovery time	t_{RCS}			5			6			8	ns	
Address access time	t_{AA}			8			10			15	ns	
Write Operation												
Write pulse width	t_W	6			10			15			ns	
Data setup time	t_{WSD}	1			2			2			ns	
Data hold time	t_{WHD}	1			2			2			ns	
Address setup time	t_{WSA}	1			3			3			ns	
Address hold time	t_{WHA}	1			2			2			ns	
Chip select setup time	t_{WSCS}	1			2			2			ns	
Chip select hold time	t_{WHCS}	1			2			2			ns	
Write disable time	t_{WS}			5			6			8	ns	
Write recovery time	t_{WR}			8			10			10	ns	
Output Rise and Fall Times												
Output rise time	t_R		2			2			2		ns	
Output fall time	t_F		2			2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

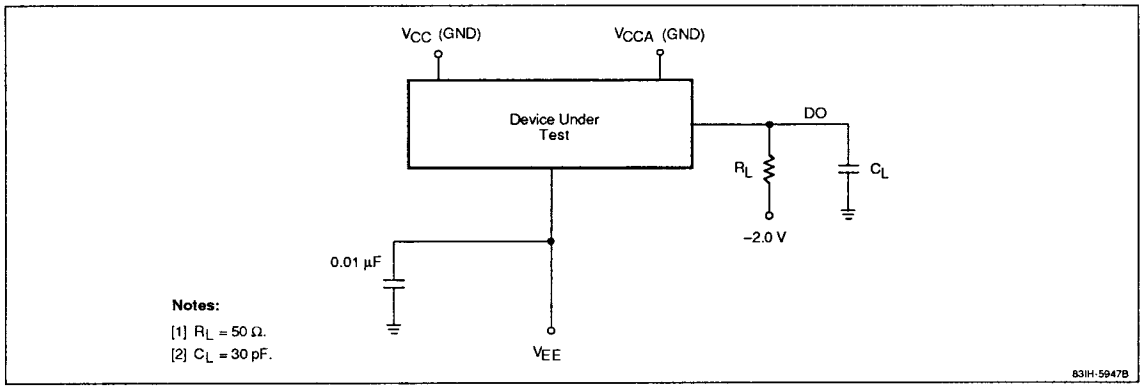
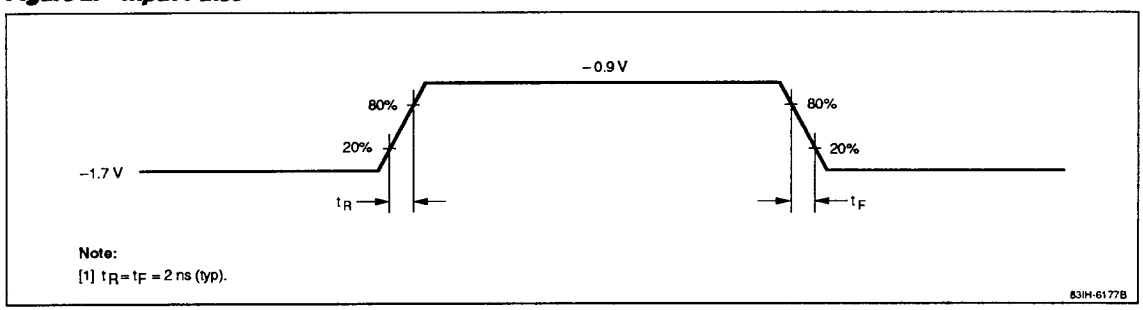
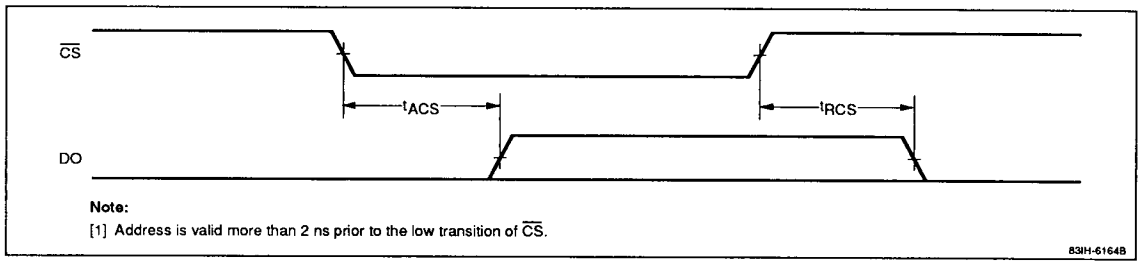


Figure 2. Input Pulse



Timing Waveforms

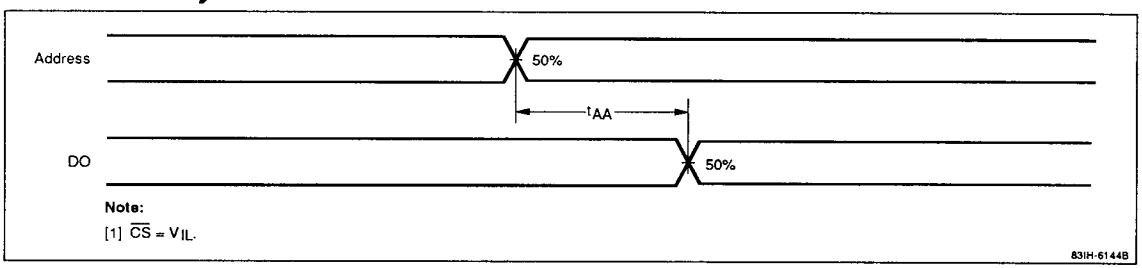
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

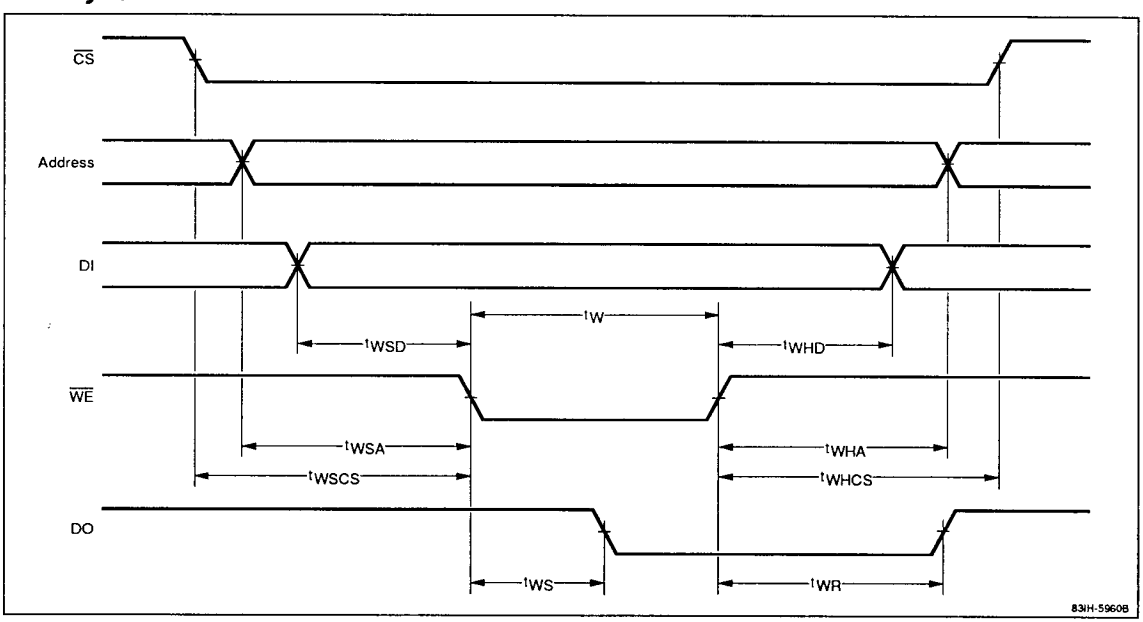
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5960B