Distributed System Interface (DSI) Sensor Interface

The 33793 is a slave Distributed System Interface (DSI) device that is optimized as a sensor interface. The device contains circuits to power sensors such as accelerometers and to digitize the analog level from the sensor. The device is controlled by commands over the DSI bus and returns measured data over the bus.

Features

- Conforms to DSI Specification Version 1
- 4-Channel, 8-Bit Analog-to-Digital Converter (ADC)
- 4 Pins Configurable as Analog or Logic Inputs or as Logic Outputs
- Provides Regulated +5.0 V Output for Sensor Power from Bus
- Additional High-Drive Logic Output
- Undervoltage Fault Detection and Signaling
- On-Board Clock (No External Elements Required)
- Field-Programmable Address
- Default and Field-Programmable as a DSI Daisy Chain Device
- Recognizes Reverse Initialization for Open Bus Fault Tolerance
- Detects Short to Battery on Bus Switch and Prevents Its Closure
- Pb-Free Packaging Designated by Suffix Code EF

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DISTRIBUTED SYSTEM INTERFACE

D SUFFIX
EF SUFFIX (Pb-FREE)
98ASB42566B
16-PIN SOICN

ORDERING INFORMATION

Device	Temperature Range (T$_J$)	Package
MC33793D/R2		
MCZ33793EF/R2	-40°C to 150°C	16 SOICN
MCZ33793AEF/R2		
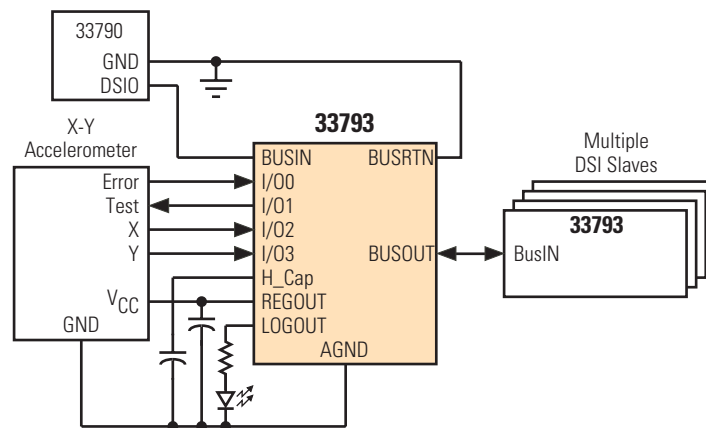
Figure 1. 33793 Simplified Application Diagram

DEVICE VARIATIONS

Table 1. Device Variations

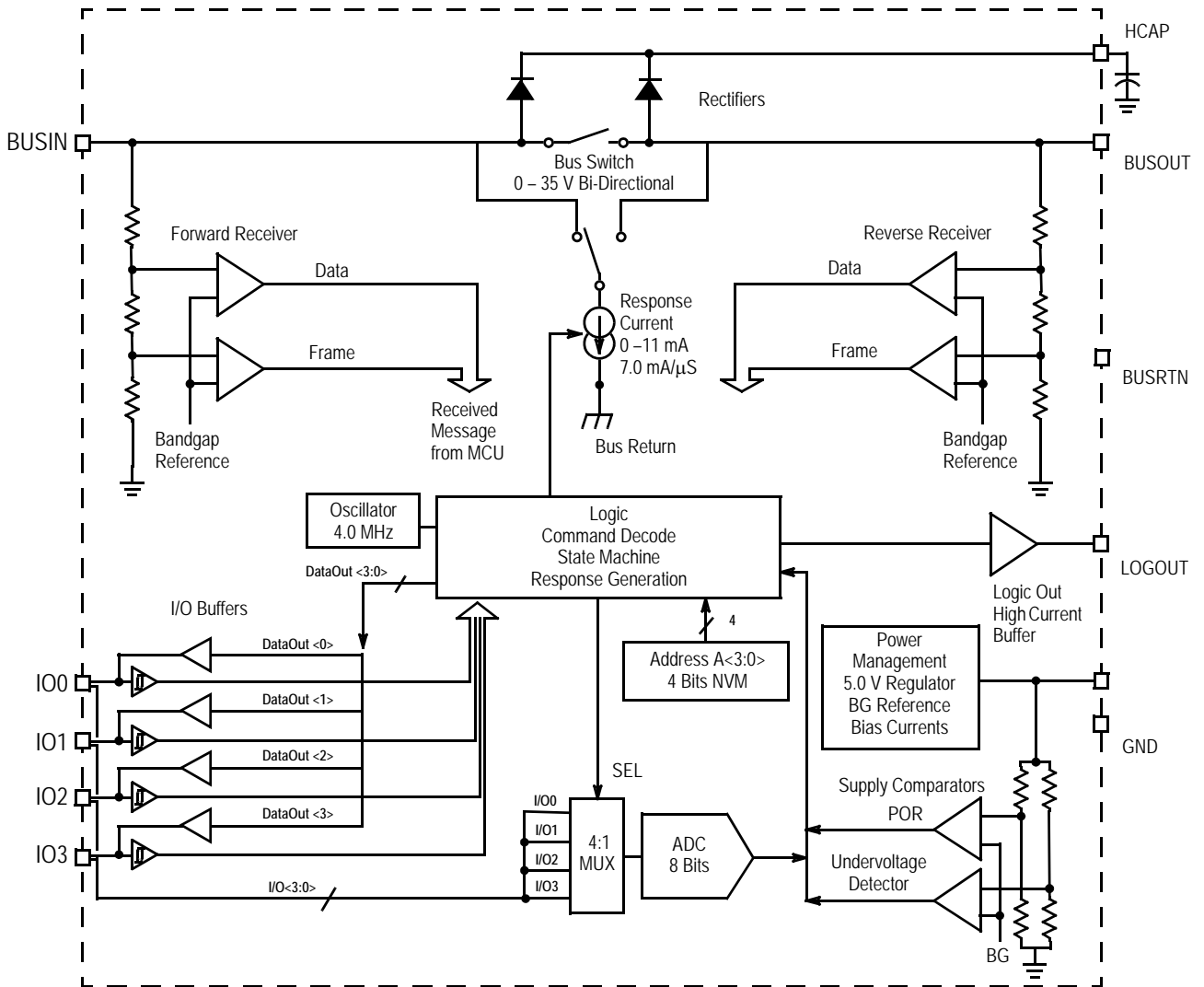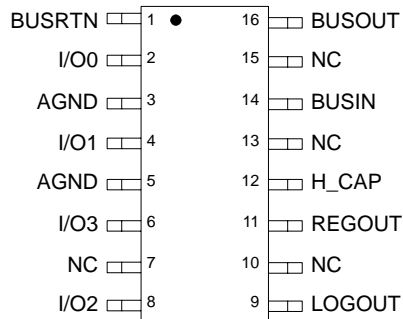| Freescale Part No.	Other Significant Device Variations
MCZ33793EF/R2	Existing capacity
MCZ33793AEF/R2	Capacity expansion

INTERNAL BLOCK DIAGRAM

Figure 2. 33793 Simplified Internal Block Diagram

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PIN CONNECTIONS

Figure 3. 33793 Pin Connections

Table 2. 33793 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on .

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	BUSRTN	Power	Bus Return	This pin provides the common return for power and signalling.
2	I/O0	Input/Output	Logic I/O	This pin can be used to provide a logic level output, a logic input, or an analog-to-digital (A/D) input.
3, 5	AGND	Ground	Analog Ground	This pin is the low reference level and power return for the analog-to-digital converter (ADC).
4	I/O1	Input/Output	Logic I/O	This pin can be used to provide a logic level output, a logic input, or an A/D input.
6	I/O3	Input/Output	Logic I/O	This pin can be used to provide a logic level output, a logic input, or an A/D input.
7, 10, 13, 15	NC	No Connect	No Connect	These pins have no internal connections.
8	I/O2	Input/Output	Logic I/O	This pin can be used to provide a logic level output, a logic input, or an A/D input.
9	LOGOUT	Output	Logic Out	This is a logic output with higher pull-up drive capability than the standard logic I/O.
11	REGOUT	Output	Regulator Output	This pin provides a regulated 5.0 V output. The power is derived from the bus.
12	H_CAP	Output	Holding Capacitor	A capacitor attached to this pin is charged by the bus during bus idle and supplies current to run the device and for external devices via the REGOUT pin during non-idle periods.
14	BUSIN	Input	DSI Bus Input	This pin attaches to the bus and responds to initialization commands.
16	BUSOUT	Output	DSI Bus Output	This pin attaches to the bus and responds to reverse initialization commands.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
I/O Pin Voltage	V_{IO}	-0.3 to V_{REGOUT} + 0.5	V
I/O Pin Current	I_{IO}	5.0	mA
BUSIN, BUSOUT, BUSRTN, and H_CAP Voltage	V_{IN}	-0.3 to 40	V
BUSIN, BUSOUT, BUSRTN, and H_CAP Current (Continuous)	I_{IN}	250	mA

ESD Protection [1]
    Human Body Model
    Machine Model
	V_{ESD1}
	V_{ESD2}
		±2000
		±200
			V

THERMAL RATINGS			
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Peak Package Reflow Temperature During Reflow [2], [3]	T_{PPRT}	Note 3.	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	150	°C/W

Notes

1. ESD1 performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).

2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

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STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions -0.3 V $\leq$ V$_{BUSIN}$ or V$_{BUSOUT}$ $\leq$ 30 V, 5.5 V $\leq$ V$_{H\_CAP}$ $\leq$ 30 V, -40°C $\leq$ T$_A$ $\leq$ 85°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T$_A$ = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Quiescent Current Drain V$_{H\_CAP}$ = 25 V, Logout = 0, I/O = Input	I$_Q$	– 	– 	 3.0	mA
BUSIN or BUSOUT to H_CAP Rectifier Voltage Drop I$_{BUSIN}$ or I$_{BUSOUT}$ = 15 mA I$_{BUSIN}$ or I$_{BUSOUT}$ = 100 mA	V$_{RECT}$	 – –	 0.75 0.9	 1.0 1.2	V
BUSIN + BUSOUT Bias Current V$_{BUSIN}$ or V$_{BUSOUT}$ = 8.0 V, V$_{H\_CAP}$ = 9.0 V V$_{BUSIN}$ or V$_{BUSOUT}$ = 0.5 V, V$_{H\_CAP}$ = 25 V	I$_{BIAS}$	 -100 	 – –	 100 20	μA
Rectifier Leakage Current V$_{BUSIN}$ or V$_{BUSOUT}$ = 5.0 V, V$_{H\_CAP}$ = 25 V	I$_{RLKG}$	 -20	 –	 100	μA
Reg0ut 5.5 V $\geq$ V$_{H\_CAP}$ $\geq$ 25 V, I$_{RO}$ = 12 mA	V$_{REG}$	 4.75	 5.0	 5.25	V
RegOut Line Regulation I$_{RO}$ = 12 mA, 5.5 V $\geq$ V$_{H\_CAP}$ $\geq$ 25 V	VR$_{LINE}$	 –	 71	 180	mV
RegOut Load Regulation I$_{RO}$ = 0 to 12 mA, 5.5 V $\geq$ V$_{H\_CAP}$ $\geq$ 25 V	VR$_{LD}$	 –	 2.3	 100	mV
Undervoltage Lockout Proportional to unloaded V$_{REGOUT}$	V$_{UVL}$	 0.93	 0.95	 0.97	V$_{RO}$
Bus Switch Resistance V$_{BI}$ = 8.0 V, I$_{BO}$ = -80 mA (Bus Switch Active)	R$_{SW}$	 –	 4.0	 8.0	Ω
I/O0 and I/O3 Pull-Down Current 0 < V$_{BUSIN}$ or V$_{BUSOUT}$ < 1.0 V	I$_{PD}$	 7.0	 11	 13	μA
I/O1 and I/O2 Pull-Up Current V$_{RO}$ < V$_{BUSIN}$ or V$_{BUSOUT}$ < V$_{RO}$ - 1.0 V	I$_{PU}$	 -7.0	 -11	 -13	μA
BUSIN and BUSOUT Logic Thresholds Low High	 V$_{THL}$ V$_{THH}$	 2.8 5.5	 3.0 6.0	 3.2 6.5	V
Logic Duty Cycle (assured by design) Logic 0 Logic 1	 D$_{CL}$ D$_{CH}$	 10 60	 33 67	 40 90	%
BUSIN + BUSOUT Response Current V$_{BUSIN}$ and/or V$_{BUSOUT}$ = 4.0 V	I$_{RSP}$	 9.9	 11	 12.1	mA
ADC Code Conversion Error (INL)	ADC$_{INL}$	–	–	< 1.0	LSB
ADC Full-scale Error	ADC$_{FS}$	–	–	3	counts
I/O Logic Input Thresholds Logic High Logic Low	 V$_{IH}$ V$_{IL}$	 0.7 –	 0.54 0.51	 – 0.3	V$_{RO}$

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions -0.3 V $\leq$ V$_{BUSIN}$ or V$_{BUSOUT}$ $\leq$ 30 V, 5.5 V $\leq$ V$_{H\_CAP}$ $\leq$ 30 V, -40°C $\leq$ T$_A$ $\leq$ 85°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T$_A$ = 25°C under nominal conditions unless otherwise noted.

| Characteristic	Symbol	Min	Typ	Max	Unit
I/O Logic Output Levels					
Output Low (I$_L$ = 1.0 mA)	V$_{OL}$	0	0.08	0.5	V
Output High (I$_L$ = -500 µA)	V$_{OH}$	0.8	0.985	1.0	V$_{RO}$
LOGOUT Output Levels					V
Output Low (I$_L$ = 500 µA)	V$_{LOL}$	0	0.2	0.5	
Output High (I$_L$ = -10 mA, 6.2 V $\leq$ V$_{H\_CAP}$ $\leq$ 25 V)	V$_{LOH1}$	4.7	5.0	5.3	
Output High (I$_L$ = -100 µA, 6.2 V $\leq$ V$_{H\_CAP}$ $\leq$ 25 V)	V$_{LOH2}$	–	–	V$_{RO}$+0.5	
Programming Time	T$_{PROG}$				ms
From Positive Edge of BUSIN or BUSOUT $\geq$ V$_{THH}$ on Program Command to Following Command Negative Transition $\leq$ V$_{THH}$		100	200	1000	
NVM BUSIN or BUSOUT Programming Voltage	NVM$_{VP}$	22.25	–	30	V

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DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions -0.3 V $\leq$ V_{BUSIN} or V_{BUSOUT} $\leq$ 30 V, 5.5 V $\leq$ V_{H_CAP} $\leq$ 30 V, -40°C $\leq$ T_A $\leq$ 85°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

| Characteristic	Symbol	Min	Typ	Max	Unit
Initialization to Bus Switch Closing	t_{BS}	100	150	200	μs
Loss of Signal Reset Time 　　Maximum Time Below Frame Threshold	t_{TO} –	 –	 –	 100	ms
ADC Code Conversion Time (Go, No-Go Test)	t_{ADC}	–	–	27	μs
BUSIN and BUSOUT Response Current Transition Time 　　1.0 mA to 9.0 mA Transition, 9.0 mA to 1.0 mA	t_{ITR} –	 7.0	 10	mA/μs
BUSIN or BUSIN Timing to Response Current 　　BUSIN or BUSOUT Negative Voltage Transition = 3.0 V to I_{RSPH} = 7.0 mA 　　BUSIN or BUSOUT Negative Voltage Transition = 3.0 V to I_{RSPL} = 5.0 mA	 t_{RSPH} t_{RSPL}	 – –	 – –	 3.3 3.3	μs

TIMING DIAGRAMS
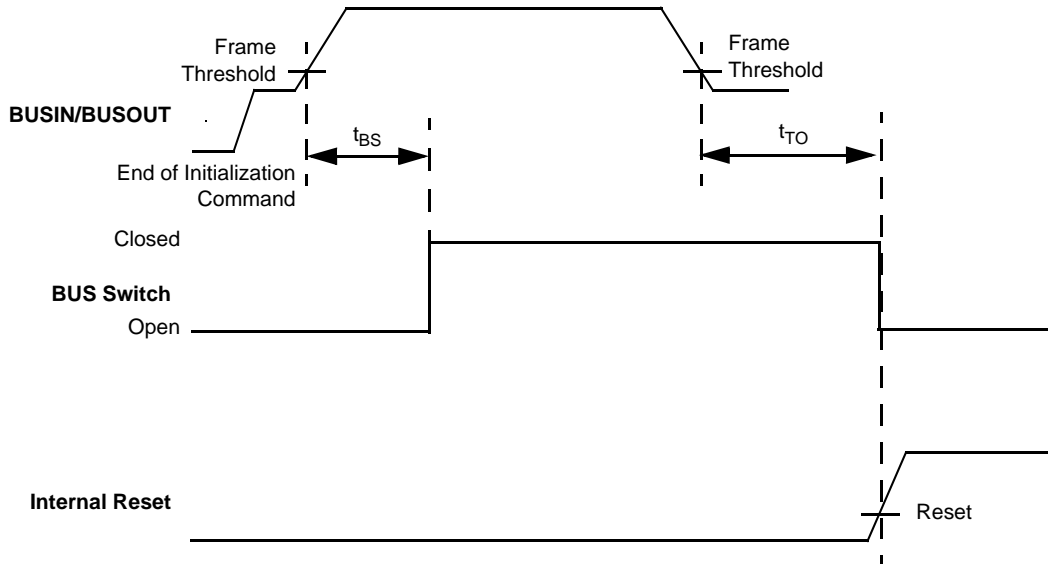
Figure 4. Bus Switch and Reset Timing
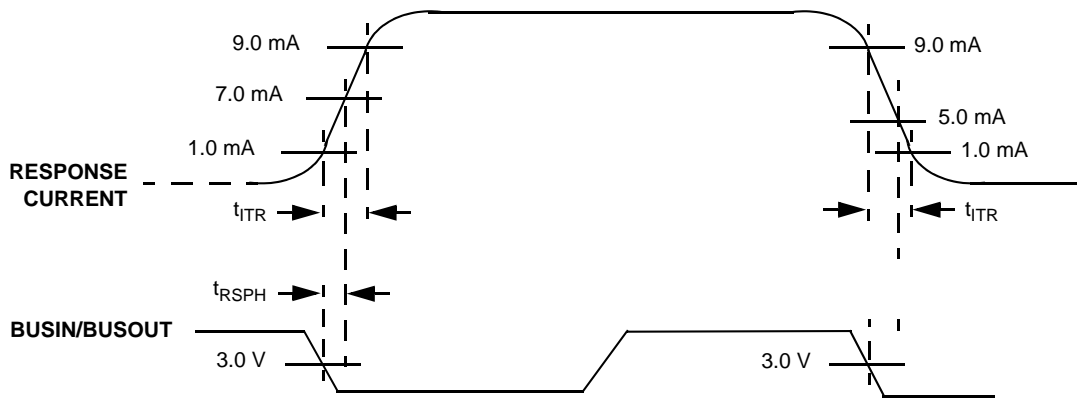
Figure 5. Response Current Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33793 is designed to be used with a sensor at a location that is remote from a centralized MCU. This device provides power, measurement, and communications between the remote sensor and the centralized MCU over a DSI bus. Sensors such as accelerometers can be powered from the regulated output of the device, and the resulting analog value from the sensor can be converted from an analog level to a digital value for transmission over the DSI bus in response to a query from the MCU. Four I/O lines can be configured by the central MCU over the DSI bus as analog inputs, digital inputs, or digital outputs. This allows more than one sensor to be remotely controlled and measured by a single 33793. Additionally, a high drive logic output is provided that can be used to power other low-power sensors.

Power is passed from BUSIN or BUSOUT through on-board rectifiers to a storage capacitor (referred to as the H_CAP). The H_CAP stores energy during the highest voltage excursions of the BUSIN or BUSOUT pin (idle) and

supplies energy to power the device during low excursions of BUSIN and BUSOUT.

The Regulator supplies an on-board regulated voltage for internal use, and the Power on Reset (POR) circuit provides a reset signal during low-voltage conditions and during power up/down. Some current is available for low-power sensors.

Data from the Central Control Unit (CCU) is applied to the BUSIN and/or BUSOUT pins as voltage levels that are sensed by the Level Detection circuitry. The Serial Decoder detects these transitions and decodes the incoming data. The Control Logic provides overall control of the 33793. It controls diagnostic testing and formats responses to commands with the message encoder. Responses are formed via a switched current source that is slew-rate controlled.

The one-time programmable (OTP) memory array provides the nonvolatile storage for the pre-programmed address. It is accessed via the Read/Write NVM command. It has a built-in hardware lock that only allows one write.

FUNCTIONAL PIN DESCRIPTION

BUS RETURN (BUSRTN)

This pin provides the common return for power and signalling.

INPUT/OUTPUT (I/O0, I/O1, I/O2, I/O3)

This pin can be used to provide a logic level output, a logic input, or an analog-to-digital (A/D) input.

ANALOG GROUND (AGND)

This pin is the low reference level and power return for the analog-to-digital converter (ADC).

LOGIC OUT (LOGOUT)

This is a logic output with higher pull-up drive capability than the standard logic I/O.

REGULATOR OUTPUT (REGOUT)

This pin provides a regulated 5.0 V output. The power is derived from the bus.

HOLDING CAPACITOR (H_CAP)

A capacitor attached to this pin is charged by the bus during bus idle and supplies current to run the device and for external devices via the REGOUT pin during non-idle periods.

DSI BUS INPUT (BUSIN)

This pin attaches to the bus and responds to initialization commands.

DSI BUS OUTPUT (BUSOUT)

This pin attaches to the bus and responds to reverse initialization commands.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

Refer to Figure 2, 33793 Internal Block Diagram, page 3, for a simplified representation of the 33793's components.

RECTIFIER

This rectifier or switch peak detects the bus signal into an external capacitor attached to H_CAP. The capacitor supplies power during signaling while the input voltage is at a lower level.

The voltage waveform at BUSIN and/or BUSOUT and the size of the filter capacitor at H_CAP must be such that the

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voltage at H_CAP will not drop below the frame threshold during signaling.

POR

The 33793 leaves the reset state when the voltage on H_CAP rises above the Power-ON Reset threshold.

TIMEOUT

A timeout timer keeps track of the length of the time when the input is not in idle mode. If this time exceeds a limit, the

part is reset. The purpose of this is to allow the part to reset itself if the connection to the master is lost or if power is removed from the system.

5.0 V REGULATOR

The 5.0 V regulator supplies internal power for the device and also provides approximately 6.0 mA through the REGOUT pin to power an external sensor.

UNDERVOLTAGE DETECTOR

The undervoltage detector monitors the output voltage of the 5.0 V regulator. If the REGOUT voltage drops too low for accurate A/D operation, a signal is sent to the control logic. The control logic will interpret this signal and, in response to a command, report a status indicating an undervoltage condition to have existed. When received, the command will clear the signal after having read the status. If the voltage is too low when the A/D conversion was completed, the returned value will be zero (binary 00000000).

IO PINS 0 TO 3

The IO pins can serve as logic inputs, logic outputs, or analog inputs. At power-up or after a clear, the pins are all logic inputs and can be used to measure an analog level value for an analog value request command. The pins can be individually configured as logic inputs or outputs by the IO Control command. If the pin is configured as a logic output, reading the analog value will return the analog level the output is being driven to.

ANALOG-TO-DIGITAL CONVERTER

The ADC is an 8-bit successive approximation type using on-board capacitive division. It uses the Clk signal from the on-board oscillator for sequencing.

The ADC uses REGOUT as a full-scale reference voltage and ground AGND for a zero-level reference.

The ADC signals when it has made a valid conversion by asserting a signal to the controller. If this signal is not asserted when a value is being captured by the controller, the controller will signal that an invalid A/D value was obtained.

The value of "0" (binary 00000000) is reserved by the control logic to signal an error. A value of "0" from the ADC will be reported as "1" (binary 00000001) by the control logic.

SERIAL ENCODER

The Serial Encoder accepts the digitized value from the ADC and formatting/data from the Control Logic. A logic transition from Idle to Signal High and then to Signal Low at BUSIN will cause the first bit to be presented to the current switch (Response Loading). A transition to Signal High and back to Signal Low will cause the next bit to be presented to the current switch. This will continue until a transition back to Idle turns off the current switch.

SLEW

The slew circuit serves to reduce EMI produced as a result of switching the bus loading current sink element. The slew

circuit limits the rise and fall time of current loading the bus by controlling the current sinking element.

SWITCHED CURRENT SOURCE

A "1" data return bit will be signaled by turning on a fixed current source. During signaling time, the 33793 will be using power from H_CAP and not loading the bus for power. The current will be drawn from either BUSIN or BUSOUT or split between them. The split can be in any proportion as long as the total is correct.

The current source is turned off whenever the bus is at Idle level.

LEVEL DETECTOR

The level detector contains comparators to determine if the BUSIN or BUSOUT is at idle, logic high, or logic low. The inputs from BUSIN and BUSOUT are sensed by the device so that if either side is driven by the signaling waveform while the other is not, the signaling will be detected. This circuit also provides a signal to indicate if the signal is being received on the BUSOUT pin. If a "reverse initialization" command is received, it can only be acted upon if the device is not already initialized and if the signal is present on BUSOUT.

SERIAL DECODER

The Serial Decoder monitors transitions on the BUSIN or BUSOUT. When the 33793 is Idle and supplying power to itself and the external device(s) (via REGOUT), the input to BUSIN will be in the Idle state. A transition from this level to Signal Low (through Signal High) will start the process of decoding a word of data. BUSIN is driven from Signal Low to Signal High for each bit and back to Signal Low to start the next bit. The determination of whether the bit was a one or a zero is made by determining whether it spent more time low (a zero) or high (a one). The end of the word is signaled by a transition at the end of the last bit from Signal High to Idle. The advantage of this method is that it will accept data over a wide range of rates and is not dependent on an accurate clock.

The controller will typically indicate a logic zero by spending 2/3 of the bit period at Signal Low and 1/3 at Signal High. A logic one would be 1/3 of the bit period at Signal Low and 2/3 at Signal High.

CONTROL LOGIC

The control logic performs the digital operations carried out by this device. Its principle functions include:

- Decoding input instructions.
- Control the general purpose I/O and LOGICOUT in response to BUSIN or BUSOUT commands.
- Control A/D conversions.
- Form response word.
- Capture and store address.
- Control BUSSW.
- Reset device on power-up.
- Control the general purpose I/O logic configuration.

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- Read the general purpose I/O logic values and respond to request for these values.
- Generating a cycle redundancy check (CRC) for the received data and transmitted data in conformance with the DSI Bus Standard.

Additionally, the control logic performs error checking on the received data. If errors are found, no action is taken and no response is made. Errors include:

- CRC received doesn't match CRC of received data.
- Number of received bits is not 12 or 20.

CLOCK

The clock is a low-stability type with the capacitor integrated onto the die. The signaling system and all internal operations are such that no external precision timing device is needed in the normal operation of this device.

BUS SWITCH (BUSSW)

The bus switch passes signaling and power to all subsequent devices on the bus. It can block a voltage of either polarity up to the highest idle state level between BUSIN and BUSOUT.

LOGICOUT

LOGICOUT is a logic level output with enhanced high-side drive capability.

ADDRESSING

The 33793 IC supports both runtime programmable and pre-programmed addressing as defined in the DSI Specification. Runtime programmable addressing uses the daisy chain bus connection. Pre-programmed devices may either be connected in daisy chain or in parallel on the bus wires.

Programmable address devices all power up with a device address of $0 in their address register and their bus switches open. In the daisy chain, if the first device receives the initialization command device on BUSIN, it will accept the address in the command and close its switch at the end of the command. The next device in the chain will now be able to receive the initialization command on its BUSIN and will accept the next address. This proceeds down the chain until the last device is addressed. The devices can also be initialized by the reverse initialization command if the signal is applied to BUSOUT.

Pre-programmed devices power up with their pre-programmed address in its address register. It will ignore all Initialization commands unless the address in the command matches its pre-programmed address. In this event the device stores the other information contained in the Initialization command.

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FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

A device may be permanently programmed one time with an address using a two-command sequence. The first step is satisfied on the reception of an Initialization command with address set to zero, the PA[3:0] set to the address to be programmed, and the NV bit set. This will cause the address contained in the PA[3:0] bits to be stored in the address register and the bus switch closed. The second step is taken when a Read/Write NVM command is received with the PA[3:0] bits matching the A[3:0] bits and also matching the bits stored in the 33793 address register. This will cause the 33793 to permanently store this address into an internal NVM area.

MESSAGES

The messages follow the format defined in the Distributed Systems Interface Specification rev 1.0 unless otherwise noted.

DSI BUS COMMANDS

This device can recognize and respond to both long-word and short-word commands. A command word summary is shown in Table 6. SW in the "Size" column of the table indicates short-word commands and LW indicates long-word commands. Short-word commands may also be sent in the long-word format. However, when these commands are sent in the long-word format, it is recommended that the data byte be sent as $00 to maintain future compatibility. All commands marked reserved should not be sent to 33793 slaves.

Table 6. DSI Bus Commands

Command				Size	Description	Data							
C3	C2	C1	C0			D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	LW	Initialization	NV	BS	G1	G0	PA3	PA2	PA1	PA0
0	0	0	1	SW	Request Status	–	–	–	–	–	–	–	–
0	0	1	0	SW	Request Value 0	–	–	–	–	–	–	–	–
0	0	1	1	LW	I/O Control	L3	L2	L1	L0	DR3	DR2	DR1	DR0
0	1	0	0	SW	Request ID Information	–	–	–	–	–	–	–	–
0	1	0	1	SW	Request Value 1	–	–	–	–	–	–	–	–
0	1	1	0	SW	Request Value 2	–	–	–	–	–	–	–	–
0	1	1	1	SW	Clear	–	–	–	–	–	–	–	–
1	0	0	0	SW	Request Value 3	–	–	–	–	–	–	–	–
1	0	0	1	LW	Read/Write NVM	1	1	1	1	PA3	PA2	PA1	PA0
1	0	1	0		Reserved								
1	0	1	1		Reserved								
1	1	0	0	SW	Clear Logic Out	–	–	–	–	–	–	–	–
1	1	0	1	SW	Set Logic Out	–	–	–	–	–	–	–	–
1	1	1	0		Reserved								
1	1	1	1	LW	Reverse Initialization	NV	BS	G1	G0	PA3	PA2	PA1	PA0

Legend

BS = Controls closing of the Bus Switch (1 = close).

DR[3:0] = Direction of I/O. 1 = Output.

G[1:0] = Group assignment (the 33793 does not use these bits).

L[3:0] = Level to output on I/O if configured as outputs.

LO = Logic Out level.

PA[3:0] = Bus Address to set the device to.

NV = Allows nonvolatile address programming if set to "1".

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LONG- AND SHORT-WORD RESPONSES

The device responds to Long-word commands with long-word responses and short-word commands with short-word responses. Responses are sent during the next message following the command. A long-word response summary is found in Table 7 and a short-word response summary is found in Table 8, page 15.

Table 7. Long-Word Response Summary

CMD hex	Command Description	Response															
0	Initialization	A3	A2	A1	A0	0	0	0	BF	NV	BS	G1	G0	PA3	PA2	PA1	PA0
1	Request Status	A3	A2	A1	A0	0	0	0	0	NV	U	LO	BS	IO3	IO2	IO1	IO0
2	Request Value 0	A3	A2	A1	A0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
3	I/O Control	A3	A2	A1	A0	0	0	0	0	L3	L2	L1	L0	DR3	DR2	DR1	DR0
4	Request ID	A3	A2	A1	A0	0	0	0	0	V2	V1	V0	0	0	0	1	1
5	Request Value 1	A3	A2	A1	A0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
6	Request Value 2	A3	A2	A1	A0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
7	Clear	No Response															
8	Request Value 3	A3	A2	A1	A0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
9	Read/Write NVM	A3	A2	A1	A0	0	0	0	0	1	1	1	1	PA3	PA2	PA1	PA0
A	Reserved																
B	Reserved																
C	Clear Logic Out	A3	A2	A1	A0	0	0	0	0	NV	U	LO	BS	IO3	IO2	IO1	IO0
D	Set Logic Out	A3	A2	A1	A0	0	0	0	0	NV	U	LO	BS	IO3	IO2	IO1	IO0
E	Reserved																
F	Reverse Initialization	A3	A2	A1	A0	0	0	0	BF	NV	BS	G1	G0	PA3	PA2	PA1	PA0

Legend

A[3:0] = Address bits. The slave address.

B[7:0] = 8-bit A/D value.

BF = Bus Fault

BS = Status of the Bus Switch (1 = close).

DR[3:0] = I/O direction bits (1 = Output).

G[1:0] = Group assignment (the 33793 does not use these bits).

IO[3:0] = Logic level of I/O.

L[3:0] = Level to output on I/O if configured as outputs.

LO = Logic Out level at the Logic Out pin.

NV = Allows nonvolatile address programming if set to "1".

PA[3:0] = Bus Address to set the device to.

U = Undervoltage Flag.

V[2:0] = Version number.

Table 8. Short-Word Response Summary

Command	Command Description	Response							
0000	Initialization	Not Valid							
0001	Request Status	NV	U	LO	BS	IO3	IO2	IO1	IO0
0010	Request Value 0	B7	B6	B5	B4	B3	B2	B1	B0
0011	I/O Control	Not Valid							
0100	Request ID Information	V2	V1	V0	0	0	0	1	1
0101	Request Value 1	B7	B6	B5	B4	B3	B2	B1	B0
0110	Request Value 2	B7	B6	B5	B4	B3	B2	B1	B0
0111	Clear	No Response							
1000	Request Value 3	B7	B6	B5	B4	B3	B2	B1	B0
1001	Read/Write NVM	Not Valid							
1010	Reserved								
1011	Reserved								
1100	Clear Logic Out	NV	U	LO	BS	IO3	IO2	IO1	IO0
1101	Set Logic Out	NV	U	LO	BS	IO3	IO2	IO1	IO0
1110	Reserved								
1111	Reverse Initialization	Not Valid							

Legend

B[7:0] = 8-bit A/D value.

BS = Status of the Bus Switch (1 = close).

LO = Logic Out level at the Logic Out pin.

IO[3:0] = Logic level of I/O.

NV = Allows nonvolatile address programming if set to "1".

PA[3:0] = Bus Address to set the device to.

U = Undervoltage Flag.

V[2:0] = Version number.

DSI COMMANDS AND RESPONSES

INITIALIZATION COMMAND

The Initialization command must be sent to the 33793 before it may commence communications over the bus. The command may be used three ways. The first is to initialize a programmable address device. The second is the first step in assigning a pre-programmed address. The third is to initialize a pre-programmed device.

For the first case this command is sent to address zero with the NV bit set to zero. The command will be received by the next daisy chain device with its bus switch open. Reception of this command will assign the device address and group number.

For the second case the Initialization command is sent the same as the first except that the NV bit is set to one.

Reception of the command will assign the device address and group number. A Read/Write NVM command then may be sent to complete the setting of a pre-programmed address.

A pre-programmed device must be initialized by putting its address in both PA3:PA0 and A3:A0 fields.

Once a device has received an initialization command, it will ignore further initialization commands unless it has received a Clear command or undergone a power-up reset.

If BS = 1 and no faults are detected, initialization will cause the bus switch to close.

The command format is found in Table 9.

Table 9. Initialization Command Format

Data								Address				Command				CRC			
NV	BS	G1	G0	PA3	PA2	PA1	PA0	A3	A2	A1	A0	0	0	0	0	X3	X2	X1	X0

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Table 9. Initialization Command Format

Legend

A[3:0] = Address bits. The slave address.

BS = Bus Switch Position (1 = closed).

G[1:0] = Group bits (unused).

NV = Nonvolatile Memory Write. The value of the NV bit in the slave.

PA[3:0] = Bus Address to set the device to.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

INITIALIZATION RESPONSE

This response message is sent during the next message following a valid Initialization command to the addressed device. The response is shown in Table 10. Because this is a long-word only command, the short-word response is invalid.

Table 10. Initialization Response Format

High Byte								Low Byte								CRC			
A3	A2	A1	A0	0	0	0	BF	NV	BS	G1	G0	PA3	PA2	PA1	PA0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The slave address.

BF = Bus Fault. Bus out short to battery detected.

BS = Bus Switch Position (1 = closed).

G[1:0] = Group bits (unused).

NV = Nonvolatile Memory Write. The value of the NV bit in the slave.

PA[3:0] = Bus Address to set the device to.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

REQUEST STATUS COMMAND

This command will cause the addressed device to return the status of the NV, U, and BS bits and the logic levels of the I/O and LOGICOUT. The command format is found in Table 11.

Table 11. Request Status Command Format

Data								Address				Command				CRC			
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	0	0	1	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The address of the selected device. An address value of "0000" is ignored by all devices.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

REQUEST STATUS RESPONSE

This response message is sent during the next message following a valid Request Status command to the addressed device. The response format is found in Table 12. The high byte is omitted during the short-word response. No response is generated if the command address field was $0.

Table 12. Request Status Response Format

High Byte								Low Byte								CRC			
A3	A2	A1	A0	0	0	0	0	NV	U	LO	BS	IO3	IO2	IO1	IO0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The slave address.

BS = Bus Switch Position (1 = closed).

LO = Logic out driven level.

IO[3:0] = Values at logic I/Os.

NV = Nonvolatile Memory Write. The value of the NV bit in the slave.

U = Undervoltage indicated true by a "1".

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

REQUEST VALUE n COMMAND

This command will cause the analog level at one of the four I/O lines to be measured and returned on the following command. The command format is found in Table 13. The analog input measured is defined in Table 14.

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Table 13. Request Value n Command Format

Data								Address				Command				CRC			
–	–	–	–	–	–	–	–	A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The address of the selected device. An address value of "0000" is ignored by all devices.

C[3:0] = Command number.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

Table 14. Analog Input Selection

Command	A/D Input
0010	I/O0
0101	I/O1
0110	I/O2
1000	I/O3

REQUEST VALUES RESPONSE

This response is an 8-bit value representing the value measured by the ADC. The selection of "n" is a function of the command. This is shown in Table 15.

The read will be completed during the idle period and will represent the voltage at the end of the command. If an undervoltage condition exists at any time during the command or the measurement has not completed properly, a value of "00000000" will be returned. This is a reserved value to indicate a problem with the measurement. The minimum valid level reported will be "00000001". No response is generated if the command address field was $0.

Table 15. Request Values Response Format

High Byte								Low Byte								CRC			
A3	A2	A1	A0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The address of the selected device. An address value of "0000" is ignored by all devices.

D[7:0] = Measured value (MSB = D7).

X[3:0] = Cyclic Redundancy Check (CRC).

I/O CONTROL COMMAND

This register controls the I/O ports. When the "DR" bits are set, the corresponding I/O is enabled as an output. The "L" bit settings control the level of the corresponding I/O if it is enabled as an output. The format of this command is shown in Table 16.

Table 16. I/O Control Command Format

Data								Address				Command				CRC			
L3	L2	L1	L0	DR3	DR2	DR1	DR0	A3	A2	A1	A0	0	0	1	1	X3	X2	X1	X0

Legend

A[3:0] = Address bits.

DR[3:0] = I/O direction bits. 1 = Output. All bits are set to "0" by reset/clear.

L[3:0] = Level to output on I/O if configured as output. All bits are set to "0" by reset/clear

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

I/O CONTROL RESPONSE

The response indicates which I/O has been configured as outputs and their current values.

The values returned will be the values programmed. The values at the pins will not be the ones that were programmed if the pin has been forced to the opposite state. The response format is shown in Table 17. No response is generated if the command address field was $0.

Table 17. I/O Control Response Format

High Byte	Low Byte	CRC

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Table 17. I/O Control Response Format

A3	A2	A1	A0	0	0	0	0	L3	L2	L1	L0	DR3	DR2	DR1	DR0	X3	X2	X1	X0

Legend

A[3:0] = Address bits.

DR[3:0] = I/O enabled as outputs (1 = enabled as output).

L[3:0] = Programmed values.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

REQUEST ID COMMAND

This command will cause the device ID information to be read from internal storage and returned to the master during the response to the next message. The command format is found in Table 18.

Table 18. Request ID Command Format

Data								Address				Command				CRC			
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	0	0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The address of the selected device. An address value of "0000" is ignored by all devices.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

REQUEST ID RESPONSE

This response message is sent during the next message following a valid long-word Request ID command to the addressed device. The response format is found in Table 19. The high byte is omitted during the short-word response. No response is generated if the command address field was $0.

Table 19. Request ID Response Format

Address				Status				Data								CRC			
A3	A2	A1	A0	0	0	0	0	V2	V1	V0	0	0	0	1	1	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The slave address.

V[2:0] = Device version number. The silicon version number of the device. For this device the device type is 00011 as indicated by the lowest bits.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

CLEAR COMMAND

This command will open the bus switch and reset all registers to the reset state. The command format is found in Table 20. No response is generated for the Clear command.

Table 20. Clear Command Format

Data								Address				Command				CRC			
–	–	–	–	–	–	–	–	A3	A2	A1	A0	0	1	1	1	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The address of the selected device. An address value of "0000" clears all devices.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

READ/WRITE NVM COMMAND

If the NV bit has been set by a previous Initialization command and the NVM has not been programmed previously, this command will permanently program the device's one-time programmable address and return the programmed value during the next message time. Once programmed, this nonvolatile address is used to set the device address register on the next and all subsequent power-ups. If the device is not blank, this command will return the programmed value during the next message time.

Programming the NVM address to $0 is allowed. This ensures that the device always acts as a dynamically

addressable device and would be immune to any inadvertent future NVM programming sequences.

Reads and writes are long-word commands only. The command format is found in Table 21.

Table 21. Read/Write NVM Command Format

Data								Address				Command				CRC			
1	1	1	1	PA3	PA2	PA1	PA0	A3	A2	A1	A0	1	0	0	1	X3	X2	X1	X0

Legend

A[3:0] = Address bits. These bits are the address of the device previously sent with the Initialization command. They must match the address in the PA[3:0] field and the address stored in the device address register.

PA[3:0] = Program Address bits. These bits are the address that is to be programmed into the slave.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

READ/WRITE NVM RESPONSE

This response message is sent during the next message following a valid Read/Write NVM command to the addressed device. The response format is found in Table 22. The high byte is omitted during the short-word response. No response is generated if the command address field was $0.

Table 22. Read/Write NVM Response Format

High Byte								Low Byte								CRC			
A3	A2	A1	A0	0	0	0	0	1	1	1	1	PA3	PA2	PA1	PA0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The slave address.

PA[3:0] = Programmed Address bits. The address that was programmed into the NVM address bits of the slave.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

CLEAR LOGIC OUT COMMAND

The Clear Logic Out command sets the Logic Out pin to a logic low. The compliment to this command is the Set Logic Out. The Logic Out is also cleared at power-up or following a Clear command. The format of the Clear Logic Out command is shown in Table 23.

Table 23. Clear Logic Out Command Format

Data								Address				Command				CRC			
–	–	–	–	–	–	–	–-	A3	A2	A1	A0	1	1	0	0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The address of the selected device.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

CLEAR LOGIC OUT RESPONSE

This response message is sent during the next message following a valid Clear Logic Out command to the addressed device. The response is shown in Table 24. No response is generated if the command address field was $0.

Table 24. Clear Logic Out Response Format

High Byte								Low Byte								CRC			
A3	A2	A1	A0	0	0	0	0	NV	U	LO	BS	IO3	IO2	IO1	IO0	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The slave address.

BS = Bus Switch Position (1=closed).

LO = Logic out driven level.

IO[3:0] = Values at logic I/Os.

NV = Nonvolatile Memory Write. The value of the NV bit in the slave.

U = Undervoltage indicated true by a "1".

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

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SET LOGIC OUT COMMAND

The Set Logic Out command sets the Logic Out pin to a logic high. The compliment to this command is the Clear Logic Out. The Logic Out is cleared at power-up or following a Clear command. The format of the Clear Logic Out command is shown in Table 25.

Table 25. Set Logic Out Command Format

Data								Address				Command				CRC			
-	-	-	-	-	-	-	-	A3	A2	A1	A0	1	1	0	1	X3	X2	X1	X0

Legend

A[3:0] = Address bits. The address of the selected device.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

SET LOGIC OUT RESPONSE

This response message is sent during the next message following a valid Set Logic Out command to the addressed device. The response is shown in Table 26. No response is generated if the command address field was $0.

Table 26. Set Logic Out Response Format

High Byte								Low Byte								CRC			
A3	A2	A1	A0	0	0	0	0	NV	U	LO	BS	IO3	IO2	IO1	IO0	X3	X2	X1	X0

Legend

A[3:0] - Address bits. The slave address.

BS = Bus Switch Position (1=closed)

IO[3:0] = Values at logic I/Os.

LO = Logic out driven level.

NV = Nonvolatile Memory Write. The value of the NV bit in the slave.

U = Undervoltage indicated true by a "1".

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

REVERSE INITIALIZATION

The Reverse Initialization is similar to the Initialization command and will only work under the condition that it has not already been initialized. The command may be used three ways. The first is to initialize a programmable address device. The second is the first step in assigning a pre-programmed address. The third is to initialize a pre-programmed device.

For the first case this command is sent to address zero with the NV bit set to zero. The command will be received by the next daisy chain device with its bus switch open. Reception of this command will assign the device address and the group number. Reception of this command will also cause the bus switch to close if BS = 1 and no fault is detected.

For the second case the Initialization command is sent the same as the first except that the NV bit is set to one. Reception of the command will assign the device address and the group number and cause the bus switch to close if BS = 1 and there are no faults. A Read/Write NVM command then may be sent to complete the setting of a pre-programmed address.

A pre-programmed device must be initialized by putting its address in both PA3:PA0 and A3:A0 fields.

Once a device has received a reverse initialization command, it will ignore further reverse initialization commands or initialization commands unless it has received a Clear command or undergone a power-up reset.

The command format is found in Table 27.

Table 27. Reverse Initialization Command Format

Data								Address				Command				CRC			
NV	BS	G1	G0	PA3	PA2	PA1	PA0	A3	A2	A1	A0	1	1	1	1	X3	X2	X1	X0

Table 27. Reverse Initialization Command Format

Legend

A[3:0] = Address bits. These bits are the slave address. For programmable devices these bits are all set to zero. For pre-programmed devices these bits contain the pre-programmed address and must match the PA[3:0] bits.

G[1:0] = Group bits. These bits are the group number for the slave. These bits are not used by this device and should be set to "0".

PA[3:0] = Program Address bits. These bits are the address that is to be stored into the slave's address register.

NV = Nonvolatile Memory Write. When set to a one, this bit allows a subsequent NVM command to store a nonvolatile address. When set to a zero, NVM programming is disallowed. Once a permanent address has been stored in the device, setting the NV bit to a one has no effect.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the master.

REVERSE INITIALIZATION RESPONSE

This response message is sent during the next message following a valid Reverse Initialization command to the addressed device. The response is shown in Table 28. Since this is a long-word only command, the short-word response is invalid. No response is generated if the command address field was $0.

Table 28. Reverse Initialization Response Format

High Byte								Low Byte								CRC			
A3	A2	A1	A0	0	0	0	BF	NV	BS	G1	G0	PA3	PA2	PA1	PA0	X3	X2	X1	X0

Legend

A[3:0] = Address bits.The slave address.

BF = Bus Fault. BUSIN short to battery detected.

BS = Controls closing of the Bus Switch (1=close).

G[1:0] = Group bits. Not used on this part, will be set to "0". The group number programmed into the slave.

NV = Nonvolatile Memory Write. The value of the NV bit in the slave.

PA[3:0] = Bus Address to set the device to.

X[3:0] = Cyclic Redundancy Check (CRC). The CRC as calculated by the slave.

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TYPICAL APPLICATIONS
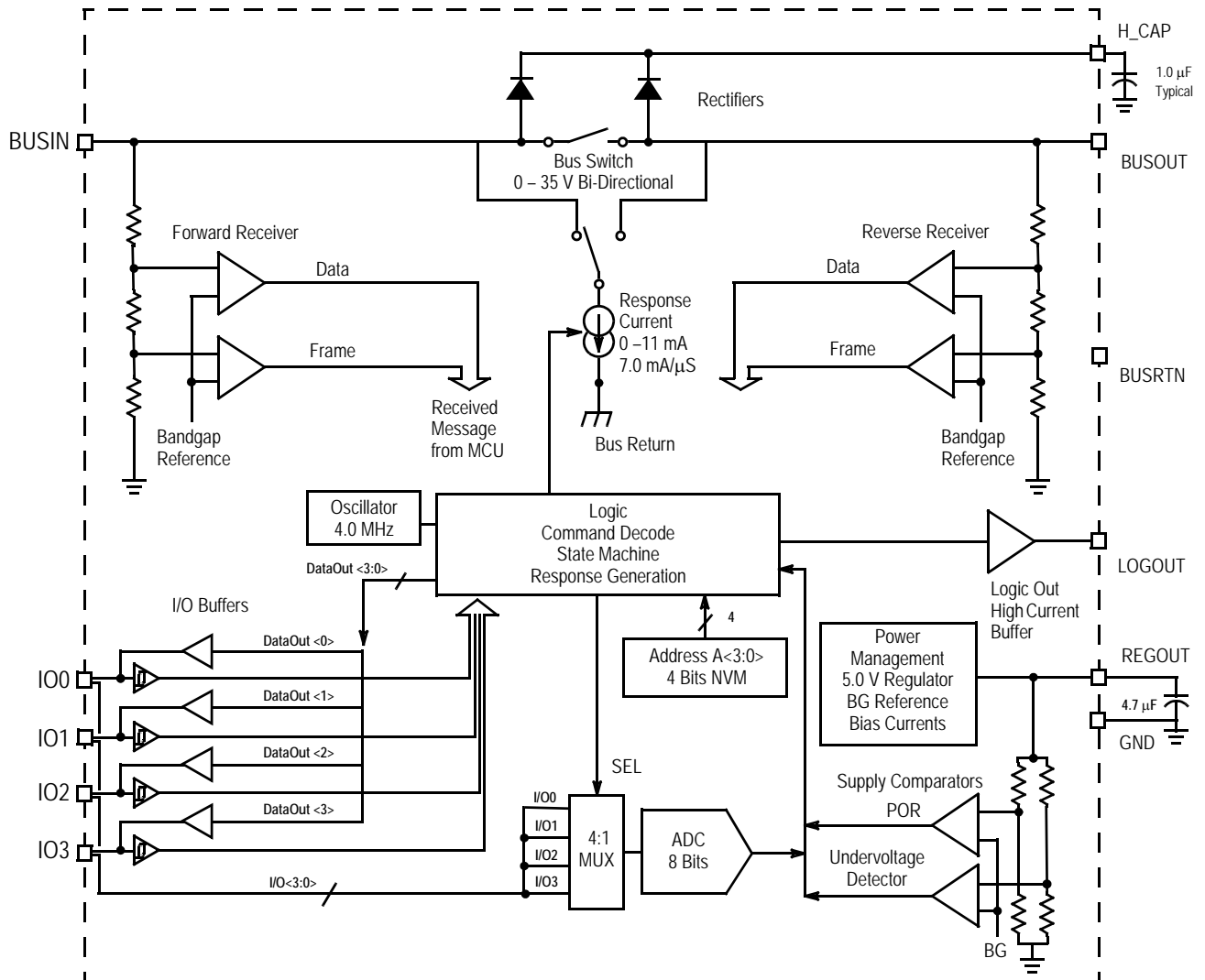
COMMUNICATION FORMAT

DSI messages are composed of individual words separated by a frame delay. Transfers are full duplex. Command messages from the master occur at the same time as responses from the slaves. Slave responses to commands occur during the next command message. This allows slaves time to decode the command, retrieve the information and prepare to send it to the master. A bus traffic example is shown in Figure 6.

The example shows three commands separated by the minimum frame delay followed by a command after a longer delay.
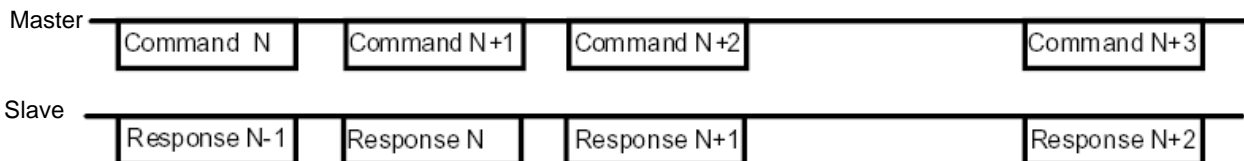
Figure 6. Bus Traffic Example

In case there is a bus error (due to induced noise or a bus fault), both the master and slave devices will read bad data. The slave reacts to bad data by not sending a response during the next frame. The master will detect a CRC error once it receives the corrupted data sent by the slave, and once again when the slave fails to respond. This is illustrated in Figure 7. When this error occurs, the system software needs to acknowledge this condition and resend a command (any command of same size) so that it can receive the

previous response just prior to the bus fault condition (in this case, Command N).

Failure to take corrective action will result in unintended errors as shown in Figure 7. In this case, the master will miss Responses N+1 and N+2 and will mistake them for N+3 and N+4. The master should send another N+1 command after the error is acknowledged to re-synchronize the command-response sequence.
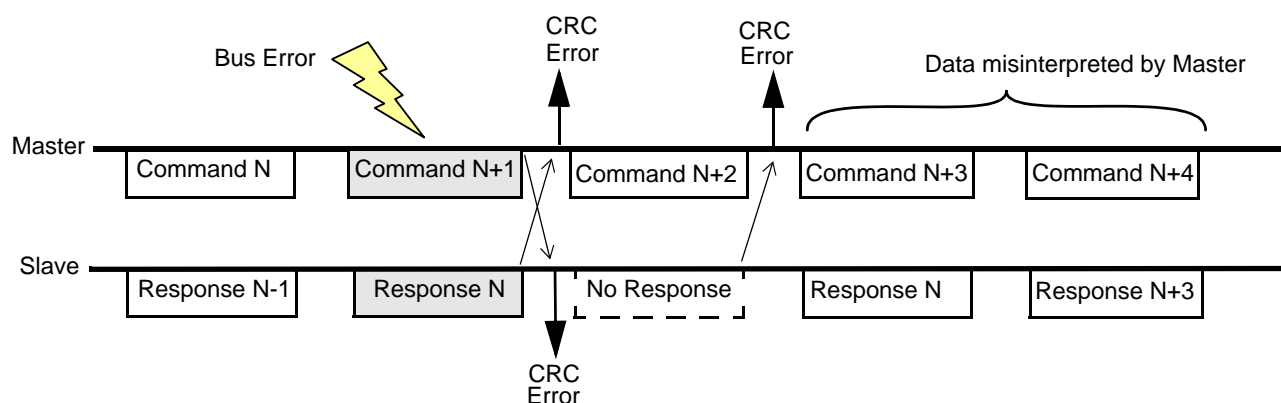
Figure 7. Bus Traffic With Receive Errors (Master Reads Incorrect Data)

POWER UP RESET

When power is first applied to the DSI bus, the system must allow enough time for the internal 5 volt regulator of each device to come up to a proper level. This implies that H_CAP must charge up to V_{RECT} + 5 V, or approximately 6 volts. The time this takes is a function of the size of H_CAP, and the current drive of the Master. The following equation can be used to estimate the minimum time to wait before sending an Initialization Command:

$$t_{MIN} \cong (H\_CAP \times 6V) / I_{CHARGE}$$

where I_{CHARGE} is the charging current provided by the DSI Master.

The above assumes a daisy-chain type of bus topology, and enough time must be allowed for all down-stream devices in the chain to charge up. For example, if device #1 has it's switch closed after its Initialization Command, then the system must wait for device #2 to power up before sending its Initialization Command, and so on down the line.

If the devices are attached in a parallel or point-to-point bus configuration, then the total capacitor value is the sum of all H_CAPS.

In addition to the charge up time, enough time must be allocated for the bus fault test (see next section).

BUS FAULTS

A bus fault is defined as an external voltage on the "Inactive Side" of the Bus Switch that is greater than 3V (typical). *Inactive* refers to the side of the bus that is not yet connected to the bus. Just before a device is Forward Initialized, the inactive side is defined as BUSOUT. Similarly,

just before a device is Reverse Initialized, the BUSIN is defined as the inactive side.

The test for a bus fault is only performed once during Forward or Reverse Initialization (when BS bit is set) by applying an 11mA pull-down current to the inactive side of the Bus Switch and monitoring the voltage. The fault test takes approximately 200uS. If no fault is detected, the bus switch will be closed, and if a fault is detected, the bus switch will not close. The fault test applies to both programmed and unprogrammed devices.

Exception: In the case of a daisy-chain bus topology where the last device BUSOUT line connects to BUSIN of the first device (loop-back), then the fault test will NOT be executed since both BUSIN and BUSOUT are connected to active busses. It is up to the system software to run the appropriate diagnostic tests to resolve this special case. (One alternative is to use a separate DSI Master to handle the loop-back signal path. This second DSI Master is only activated in the case of a bus fault so that the last device can be accessed by means of a reverse initialization.)

GLOBAL ADDRESS 0

Any time an Initialization or Reverse Initialization command is sent to the 33793 with an address of 0x0 (global address), the device behaves as follows:

- Device initializes to address 0.
- Bus switch remains open. This implies that in a daisy-chain bus topology, all devices past the first device will remain off.
- NV and BS bits are not stored and have no effect.

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- Device will respond to further commands at address 0 (such as setting and clearing the I/O bits and LOGOUT) but there is no response (Master will read all zeros). If the devices are connected in a daisy chain, then only the fist device will respond.
- Subsequent writes to re-initialize the device will not be possible until the device is cleared.

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PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the "98A" listed below.
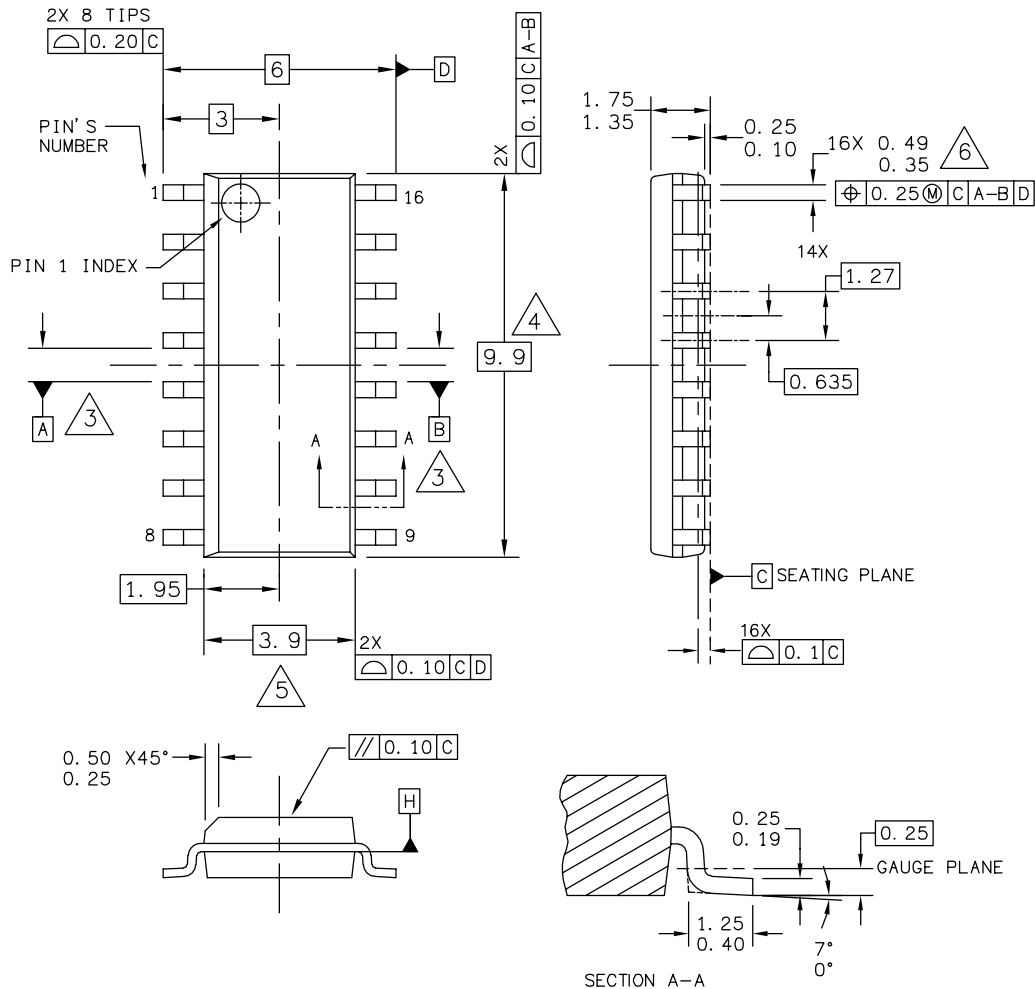
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TITLE: 16LD SOIC N/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42566B	REV: M	
	CASE NUMBER: 751B-05	06 FEB 2006	
	STANDARD: JEDEC MS-012AC		

EF SUFFIX
(PB-FREE)
16-PIN PLASTIC PACKAGE
98ASB42566B
ISSUE M

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
12.0	8/2006	• Implemented Revision History page • Converted to Freescale format • Added PC33793EF • Added Feature bullets • Rewrote and enhanced Device Operation - No electrical changes • Updated to the prevailing Freescale form and style • Removed PC33793EF and replaced with MCZ33793EF/R2 in the Ordering Information block
13.0	11/2006	• Added MCZ33793AEF/R2 to the Ordering Information • Added Device Variations table on page 2 • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 5. Added note with instructions to obtain this information from www.freescale.com.

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