The DLX713X, 5x7 Dot Matrix Intelligent Display® Device Appnote 25

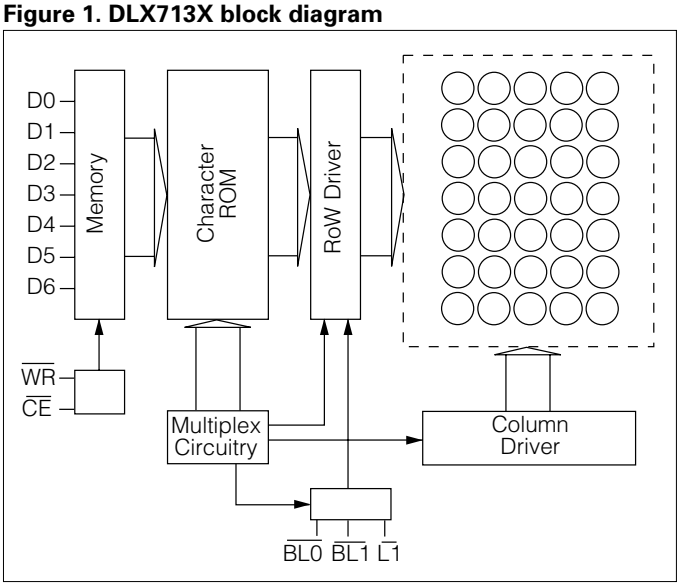
This application note is intended to serve as a design and application guide for users of the DLO7135 and DLG7137 OSRAM Intelligent Displays. This appnote covers device electrical description, operation, general circuit design considerations and interfacing to microprocessors.

Electrical Description

The DLX713X intelligent alphanumeric 5x7 dot matrix display contains memory, character generator, multiplexing circuits, and drivers built into a single package.

Figure 1 is a block diagram of the DLX713X. The unit consists of 35 LED die arranged in a 5x7 pattern and a single CMOS integrated circuit chip. The IC chip contains the column drivers, row drivers, 128 character generator ROM, memory, multiplex and blanking circuitry.

Figure 1. DLX713X block diagram



Package

Thirty-five dots form a 0.48 x 0.68 inch overall c
a 0.700 x 0.800 inch dual-in-line package. The ±5
viewing angle complements the large display ar
display for industrial control applications. Display
filled reflector type with the intregrated circuit in
filled with IC-grade epoxy. This results in a very
which is resistant to moisture, shock, and vibrat

Figure 2. Physical dimensions in inches (mm

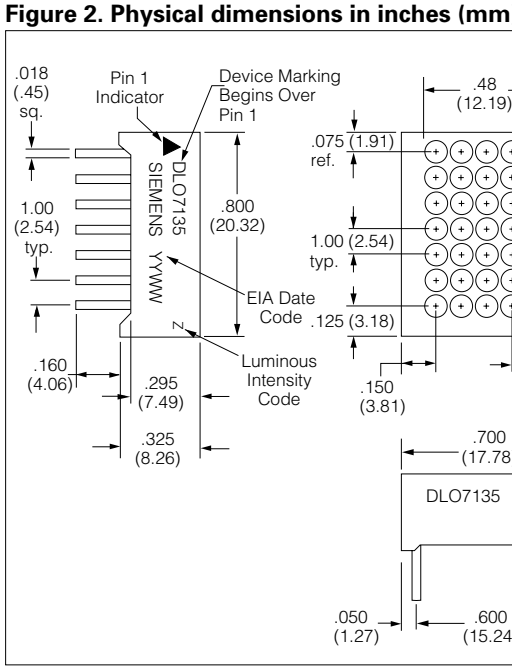


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Table 1. Electrical inputs

Pin	Name	Pin	Name
1	V_{CC}	14	D6 data input (MSD)
2	$\overline{LT}$ lamp test	13	D5 data input
3	$\overline{CE}$ chip enable	12	D4 data input
4	$\overline{WR}$ write	11	D3 data input
5	$\overline{BL1}$ brightness	10	D2 data input
6	$\overline{BL0}$ brightness	9	D1 data input
7	GND	8	D0 data input (LSD)

Table 2. Pin description

V_{CC}	Positive Supply +5 V
GND	Ground
D0–D6	Data Lines, see Figure 3 (Character set)
$\overline{CE}$	Chip Enable (active low) Determines which device in an array will accept data
$\overline{WR}$	Write (active low) Data and chip enable must be present and stable before and after the write pulse (see DLX713X data sheet for timing)
$\overline{BL0}$, $\overline{BL1}$	Blanking Control Input (active low) Used to control level of display brightness
$\overline{LT}$	Lamp Test (active low) Causes all dots to light at 1/2 brightness

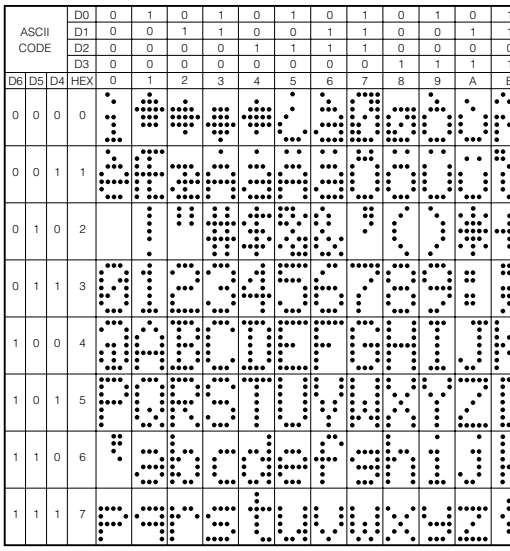
Operation

In a dot matrix display system, it is advantageous to use a multiplexed approach with 12 drivers (5 digit plus 7 segments) rather than 35 segment drivers, reducing the number of drives and interconnections required. A multiplexed system must be a synchronous system or the digits or elements may have different on (lit) times and therefore varying brightness.

The DLX713X is an internally multiplexed display but the data entry is asynchronous. Loading data is similar to writing into a RAM. Present the data, select the chip, and give a write signal. For a multidigit system, each digit has its own unique location and will display its contents until replaced by another code.

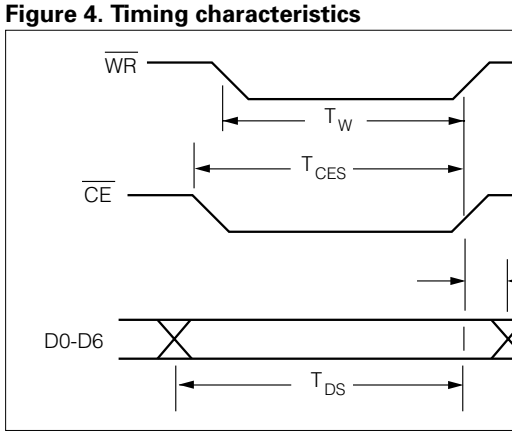
The waveforms of Figure 4 demonstrates the relationship of the signals required to generate a write cycle. Check the data sheet for minimum values required for each signal.

Figure 3. Character set



1. High=1 level. 2. Low=0 level.

Figure 4. Timing characteristics



Display Blanking and Dimming

The DLX713x Intelligent Display has the capab
levels of brightness plus blank. Figure 5 shows
tion of $\overline{BL0}$ and $\overline{BL1}$ for the different levels of b
$\overline{BL0}$ and $\overline{BL1}$ inputs are independent of write a
and does not affect the contents of the interna
flashing display can be achieved by pulsing the
at a 1–2 hertz rate. Either $\overline{BL0}$ or $\overline{BL1}$ should be
light up the display.

Table 3. Dimming and blanking control

Brightness Level	$\overline{BL1}$
Blank	0
1/7 brightness	0
1/2 brightness	1
full brightness	1

Lamp Test

The lamp test when activated causes all dots on the display to be illuminated at 1/7 brightness. It does not destroy any previously stored characters. The lamp test function is independent of chip enable, write, and the settings of the blanking inputs.

This convenient test gives a visual indication that all dots are functioning properly. Because lamp test does not affect the display memory, it can be used as a cursor or pointer in a line of displays.

General Design Considerations

When using the DLX713X on a separate display board having more than six inches of cable length, it may be necessary to buffer all of the input lines. A non-inverting 74LS244 buffer can be used. The object is to prevent transient current into the DLX713x protection diodes. The buffers should be located on the display board and as close to the displays as possible.

Because of high switching currents caused by the multiplexing, local power supply bypass capacitors are also needed in many cases. These should be 10 volt, tantalum type having 10 uf capacitance. The capacitors may only be required every 2 displays depending on the line regulation and other noise generators.

Decoupling capacitors should also be used across V_{CC} and ground of each display. Typical value of these capacitors is 0.01 mF/10 V.

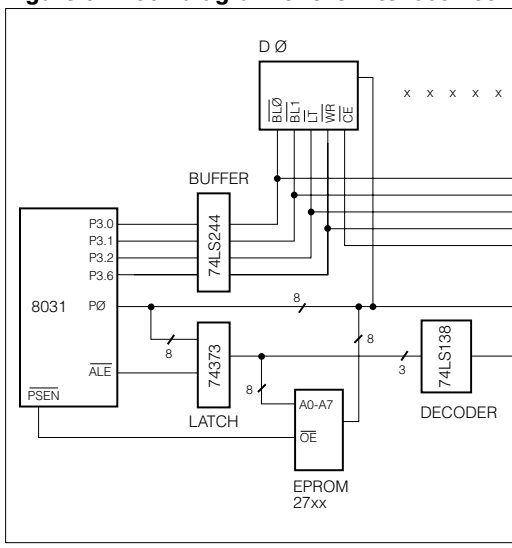
If small wire cables are used it is good engineering practice to calculate the wire resistance of the ground and the +5 volt wires. More than 0.2 volt drop (at 100 ma per digit) should be avoided, since this loss is in addition to any inaccuracies or load regulation of the power supply.

The 5 volt power supply for the DLX713X should be the same one supplying the V_{CC} to all logic devices. If a separate supply must be used then local buffers should be used on all the inputs and these buffers should be powered from the display power supply. This precaution is to avoid line transients or any logic signals to be higher than V_{CC} during power up.

Interfacing

For an eight digit display using the DLX713X, int
single chip microprocessor is easy and straight

Figure 5. Block diagram of the Intel 8031 con



Conclusion

Note that although other manufacturers' product
the examples, this application note does not imp
endorsement, or warranty of other manufacturer
OSRAM. The interface schemes shown demons
plicity of using the DLX713X dot matrix Intelligen
timing differences may be encountered for variou
sors, but can be resolved similar to those encour
using different RAM's. The techniques used in th
were shown for their generality. The user will und
other schemes to optimize his particular system
ments.

Program Listing

```
1                                       ; BY DAN WATSON
2                                       ; TO DO LAMP TEST,SET 100% BRIGHTNESS
3                                       ; AND WRITE 'SIEMENS*'
4
5                                       ; P3.0 = BLO\
6                                       ; P3.1 = BL1\
7                                       ; P3.2 = LT\
8                                       ; P3.6 = WR\
9
10                                      ; RO = DIGIT ADDRESS ( CHIP ENABLES – CE\ )
11                                      ; R1 = DIGIT COUNTER
12                                      ; R7 = R6 = R5 = WAIT REGISTERS
13
14      0000                            .ORG 00H
15      0000    02 00 03                    INIT:JMP BEGIN
16      0003    12 00 24                    BEGIN:CALL WAIT1            ; DELAY FOR uC TO STABILIZE
17      0006    75 B0 00                        MOV P3,#00H             ; LAMP TEST
18      0009    12 00 24                        CALL WAIT1              ; DISPLAY LT\ FOR A WHILE
19      000C    75 B0 07                        MOV P3,#07H             ; SET ALL 8 DISPLAYS TO 100% B
20      000F    00                              NOP
21      0010    00                              NOP
22      0011    78 00                           MOV R0,#00H             ; DIGIT 7 ADDRESS
23      0013    79 08                           MOV R1,#08H             ; 8 DIGIT COUNTER
24      0015    74 00                           MOV A,#00H              ; CLEAR ACC.
25      0017    90 00 37                        MOV DPTR,#TEXT          ; ADDRESS OF THE MESSAGE
26      001A    93                          WRT:MOVC A,@A+DPTR          ; LOAD FIRST CHAR. INTO THE AC
27      001B    F2                              MOVX @R0,A              ; DIGIT ADDRESS AND DATA WRI
28      001C    A3                              INC DPTR                ; NEXT CHARACTER ADDRESS
29      001D    08                              INC R0                  ; NEXT DIGIT (6) ADDRESS
30      001E    E4                              CLR A
31      001F    D9 F9                           DJNZ R1,WRT             ; WRITE ALL 8 CHAR.
32      0021    00                          GO:NOP
33      0022    01 21                           JMP GO                  ; MESSAGE ALWAYS ON
34      0024
35      0024
36      0024    7F 88                       WAIT1:MOV R7,#88H           ; DELAY LOOPS
37      0026    00                              NOP
38      0027    7E FF                       WAIT2:MOV R6,#FFH
39      0029    00                              NOP
40      002A    7D FF                       WAIT3:MOV R5,#FFH
41      002C    00                              NOP
42      002D    DD FE                           DJNZ R5,$
43      002F    00                              NOP
44      0030    DE F8                           DJNZ R6,WAIT3
45      0032    00                              NOP
46      0033    DF F2                           DJNZ R7,WAIT2
47      0035    00                              NOP
48      0036    22                              RET
49
50      0037    53 49 45 4D 45          TEXT:DB 'SIEMENS*'
        003C    4E 53 2A
51      003F
52      003F                            .END
```