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SSI 32H6811/6811B
Servo Motor Speed 5V Driver/DACs

Advance Information

May 1994

DESCRIPTION

The SSI 32H6811/6811B Servo and MSC Drivers, a CMOS monolithic integrated circuit housed in a 64-lead TQFP package, operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor commutator with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The commutator in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. It also includes two 10-bit D/A converters, with a serial interface to commonly used μP or DSP, for commanding the servo positioner and the spindle motor respectively. The device is ideal for use in 5V small-form disk driver applications.

FEATURES

- **Internal 1.0A servo driver with no deadband, class-B output**
- **Thermal overload protection**
- **Power fault detection with built-in retract circuitry**
- **10-bit VCM D/A converter with 4 μs digital delay**
- **Gain select switch for a wide dynamic range of servo inputs**
- **Internal precision voltage reference**
- **Programmable commutation delay for optimal motor efficiency**
- **10-bit MSC D/A converter with 4 μs digital delay**
- **Internal 1.0A spindle driver**
- **Switch-mode current limiting for spindle motor start-up**
- **Serial interface compatible with 80C196 and 68HC16**
- **Low power CMOS design with Sleep and Power Saving modes**
- **64-lead TQPF package**

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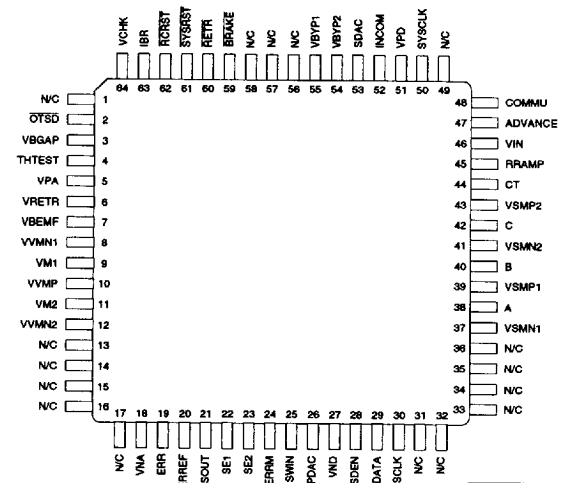
PIN DIAGRAM



64-LEAD TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

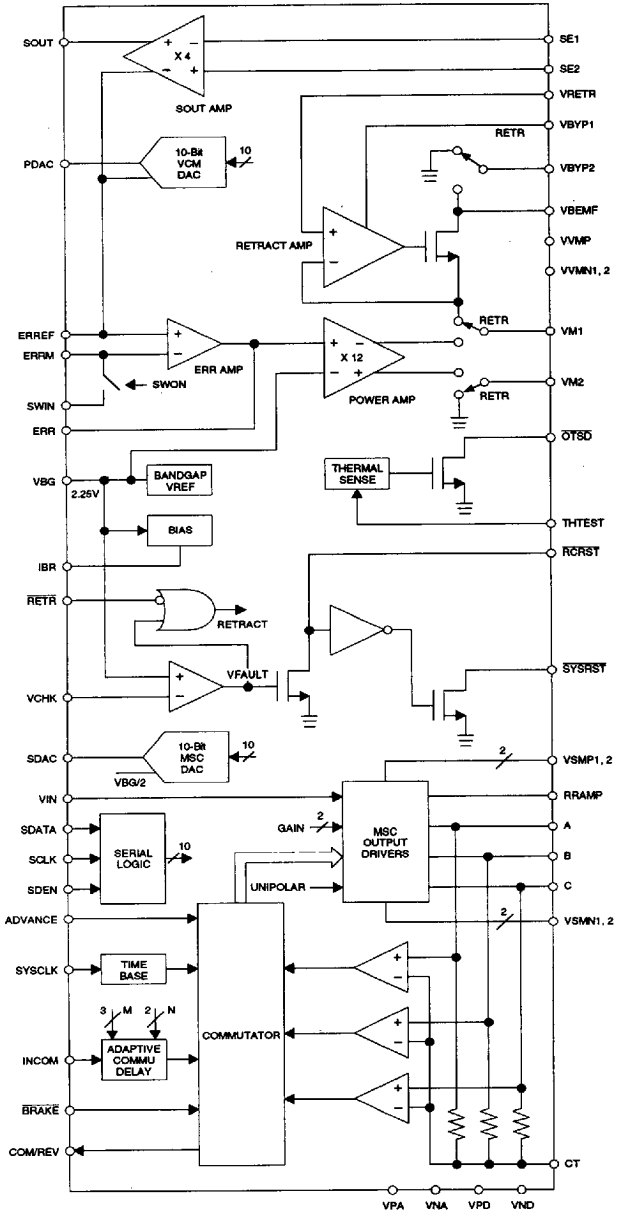


FIGURE 1: SSI 32H6811/6811B Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H6811 can be divided into four major sections: Servo positioner, Spindle motor commutator/driver, Control circuitry and Serial interface port.

Servo Positioner

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two Primary modes of operation, normal (or linear) and retract. The Retract mode is activated by a power supply failure or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high. Otherwise the device operates in Linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier and 10-bit VCM D/A converter.

SOUT Amplifier

The SOUT amplifier generates a voltage at SOUT, proportional to positioner current, by sensing the voltage across Rs, amplifying and referencing to ERREF. Since the Common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with a high input common mode rejection and low input offset.

ERR Amplifier

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

Power Amplifier

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP.

Retract Amplifier

When a voltage fault is sensed, or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high, the servo positioner enters into Retract mode. In this mode, it is assumed that no current is available for VVMP. Thus power for this mode comes from VBEMF, the rectified spindle back emf voltage, and from VBYP1, a voltage generated from an external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

VCM D/A Converter

Switched-capacitor circuit technique is employed to implement the VCM D/A converter with two non-overlapped clock phases, one phase for auto-zeroing and another one for evaluation. These two phases run synchronously with an internal 500 kHz clock, which is derived directly from the system clock at SYSCLK.

The request of the VCM D/A converter is initiated by writing to the VCM D/A register (00) through the serial interface port. The input data word must be coded in two's complement form. Note that there would be a maximum of 2 µs of latency between a conversion request and the actual start of conversion. The conversion delay from the actual start of conversion to when the analog output begins to slew to a new value is 2 µs. Therefore a maximum of 4 µs is required for a conversion in addition to the time needed for completion of a serial data transfer, which is equal to 16/SCLK.

The VCM D/A converter provided at PDAC is referenced to ERREF, which also serves as a reference voltage for the error amplifier and the current sense amplifier.

Spindle Motor Commutator/Driver

The spindle motor commutator in conjunction with external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors. The speed regulation control loop is completed with a µP or DSP external to this device.

Commutator

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back EMF from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back EMF is compared with a reference at CT and initiates commutation "events" when the appropriate comparison is made. Commutation is the sequential switching of drive cur-

rent to the motor windings. Because the back EMF comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. There are two modes of commutation delay, namely adaptive or one-shot, which can be selected via the M, N bits in the MODE1 register (10) per Table 1. In Adaptive mode (default), the commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents the circuit from responding back EMF comparison events for a period of time equal to the maximum of 5/7 of the interval between events and 64 µs after the comparison event. INCOM pin can be selected as a test pin if it is high impedance, otherwise it should be selected as "IN" for the Adaptive mode to work properly.

In one-shot mode, an input voltage at INCOM pin will provide a fixed delay and noise blank. For start-up, INCOM = VDD/2 is recommended; delay will be about 500 microseconds and noise blank about 850 microseconds. The commutation table is described in Table 2.

Motor speed control may be accomplished by measuring the period of the output signal at COM/REV. COM/REV may be defined as COMMU, the LSB of the commutation counter; REVCLK, the revolution clock of the motor; or RAWCOM, the back EMF comparator output. These are selected by the COMMUX0 and the COMMUX1 bits.

Transconductance Amplifier

Input pin VIN is the non-inverting input of a transconductance amplifier which uses the lower driver transistor, that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the current flowing through the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 5, 10, 20 or 30 selected by the GAIN bits in the MODE1 register) and fed to the inverting input of the transconductance output stage.

The 10-bit MSC D/A converter, referenced to VBG/2, is provided at SDAC for converting the commanding signal in digital format into an analog voltage. Its operation is similar to the VCM D/A converter, but is initiated by writing to the MSC D/A register (01) in two's complement form.

Power Amplifier

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pullup to VSMP1 or VSMP2 and one for pulldown to VSMN1 or VSMN2. The pullup FET functions as a switch (1.5Ω maximum) with voltage rise and fall times of about 25 microseconds. The pulldown FET is a part of the transconductance amplifier which converts the voltage VIN into motor current (Imotor = VIN/(Rsense • Av), where Av is either 5, 10, 20 or 30). When the pulldown output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per microseconds, where RRAMP is measured in kΩ.

TABLE 1: Modes of Commutation Delay

MODE1 REGISTER (10) M	N	SWITCH MODE	DELAY MODE	INCOM PIN
0	0	NO	Adaptive	Test (default)
0	1,2	NO	Adaptive	In
0	3	NO	One shot	In
>0	X	YES	One shot	In

Motor Start-Up

Motor starting is accomplished by a companion µP or DSP via ADVANCE, $\overline{\text{RETR}}$, $\overline{\text{BRAKE}}$ and COM/REV. The µP can assert $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ low to initialize the commutation counter and then increment the counter with ADVANCE. After $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ are asserted low and de-asserted (the power-up condition for preparation to begin a starting sequence), the commutation state will be state 0 per Table 2, but the lower driver output B remains inactive to prevent current flowing through the motor (out of A which is high). On the first ADVANCE set high, the commutation state 1 is selected and the drivers are per Table 2. ADVANCE at logic high excludes internal commutations. COM/REV provides feedback to the µP on motor activity.

Switch-Mode Operation

Switch-mode operation is provided for limiting the motor current during motor start-up. Two values M and N, loaded into the MODE1 register (10) through the serial interface, determines the basic switching parameters for the operation. The M (3 bits) sets the minimum "on" time of the lower drivers and sample delay time. The N (2 bits) sets the switching period. The timing is given by:

Minimum "on" time = (M+1) • 4 µs

Sample delay time = M • 4 µs

Switching period = (N+2) • (M+1) • 4 µs

Hence, Minimum duty cycle = 1/(N+2)

Sample delay time, defined as the time from turning the lower drivers "on" until switching transients have settled, is a function of the particular application and will be determined by the user.

The value of M=0 is defined as Linear mode, no switching except normal commutation will occur.

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TABLE 2: Commutation States

STATE	COMMU	Pulldowns A	Pulldowns B	Pulldowns C	Pullups A	Pullups B	Pullups C
0	0	OFF	ON	OFF	ON	OFF	OFF
1	1	OFF	OFF	ON	ON	OFF	OFF
2	0	OFF	OFF	ON	OFF	ON	OFF
3	1	ON	OFF	OFF	OFF	ON	OFF
4	0	ON	OFF	OFF	OFF	OFF	ON
5	1	OFF	ON	OFF	OFF	OFF	ON

TABLE 3: Modes of Operation

STANDBY	$\overline{\text{OTSD}}$	VCHK > VBG	$\overline{\text{RETR}}$	$\overline{\text{BRAKE}}$	Mode	VCM Analog	SPM Analog	VCM Driver	SPM Driver
x	0	x	x	x	Shutdown	OFF	ON	Float	Float
x	1	0	x	0	Fault/Brake	OFF	OFF	Retract	Low Z
x	1	0	x	1	Fault/Retract	OFF	OFF	Retract	Float
x	1	1	0	0	Sleep	OFF	OFF	Float	Float
x	1	1	0	1	Retract	OFF	ON	Retract	Float
x	1	1	1	0	Brake	OFF	ON	Float	Low Z
0	1	1	1	1	Run	ON	ON	Active	Active
1	1	1	1	1	Standby	OFF	ON	Retract	Active

Switch-Mode Operation (continued)

For a proper switch-mode operation, three flyback diodes from outputs A, B, and C, and a blocking diode from the system power supply VCC to the VSMP1 and VSMP2 pins are required. The flyback diodes will provide power for retract (during power failure) at pins VSMP1 and VSMP2.

Control Circuitry

The control circuitry consists of a power fault detector, a thermal overload circuit, and control logic. The inputs to the control circuitry are VCHK, $\overline{\text{RETR}}$, $\overline{\text{BRAKE}}$, and the STANDBY bit in MODE2 register, along with the internal signals from the thermal overload detector. The voltage fault detector monitors the system power supply VCC to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG.

Five operating modes are selected via $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ (when the system power supply is present) per Table 3. With $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ asserted low, both VCM and SPM drivers are in a high impedance state, and analog circuits are de-biased. This is the "Sleep" mode. With $\overline{\text{RETR}}$ asserted, $\overline{\text{BRAKE}}$ de-asserted, both VCM and SPM drivers are in a high impedance state, and the retract amplifier is activated and powered by the back emf of a spinning motor for retracting heads. For $\overline{\text{BRAKE}}$ asserted, and $\overline{\text{RETR}}$ de-asserted, the VCM drivers are in a high impedance state, the SPM driver outputs are low impedance to ground (without current limiting). Normal mode is given for $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ de-asserted and the STANDBY bit is low. When the STANDBY bit is high with $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ de-asserted, the VCM driver is in retract while the SPM driver remains active. Notice that whenever VCM drivers are in either Retract or Float mode, the VCM analog circuitry is turned off except the retract amplifier.

When a power failure is sensed, the $\overline{\text{SYSRST}}$ is asserted low and the Retract mode is activated. If the die temperature exceeds approximately 135°C, the $\overline{\text{OTSD}}$ is asserted low and all output drivers (both VCM and SPM) are turned off. The drivers will become operative after the temperature is reduced and the ADVANCE is asserted high.

Serial Interface Port

A synchronous serial port, compatible with the commonly used µP such as 80C196 and 68HC16, is used to input digital words for D/A converters and mode registers. It is shift register based I/O interface and consists of three pins SDEN, SCLK and SDATA. Data from uP is transferred 8 bits (one byte) at a time with the LSB first. A complete transfer requires two bytes which are formatted into an instruction and a data field.

Data received through SDATA is clocked into an internal 16-bit shift register at the rising edge of SCLK while SDEN is active high. At the end of each transfer, SDEN must return low. If SDEN remains high after the last bit (which is the MSB of the second byte) is received, any additional data on SDATA will be ignored. Data must be two bytes for each transfer. If, for any reasons, SDEN is brought low prior to the completion of the second byte, the write operation of the data will be aborted.

The instruction field includes the first six bits of the first byte and is defined per the table below. The data field is 10-bit wide and includes the last two bits of the first byte and the second byte.

TABLE 4: COMM/REV Selection Modes

COMMUX1	COMMUX0	COM/REV Selection
0	0	LSB of commutation state counter (default)
0	1	Revolution clock
1	X	Back EMF comparator output RAWCOM

REGISTER DESCRIPTION

BIT	NAME	DESCRIPTION
0 (LSB)	R/W	Read/Write control. It must be '0' for this device since all of its registers are write only.
1, 2, 3	DID0..2	Device ID. These three bits define the SSI device for which the serial communication is to be established. '111' is designated for this device.
4, 5	ADDR0..1	Register address. These two bits define the internal register to which data is transferred. ADDR1 / ADDR0 / Register 0 / 0 / VCM D/A 0 / 1 / MSC D/A 1 / 0 / MODE1 1 / 1 / MODE2
The MODE1 register (10) is defined as:		
0	SWON	Analog switch enable
1, 2	GAIN0, 1	Sense amplifier gain select GAIN1 / GAIN0 / Gain 0 / 0 / 30 (defaut) 0 / 1 / 20 1 / 0 / 10 1 / 1 / 5
3	UNIPOLAR	Unipolar mode enable
4	N0	LSB of N value - Combinations of N and M will determine the modes of commutation delays and basic switching mode operation parameters. (See Table 1).
5	N1	MSB of N value
6	M0	LSB of M value
7	M1	M value
8	M2	MSB of M value.
9	COMMUX0	Works with COMMU1 in MODE2 register as shown in Table 4.
The MODE2 register (11) is defined as:		
0	COMMUX1	Works with COMMUX0 in MODE1 register as shown in Table 4.
1	STANDBY	Standby mode control bit, see Table 3.

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	-	Analog positive supply.
VNA	-	Analog ground.
VPD	-	Digital positive supply. It should be shorted externally with VPA.
VND	-	Digital ground. It should be shorted externally with VNA. VND is also the low side input to the current sense amplifier of the spindle motor and thus care should be taken to keep VND and the low side of the external resistor Rsense at the same potential.
VVMP *	-	Positive supply used for voice coil motor.
VVMN1, 2	-	Negative supply used for voice coil motor.
VSMP1, 2	-	Positive supply used for spindle motor.
VSMN1, 2	-	Negative supply used for spindle motor. They are also the high side inputs to the current sense amplifier of the spindle motor.

* The circuit board contacts for VVMP, VVMN1, VVMN2, VSMP1, VSMP2, VSMN1, and VSMN2 must be sized in accordance with anticipated motor currents. All pins must be connected with low resistance circuit board traces.

SERVO POSITIONER

SWIN	I	The analog switch input. The other side of the switch is connected to ERRM.
ERRM	I	The inverting input of the error amplifier.
ERREF	I	The reference voltage for the error amplifier, the VCM D/A converter and the current sense amplifier.
ERR	O	The error amplifier output. ERR is to provide compensation to the transconductance loop and is reference to VBG.
SOUT	O	The current sense amplifier output. SOUT is referenced to ERREF.
VRETR	I	The retract voltage. It must be provided externally at VRETR pin.
VBYP1	I	The bypassed power supply. An external voltage for Brake and Retract circuits. An external capacitor is connected to this pin and BYP2 and an internal circuit will charge this pin to Vdd. The charge stored on this external capacitor is used by Brake and Retract circuits when Vdd is removed (power-off). The capacitor must hold sufficient charge during the period when Vdd is lost while retract is taking place (20 to 50 milliseconds) so it will have enough voltage to drive the outputs during braking. Very little current is used during power-off braking so that the external capacitor C can be chosen from the retract conditions: $C \geq T_{RETRACT} \bullet I_{VBYP}$ (Float mode)/0.5V or approximately: $C \geq 40E\text{-}6 \bullet T_{RETRACT}$ This pin is normally a diode drop below Vdd, rising by VBEMF during retract.

SERVO POSITIONER (continued)

NAME	TYPE	DESCRIPTION
VBYP2	I	The other side of the bypass capacitor is connected to this pin. It is normally at ground, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This input provides current to the internal retract power amplifier.
VM1	O	One side of the voice coil motor.
VM2	O	The other side of the voice coil motor and sense resistor combination.
SE1,SE2	I	The voltage across the sense resistor for the voice coil motor current.
$\overline{\text{RETR}}$	I	When asserted low, it forces a retract. Refer to Table 3.
PDAC	O	The 10-bit VCM D/A converter output. It is referenced to ERREF.

SPINDLE MOTOR COMMUTATOR/DRIVER

SYSCLK	I	System clock input. SYSCLK is internally divided by a divider to generate an internal clock. SYSCLK is nominally 8 MHz resulting in a 4 MHz internal clock. Varying SYSCLK, varies the internal clock. SYSCLK values between 6 and 10 MHz are possible.
COM/REV	O	Multiplexed output signal of COMMU, REVCLK, or RAWCOM selected through COMMUX1 and COMMUX0 bits, see Table 4.
ADVANCE	I	ADVANCE is used to increment the commutation counter externally. The rising edge of ADVANCE will increment the counter by 1. When held high, it inhibits the counter from internal incrementing. When held low, it permits the normal operation of commutation from back emf events.
INCOM	I	Commutation delay control. Adaptive commutation delay may be adjusted from its nominal value of one half the commutation interval by sinking or sourcing current from this pin. This should be done via an external control loop which can compensate for the range of internal circuit parameter variations.
SDAC	O	The 10-bit MSC D/A converter output. It is referenced to VBG/2.
VIN	I	Control voltage input. The combination of the MOSFET drivers and the predriver circuit forms a transconductance amplifier which sets the motor current in relation to VIN. In conjunction with Rsense connected at VSMN and the gain of the sense amplifier, the transconductance is defined by: Gm = Im/VIN = 1/Rsense • gain, gain = 5, 10, 20, 30
A, B, C	O	Spindle motor driver outputs.
CT	I	Back emf input from spindle motor coil center tap. Internal circuit uses the back emf voltages to determine the rotor position and effect commutation.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPA to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is approximately given by the relationship: dv/dt=15/RRAMP, where dv/dt is expressed in volts/µs and RRAMP in kΩ.
$\overline{\text{BRAKE}}$	I	$\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of fault-induced head retract and spindle motor braking. A capacitor to ground and a resistor to $\overline{\text{SYSRST}}$ are selected such that 1.2RC is equal to the maximum time required for retract.

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CONTROL CIRCUITRY

NAME	TYPE	DESCRIPTION
VCHK	I	Comparator input for power supply monitoring. When VCHK is below VBG, an internal voltage fault is generated.
VBG	O	Voltage reference, generated from the internal bandgap voltage, for use with the power supply monitor comparator.
IBR	O	A resistor is tied from this pin to ground to establish a bias current for internal circuitry.
$\overline{\text{RCRST}}$	O/C	This pin serves the dual purpose of providing power-on-reset and stretching short internal VFAULT pulses to a width suitable for the host micro controller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse. If $\overline{\text{RCRST}}$ is pulled low by external circuitry, this device will pull $\overline{\text{SYSRST}}$ low.
$\overline{\text{SYSRST}}$	O/C	When low, this open-collector output indicates that an internal voltage fault has occurred.
$\overline{\text{OTSD}}$	O/C	Thermal shut-down. When low, this open- collector output indicates that the junction temperature has exceeded the recommended operating range and the device is in thermal shut-down. In thermal shut-down, all output drivers are turned off and analog circuit de-biased.
THTEST	I	Biased low with an internal pull-down. When asserted high, $\overline{\text{RETR}}$ will be connected to the thermal overload test circuitry for use as a test input.

SERIAL INTERFACE PORT

SDATA	I	Serial data input passing digital words for internal registers.
SCLK	I	Serial data timing reference. The rising edge of the SCLK is to strobe SDATA while SDEN is asserted high.
SDEN	I	Serial data transfer enable. When active high, the serial data transfer is enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER		RATING
Supply voltage @ VPA, VPD, VVMP, VSMP1, VSMP2	Vdd	-0.3 to 7.0V
Motor current @ A, B, C, VM1, VM2	Imax	±1.0 A
Max Output Current Duration	Ta = 70°C Output Current = 1.0 A	8 seconds
Input voltage @		
	CT, A, B, C, VBEMF, VBYP1, VBYP2	-0.3 to 12.0V
	VM1, VM2, SE1, SE2	-0.3 to 7.0V
	Other pins	-0.3 to (Vdd + 0.3)V
Storage temperature	Tstg	-65 to 150°C
Lead temperature (10 sec duration)	Tlead	0 to 300°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage	Vdd		4.5		5.5	V
Supply current						
VPA,VPD	Idd				20	mA
Sleep mode	Isleep				2.0	mA
Standby mode	Istandby				15	mA
VBYP1,braking	Ibrk				10	µA
VBYP1,retract	Iret				20	µA
Input voltage @ VBEMF	VBEMF		1.0		10	V
Input voltage @ ERREF	ERREF		0.5	VBG	Vdd-2.0	V
Input voltage @ VIN	VIN		0		2.5	V
Input voltage @ VSMN	VSMN		0		0.5	V
ADVANCE active low pulse width			0.1		12	µs
Ambient temperature	Ta		0		70	°C
Capacitive load on digital outputs	Cl				100	pF

RECOMMENDED OPERATING CONDITIONS (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Analog output load	Cl				40	pF
	Rl		10			kΩ
System clock						
Frequency tolerance	*fc*		6		10	MHz
Pulse width	Twh, Twl		40			ns
Biasing resistor Rbias = 22.6 kΩ	Rbias		22		24	kΩ
External resistors	Rf,Rc		10			kΩ

PERFORMANCE SPECIFICATIONS

DIGITAL I/O

Digital input @ SDATA, SCLK, SDEN, ADVANCE, SYSCLK, $\overline{\text{RETR}}$	Vil		0.8			V
	Vih				2.0	V
	Iil, Iih				±1	µA
Digital input @ $\overline{\text{BRAKE}}$	Vil		1.2			V
	Vih				2.4	V
	Iil, Iih				±1	µA
Digital O/C output @ $\overline{\text{RCRST}}$,	Ioh	Voh = Vdd			1	µA
$\overline{\text{SYSRST}}$, $\overline{\text{OTSD}}$	Iol	Vol = 0.4	4			mA
Digital Output @ COM/REV	Vol	Iol = 2.0 mA			0.4	V
	Voh	Ioh = -100 µA	2.4			V

SERVO POSITIONER

The following VCM performance specifications are measured with 16Ω resistive load and 0.5Ω sense resitor for 8 MHz SYSCLK, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BEMF current					
Normal mode	VBEMF = 4V			300	µA
Retract mode	VBEMF = 3V, Power off VRETR = 0.5V, VBYP1 = 4V			20	µA
SOUT amplifier					
Gain		3.9		4.1	V/V
Input offset	SOUT = ERREF	-3		3	mV
Output swing	R_L = 10 kΩ to ERREF	0.15		Vdd-1	V
ERRAMP amplifier					
Input offset	ERR = ERRM			±15	mV
Output swing		0.15		Vdd-1.25	V
Gain		60			dB
Unit Gain Bandwidth		1			MHz
Power amplifier (VCM Driver)					
Gain (VM1-VM2)/(ERR-VBG)		11		13	V/V
Output voltage drop	Imotor = 0.2A			0.5	V
VCM transconductance		0.4		0.6	A/V
Bridge crossover time					
Ivcm = 10 mA, pk	Step input			10	µs
VCM output THD					
Ivcm=100 mA, pk @ 100 Hz	R_L = 16Ω			2	%
SWIN on resistance				250	Ω
Retract amplifier (retract), VRETR = 0.5V, VBEMF ≥ 1V					
offset		-100		0	mV
Maximum output current, VRETR = 0.5V, VBYP1 = 4.5V					
VBEMF = 1V, VM1 = VM2		60			mA
VBEMF = 1.5V, VM1 = VM2		100			mA
Retract Amplifier (normal)					
VRETR leakage				±1	µA

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SPINDLE MOTOR COMMUTATOR/DRIVER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input current @ VIN	0 ≤ VIN ≤ 2.5V			±1	µA
Total FETs voltage drop	Imotor = 0.5A			0.85	V
Outputs @ CT, A, B, C while not driving Rin	-0.3V ≤ Vin ≤ 7V	10			kΩ
Outputs @ CT while not driving Rin	-0.3V ≤ Vin ≤ 7V	3			kΩ

CONTROL CIRCUITRY

Vdd voltage for $\overline{\text{SYSRST}}$ & $\overline{\text{RCRST}}$ in operation		2		5.5	V
VBG	Iout < ±0.2 mA	2.13		2.37	V
VCHK comparator offset				±15	mV
Thermal shutdown Temperature threshold			125		°C

D/A CONVERTER

Full-scale voltage			VBG		V
Resolution			10		bits
Digital Delay				4	µs
LSB volatge			VBG/1024		V
Differential nonlinearity				±1	LSB

SERIAL INTERFACE PORT

SDEN setup time prior to SCLK	Tsens	35			ns
SDEN hold time after SCLK	Tsenh	50			ns
SDATA setup time prior to SCLK rise	Tds	15			ns
SDATA hold time after SCLK fall	Tdh	15			ns
SCLK pulse width	Tpw	100			ns

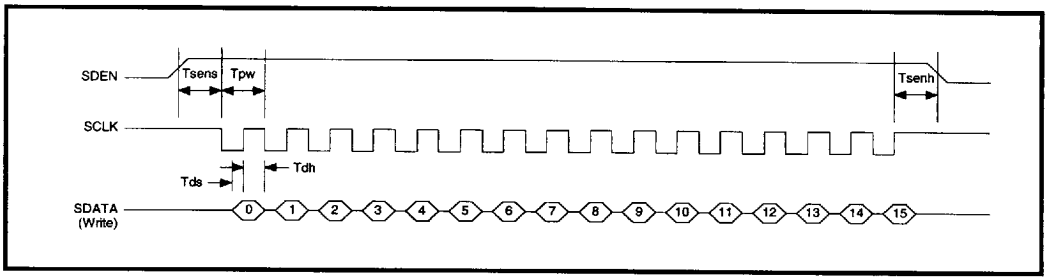


FIGURE 2: SSI 32H6811 Serial Interface Timing Diagram

APPLICATIONS INFORMATION

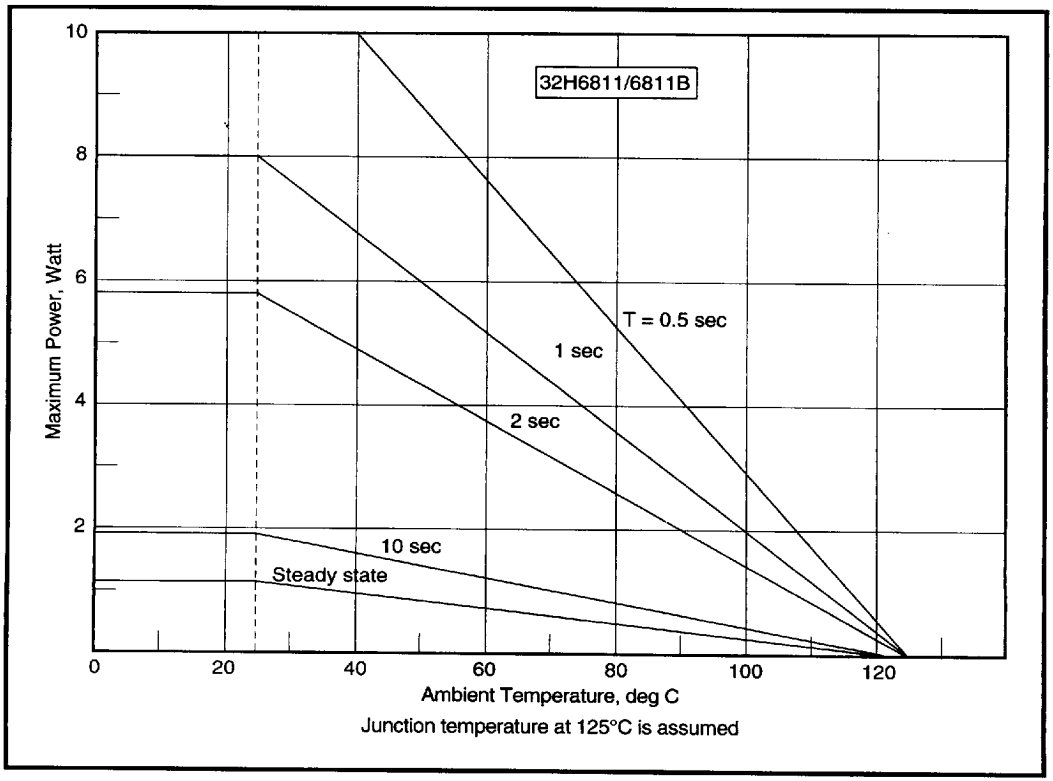
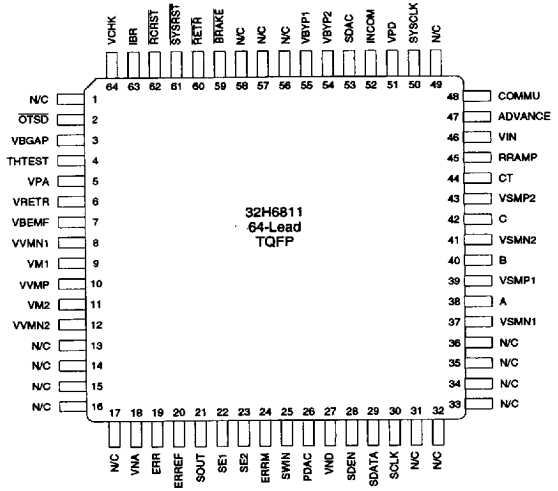


FIGURE 3: Power Dissipation Derating

SSI 32H6811/6811B
Servo Motor Speed
5V Driver/DACs

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



64-LEAD TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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