NEC

MOS INTEGRATED CIRCUIT

μPD442000L-X

2M-BIT CMOS STATIC RAM
256K-WORD BY 8-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD442000L-X is a high speed, low power, 2,097,152 bits (262,144 words by 8 bits) CMOS static RAM.

The μPD442000L-X has two chip enable pins (/CE1, CE2) to extend the capacity. And battery backup is available.

B, C and D versions are low voltage versions.

The μPD442000L-X is packed in 32-pin plastic TSOP (I) and 36-pin plastic FPBGA.

Features

- 262,144 words by 8 bits organization
- Fast access time : 70, 85,100,120,150,180, 250 ns (MAX.)
- Low voltage operation (B version: V_{CC} = 2.7 to 3.6 V, C version: V_{CC} = 2.2 to 3.6 V, D version: V_{CC} = 1.8 to 3.6 V)
- Operating ambient temperature (X version: T_A = –25 to +85 °C)
- 1.5 V (MIN.) data retention
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
μPD442000L-BxxX	70[Note], 85, 100	2.7 to 3.6	–25 to +85	35	2	2
μPD442000L-CxxX	100, 120, 150	2.2 to 3.6		30		
μPD442000L-DxxX	150, 180, 250	1.8 to 3.6		25		

Note Under development

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The mark ★ shows major revised points.

Ordering Information (1/2)

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating Temperature °C	Remark
μPD442000LGU-B70X-9JH [Note]	32-pin Plastic TSOP (I)	70	2.7 to 3.6	−25 to +85	B Version
μPD442000LGU-B85X-9JH	(8×13.4 mm) (Normal bent)	85			
μPD442000LGU-B10X-9JH		100			
μPD442000LGU-B70X-9KH [Note]	32-pin Plastic TSOP (I)	70			
μPD442000LGU-B85X-9KH	(8×13.4 mm) (Reverse bent)	85			
μPD442000LGU-B10X-9KH		100			
μPD442000LGZ-B70X-KJH [Note]	32-pin Plastic TSOP (I)	70			
μPD442000LGZ-B85X-KJH	(8×20.0 mm) (Normal bent)	85			
μPD442000LGZ-B10X-KJH		100			
μPD442000LGZ-B70X-KKH [Note]	32-pin Plastic TSOP (I)	70			
μPD442000LGZ-B85X-KKH	(8×20.0 mm) (Reverse bent)	85			
μPD442000LGZ-B10X-KKH		100			
μPD442000LF1-BS1-B70X [Note]	36-pin Plastic FPBGA	70			
μPD442000LF1-BS1-B85X [Note]	(6.5×10.5 mm)	85			
μPD442000LF1-BS1-B10X [Note]		100			
μPD442000LGU-C10X-9JH	32-pin Plastic TSOP (I)	100	2.2 to 3.6	−25 to +85	C Version
μPD442000LGU-C12X-9JH	(8×13.4 mm) (Normal bent)	120			
μPD442000LGU-C15X-9JH		150			
μPD442000LGU-C10X-9KH	32-pin Plastic TSOP (I)	100			
μPD442000LGU-C12X-9KH	(8×13.4 mm) (Reverse bent)	120			
μPD442000LGU-C15X-9KH		150			
μPD442000LGZ-C10X-KJH	32-pin Plastic TSOP (I)	100			
μPD442000LGZ-C12X-KJH	(8×20.0 mm) (Normal bent)	120			
μPD442000LGZ-C15X-KJH		150			
μPD442000LGZ-C10X-KKH	32-pin Plastic TSOP (I)	100			
μPD442000LGZ-C12X-KKH	(8×20.0 mm) (Reverse bent)	120			
μPD442000LGZ-C15X-KKH		150			
μPD442000LF1-BS1-C10X [Note]	36-pin Plastic FPBGA	100			
μPD442000LF1-BS1-C12X [Note]	(6.5×10.5 mm)	120			
μPD442000LF1-BS1-C15X [Note]		150			

Note Under development

Ordering Information (2/2)

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating Temperature °C	Remark
μPD442000LGU-D15X-9JH	32-pin Plastic TSOP (I) (8×13.4 mm) (Normal bent)	150	1.8 to 3.6	−25 to +85	D Version
μPD442000LGU-D18X-9JH		180			
μPD442000LGU-D25X-9JH		250			
μPD442000LGU-D15X-9KH	32-pin Plastic TSOP (I) (8×13.4 mm) (Reverse bent)	150			
μPD442000LGU-D18X-9KH		180			
μPD442000LGU-D25X-9KH		250			
μPD442000LGZ-D15X-KJH	32-pin Plastic TSOP (I) (8×20.0 mm) (Normal bent)	150			
μPD442000LGZ-D18X-KJH		180			
μPD442000LGZ-D25X-KJH		250			
μPD442000LGZ-D15X-KKH	32-pin Plastic TSOP (I) (8×20.0 mm) (Reverse bent)	150			
μPD442000LGZ-D18X-KKH		180			
μPD442000LGZ-D25X-KKH		250			
μPD442000LF1-BS1-D15X Note	36-pin Plastic FPBGA (6.5×10.5 mm)	150			
μPD442000LF1-BS1-D18X Note		180			
μPD442000LF1-BS1-D25X Note		250			

Note Under development

Pin Configuration (Marking Side)

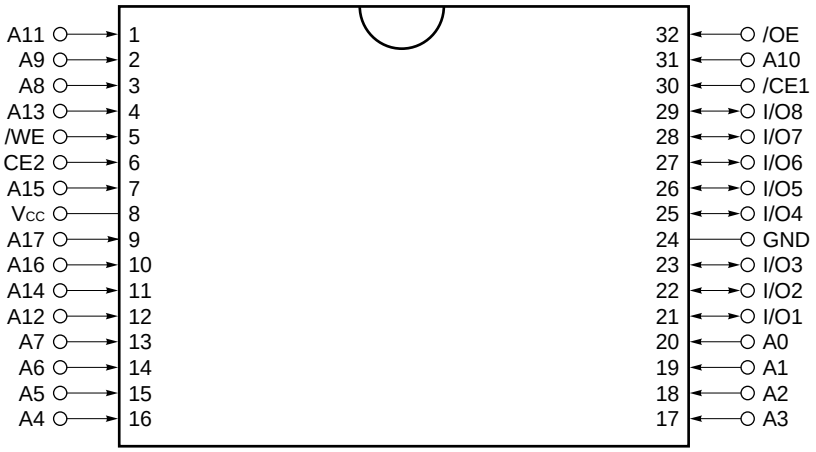
/xxx indicates active low signal.

32-pin Plastic TSOP (I) (8×13.4 mm) (Normal bent)

[μPD442000LGU-BxxX-9JH]

[μPD442000LGU-CxxX-9JH]

[μPD442000LGU-DxxX-9JH]



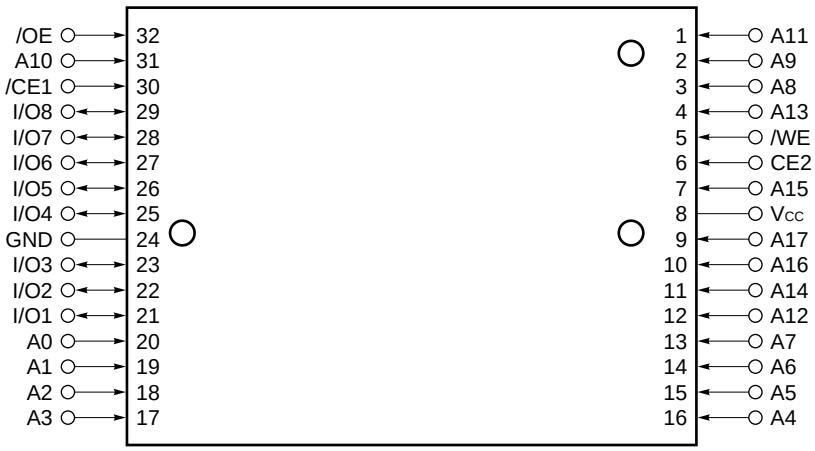
A0 - A17	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground

32-pin Plastic TSOP (I) (8x13.4 mm) (Reverse bent)

[μPD442000LGU-BxxX-9KH]

[μPD442000LGU-CxxX-9KH]

[μPD442000LGU-DxxX-9KH]



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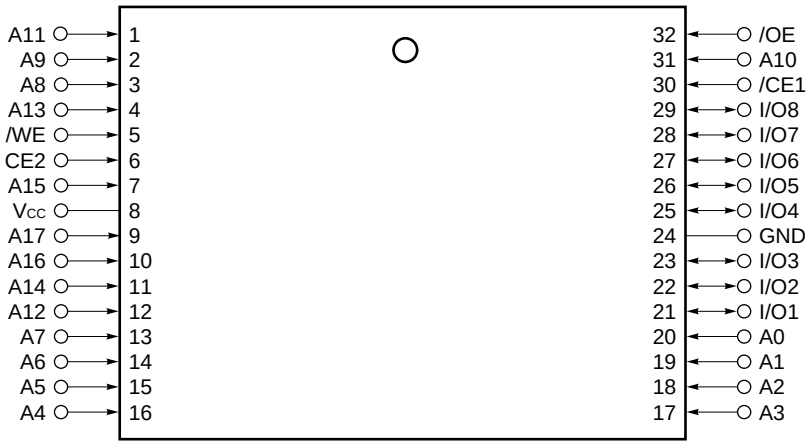
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground

32-pin Plastic TSOP (I) (8×20.0 mm) (Normal bent)

[μPD442000LGZ-BxxX-KJH]

[μPD442000LGZ-CxxX-KJH]

[μPD442000LGZ-DxxX-KJH]



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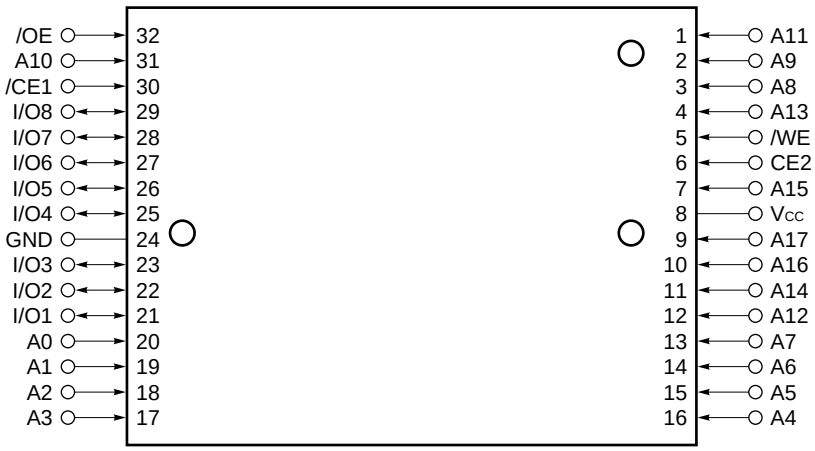
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground

32-pin Plastic TSOP (I) (8×20.0 mm) (Reverse bent)

[μPD442000LGZ-BxxX-KKH]

[μPD442000LGZ-CxxX-KKH]

[μPD442000LGZ-DxxX-KKH]



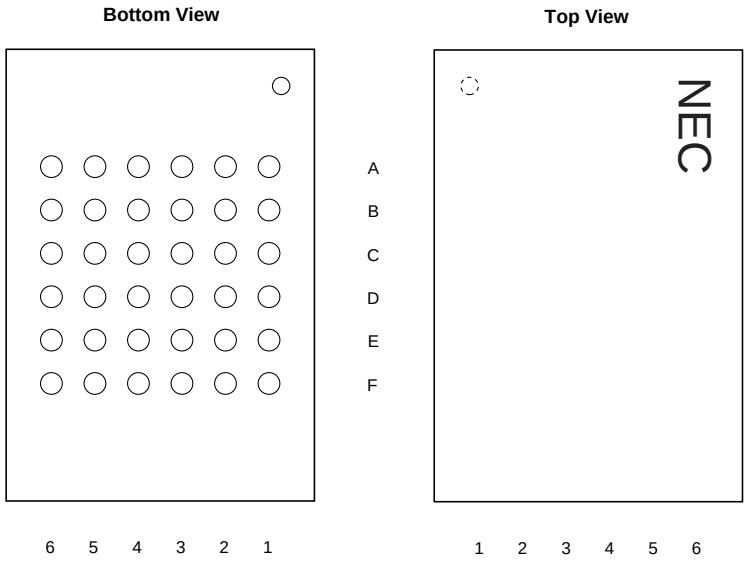
A0 - A17	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground

36-pin Plastic FPBGA (6.5×10.5 mm)

[μPD442000LF1-BS1-BxxX]

[μPD442000LF1-BS1-CxxX]

[μPD442000LF1-BS1-DxxX]

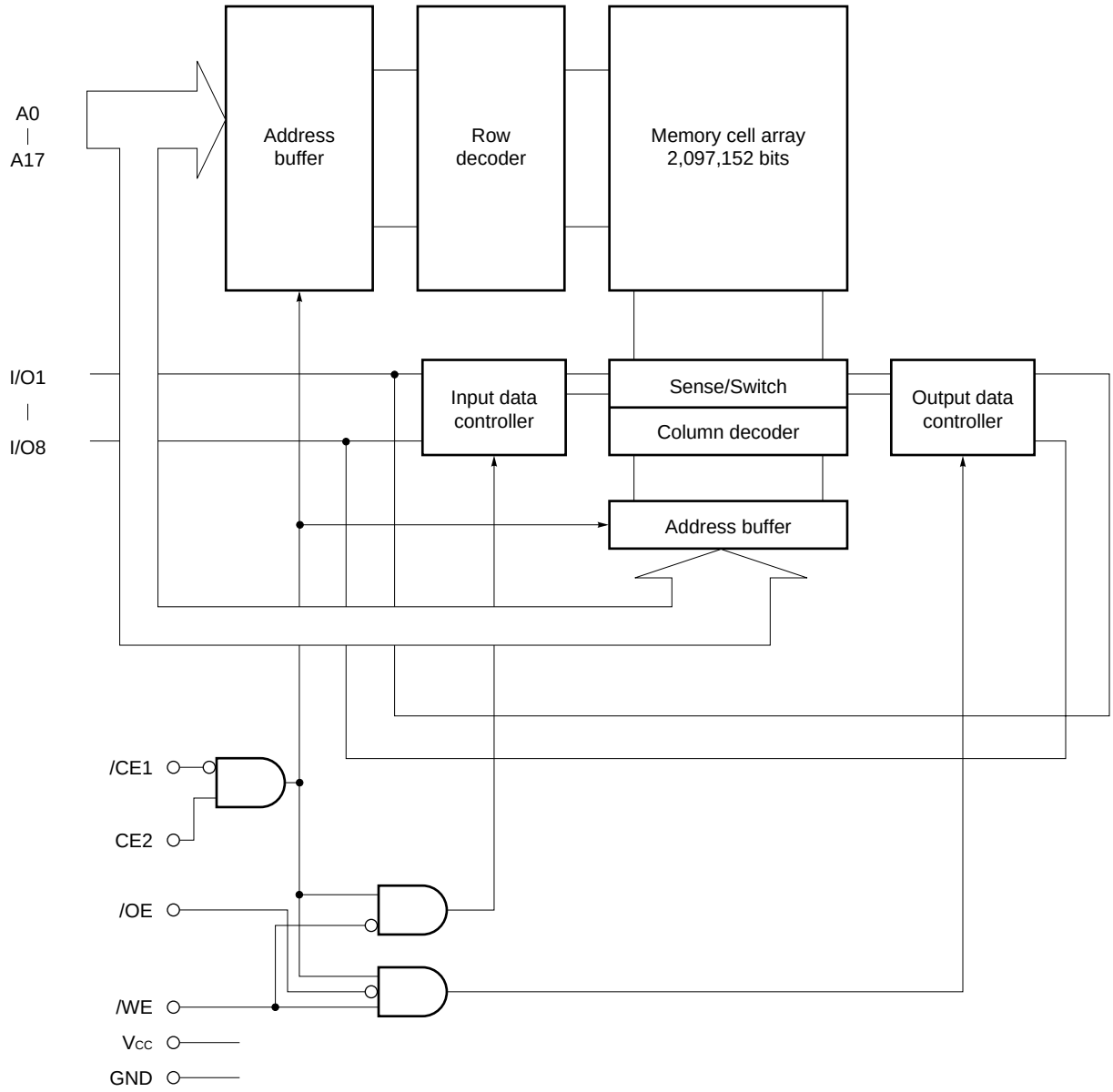


	6		5		4		3		2		1	
	Pin No.	Func.	Pin No.	Func.	Pin No.	Func.	Pin No.	Func.	Pin No.	Func.	Pin No.	Func
A	A6	A12	A5	A14	A4	A17	A3	V_{CC}	A2	CE2	A1	A13
B	B6	A6	B5	A7	B4	A16	B3	A15	B2	/WE	B1	A8
C	C6	A4	C5	A5	C4	IC	C3	IC	C2	A11	C1	A9
D	D6	A3	D5	A2	D4	IC	D3	IC	D2	A10	D1	/OE
E	E6	A1	E5	I/O2	E4	I/O3	E3	I/O4	E2	I/O6	E1	/CE1
F	F6	A0	F5	I/O1	F4	GND	F3	I/O5	F2	I/O7	F1	I/O8

A0 - A17 : Address inputs
I/O1 - I/O8 : Data inputs / outputs
/CE1, CE2 : Chip Enable 1, 2
/WE : Write Enable
/OE : Output Enable
V_{CC} : Power supply
GND : Ground
IC[Note] : Internal Connection

Note Leave this pin unconnected or connect to GND.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
H	×	×	×	Not selected	High impedance	I_{SB}
×	L	×	×			
L	H	H	H	Output disable		I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +4.6	V
Input / Output voltage	V_T		–0.5 Note to V_{CC}+0.5	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Conditions	μPD442000L-BxxX		μPD442000L-CxxX		μPD442000L-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V_{IH}	2.7 V≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	V
		2.2 V≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	
		1.8 V≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.5	
Low level input voltage	V_{IL}		–0.3 Note	+0.5	–0.3 Note	+0.3	–0.3 Note	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –1.5 V (MIN.) (Pulse width : 30 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		μPD442000L-BxxX			μPD442000L-CxxX			μPD442000L-DxxX			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH},			30	35		25	30		20	25	mA
		$I_{I/O}$ = 0 mA,	$V_{CC} \leq 2.7$		–	–		20	25		15	20	
		Minimum cycle time	$V_{CC} \leq 2.2$		–	–		–	–		10	15	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH},				10			10			10	
		$I_{I/O}$ = 0 mA	$V_{CC} \leq 2.7$			–			8			8	
			$V_{CC} \leq 2.2$			–			–			5	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA,				8			8			8	
		$V_{IL} \leq 0.2$ V,	$V_{CC} \leq 2.7$			–			6			6	
		$V_{IH} \geq V_{CC}$ – 0.2 V	$V_{CC} \leq 2.2$			–			–			5	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL}				0.3			0.3			0.3	mA
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V,			0.1	2		0.1	2		0.1	2	μA
		CE2 ≥ V_{CC} – 0.2 V	$V_{CC} \leq 2.7$		–	–		0.08	2		0.08	2	
			$V_{CC} \leq 2.2$		–	–		–	–		0.05	1.5	
	I_{SB2}	CE2 ≤ 0.2 V			0.1	2		0.1	2		0.1	2	
			$V_{CC} \leq 2.7$		–	–		0.08	2		0.08	2	
			$V_{CC} \leq 2.2$		–	–		–	–		0.05	1.5	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			2.4			2.4			V
			$V_{CC} \leq 2.7$	–			1.8			1.8			
			$V_{CC} \leq 2.2$	–			–			1.5			
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4			0.4			0.4	V

Remarks 1. V_{IN} : Input voltage

2. These DC characteristics are in common regardless of package types and access time.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

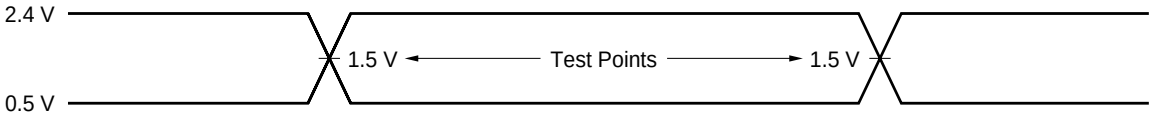
2. These parameters are periodically sampled and not 100% tested.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

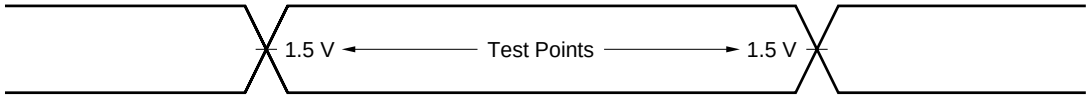
AC Test Conditions

μPD442000L-B70X, 442000L-B85X, 442000L-B10X

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 50pF

μPD442000L-C10X, 442000L-C12X, 442000L-C15X

Input Waveform (Rise and Fall Time ≤ 5 ns)

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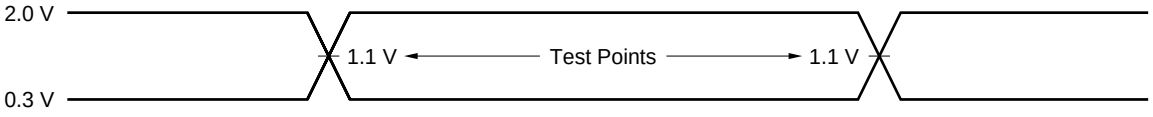
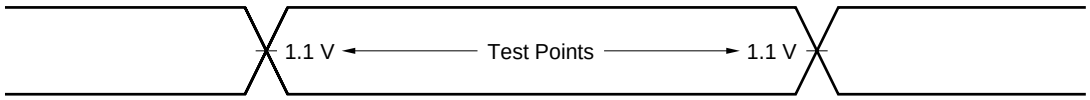


Output Waveform

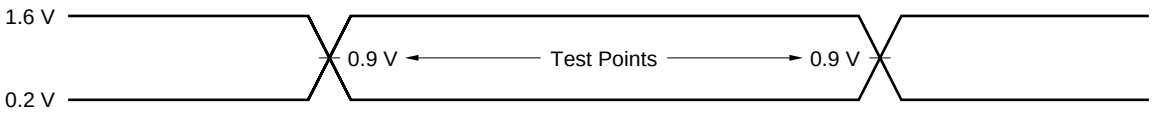


Output Load

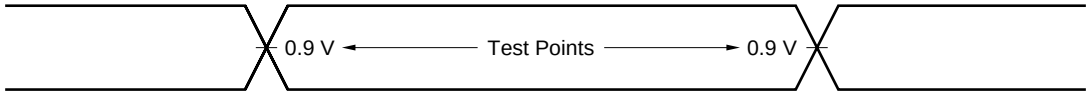
1TTL + 50pF

μPD442000L-D15X, 442000L-D18X, 442000L-D25X

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 50pF

Read Cycle (B version)

Parameter	Symbol	–B70X		–B85X		–B10X		Unit	Conditions
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note1**
/CE1 access time	t_{CO1}		70		85		100	ns	
CE2 access time	t_{CO2}		70		85		100	ns	
/OE to output valid	t_{OE}		35		40		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	**Note2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		25		30		35	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35	ns	
/OE to output hold in high impedance	t_{OHZ}		25		30		35	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (C version)

Parameter	Symbol	–C10X		–C12X		–C15X		Unit	Conditions
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		150		ns	
Address access time	t_{AA}		100		120		150	ns	**Note1**
/CE1 access time	t_{CO1}		100		120		150	ns	
CE2 access time	t_{CO2}		100		120		150	ns	
/OE to output valid	t_{OE}		50		60		70	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	**Note2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		35		40		45	ns	
CE2 to output in high impedance	t_{HZ2}		35		40		45	ns	
/OE to output hold in high impedance	t_{OHZ}		35		40		45	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (D version)

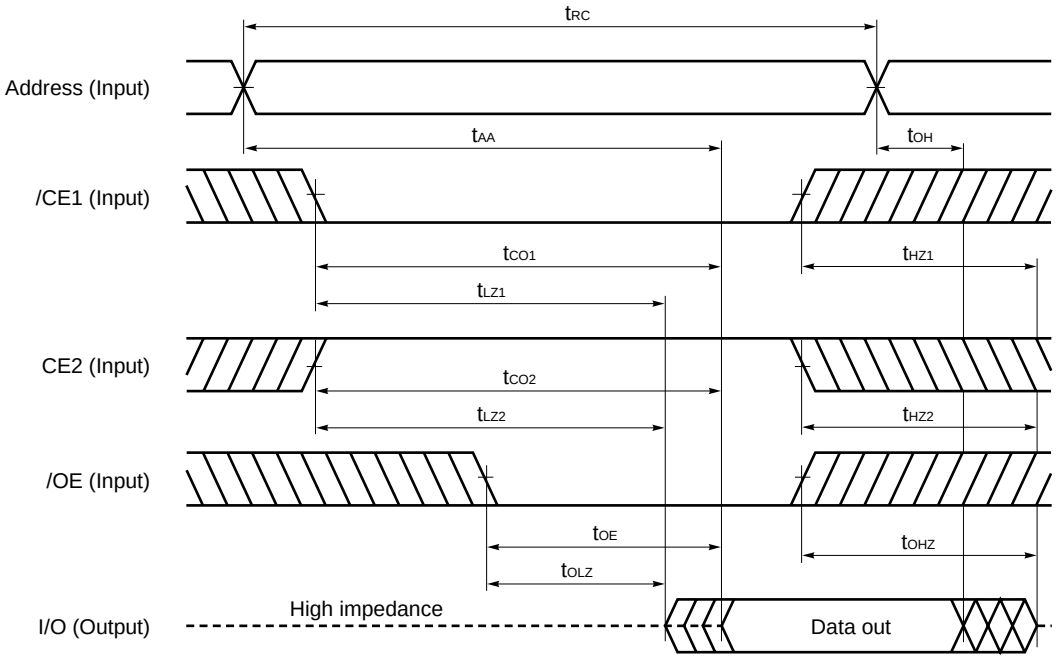
Parameter	Symbol	–D15X		–D18X		–D25X		Unit	Conditions
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	150		180		250		ns	
Address access time	t_{AA}		150		180		250	ns	**Note1**
/CE1 access time	t_{CO1}		150		180		250	ns	
CE2 access time	t_{CO2}		150		180		250	ns	
/OE to output valid	t_{OE}		70		80		100	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	**Note2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		45		50		60	ns	
CE2 to output in high impedance	t_{HZ2}		45		50		60	ns	
/OE to output hold in high impedance	t_{OHZ}		45		50		60	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (B version)

Parameter	Symbol	–B70X		–B85X		–B10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CE1 to end of write	t_{CW1}	55		70		80		ns	
CE2 to end of write	t_{CW2}	55		70		80		ns	
Address valid to end of write	t_{AW}	55		70		80		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		60		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle (C version)

Parameter	Symbol	–C10X		–C12X		–C15X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		150		ns	
/CE1 to end of write	t_{CW1}	80		100		120		ns	
CE2 to end of write	t_{CW2}	80		100		120		ns	
Address valid to end of write	t_{AW}	80		100		120		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	60		80		100		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	40		50		60		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		35		40		50	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

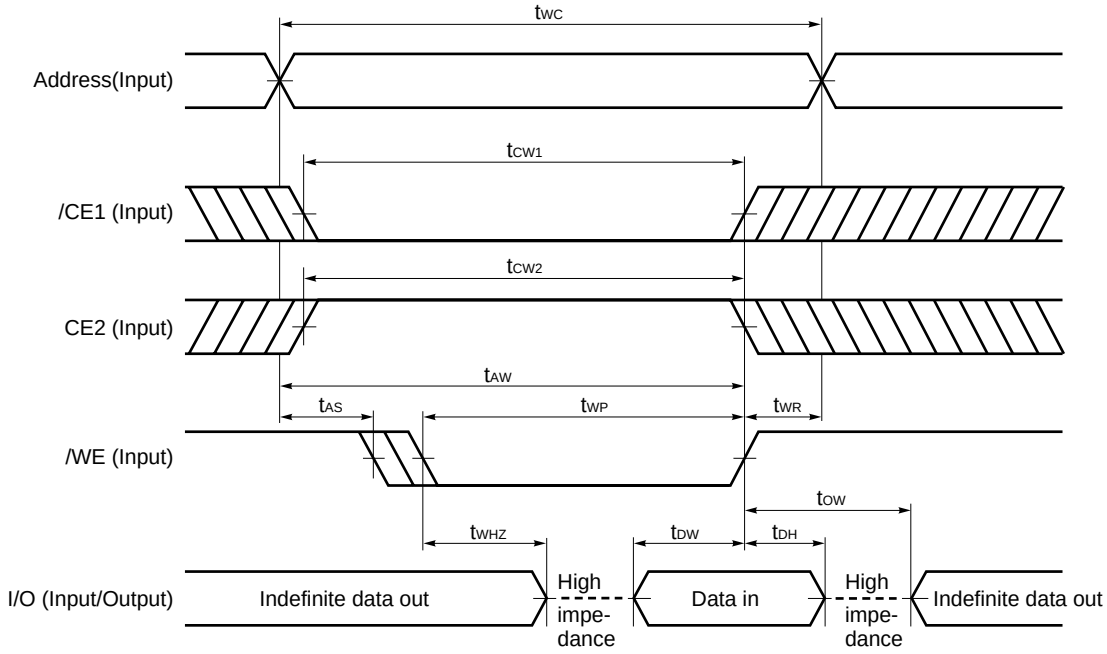
Write Cycle (D version)

Parameter	Symbol	–D15X		–D18X		–D25X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	150		180		250		ns	
/CE1 to end of write	t_{CW1}	120		150		200		ns	
CE2 to end of write	t_{CW2}	120		150		200		ns	
Address valid to end of write	t_{AW}	120		150		200		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	100		120		160		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	60		75		100		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		50		60		80	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

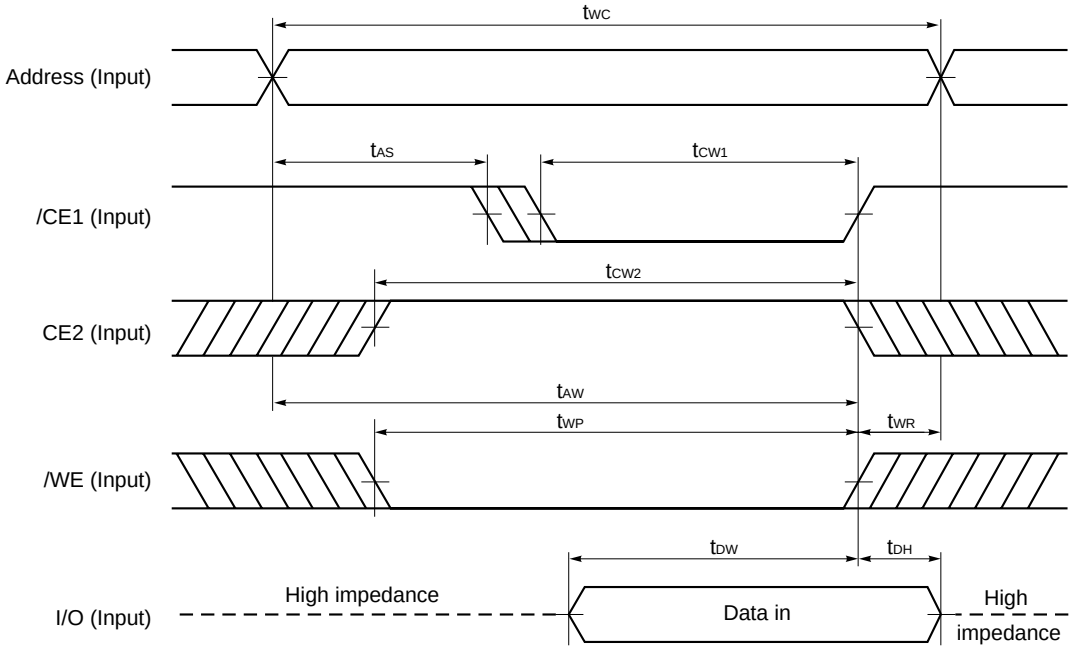
2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

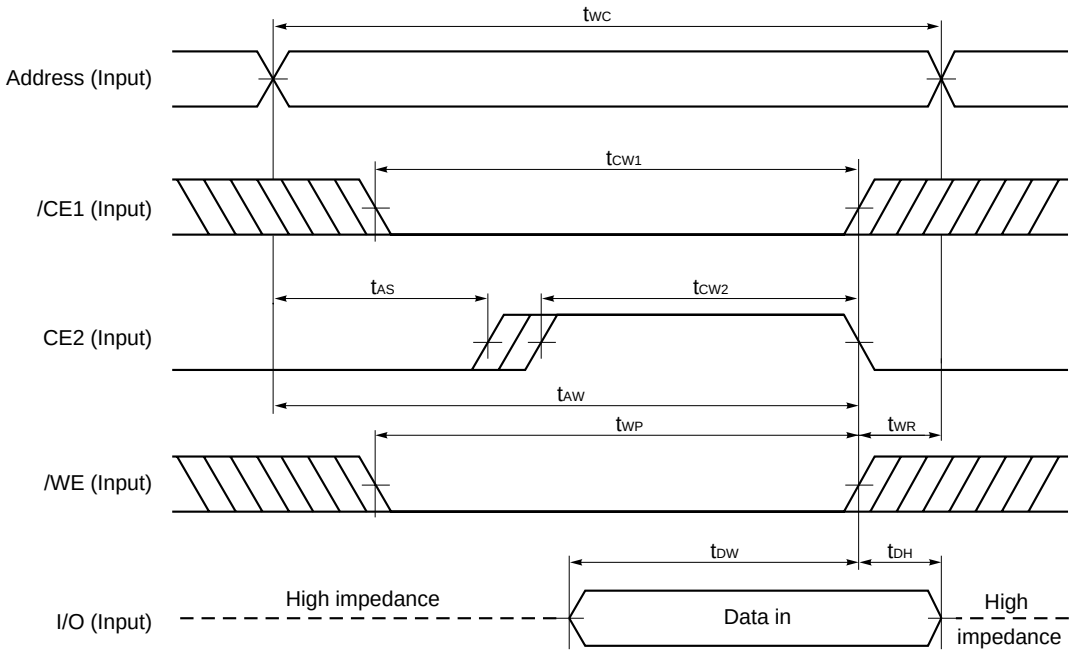


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

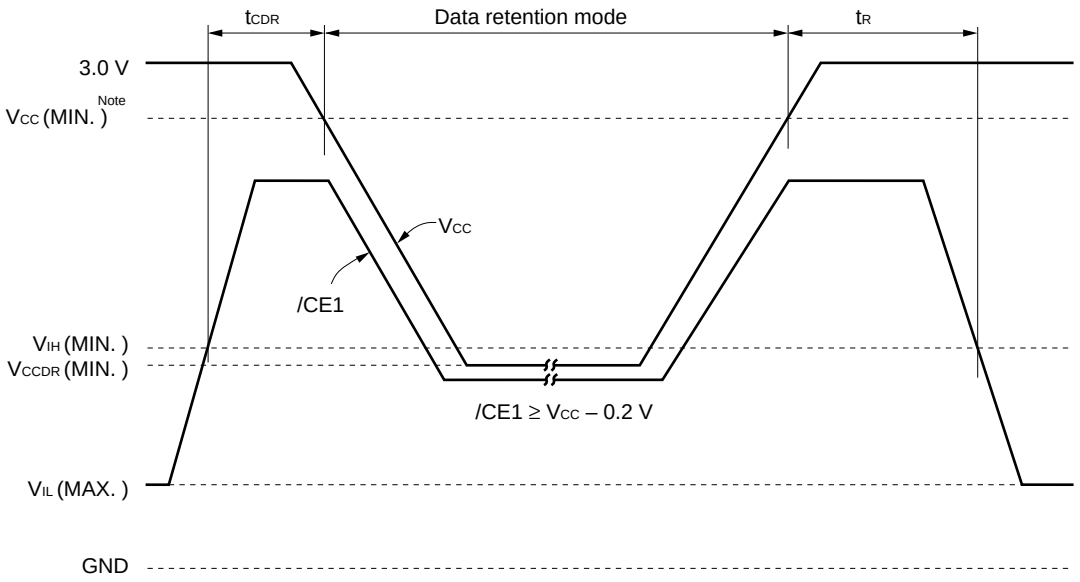
Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2V	1.5		3.6	V
	V_{CCDR2}	CE2 ≤ 0.2 V	1.5		3.6	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		0.1	2	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.1	2	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		t_{RC} Note			ns

Note t_{RC} : Read cycle time.

Data Retention Timing Chart

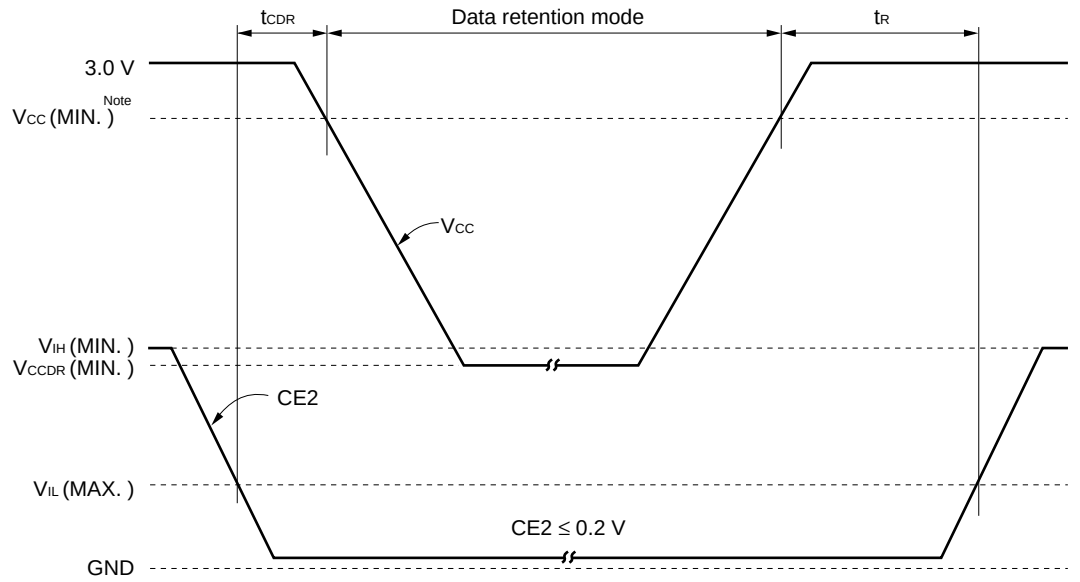
(1) /CE1 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

(2) CE2 Controlled

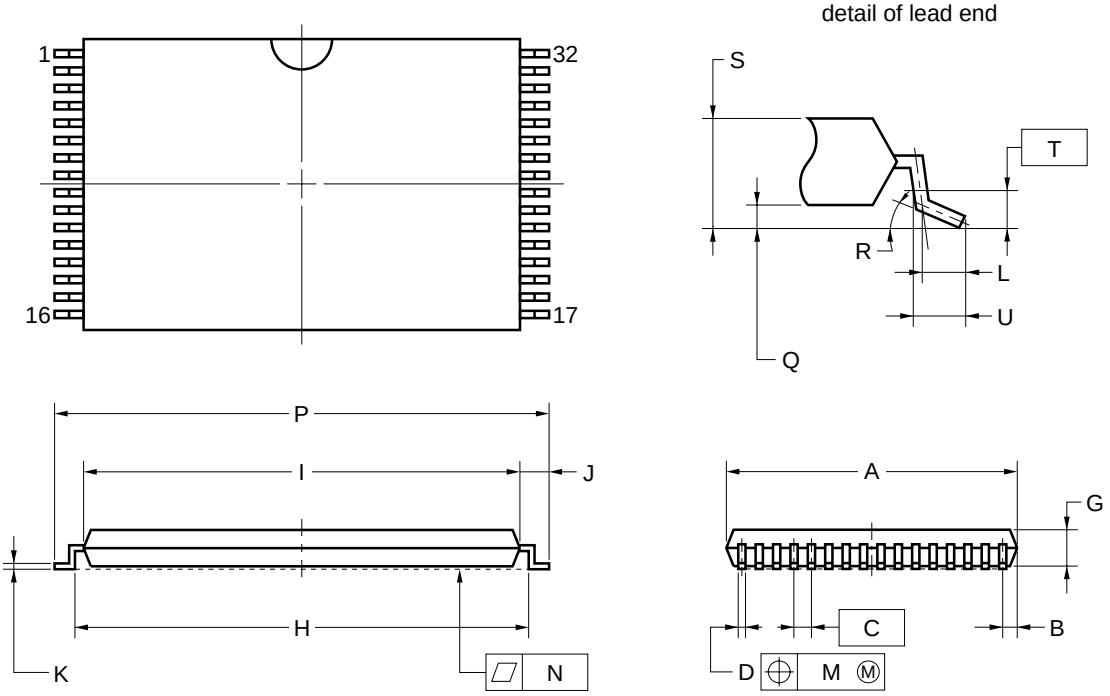


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark The other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

32PIN PLASTIC TSOP (I) (8x13.4)



NOTE

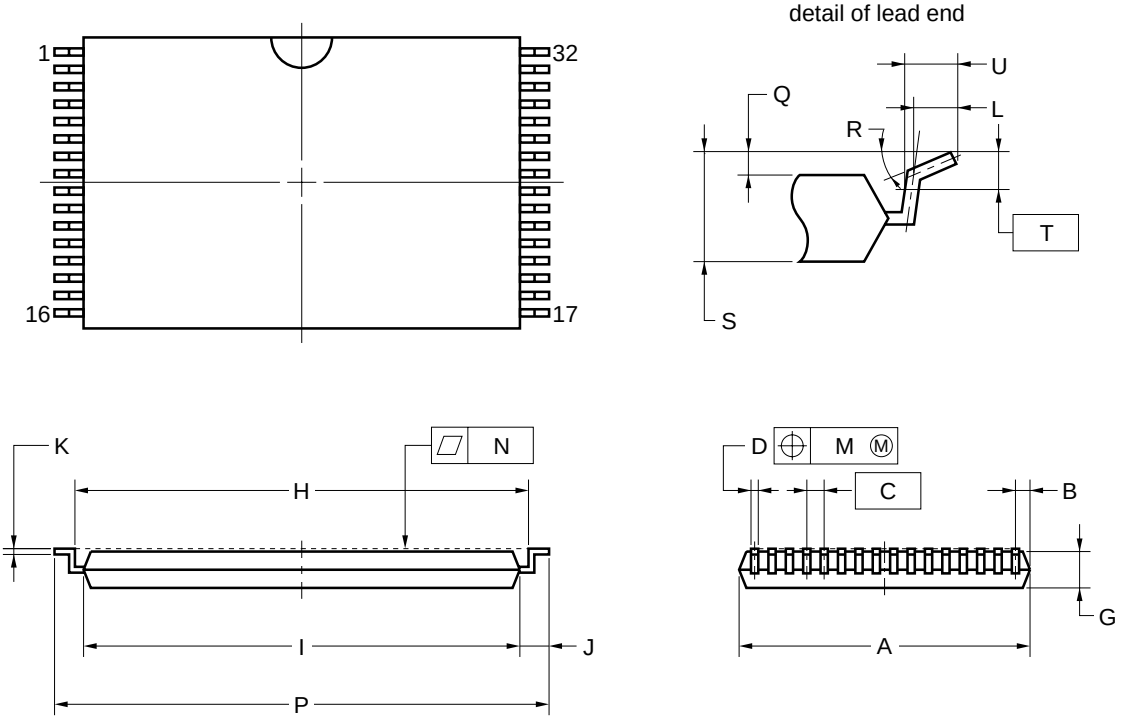
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.331 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22 ± 0.05	$0.009^{+0.002}_{-0.003}$
G	1.0 ± 0.05	$0.039^{+0.003}_{-0.009}$
H	12.4±0.2	0.488±0.008
I	11.8±0.1	$0.465^{+0.004}_{-0.005}$
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
M	0.08	0.003
N	0.08	0.003
P	13.4±0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1±0.05	0.004±0.002
R	$3^\circ{}^{+5^\circ}_{-3^\circ}$	$3^\circ{}^{+5^\circ}_{-3^\circ}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.010
U	0.6±0.15	$0.024^{+0.006}_{-0.007}$

P32GU-50-9JH-1

32PIN PLASTIC TSOP (I) (8x13.4)



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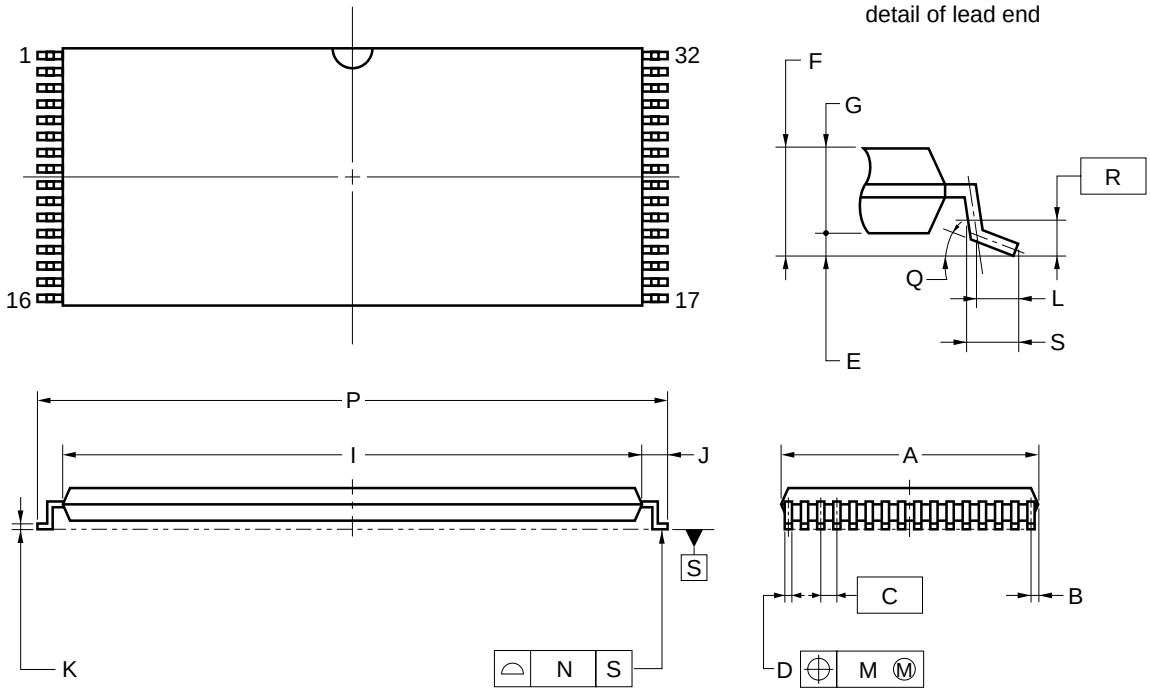
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.010
U	0.6±0.15	$0.024^{+0.006}_{-0.007}$

P32GU-50-9KH-1

32 PIN PLASTIC TSOP (I) (8×20)



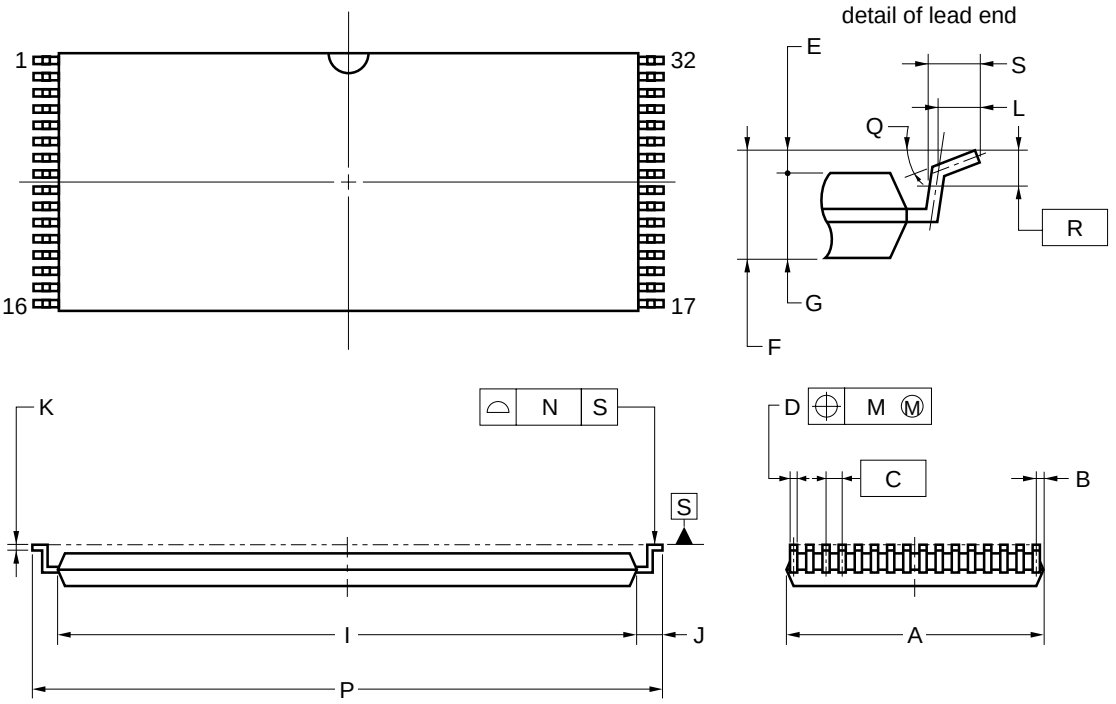
NOTES

1. Controlling dimension —— Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22 ± 0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97 ± 0.08	$0.038^{+0.004}_{-0.003}$
I	18.4 ± 0.1	$0.724^{+0.005}_{-0.004}$
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	0.145 ± 0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0 ± 0.2	$0.787^{+0.009}_{-0.008}$
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25	0.010
S	0.60 ± 0.15	$0.024^{+0.006}_{-0.007}$

S32GZ-50-KJH1

32 PIN PLASTIC TSOP (I) (8×20)



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2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
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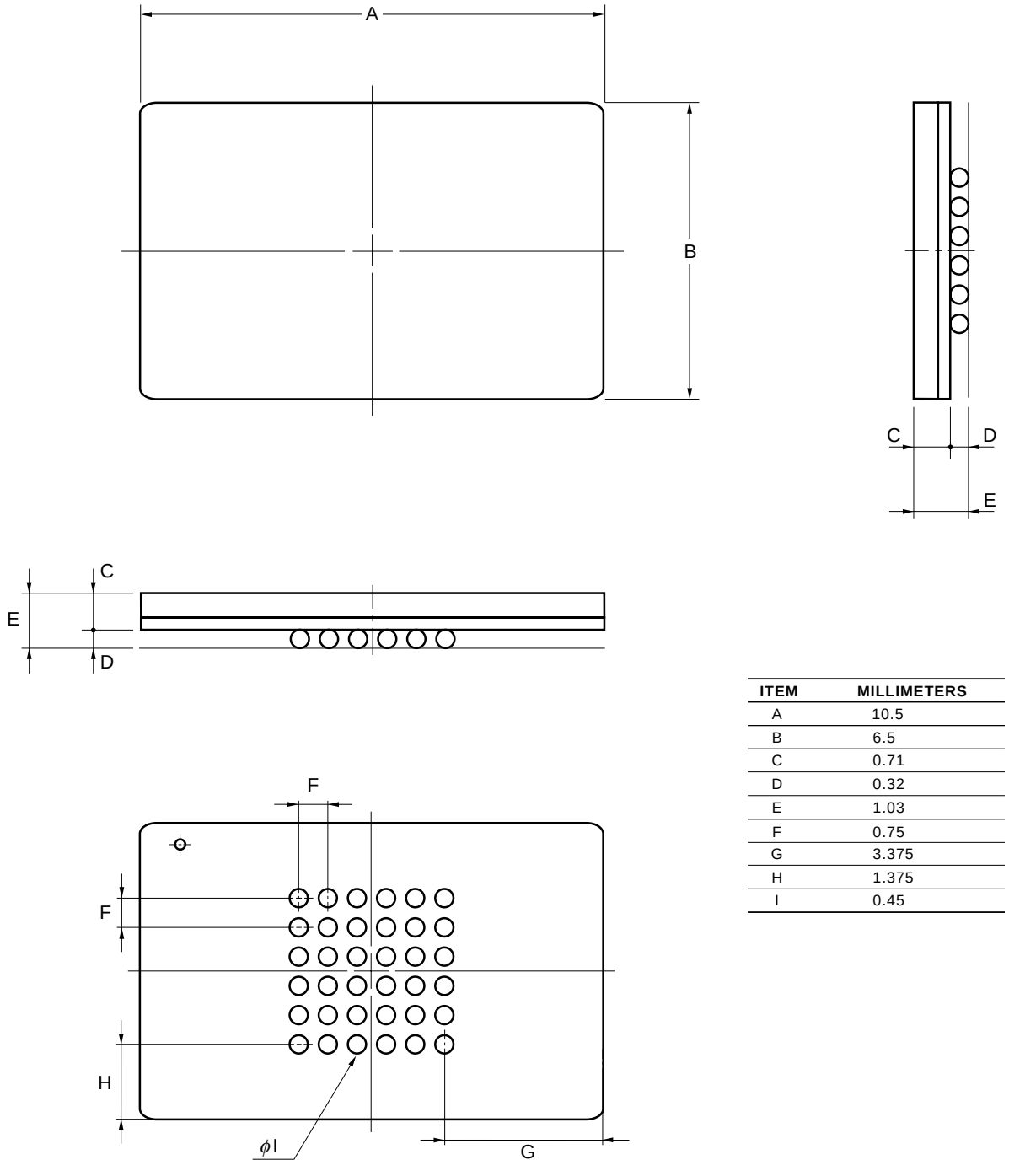
ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22 ± 0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97 ± 0.08	$0.038^{+0.004}_{-0.003}$
I	18.4 ± 0.1	$0.724^{+0.005}_{-0.004}$
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	0.145 ± 0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0 ± 0.2	$0.787^{+0.009}_{-0.008}$
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25	0.010
S	0.60 ± 0.15	$0.024^{+0.006}_{-0.007}$

S32GZ-50-KKH1

36 PIN PLASTIC-FPBGA (6.5 × 10.5)



ITEM	MILLIMETERS
A	10.5
B	6.5
C	0.71
D	0.32
E	1.03
F	0.75
G	3.375
H	1.375
I	0.45

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD442000L-X.

Type of Surface Mount Device

μPD442000LGU-BX-9JH: 32-pin Plastic TSOP (I) (8×13.4 mm) (Normal bent)
μPD442000LGU-CX-9JH: 32-pin Plastic TSOP (I) (8×13.4 mm) (Normal bent)
μPD442000LGU-DX-9JH: 32-pin Plastic TSOP (I) (8×13.4 mm) (Normal bent)
μPD442000LGU-BX-9KH: 32-pin Plastic TSOP (I) (8×13.4 mm) (Reverse bent)
μPD442000LGU-CX-9KH: 32-pin Plastic TSOP (I) (8×13.4 mm) (Reverse bent)
μPD442000LGU-DX-9KH: 32-pin Plastic TSOP (I) (8×13.4 mm) (Reverse bent)
μPD442000LGZ-BX-KJH: 32-pin Plastic TSOP (I) (8×20.0 mm) (Normal bent)
μPD442000LGZ-CX-KJH: 32-pin Plastic TSOP (I) (8×20.0 mm) (Normal bent)
μPD442000LGZ-DX-KJH: 32-pin Plastic TSOP (I) (8×20.0 mm) (Normal bent)
μPD442000LGZ-BX-KKH: 32-pin Plastic TSOP (I) (8×20.0 mm) (Reverse bent)
μPD442000LGZ-CX-KKH: 32-pin Plastic TSOP (I) (8×20.0 mm) (Reverse bent)
μPD442000LGZ-DX-KKH: 32-pin Plastic TSOP (I) (8×20.0 mm) (Reverse bent)
μPD442000LF1-BS1-BX: 36-pin Plastic FPBGA (6.5×10.5 mm)
μPD442000LF1-BS1-CX: 36-pin Plastic FPBGA (6.5×10.5 mm)
μPD442000LF1-BS1-DX: 36-pin Plastic FPBGA (6.5×10.5 mm)

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed imme-diately after power-on for devices having reset function.

[MEMO]