USER'S MANUAL

NEC

AS17012 DEVICE FILE

PC-9800 SERIES(MS-DOS™)BASED

IBM PC/AT™(PC DOS™)BASED

VERSION 1

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VERSION 1

The AS17012 is a device file for use with the AS17K assembler unit to assemble uPD17012 programs.

The AS17012 provides upon assemble the uPD17012 program memory capacity, data memory capacity, usable instructions, reserved symbols, etc.

Refer to the AS17K User's Manual EEU-603 for details of the AS17K assembler unit and AS17012 device file manipulating procedure.

CONTENTS

CHAPTER 1. DEVICE INFORMATION

The AS17012 device file provides upon assembly the following information concerning the uPD17012.

(1) Program memory (ROM) capacity

8K bytes (4096 x 16 bits, 0000H to 0FFFH)

(2) Data memory (RAM) capacity

336 x 4 bits (BANK 0 to BANK 2)

(3) Usable instructions

Refer to Chapter 2 "uPD17012 Instruction Set".

(4) Register file, port register and peripheral register read and write information

Refer to Chapter 3 "Reserved Symbols".

(5) Reserved symbols

Refer to Chapter 3 "Reserved Symbols".

CHAPTER 2. uPD17012 INSTRUCTION SET

2.1 OUTLINE OF INSTRUCTION SET

b_{14}-b_{11} \ b_{15}		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	INC	AR		
		INC	IX		
		MOVT	DBF, @AR		
		BR	@AR		
		CALL	@AR		
		RET			
		RETSK			
		EI			
		DI			
		RETI			
		PUSH	AR		
		POP	AR		
		GET	DBF, p		
		PUT	p, DBF		
		PEEK	WR, rf		
		POKE	rf, WR		
		RORC	r		
		STOP	s		
		HALT	h		
		NOP			
1 0 0 0	8	LD	r, m	ST	m, r

b_{14}-b_{11} \ b_{15}		0		1	
BIN	HEX				
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A	MOV	@r, m	MOV	m, @r
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr (Page 0)	CALL	addr (Page 0)
1 1 0 1	D	BR	addr (Page 1)	MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

2.2 LEGEND

addr	:	Program memory address (lower 11 bits)
AR	:	Address register
$(AR)_{rom}$	:	Program memory data indicated by the address register
ASR	:	Address stack register indicated by the stack pointer
BANK	:	Bank register
CMP	:	Compare flag
CY	:	Carry flag
DBF	:	Data buffer
h	:	Halt release condition (h = 0 to 3, 8 to 0FH)
i	:	Immediate data
INTEF	:	Interrupt enable flag
INTR	:	Register saved to the stack in an interrupt
INTSK	:	System register stack register
IX	:	Index register
IXE	:	Index enable flag
M	:	Data memory address IXE = 0 : M = [(BANK), m_H, m_L] IXE = 1 : M = [(BANK), m_H, m_L] OR (IX)
m	:	Data memory address except banks
m_H	:	Data memory row address (3 bits)
m_L	:	Data memory column address (4 bits)
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
n	:	Bit position (4 bits)
PAGE	:	Page (program counter bit 11)
PC	:	Program counter
PE	:	Peripheral register
p	:	Peripheral register address
p_H	:	Peripheral register address (upper 3 bits)
p_L	:	Peripheral register address (lower 4 bits)
R	:	General register address R = [(RP), r]
r	:	General register column address
R (n)	:	General register bit n
RP	:	General register pointer

RF	:	Register file
rf	:	Register file address
rf_H	:	Register file address (upper 3 bits)
rf_L	:	Register file address (lower 4 bits)
s	:	Stop release condition
SP	:	Stack pointer
WR	:	Window register
[ ]	:	Data memory or register address
( )	:	Data memory or register value

2.3 INSTRUCTION LIST

NOTE	Mnemonic	Operands	Operation	Machine Code			
				Opcode	Operands		
Addition	ADD	r, m	(R) ← (R) + (M)	CCCCO	m_H	m_L	r
		m, #i	(M) ← (M) + i	1CCCO	m_H	m_L	i
	ADDC	r, m	(R) ← (R) + (M) + (CY)	CCO10	m_H	m_L	r
		m, #i	(M) ← (M) + i + (CY)	1CO10	m_H	m_L	i
	INC	AR	(AR) ← (AR) + 1	CO111	OOO	1001	OOOO
		IX	(IX) ← (IX) + 1	CO111	OOO	1000	OOOO
Subtraction	SUB	r, m	(R) ← (R) − (M)	CCCO1	m_H	m_L	r
		m, #i	(M) ← (M) − i	1CCO1	m_H	m_L	i
	SUBC	r, m	(R) ← (R) − (M) − (CY)	CCO11	m_H	m_L	r
		m, #i	(M) ← (M) − i − (CY)	1CO11	m_H	m_L	i
Comparison	SKE	m, #i	(M) − i, skip if zero	01CO1	m_H	m_L	i
	SKGE	m, #i	(M) − i, skip if not borrow	11OO1	m_H	m_L	i
	SKLT	m, #i	(M) − i, skip if borrow	11O11	m_H	m_L	i
	SKNE	m, #i	(M) − i, skip if not zero	01O11	m_H	m_L	i
Logical	AND	m, #i	(M) ← (M) AND i	10100	m_H	m_L	i
		r, m	(R) ← (R) AND (M)	CO100	m_H	m_L	r
	OR	m, #i	(M) ← (M) OR i	10110	m_H	m_L	i
		r, m	(R) ← (R) OR (M)	CO110	m_H	m_L	r
	XOR	m, #i	(M) ← (M) XOR i	10101	m_H	m_L	i
		r, m	(R) ← (R) XOR (M)	CO101	m_H	m_L	r
Transfer	LD	r, m	(R) ← (M)	01CCO	m_H	m_L	r
	ST	m, r	(M) ← (R)	11CCO	m_H	m_L	r
	MOV	@r, m	if MPE=1 : [(MP), (R)] ← (M) if MPE=0 : [(BANK), m_H, (R)] ← (M)	01010	m_H	m_L	r
		m, @r	if MPE=1 : (M) ← [(MP), (R)] if MPE=0 : (M) ← [(BANK), m_H, (R)]	11010	m_H	m_L	r
		m, #i	(M) ← i	11101	m_H	m_L	i
	MOVT	DBF, @AR	(SP) ← (SP) - 1, (ASR) ← (PC), (PC) ← (AR), (DBF) ← $(AR)_{rom}$, (PC) ← (ASR), (SP) ← (SP) + 1	CO111	OOO	0001	OOOO
	PUSH	AR	(SP) ← (SP) − 1, (ASR) ← (AR)	CO111	OOO	1101	OOOO
	POP	AR	(AR) ← (ASR), (SP) ← (SP) + 1	CO111	OOO	1100	OOOO
	PEEK	WR, rf	(WR) ← (RF)	CO111	rf_H	0011	rf_L

NOTE: Instruction Group

NOTE 1	Mnemonic	Operands	Operation	Machine Code			
				Opcode	Operands		
Transfer	POKE	rf, WR	(RF) ← (WR)	C0111	rf_H	0010	rf_L
	GET	DBF, p	(DBF) ← (PE)	C0111	p_H	1011	p_L
	PUT	p, DBF	(PE) ← (DBF)	C0111	p_H	1010	p_L
NOTE 2	SKT	m, #n	CMP←0, if (M) AND n=n, then skip	11110	m_H	m_L	n
	SKF	m, #n	CMP←0, if (M) AND n=0, then skip	11111	m_H	m_L	n
Branch	BR	addr	(PC) ←addr, PAGE←0	01100	addr (lower 11 bits)		
			(PC) ←addr, PAGE←1	01101			
		@AR	(PC) ← (AR)	C0111	000	0100	0000
NOTE 3	RORC	r	→ (CY)→R(3)→R(2)→R(1)→R(0) →	C0111	000	0111	r
Subroutine	CALL	addr	(SP)←(SP)−1, (ASR)←(PC)+1, (PC)←addr, PAGE←0	11100	addr (lower 11 bits)		
		@AR	(SP)←(SP)−1, (ASR)←(PC)+1, (PC) ← (AR)	C0111	000	0101	0000
	RET		(PC)←(ASR), (SP)←(SP)+1	C0111	000	1110	0000
	RETSK		(PC)←(ASR), (SP)←(SP)+1, and skip	C0111	001	1110	0000
	RETI		(PC) ← (ASR), (SP) ← (SP)+1, INTR← (INTSK)	C0111	100	1110	0000
NOTE 4	EI		INTEF←1	C0111	000	1111	0000
	DI		INTEF←0	C0111	001	1111	0000
Others	STOP	s	stop clock if CE=low	C0111	010	1111	s
	HALT	h	halt	C0111	011	1111	h
	NOP		No operation	C0111	100	1111	0000

NOTE 1: Instruction Group
2: Decision
3: Rotation
4: Interrupt

2.4 ASSEMBLER (AS17K) INTRINSIC MACRO INSTRUCTIONS

Legend

flag : One of flag1 to flagn
flag1 to flagn: Reserved words or symbol-difined flag names.
n : Number
< > : May be omitted.

	Mnemonic	Operands	n	Operation
Intrinsic macro instructions	SKTn	flag1, ... flagn	$1 \leq n \leq 4$	if (flag1) to (flagn) = all "1", then skip
	SKFn	flag1, ... flagn	$1 \leq n \leq 4$	if (flag1) to (flagn) = all "0", then skip
	SETn	flag1, ... flagn	$1 \leq n \leq 4$	(flag1) to (flagn) ← 1
	CLRn	flag1, ... flagn	$1 \leq n \leq 4$	(flag1) to (flagn) ← 0
	NOTn	flag1, ... flagn	$1 \leq n \leq 4$	if (flag) = "0", then (flag) ← 1 if (flag) = "1", then (flag) ← 0
	INITFLG	<NOT> flag1, ... <NOT> flagn	$1 \leq n \leq 4$	if description = NOT flag, (flag) ← 0 if description = flag, (flag) ← 1
	BANKn		$0 \leq n \leq 2$	(BANK) ← n

CHAPTER 3. RESERVED SYMBOLS

The symbols defined in the uPD17012 device file are shown below and on the following pages. The defined symbols are listed below.

- System register
- Data buffer
- LCD segment register
- Port register
- Register file (control register)
- Peripheral register

3.1 SYSTEM REGISTER

Symbol Name	At-trib-ute	Value	R/W	Description
AR3	MEM	0.74H	R/W	Bits 15 to 12 of address register
AR2	MEM	0.75H	R/W	Bits 11 to 8 of address register
AR1	MEM	0.76H	R/W	Bits 7 to 4 of address register
ARO	MEM	0.77H	R/W	Bits 3 to 0 of address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Bits 11 to 8 of index register
MPH	MEM	0.7AH	R/W	Bits 7 to 4 of memory pointer
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Bits 7 to 4 of index register
MPL	MEM	0.7BH	R/W	Bits 3 to 0 of memory pointer
IXL	MEM	0.7CH	R/W	Bits 3 to 0 of index register
RPH	MEM	0.7DH	R/W	Bits 7 to 4 of register pointer
RPL	MEM	0.7EH	R/W	Bits 3 to 0 of register pointer
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD operation flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

3.2 DATA BUFFER

Symbol Name	At-trib-ute	Value	R/W	Description
DBF3	MEM	0.0CH	R/W	Bits 15 to 12 of data buffer
DBF2	MEM	0.0DH	R/W	Bits 11 to 8 of data buffer
DBF1	MEM	0.0EH	R/W	Bits 7 to 4 of data buffer
DBF0	MEM	0.0FH	R/W	Bits 3 to 0 of data buffer

3.3 LCD SEGMENT REGISTER

Symbol Name	At-trib-ute	Value	R/W	Description
LCDD19	MEM	2.5CH	R/W	LCD segment register
LCDD18	MEM	2.5DH	R/W	LCD segment register
LCDD17	MEM	2.5EH	R/W	LCD segment register
LCDD16	MEM	2.5FH	R/W	LCD segment register
LCDD15	MEM	2.60H	R/W	LCD segment register
LCDD14	MEM	2.61H	R/W	LCD segment register
LCDD13	MEM	2.62H	R/W	LCD segment register
LCDD12	MEM	2.63H	R/W	LCD segment register
LCDD11	MEM	2.64H	R/W	LCD segment register
LCDD10	MEM	2.65H	R/W	LCD segment register
LCDD9	MEM	2.66H	R/W	LCD segment register
LCDD8	MEM	2.67H	R/W	LCD segment register
LCDD7	MEM	2.68H	R/W	LCD segment register
LCDD6	MEM	2.69H	R/W	LCD segment register
LCDD5	MEM	2.6AH	R/W	LCD segment register
LCDD4	MEM	2.6BH	R/W	LCD segment register
LCDD3	MEM	2.6CH	R/W	LCD segment register
LCDD2	MEM	2.6DH	R/W	LCD segment register
LCDD1	MEM	2.6EH	R/W	LCD segment register
LCDD0	MEM	2.6FH	R/W	LCD segment register

3.4 PORT REGISTER

Symbol Name	At-trib-ute	Value	R/W	Description
POA2	FLG	0.70H.2	R/W	Bit 2 of port OA
POA1	FLG	0.70H.1	R/W	Bit 1 of port OA
POA0	FLG	0.70H.0	R/W	Bit 0 of port OA
POB3	FLG	0.71H.3	R/W	Bit 3 of port OB
POB2	FLG	0.71H.2	R/W	Bit 2 of port OB
POB1	FLG	0.71H.1	R/W	Bit 1 of port OB
POB0	FLG	0.71H.0	R/W	Bit 0 of port OB
POC3	FLG	0.72H.3	R/W	Bit 3 of port OC
POC2	FLG	0.72H.2	R/W	Bit 2 of port OC
POC1	FLG	0.72H.1	R/W	Bit 1 of port OC
POC0	FLG	0.72H.0	R/W	Bit 0 of port OC
POD3	FLG	0.73H.3	R/W	Bit 3 of port OD
POD2	FLG	0.73H.2	R/W	Bit 2 of port OD
POD1	FLG	0.73H.1	R/W	Bit 1 of port OD
POD0	FLG	0.73H.0	R/W	Bit 0 of port OD
P1A2	FLG	1.70H.2	R/W	Bit 2 of port 1A
P1A1	FLG	1.70H.1	R/W	Bit 1 of port 1A
P1A0	FLG	1.70H.0	R/W	Bit 0 of port 1A
P1B3	FLG	1.71H.3	R/W	Bit 3 of port 1B
P1B2	FLG	1.71H.2	R/W	Bit 2 of port 1B
P1B1	FLG	1.71H.1	R/W	Bit 1 of port 1B
P1B0	FLG	1.71H.0	R/W	Bit 0 of port 1B

(to be continued)

(cont'd)

Symbol Name	At-trib-ute	Value	R/W	Description
P1C3	FLG	1.72H.3	R/W	Bit 3 of port 1C
P1C2	FLG	1.72H.2	R/W	Bit 2 of port 1C
P1C1	FLG	1.72H.1	R/W	Bit 1 of port 1C
P1C0	FLG	1.72H.0	R/W	Bit 0 of port 1C
P1D3	FLG	1.73H.3	R/W	Bit 3 of port 1D
P1D2	FLG	1.73H.2	R/W	Bit 2 of port 1D
P1D1	FLG	1.73H.1	R/W	Bit 1 of port 1D
P1D0	FLG	1.73H.0	R/W	Bit 0 of port 1D
P2E0	FLG	2.5FH.0	R/W	Bit 0 of port 2E
P2F0	FLG	2.5EH.0	R/W	Bit 0 of port 2F
P2G0	FLG	2.5DH.0	R/W	Bit 0 of port 2G
P2H0	FLG	2.5CH.0	R/W	Bit 0 of port 2H

3.5 REGISTER FILE (CONTROL REGISTER)

Symbol Name	At-trib-ute	Value	R/W	Description
SP	MEM	0.81H	R/W	Stack pointer
SIO1TS	FLG	0.82H.3	R/W	SIO_1 start flag
SIO1HIZ	FLG	0.82H.2	R/W	POA_1/SO_1 pin selection flag
SIO1CK1	FLG	0.82H.1	R/W	SIO_1 clock select flag
SIO1CK0	FLG	0.82H.0	R/W	SIO_1 clock select flag
IFCG	FLG	0.84H.0	R	IF counter gate status flag
PLLUL	FLG	0.85H.0	R	PLL unlock FF flag
ADCCMP	FLG	0.86H.0	R	ADC judge flag
CE	FLG	0.87H.0	R	CE pin status flag
BTM0CK1	FLG	0.89H.3	R/W	Basic timer 0 clock select flag
BTM0CK0	FLG	0.89H.2	R/W	Basic timer 0 clock select flag
BTM1CK1	FLG	0.89H.1	R/W	Basic timer 1 clock select flag
BTM1CK0	FLG	0.89H.0	R/W	Basic timer 1 clock select flag
TMCK	FLG	0.8CH.0	R/W	Timer counter clock select flag
TMOVF	FLG	0.8DH.0	R	Timer overflow detection flag
TMRPT	FLG	0.8EH.2	R/W	Timer mode (repeat) select flag
TMRES	FLG	0.8EH.1	R/W	Timer reset flag
TMEN	FLG	0.8EH.0	R/W	Timer start/stop flag
KSEN	FLG	0.90H.2	R/W	Key source latch enable flag
LCDEN	FLG	0.90H.1	R/W	LCD enable flag
PYASEL	FLG	0.90H.0	R/W	Port YA select flag
P2HSEL	FLG	0.91H.3	R/W	Port 2H select flag
P2GSEL	FLG	0.91H.2	R/W	Port 2G select flag
P2FSEL	FLG	0.91H.1	R/W	Port 2F select flag

(to be continued)

(cont'd)

Symbol Name	At-trib-ute	Value	R/W	Description
P2ESEL	FLG	0.91H.0	R/W	Port 2E select flag
IFCMD1	FLG	0.92H.3	R/W	IF counter mode select flag
IFCMD0	FLG	0.92H.2	R/W	IF counter mode select flag
IFCCK1	FLG	0.92H.1	R/W	IF counter mode select flag
IFCCK0	FLG	0.92H.0	R/W	IF counter mode select flag
PWM1SEL	FLG	0.93H.1	R/W	POC_1/PWM_1 pin select flag
PWM0SEL	FLG	0.93H.0	R/W	POC_0/PWM_0 pin select flag
ADCCH1	FLG	0.94H.1	R/W	A/D converter channel select
ADCCH0	FLG	0.94H.0	R/W	A/D converter channel select
BEEP1SEL	FLG	0.95H.1	R/W	$POB_1/BEEP_1$ pin select flag
BEEP0SEL	FLG	0.95H.0	R/W	$POB_0/BEEP_0$ pin select flag
KEYJ	FLG	0.96H.0	R	Key input judge flag
BTM0CY	FLG	0.97H.0	R	Basic timer 0 carry flag
IEG	FLG	0.9FH.0	R/W	INT pin interrupt edge select flag
PLLMD1	FLG	0.0A1H.1	R/W	PLL mode select flag
PLLMD0	FLG	0.0A1H.0	R/W	PLL mode select flag
IFCSTRT	FLG	0.0A3H.1	R/W	IF counter start flag
IFCRES	FLG	0.0A3H.0	R/W	IF counter start flag
FCGCH1	FLG	0.0A4H.1	R/W	External counter channel select flag
FCGCH0	FLG	0.0A4H.0	R/W	External counter channel select flag
BEEP1CK1	FLG	0.0A5H.3	R/W	$BEEP_1$ clock select flag
BEEP1CK0	FLG	0.0A5H.2	R/W	$BEEP_1$ clock select flag
BEEP0CK1	FLG	0.0A5H.1	R/W	$BEEP_0$ clock select flag
BEEP0CK0	FLG	0.0A5H.0	R/W	$BEEP_0$ clock select flag

(to be continued)

(cont'd)

Symbol Name	At-trib-ute	Value	R/W	Description
P1DGIO	FLG	0.0A7H.0	R/W	Port ID group I/O select flag
IPSIO1	FLG	0.0AFH.3	R/W	SIO_1 interrupt enable flag
IPBTM1	FLG	0.0AFH.2	R/W	Basic timer 1 interrupt enable flag
IPTM	FLG	0.0AFH.1	R/W	Timer interrupt enable flag
IP	FLG	0.0AFH.0	R/W	INT pin interrupt enable flag
PLLRFCK3	FLG	0.0B1H.3	R/W	PLL reference clock select flag
PLLRFCK2	FLG	0.0B1H.2	R/W	PLL reference clock select flag
PLLRFCK1	FLG	0.0B1H.1	R/W	PLL reference clock select flag
PLLRFCK0	FLG	0.0B1H.0	R/W	PLL reference clock select flag
P1ABIO2	FLG	0.0B5H.2	R/W	$P1A_2$ pin input/output select flag
P1ABIO1	FLG	0.0B5H.1	R/W	$P1A_1$ pin input/output select flag
P1ABIO0	FLG	0.0B5H.0	R/W	$P1A_0$ pin input/output select flag
POBBIO3	FLG	0.0B6H.3	R/W	POB_3 pin input/output select flag
POBBIO2	FLG	0.0B6H.2	R/W	POB_2 pin input/output select flag
POBBIO1	FLG	0.0B6H.1	R/W	POB_1 pin input/output select flag
POBBIO0	FLG	0.0B6H.0	R/W	POB_0 pin input/output select flag
POABIO2	FLG	0.0B7H.2	R/W	POA_2 pin input/output select flag
POABIO1	FLG	0.0B7H.1	R/W	POA_1 pin input/output select flag
POABIO0	FLG	0.0B7H.0	R/W	POA_0 pin input/output select flag
IRQSIO1	FLG	0.0BCH.0	R/W	SIO_1 interrupt request flag
IRQBTM1	FLG	0.0BDH.0	R/W	Basic timer 1 interrupt request
IRQTM	FLG	0.0BEH.0	R/W	Timer interrupt request flag
INT	FLG	0.0BFH.3	R	INT pin interrupt status flag
IRQ	FLG	0.0BFH.3	R/W	INT pin interrupt request flag

3.6 PERIPHERAL REGISTER

Symbol Name	At-trib-ute	Value	R/W	Description
ADCR	DAT	02H	R/W	A/D converter reference voltage (V_{REF}) setting register
SIO1SFR	DAT	03H	R/W	SIO_1 presettable shaft register
PWMR0	DAT	04H	R/W	PWM0 data register
PWMR1	DAT	05H	R/W	PWM1 data register
AR	DAT	40H	R/W	GET/PUT/PUSH/CALL/BR/MOVT/MOVTH/MOVTL instruction address register
PLLR	DAT	41H	R/W	PLL data register
KSR	DAT	42H	R/W	Key source register
PYA	DAT	42H	R/W	PYA data register
IFC	DAT	43H	R	IF counter data register
TMM	DAT	46H	R/W	Timer module register
TMC	DAT	47H	R	Timer counter

3.7 RESERVED WORD LIST (IN ALPHABETICAL ORDER)

3.7.1 INSTRUCTIONS AND PSEUDO-INSTRUCTIONS

ADD	EXIT	NIBBLE5	SBMAC
ADDC	EXITR	NIBBLE5V	SET
AND	EXTRN	NIBBLE6	SET1
BANK0	FLG	NIBBLE6V	SET2
BANK1	GET	NIBBLE7	SET3
BANK2	GLOBAL	NIBBLE7V	SET4
BELOW	HALT	NIBBLE8	SFCOND
BR	IF	NIBBLE8V	SKE
C14344	IFCHAR	NOBMAC	SKF
C4444	IFNCHAR	NOLIST	SKF1
CALL	INC	NOMAC	SKF2
CASE	INCLUDE	NOP	SKF3
CLR1	INITFLG	NOT1	SKF4
CLR2	IRP	NOT2	SKGE
CLR3	LAB	NOT3	SKLT
CLR4	LBMAC	NOT4	SKNE
CSEG	LD	OBMAC	SKT
DAT	LFCOND	OMAC	SKT1
DB	LIST	OR	SKT2
DI	LITERAL	ORG	SKT3
DW	LMAC	OTHER	SKT4
EI	MACRO	PEEK	SMAC
EJECT	MEM	POKE	ST
ELSE	MOV	POP	STOP
END	MOVT	PUBLIC	SUB
ENDCASE	NIBBLE	PURGE	SUBC
ENDIF	NIBBLE1	PUSH	SUMMARY
ENDIFC	NIBBLE2	PUT	TAG
ENDIFNC	NIBBLE2V	REPT	TITLE
ENDM	NIBBLE3	RET	XOR
ENDP	NIBBLE3V	RETI	ZZZERROR
ENDR	NIBBLE4	RETSK	ZZZMCHK
EOF	NIBBLE4V	RORC	ZZZMSG

3.7.2 REGISTERS AND FLAGS

ADCCH0	IFC	LCDD19	P0D3
ADCCH1	IFCCK0	LCDD1	P1A0
ADCCMP	IFCCK1	LCDD2	P1A1
ADCR	IFCG	LCDD3	P1A2
AR	IFCMD0	LCDD4	P1ABIO0
AR0	IFCMD1	LCDD5	P1ABIO1
AR1	IFCRES	LCDD6	P1ABIO2
AR2	IFCSTRT	LCDD7	P1B0
AR3	INT	LCDD8	P1B1
AR_EPA0	IP	LCDD9	P1B2
AR_EPA1	IPBTM1	LCDEN	P1B3
BANK	IPSIO1	MPE	P1C0
BCD	IPTM	MPH	P1C1
BEEP0CK0	IRQ	MPL	P1C2
BEEP0CK1	IRQBTM1	P0A0	P1C3
BEEP0SEL	IRQSIO1	P0A1	P1D0
BEEP1CK0	IRQTM	P0A2	P1D1
BEEP1CK1	IX	P0ABIO0	P1D2
BEEP1SEL	IXE	P0ABIO1	P1D3
BTM0CK0	IXH	P0ABIO2	P1DGIO
BTM0CK1	IXL	P0B0	P2E0
BTM0CY	IXM	P0B1	P2ESEL
BTM1CK0	KEYJ	P0B2	P2F0
BTM1CK1	KSEN	P0B3	P2FSEL
CE	KSR	P0BBIO0	P2G0
CMP	LCDD0	P0BBIO1	P2GSEL
CY	LCDD10	P0BBIO2	P2H0
DBF	LCDD11	P0BBIO3	P2HSEL
DBF0	LCDD12	P0C0	PLLMD0
DBF1	LCDD13	P0C1	PLLMD1
DBF2	LCDD14	P0C2	PLLR
DBF3	LCDD15	P0C3	PLLRFCK0
FCGCH0	LCDD16	P0D0	PLLRFCK1
FCGCH1	LCDD17	P0D1	PLLRFCK2
IEG	LCDD18	P0D2	PLLRFCK3

PLLUL
PSW
PWM0SEL
PWM1SEL
PWMR0
PWMR1
PYA
PYASEL
RPH
RPL
SIO1CK0
SIO1CK1
SIO1HIZ
SIO1SFR
SIO1TS
SP
TMC
TMCK
TMEN
TMM
TMOVF
TMRES
TMRPT
WR
Z
ZZZ0
ZZZ1
ZZZ2
ZZZ3
ZZZ4
ZZZ5
ZZZ6
ZZZ7
ZZZ8
ZZZ9
ZZZDEVID
ZZZEPA
ZZZLSARG
ZZZPRINT
ZZZSKIP
ZZZSYDOC
ZZZALBMAC
ZZZALMAC
ZZZARGC
ZZZLINE