



富相科技股份有限公司

SOLOMON Goldentek Display Corp.


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PART NO : LM6063SYR
FOR MESSRS : _____

CONTENTS

NO.	ITEM	PAGE
1.	COVER	1
2.	RECORD OF REVISION	2
3.	GENERAL SPECIFICATIONS AND MECHANICAL DATA	3
4.	ABSOLUTE MAXIMUM RATINGS	4
5.	ELECTRICAL CHARACTERISTICS	5
6.	OPTICAL CHARACTERISTICS	6~7
7.	BLOCK DIAGRAM	8
8.	TIMING CHARACTERISTICS	9
9.	OUTLINE DIMENSION	10~11
10.	POWER SUPPLY FOR LCD MODULE	12
11.	DISPLAY CONTROL INSTRUCTIONS	13~21

Accepted by : _____

Proposed by :  _____

Date : 03,19,2002

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LM6063SYR

REV : 1

PAGE : 1

RECORD OF REVISION

DATE	PAGE	SUMMARY

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LM6063SYR

REV : 1

PAGE : 2

3. GENERAL SPECIFICATIONS AND MECHANICAL DATA.

3.1 GENERAL SPECIFICATIONS.

PLEASE REFER TO :

"CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS (SP-10-000)".

3.2 THIS INDIVIDUAL SPECIFICATIONS IS PRIOR TO GENERAL SPECIFICATIONS.

3.3 MECHANICAL DATA.

- (1) NUMBER OF DOTS ----- 240W*64H DOTS
- (2) MODULE SIZE ----- 140.0W*62.0H*8.5T (MAX.) mm
- (3) VIEWING AREA ----- 111.0W*39.0H mm
- (4) DOT SIZE ----- 0.40W*0.48H mm
- (5) DOT PITCH ----- 0.44W*0.53H mm
- (6) VIEWING DIRECTION ----- 6 O'CLOCK
- (7) LCD TYPE ----- STN, YELLOW-GREEN, REFLECTIVE

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LM6063SYR

REV : 1

PAGE : 3

4. ABSOLUTE MAXIMUM RATINGS.

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
POWER SUPPLY FOR LOGIC	VDD-VSS	----	---	6.0	V
INPUT VOLTAGE	VI	VSS	---	VDD	V
STATIC ELECTRICITY	-----	----	---	100	V

NOTE(1) : TEST METHOD AND CONDITIONS AFTER CHARGING UP 200PF CAPACITOR BY STATED VOLTAGE , THE CAPACITOR IS CONNECTED WITH INTERFACE PINS OF THE MODULE.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS.

ITEM	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	0°C	50°C	-20°C	60°C	NOTE (2)
HUMIDITY	NOTE (3)		NOTE (3)		WITHOUT CONDENSATION
VIBRATION	--	4.9 m/s ² (0.5G)	--	19.6 m/s ² (2G)	10~300HZ XYZ DIRECTIONS 1 Hr.EACH
SHOCK	--	29.4 m/s ² (3G)	--	49.0 m/s ² (5G)	10 mSEC XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE(2) : Ta AT -20°C : 48HR MAX.
60°C : 168HR MAX.

NOTE(3) : Ta ≤ 40°C : 90% RH MAX.
Ta > 40°C : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 40°C. (50% RH AT 50°C)

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LM6063SYR

REV : 1

PAGE : 4

5. ELECTRICAL CHARACTERISTICS.

Ta=25°C VDD = 5.0 ± 0.25V

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LOGIC CIRCUIT POWER SUPPLY VOLTAGE	VDD-VSS	-----	4.75	5.0	5.25	V
POWER SUPPLY FOR LCD DRIVING VOLTAGE	VOUT - VSS	VDD - VSS=5.0V	-----	-----	-10	V
OUTPUT VOLTAGE NOTE(1)	VOH	H LEVEL	2.4	-----	VDD	V
	VOL	L LEVEL	0	-----	0.4	
INPUT VOLTAGE NOTE (1)	VIH	H LEVEL	2.2	-----	VDD	V
	VIL	L LEVEL	0	-----	0.8	V
LOGIC CIRCUIT POWER SUPPLY	IDD	VDD-VSS=5.0V	-----	11.0	16.0	mA
RECOMMENDED LCD DRIVING VOLTAGE NOTE (3)	VDD - VO Φ=10° θ=0° DUTY = 1/64	Ta = 0°C	-----	(13.0)	-----	V
		Ta = 25°C	-----	12.5	-----	V
		Ta = 50°C	-----	(12.0)	-----	V

NOTE(1) : RS , R/W , E , \overline{CS} , \overline{RES} , DB0~DB7

NOTE(2) : RECOMMENDED LCD DRIVING VOLTAGE MAY FLUCTUATE
ABOUT ± 0.5V BY EACH MODULE.

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LM6063SYR

REV : 1

PAGE : 5

6. OPTICAL CHARACTERISTICS.

Ta = 25°C

VDD = 5.0±0.25V

VDD - VO = 12.5V

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
VIEWING AREA	$\Phi 2 - \Phi 1$	$K \geq 1.4$	20	30	---	deg.	1,2
CONTRAST RATIO	K	$\Phi = 10^\circ$ $\theta = 0^\circ$	---	2	---	---	3
RESPONSE TIME	tr(rise)	$\Phi = 10^\circ$ $\theta = 0^\circ$	---	250	---	ms	4
	tf(fall)	$\Phi = 10^\circ$ $\theta = 0^\circ$	---	400	---	ms	4

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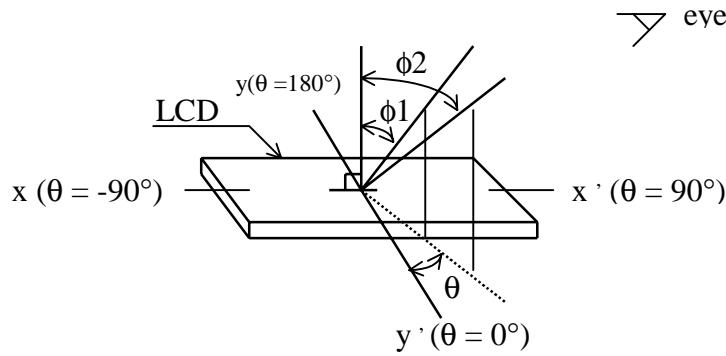
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REV : 1

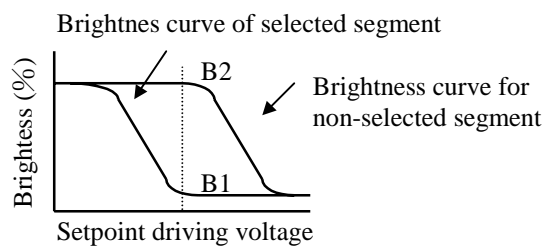
PAGE : 6

NOTE (1) : THE DEFINITION OF VIEWING ANGLE Φ AND θ

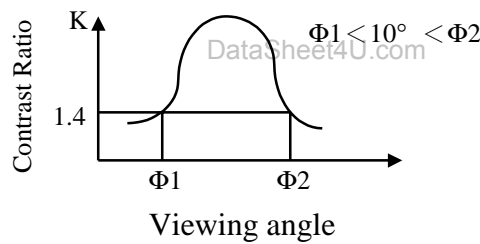


NOTE (2) : DEFINITION OF CONTRAST "K"

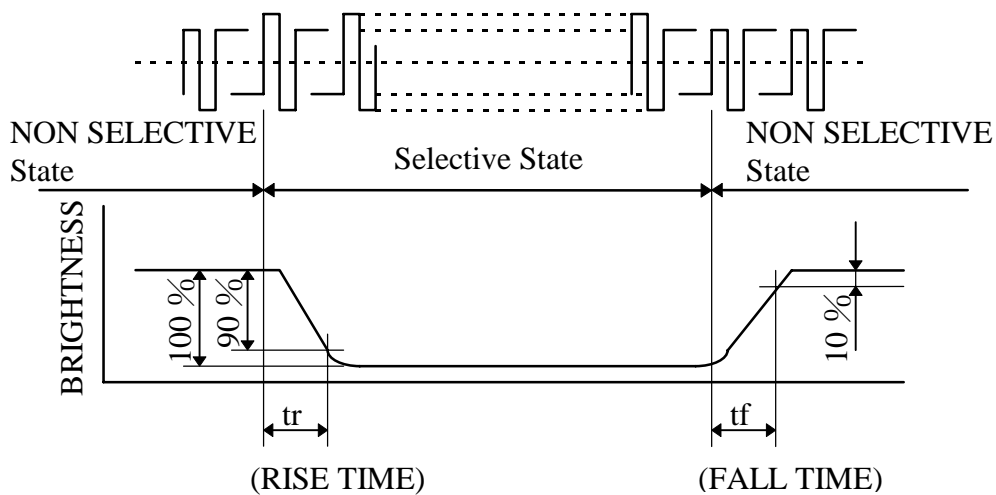
$$K = \frac{\text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$



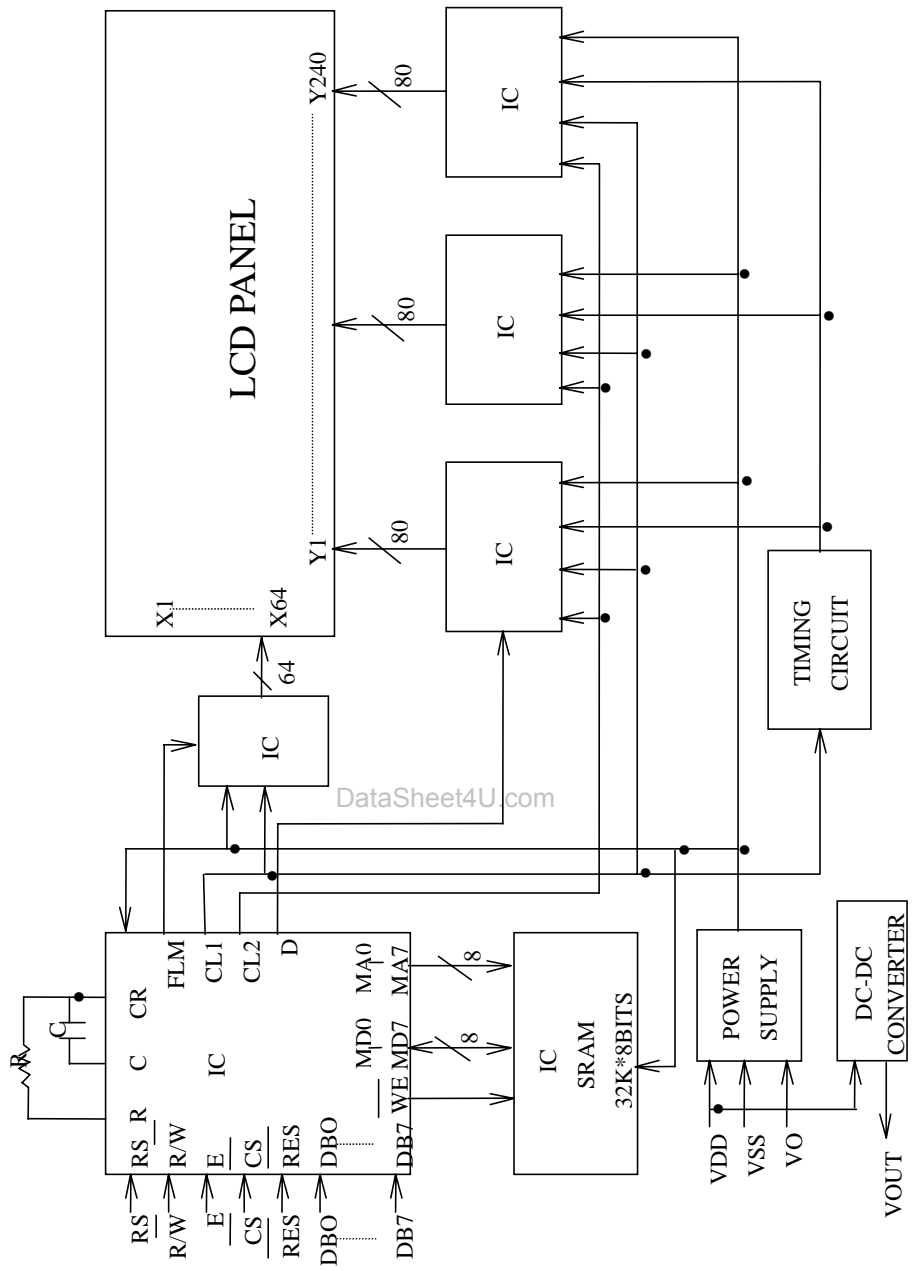
NOTE (3) : THE DEFINITION OF VIEWING Φ_1 AND Φ_2



NOTE (4) : THE DEFINITION OF OPTICAL RESPONSE

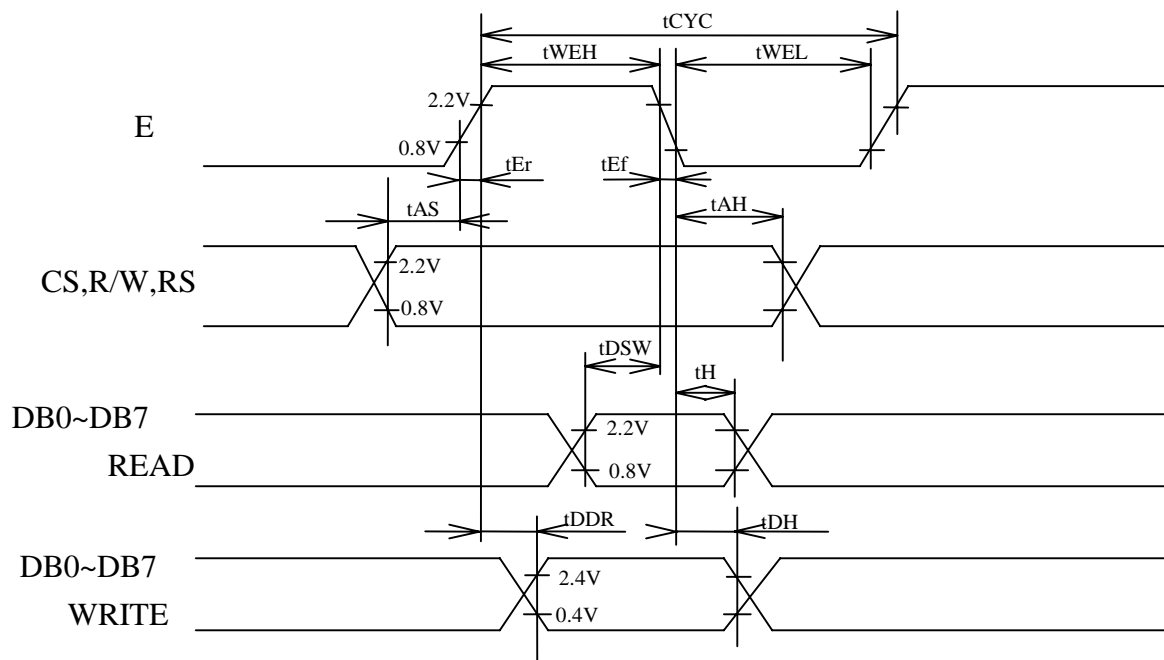


7. BLOCK DIAGRAM.



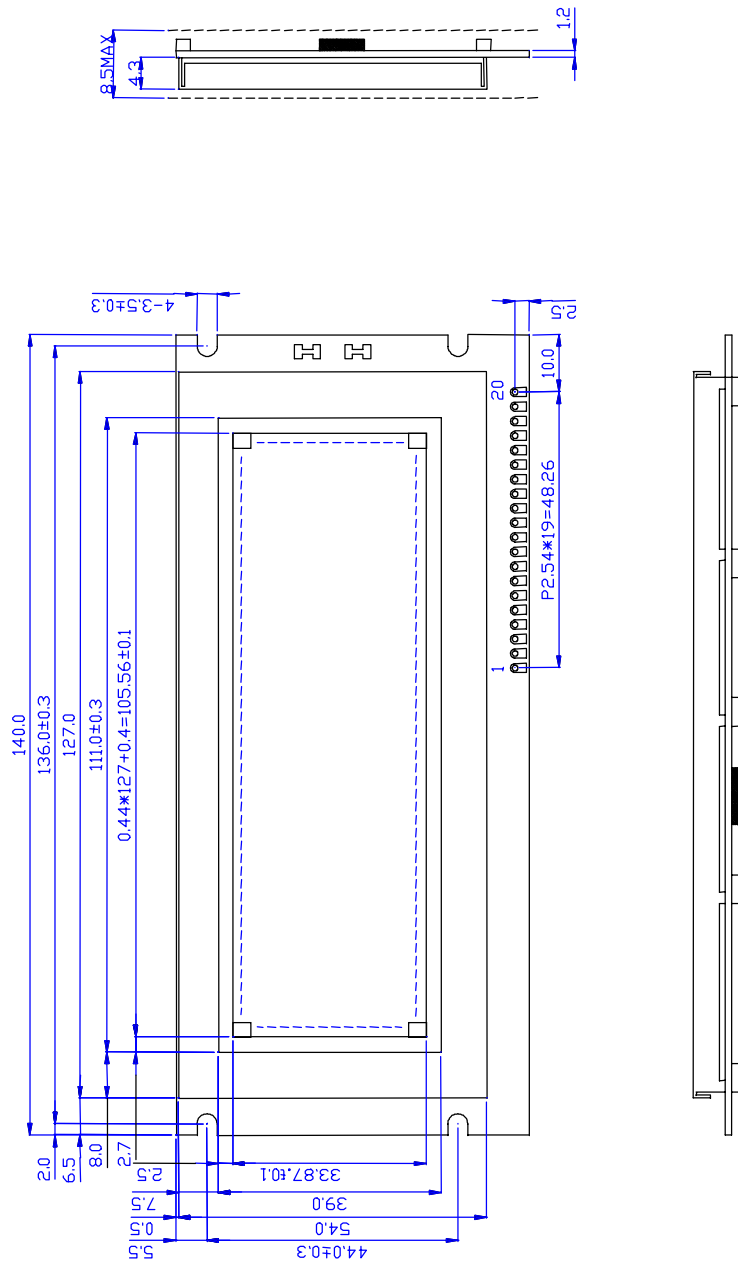
8. TIMING CHARACTERISTICS.

BUS READ/WRITE OPERATION (INTERFACE TO MPU)



ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
ENABLE CYCLE TIME	t_{CYC}	1.0	—	—	μs
ENABLE PULSE WIDTH	“H”LEVEL	0.45	—	—	μs
	“L”LEVEL	0.45	—	—	μs
ENABLE RISE TIME	t_{Er}	—	—	25	ns
ENABLE FALL TIME	t_{Ef}	—	—	25	ns
SETUP TIME	t_{AS}	140	—	—	ns
DATA SETUP TIME	t_{DSW}	225	—	—	ns
DATA DELAY TIME	t_{DDR}	—	—	225	ns
DATA HOLD TIME	t_H	10	—	—	ns
ADDRESS HOLD TIME	t_{AH}	10	—	—	ns
DATA HOLD TIME	t_{DH}	20	—	—	ns

9. OUTLINE DIMENSION.



UNIT:mm
 SCALE:1:1
 NOTE:IND SPECIFIED TOLERANCE IS +0.5

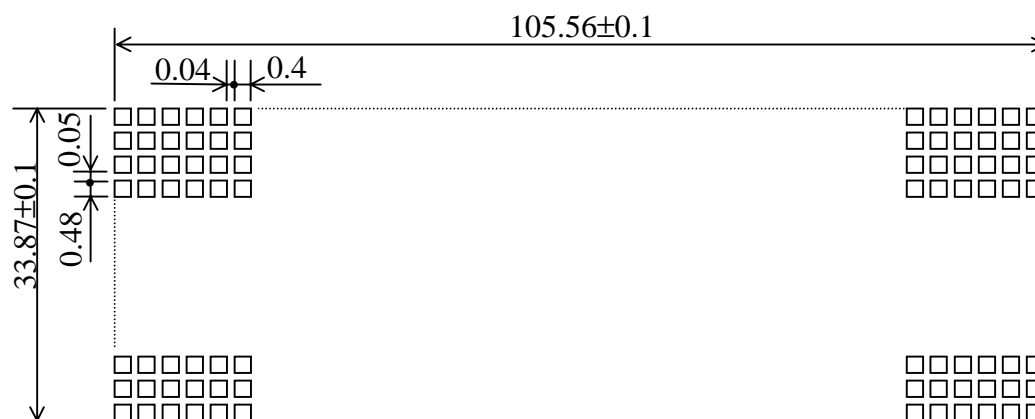
↑
 60°CLOCK

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LM6063SYR

REV : 1

PAGE : 10

NOTE1. DETAIL DRAWING OF MATRIX PATTERN.

UNIT : mm

SCALE : NTS

NO SPECIFIED TOLERANCE : ±0.01

NOTE2. INTERFACE PIN CONNECTION.

PIN NO.	SYMBOL	LEVEL	FUNCTION
1	VSS	-----	GND
2	VDD	-----	POWER SUPPLY FOR LOGIC CIRCUIT
3	VO	-----	OPERATING VOLTAGE FOR LCD DRIVING
4	RS	H/L	REGISTER SELECT
5	R/W	H/L	READ/WRITE
6	E	H/L	ENABLE
7	DB0	H/L	DATA BUS
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	\overline{CS}	L	CHIP ENABLE
16	\overline{RES}	L	RESET
17	VOUT	-----	POWER SUPPLY FOR LCD DRIVING
18	NC	-----	NOT USED
19	NC	-----	NOT USED
20	NC	-----	

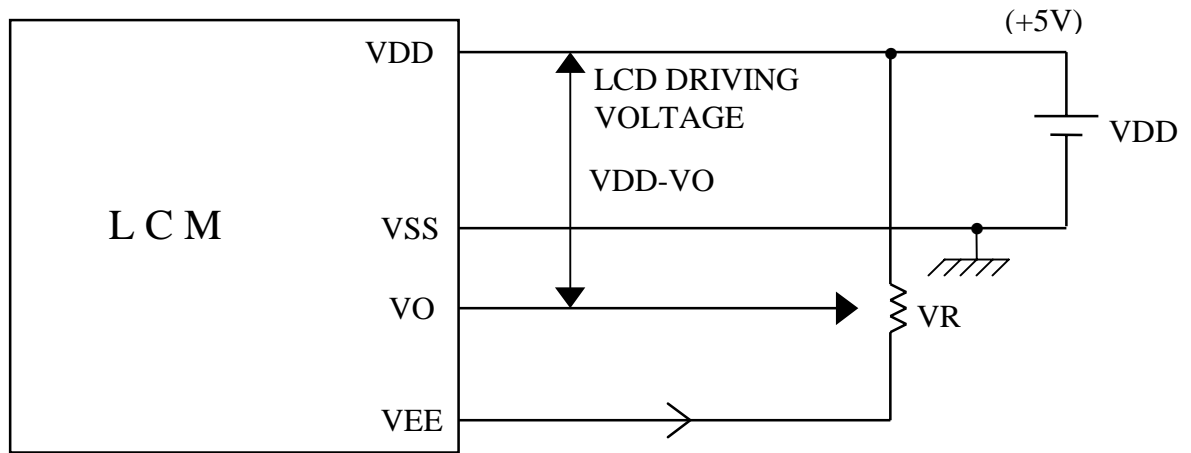
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LM6063SYR

REV : 1

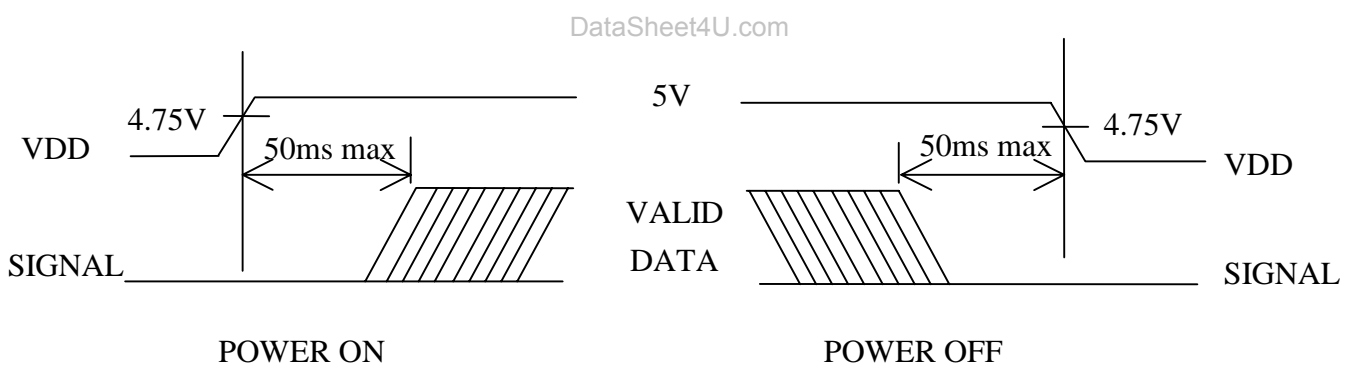
PAGE : 11

10. POWER SUPPLY FOR LCD MODULE.



VR : 10KΩ ~ 20KΩ

10.1 POWER AND INTERFACE TIMING SEQUENCE.



11. Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS=1, and the code of data register is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS=0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

(1) Mode control

code \$ "00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor OFF	Instruction CG	character display (character mode)
		0	1			Cursor ON		
		1	0			Cursor OFF,character blink		
		1	1			Cursor blink		
		0	0		1	External CG	Cursor OFF	
		0	1				Cursor ON	
		1	0				Cursor OFF,character blink	
		1	1				Cursor blink	
		0	0	1	0	Cursor OFF	External CG	Graphic mode
Display ON/OFF	Master/slave	Blink	Cursor	Graphic/ character mode	Ext./Int. CG			

- 1: Master mode
 0: Slave mode
 1: Display ON
 0: Display OFF

(2) Set character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.,	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(Vp - 1) binary				0	(Hp - 1) binary		

Vp indicates the number of vertical dots per character .The space between the vertically-displayed characters is considered for determination .

This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode .

The Hp indicates the number of horizontal dots per character in display , including the space between horizontally-displayed characters . In the graphic mode , the Hp indicates the number of bits of 1-byte display data to be displayed .

There are three Hp values .

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	Horizontal character pitch 7
8	1	1	1	Horizontal character pitch 8

(3) Set number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-character reg.	0	0	0	(HN- 1) binary						

HN indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode . If the total sum of horizontal dots on the screen is taken as n ,

$$n = H_p \times H_N$$

HN can be set with an even number of 2 to 128 (decimal).

(4) Set number of time division (inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Cursor position reg.	0	0	0	(Nx - 1) binary						

Nx indicates the number of time division in multiplex display .

1/Nx is a display duty ratio .

A value of 1 to 128 (decimal) can be set to Nx .

(5) Set cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	(Cp - 1) binary				

Cp indicates the position in a character where the cursor is displayed in the character mode . For example , in 5× 7 dot font , the cursor is displayed under a character by specifying Cp=8 (decimal) . The cursor horizontal length is equal to the horizontal character pitch Hp . A value of 1 to 16 (decimal) can be set to Cp . If a smaller value than the number of vertical character pitches Vp is set ($Cp \leq Vp$) , and a character is overlapped with the cursor , the cursor has higher priority of display (at cursor display ON) . If Cp is greater than Vp , no cursor is display . The cursor horizontal length is equal to Hp .

(6) Set display start low order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Cursor position reg. (low order byte)	0	0	(Start low order address) binary							

(7) Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Cursor position reg. (high order byte)	0	0	(Start high order address) binary							

These instructions cause display start addresses to be written in the display start address registers . The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored . In the graphic mode , the start address is composed of high/ low order 16 bits . In the character display , it is composed of the lower 4 bits of high order address (DB3~DB0) and 8 bits of low order address . The upper 4 bits of high order address are ignored .

(8) Set cursor address (low order) (RAM write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

(9) Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor addresses to be written in the cursor address counters . The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM . Namely , data at address specified by the cursor address are read/written . In the character mode , the cursor is display at the digit specified by the cursor address .

A cursor address consists of the low-order address (8 bit) and the high- order address (8 bit) . Satisfy the following requirements .
When setting the cursor address .

1.	when you want to rewrite (set) both the low order address and the high order address .	Set the low order address and then set the high order address .
2.	When you want to rewrite only the low order address .	Don't fail to set high order address again after setting the low order address .
3.	When you want to rewrite only the high order address .	Set the high order address . You don't have to set the low order address again .

The cursor address counter is a 16 bit up-counter with SET and RESET functions . When the bit N changes from 1 to 0 , the bit N+1 is added by 1 . When setting the low order address , the LSB (bit 1) of the high order address is added by 1 if the MSB (bit 8) of the low order address changes from 1 to 0 . Therefore , set both the low order address and the high order address as shown in above table .

(10) Write display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg. .	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data , character code) LSB							

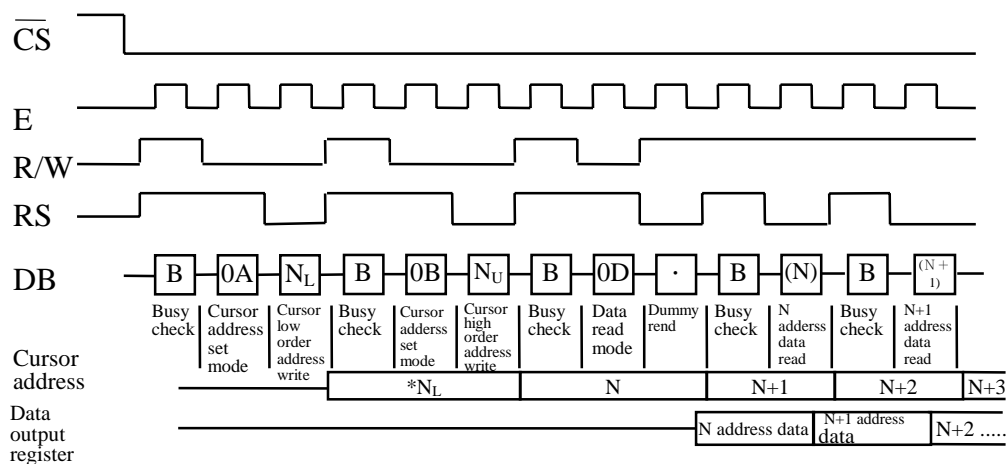
After the code \$ 'OC' is written into the instruction register with RS=1 8 bit data with RS=0 should be written into the data register . This data is transferred to the RAM specified by the cursor address as display data or character code . The cursor address is increased by 1 after this operation .

(11) Read display data

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Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg. .	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data , character code) LSB							

Data can be read from the RAM with RS=0 after writing code \$ 'OD' into the instruction register . The read procedure is as follows :



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LM6063SYR

REV : 1

PAGE : 17

This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register , also increasing the cursor address by 1. After setting the cursor address , correct data is not output at the first read but at the second time . Thus , make one dummy read when reading data after setting the cursor address .

(12) Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg. .	0	1	0	0	0	0	1	1	1	0
Bit clear reg. .	0	0	0	0	0	0	0	(N _B -1) binary		

(13) Set bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg. .	0	1	0	0	0	0	1	1	1	1
Bit clear reg. .	0	0	0	0	0	0	0	(N _B -1) binary		

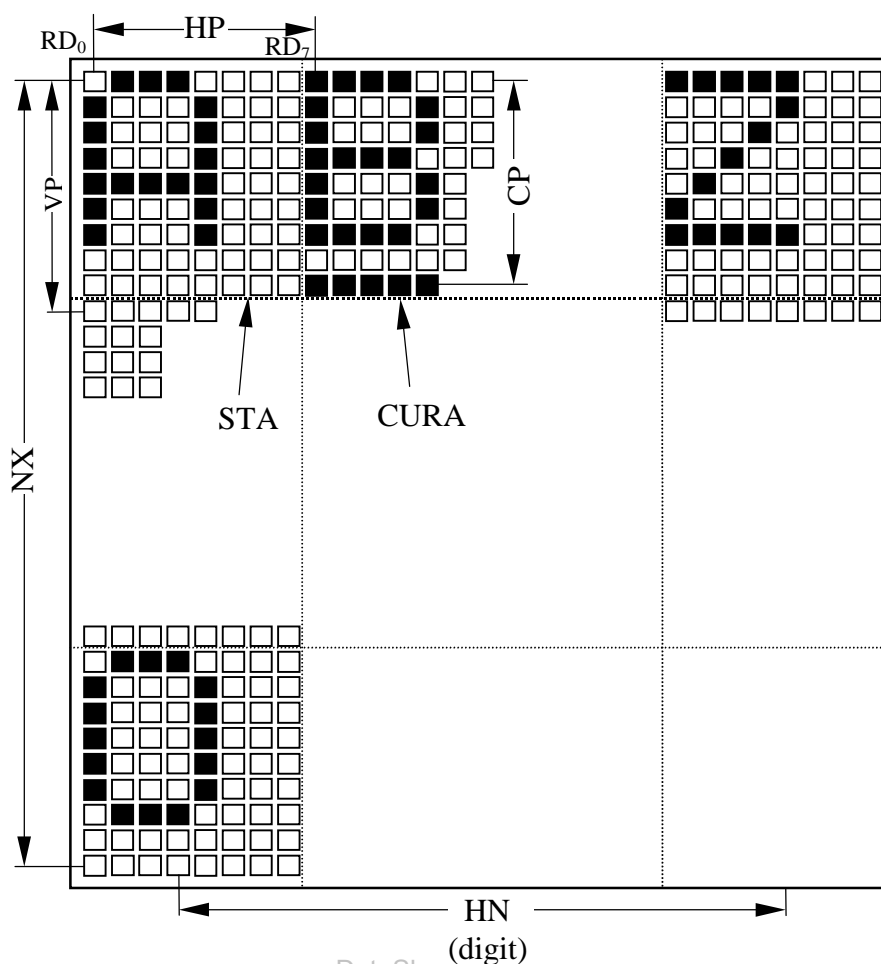
The Clear/Set Bit instruction sets 1 bit in a byte of display data RAM to 0 or 1 , respectively . The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address . After the execution of the instruction , the cursor address is automatically increased by 1. N_B is a value of 1 to 8 . N_B=1 and N_B=8 indicates LSB and MSB , respectively .

(14) Read busy flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0	*						

When the read mode is set with RS=1 , the busy flag is output to DB7 . The busy flag is set to 1 during the execution of any of instructions (1) to (13) . After the execution , it is set to 0 . The next instruction can be accepted . No instruction can be accepted when busy flag = 1. Before executing an instruction or writing data , perform a busy flag check to make sure the busy flag is 0 . When data is written in the register (RS=1) , busy flag doesn't change . Thus , no busy flag check is required just after the write operation into the instruction register with RS = 1 .

The busy flag can be read without specifying any instruction register .



Symbol	Name	Meaning	Value
H_P	Horizontal character pitch	Lateral character pitch	6 to 8 dots
H_N	Number or horizontal characters	Number of lateral characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode .	2 to 128 digits (an even number)
V_P	Vertical character pitch	Longitudinal character pitch	1 to 16 dots
C_P	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_X	Number of time division	Inverse of display duty ratio	1 to 128 lines

Note : If the number of vertical dots on screen is taken as m , and the number of horizontal dots as n ,

$$1/m = 1/N_X = \text{display duty ratio}$$

$$n = H_P \times H_N , m/V_P = \text{Number of display lines}$$

$$C_P \leq V_P$$

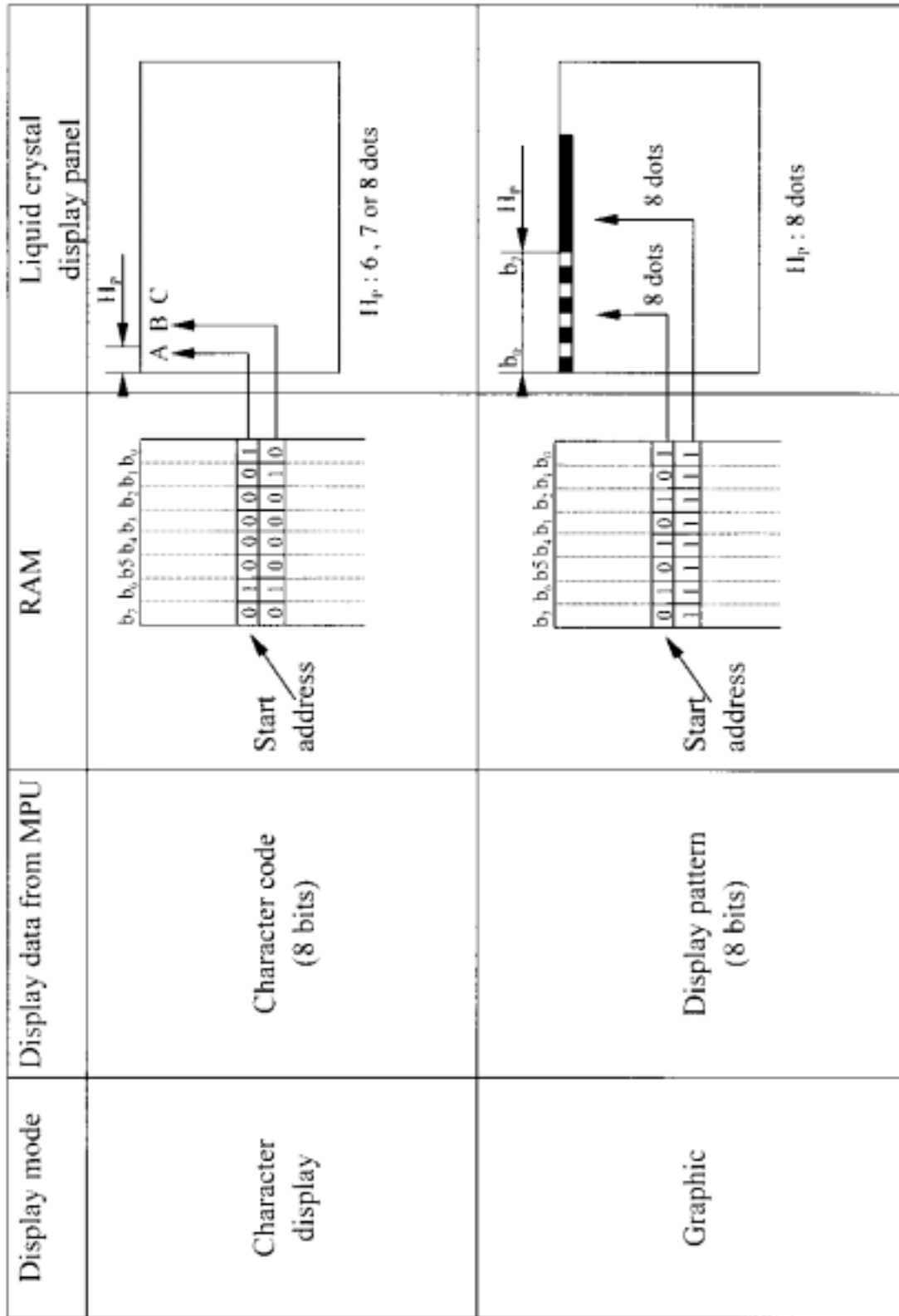
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LM6063SYR

REV : 1

PAGE : 19

(15) Display Mode



(16) Internal Character Generator Patterns and Character Codes

Lower 4 bits \ Higher 4 bits	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	0	1	2	3	4	5	6	7	8	9	A	B
xxxx0001	C	D	E	F	G	H	I	J	K	L	M	N
xxxx0010	O	P	Q	R	S	T	U	V	W	X	Y	Z
xxxx0011	[\]	^	_	`	{		}	~		
xxxx0100												
xxxx0101												
xxxx0110								¡	¢	£	¤	¥
xxxx0111	¦	§	¨	©	ª	«	¬	­	®	¯	°	±
xxxx1000	²	³	´	µ	¶	·	¸	¹	º	»	¼	½
xxxx1001	¾	¿										
xxxx1010												
xxxx1011												¡
xxxx1100	¢	£	¤	¥	¦	§	¨	©	ª	«	¬	­
xxxx1101	®	¯	°	±	²	³	´	µ	¶	·	¸	¹
xxxx1110	º	»	¼	½	¾	¿						
xxxx1111												