

**Document Title****64Kx36-Bit Synchronous Pipelined Burst SRAM, 3.3V Power  
Datasheets for 100TQFP****Revision History**

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	May. 19. 1998	Preliminary
0.1	Change t <sub>OH</sub> Min value from 1.3 to 1.0 at t <sub>CYC</sub> 5.0 Change t <sub>HZC</sub> Min value from 1.3 to 1.0 at t <sub>CYC</sub> 5.0	July. 13. 1998	Preliminary
0.2	Add t <sub>CYC</sub> 183MHz, 225MHz Change DC Characteristics. I <sub>CC</sub> value from 260mA to 280mA at -72 I <sub>SB1</sub> value from 10mA to 20mA I <sub>SB2</sub> value from 10mA to 20mA	Aug. 31. 1998	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

**64Kx36-Bit Synchronous Pipelined Burst SRAM**

**FEATURES**

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V + 0.3V / -0.165V$  Power Supply
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$  Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$ ,  $\overline{ADSC}$ ,  $\overline{ADV}$  Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A

**FAST ACCESS TIMES**

Parameter	Symbol	-44	-50	-55	-60	-67	-72	Unit
Cycle Time	tcyc	4.4	5.0	5.4	6.0	6.7	7.2	ns
Clock Access Time	tcd	3.1	3.1	3.1	3.5	3.8	4.0	ns
Output Enable Access Time	toE	3.1	3.1	3.1	3.5	3.8	4.0	ns

**GENERAL DESCRIPTION**

The KM736V689A is a 2,359,296-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications;  $\overline{GW}$ ,  $\overline{BW}$ ,  $\overline{LBO}$ , ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by  $\overline{GW}$ , and each byte write is performed by the combination of  $\overline{WEx}$  and  $\overline{BW}$  when  $\overline{GW}$  is high. And with  $\overline{CS1}$  high,  $\overline{ADSP}$  is blocked to control signals.

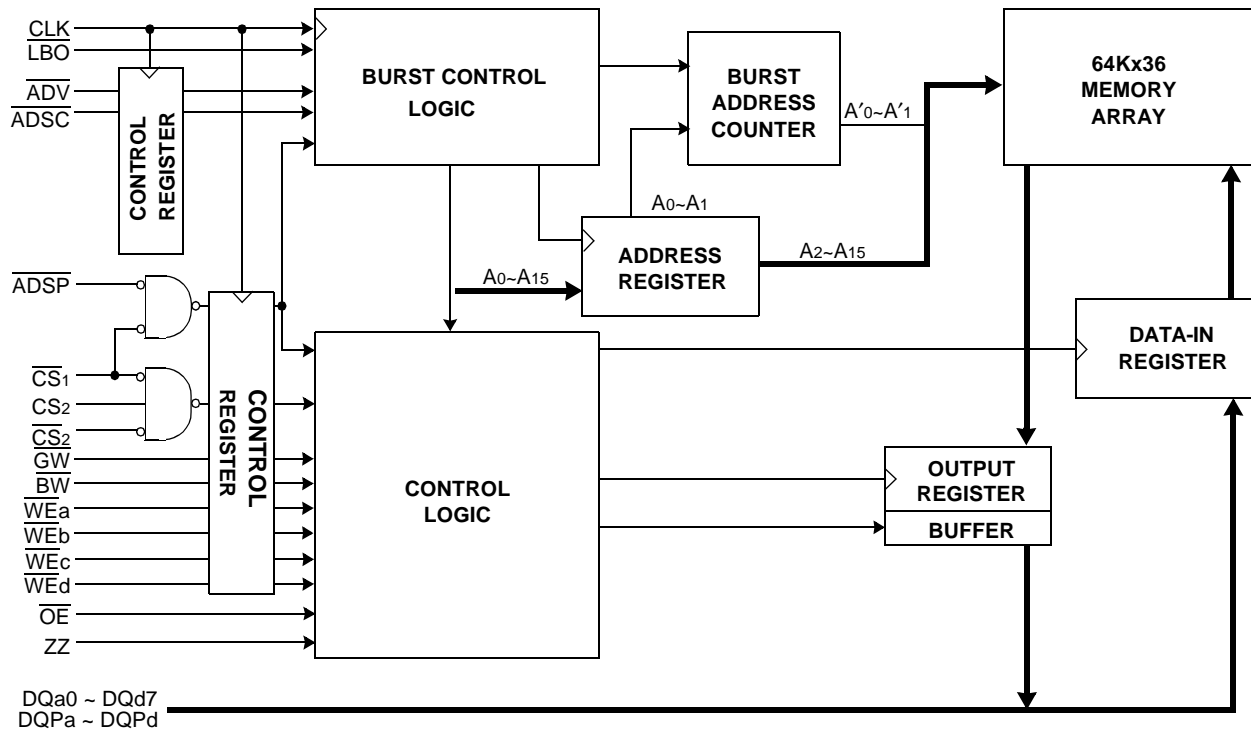
Burst cycle can be initiated with either the address status processor( $\overline{ADSP}$ ) or address status cache controller( $\overline{ADSC}$ ) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance( $\overline{ADV}$ ) input.

$\overline{LBO}$  pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

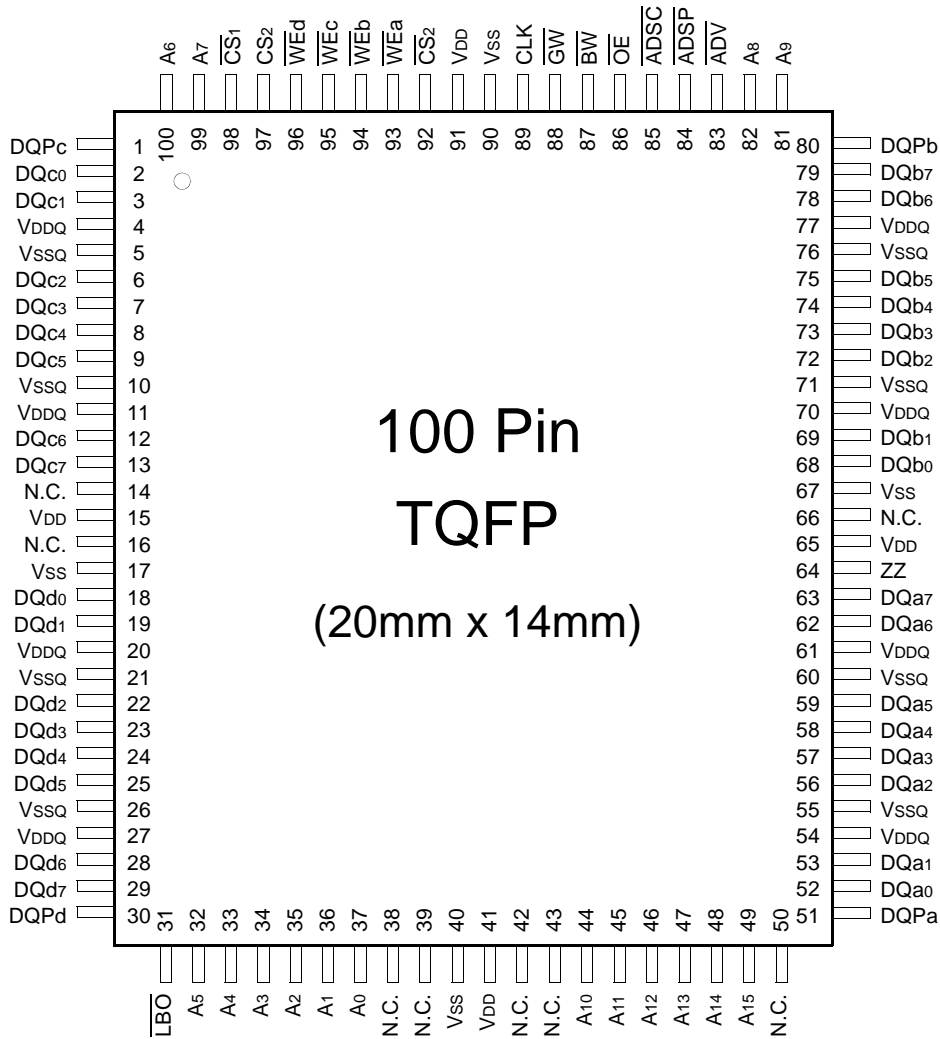
The KM736V689A is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

**LOGIC BLOCK DIAGRAM**



DQa0 ~ DQd7  
DQPa ~ DQPd

**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0-A15	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,81,82,99,100	V <sub>DD</sub>	Power Supply(+3.3V)	15,41,65,91
			V <sub>SS</sub>	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,50,66
$\overline{ADV}$	Burst Address Advance	83	DQa <sub>0</sub> ~a <sub>7</sub>	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSP}$	Address Status Processor	84	DQb <sub>0</sub> ~b <sub>7</sub>		68,69,72,73,74,75,78,79
$\overline{ADSC}$	Address Status Controller	85	DQc <sub>0</sub> ~c <sub>7</sub>		2,3,6,7,8,9,12,13
CLK	Clock	89	DQd <sub>0</sub> ~d <sub>7</sub>		18,19,22,23,24,25,28,29
$\overline{CS1}$	Chip Select	98	DQPa~Pd		51,80,1,30
$\overline{CS2}$	Chip Select	97	V <sub>DDQ</sub>	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{CS2}$	Chip Select	92	V <sub>SSQ</sub>	Output Ground	5,10,21,26,55,60,71,76
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
LBO	Burst Mode Control	31			

**FUNCTION DESCRIPTION**

The KM736V689A is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of  $\overline{OE}$ ,  $\overline{LBO}$  and  $\overline{ZZ}$ ) are sampled on rising clock edges. The start and duration of the burst access is controlled by  $\overline{ADSC}$ ,  $\overline{ADSP}$  and  $\overline{ADV}$  and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with  $\overline{ADV}$ .

When  $\overline{ZZ}$  is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When  $\overline{ZZ}$  returns to low, the SRAM normally operates after 2 cycles of wake up time.  $\overline{ZZ}$  pin is pulled down internally.

Read cycles are initiated with  $\overline{ADSP}$ (regardless of  $\overline{WEx}$  and  $\overline{ADSC}$ ) using the new external address clocked into the on-chip address register whenever  $\overline{ADSP}$  is sampled low, the chip selects are sampled active, and the output buffer is enabled with  $\overline{OE}$ . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of  $\overline{CLK}$ , are carried to the Data-out buffer by the next positive edge of  $\overline{CLK}$ . The data, registered in the Data-out buffer, are projected to the output pins.  $\overline{ADV}$  is ignored on the clock edge that samples  $\overline{ADSP}$  asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when  $\overline{WEx}$  are sampled High and  $\overline{ADV}$  is sampled low. And  $\overline{ADSP}$  is blocked to control signals by disabling  $\overline{CS1}$ .

All byte write is done by  $\overline{GW}$ (regardless of  $\overline{BW}$  and  $\overline{WEx}$ ), and each byte write is performed by the combination of  $\overline{BW}$  and  $\overline{WEx}$  when  $\overline{GW}$  is high.

Write cycles are performed by disabling the output buffers with  $\overline{OE}$  and asserting  $\overline{WEx}$ .  $\overline{WEx}$  are ignored on the clock edge that samples  $\overline{ADSP}$  low, but are sampled on the subsequent clock edges. The output buffers are disabled when  $\overline{WEx}$  are sampled Low(regardless of  $\overline{OE}$ ). Data is clocked into the data input register when  $\overline{WEx}$  sampled Low. The address increases internally to the next address of burst, if both  $\overline{WEx}$  and  $\overline{ADV}$  are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals( $\overline{WEa}$ ,  $\overline{WEb}$ ,  $\overline{WEc}$  or  $\overline{WEd}$ ) sampled low. The  $\overline{WEa}$  control  $DQa0 \sim DQa7$  and  $DQPa$ ,  $\overline{WEb}$  controls  $DQb0 \sim DQb7$  and  $DQPb$ ,  $\overline{WEc}$  controls  $DQc0 \sim DQc7$  and  $DQPc$ , and  $\overline{WEd}$  control  $DQd0 \sim DQd7$  and  $DQPd$ . Read or write cycle may also be initiated with  $\overline{ADSC}$ , instead of  $\overline{ADSP}$ . The differences between cycles initiated with  $\overline{ADSC}$  and  $\overline{ADSP}$  as are follows;

$\overline{ADSP}$  must be sampled high when  $\overline{ADSC}$  is sampled low to initiate a cycle with  $\overline{ADSC}$ .  
 $\overline{WEx}$  are sampled on the same clock edge that sampled  $\overline{ADSC}$  low(and  $\overline{ADSP}$  high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the  $\overline{LBO}$  pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

**BURST SEQUENCE TABLE**

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.

**TRUTH TABLES**

**SYNCHRONOUS TRUTH TABLE**

$\overline{CS}_1$	$CS_2$	$\overline{CS}_2$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- NOTE : 1. X means "Don't Care".  
 2. The rising edge of clock is symbolized by ↑.  
 3.  $\overline{WRITE} = L$  means Write operation in WRITE TRUTH TABLE.  
 $\overline{WRITE} = H$  means Read operation in WRITE TRUTH TABLE.  
 4. Operation finally depends on status of asynchronous input pins(ZZ and  $\overline{OE}$ ).

**WRITE TRUTH TABLE**

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- NOTE : 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

**ASYNCHRONOUS TRUTH TABLE**

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

- NOTE  
 1. X means "Don't Care".  
 2. ZZ pin is pulled down internally  
 3. For write cycles that following read cycles, the output buffers must be disabled with  $\overline{OE}$ , otherwise data bus contention will occur.  
 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.  
 5. Deselected means power down state of which stand-by current depends on cycle time.

**PASS-THROUGH TRUTH TABLE**

Previous Cycle		Present Cycle				Next Cycle
Operation	WRITE	Operation	$\overline{CS}_1$	WRITE	OE	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

**ABSOLUTE MAXIMUM RATINGS\***

Parameter	Symbol	Rating	Unit
Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.3 to 4.6	V
Voltage on V <sub>DDQ</sub> Supply Relative to V <sub>SS</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V
Voltage on Input Pin Relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.3 to 6.0	V
Voltage on I/O Pin Relative to V <sub>SS</sub>	V <sub>IO</sub>	-0.3 to V <sub>DDQ</sub> +0.5	V
Power Dissipation	P <sub>D</sub>	1.2	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>OPR</sub>	0 to 70	°C
Storage Temperature Range Under Bias	T <sub>BIAS</sub>	-10 to 85	°C

\*NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS (0°C ≤ T<sub>A</sub> ≤ 70°C)**

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V <sub>DD</sub>	3.135	3.3	3.6	V
	V <sub>DDQ</sub>	3.135	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V

**CAPACITANCE\*** (T<sub>A</sub>=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	5	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> =0V	-	7	pF

\*NOTE : Sampled not 100% tested.

**DC ELECTRICAL CHARACTERISTICS**( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$ )

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	IIL	$V_{DD}=\text{Max}$ ; $V_{IN}=V_{SS}$ to $V_{DD}$	-2	+2	$\mu\text{A}$	
Output Leakage Current	IOL	Output Disabled, $V_{OUT}=V_{SS}$ to $V_{DDQ}$	-2	+2	$\mu\text{A}$	
Operating Current	ICC	Device Selected, $I_{OUT}=0\text{mA}$ , $ZZ \leq V_{IL}$ , All Inputs= $V_{IL}$ or $V_{IH}$ Cycle Time $\geq t_{CYC}$ min	-44	-	440	mA
			-50	-	400	
			-55	-	380	
			-60	-	360	
			-67	-	320	
Standby Current	ISB	Device deselected, $I_{OUT} = 0\text{mA}$ , $ZZ \leq V_{IL}$ , $f = \text{Max}$ , All Inputs $\leq 0.2\text{V}$ or $\geq V_{DD}-0.2\text{V}$	-44	-	110	mA
			-50	-	100	
			-55	-	100	
			-60	-	90	
			-67	-	80	
	ISB1	Device deselected, $I_{OUT} = 0\text{mA}$ , $ZZ \leq 0.2\text{V}$ , $f=0$ , All Inputs=fixed ( $V_{DD}-0.2\text{V}$ or $0.2\text{V}$ )	-	-	20	mA
	ISB2	Device deselected, $I_{OUT}=0\text{mA}$ , $ZZ \geq V_{DD}-0.2\text{V}$ , $f = \text{Max}$ , All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	-	20	mA
Output Low Voltage	VOL	$I_{OL} = 8.0\text{mA}$	-	0.4	V	
Output High Voltage	VOH	$I_{OH} = -4.0\text{mA}$	2.4	-	V	
Input Low Voltage	VIL		-0.5*	0.8	V	
Input High Voltage	VIH		2.0	$V_{DD}+0.5^{**}$	V	

\*  $V_{IL}(\text{Min})=-2.0(\text{Pulse Width} \leq t_{CYC}/2)$   
 \*\*  $V_{IH}(\text{Max})=4.6(\text{Pulse Width} \leq t_{CYC}/2)$   
 \*\* In Case of I/O Pins, the Max.  $V_{IH}=V_{DDQ}+0.5\text{V}$

**TEST CONDITIONS**

( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$ , unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

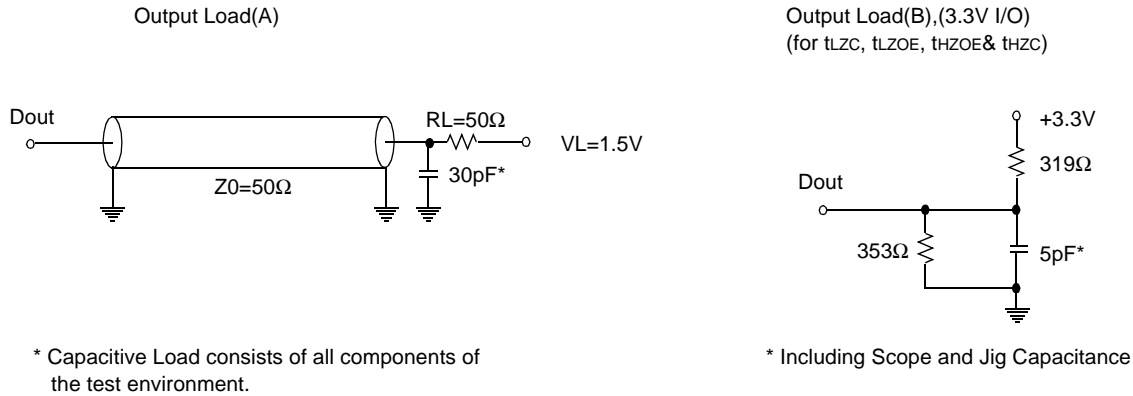


Fig. 1

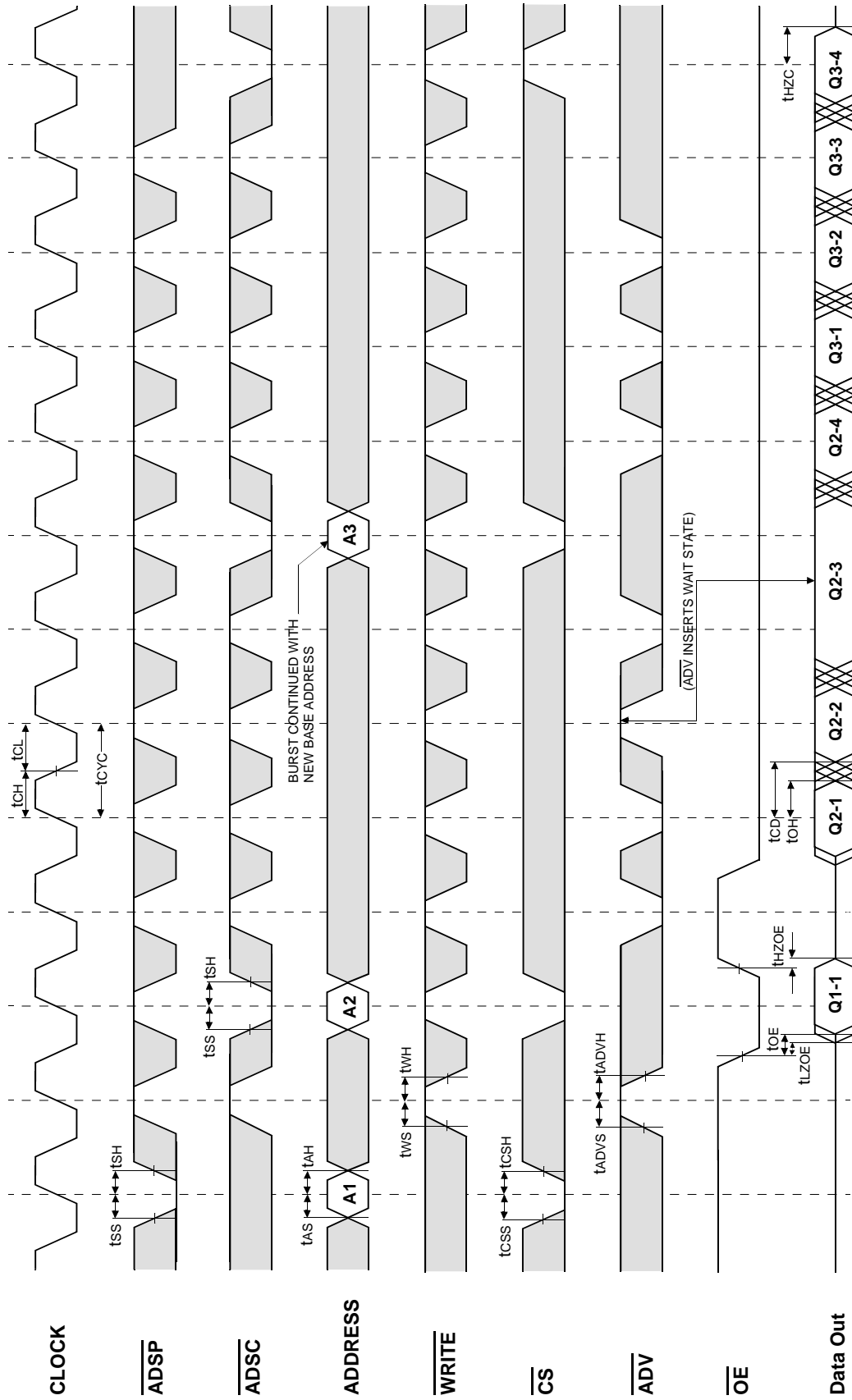
**AC TIMING CHARACTERISTICS**  
(VDD=3.3V+0.3V/-0.165V, TA=0 to 70°C)

Parameter	Symbol	-44		-50		-55		-60		-67		-72		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	4.4	-	5.0	-	5.4	-	6.0	-	6.7	-	7.2	-	ns
Clock Access Time	tCD	-	3.1	-	3.1	-	3.1	-	3.5	-	3.8	-	4.0	ns
Output Enable to Data Valid	tOE	-	3.1	-	3.1	-	3.1	-	3.5	-	3.8	-	4.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.0	-	1.0	-	1.0	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.1	-	3.1	-	3.1	-	3.5	-	3.8	-	4.0	ns
Clock High to Output High-Z	tHZC	1.0	3.1	1.0	3.1	1.0	3.1	1.5	3.5	1.5	3.8	1.5	4.0	ns
Clock High Pulse Width	tCH	2.0	-	2.0	-	2.0	-	2.0	-	2.4	-	2.8	-	ns
Clock Low Pulse Width	tCL	2.0	-	2.0	-	2.0	-	2.0	-	2.4	-	2.8	-	ns
Address Setup to Clock High	tAS	1.4	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns
Address Status Setup to Clock High	tSS	1.4	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.4	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	1.4	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.4	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.4	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever  $\overline{ADSC}$  and/or  $\overline{ADSP}$  is sampled low and  $\overline{CS}$  is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.  
 2. Both chip selects must be active whenever  $\overline{ADSC}$  or  $\overline{ADSP}$  is sampled low in order for the this device to remain enabled.  
 3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.



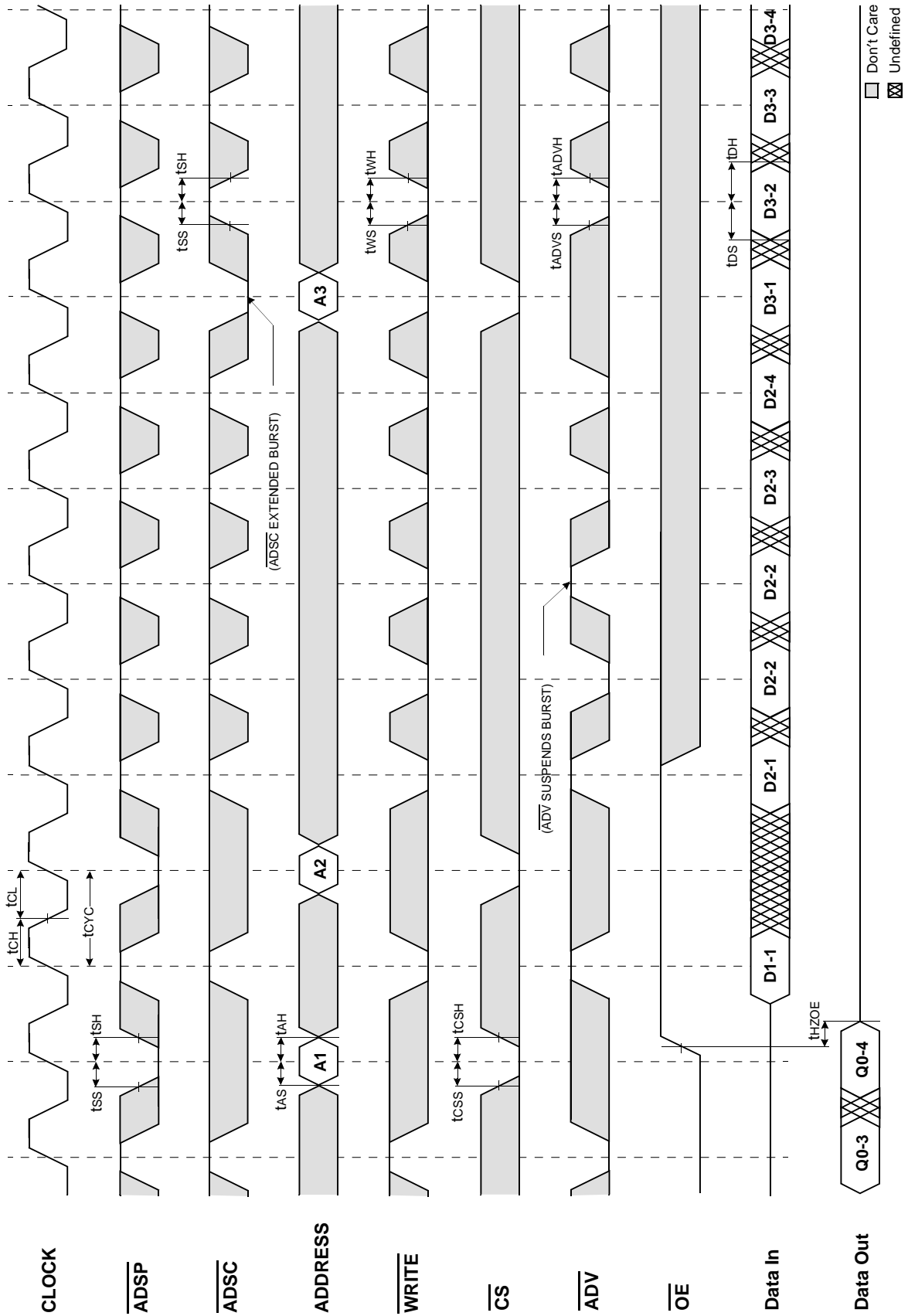
**TIMING WAVEFORM OF READ CYCLE**



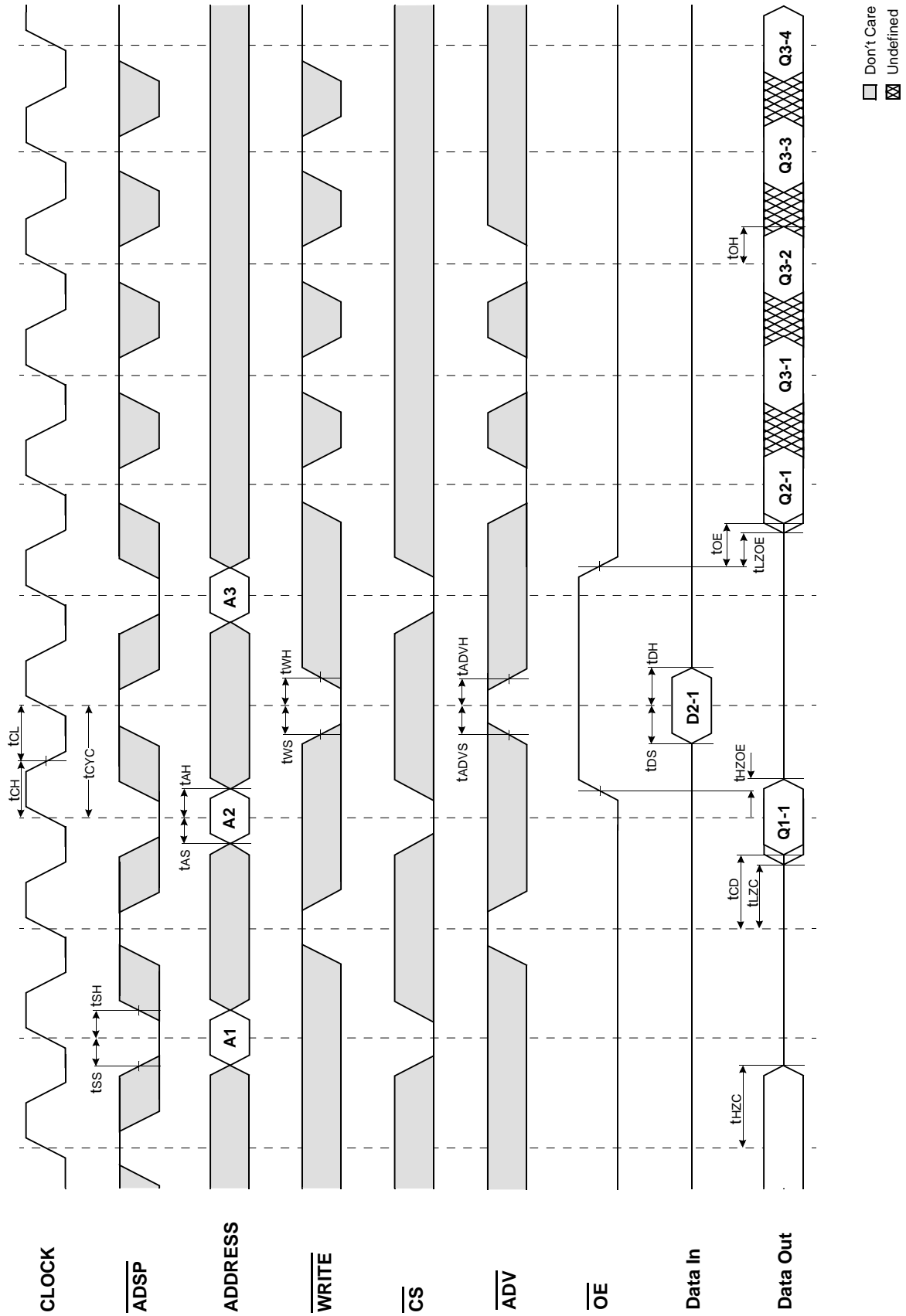
□ Don't Care  
 ☒ Undefined

NOTES :  $\overline{WRITE} = L$  means  $\overline{GW} = L$ , or  $\overline{GW} = H, \overline{BW} = L, \overline{WEX} = L$   
 $\overline{CS} = L$  means  $\overline{CS1} = L, \overline{CS2} = H$  and  $\overline{CS2} = L$   
 $\overline{CS} = H$  means  $\overline{CS1} = H$ , or  $\overline{CS1} = L$  and  $\overline{CS2} = H$ , or  $\overline{CS1} = L$ , and  $\overline{CS2} = L$

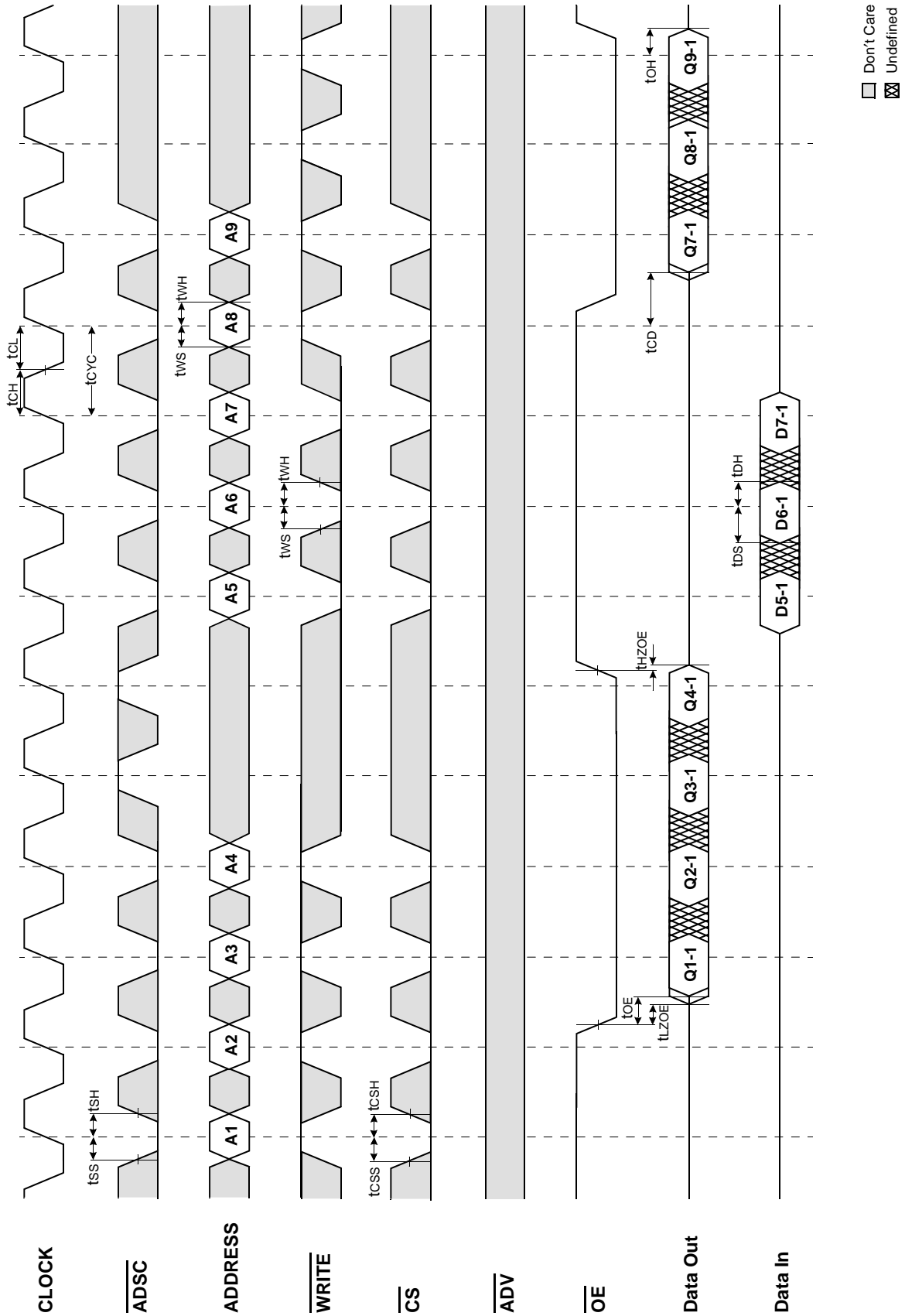
**TIMING WAVEFORM OF WRTE CYCLE**



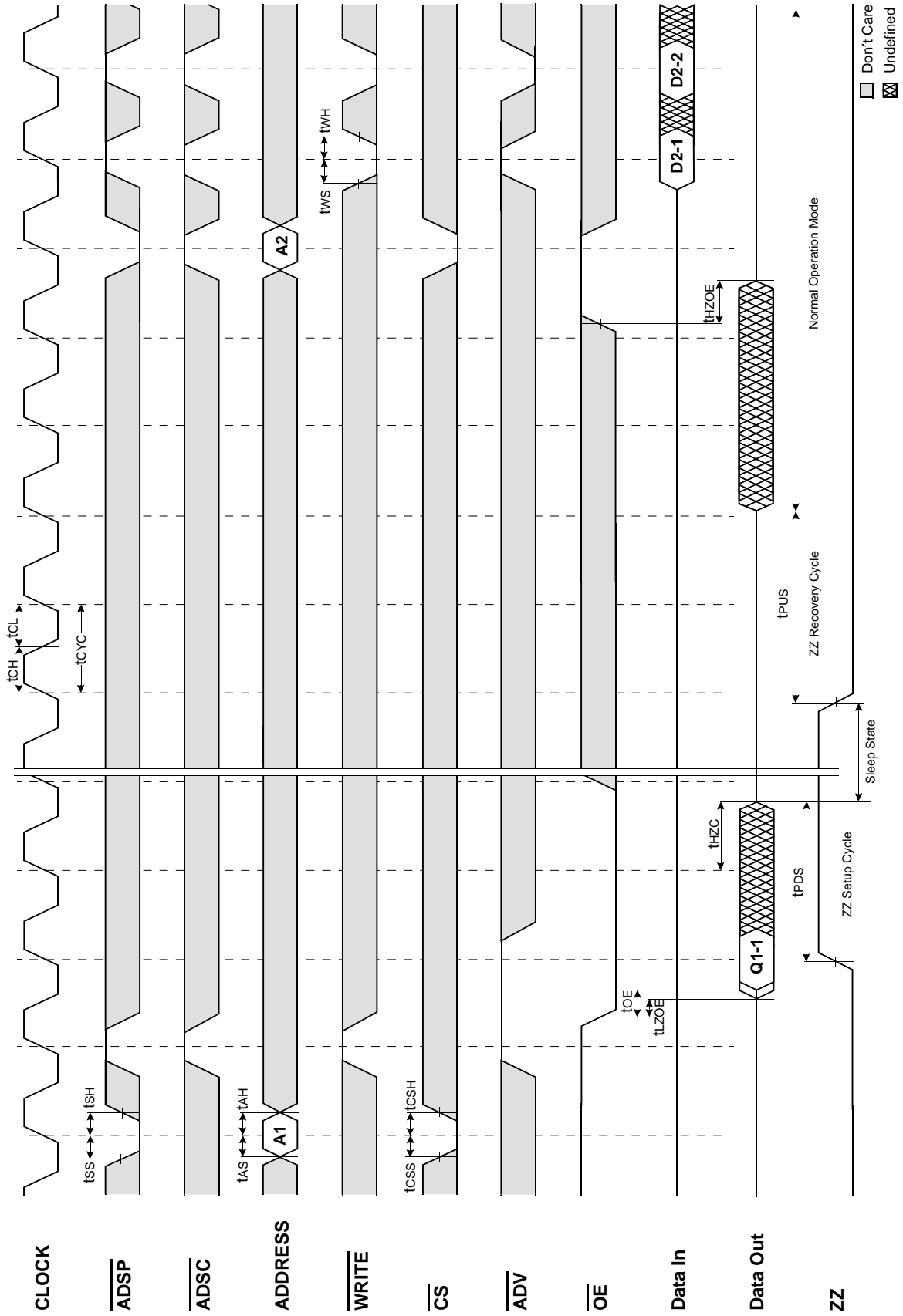
**TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED,  $\overline{\text{ADSC}}=\text{HIGH}$ )**



**TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED , ADSP=HIGH)**



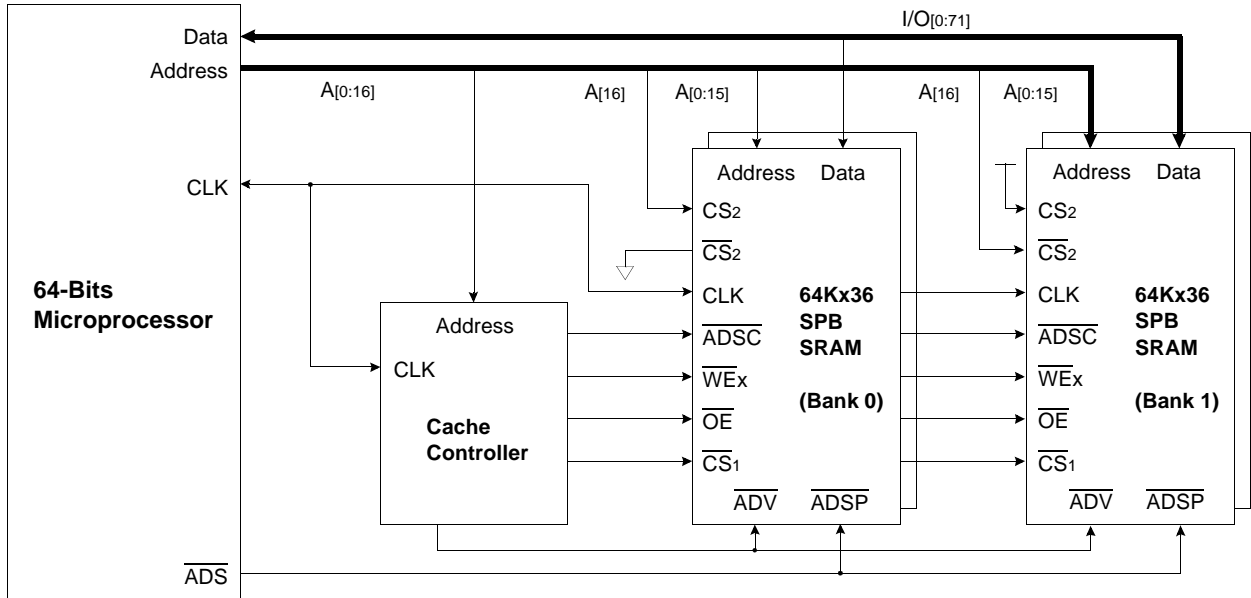
**TIMING WAVEFORM OF POWER DOWN CYCLE**



**APPLICATION INFORMATION**

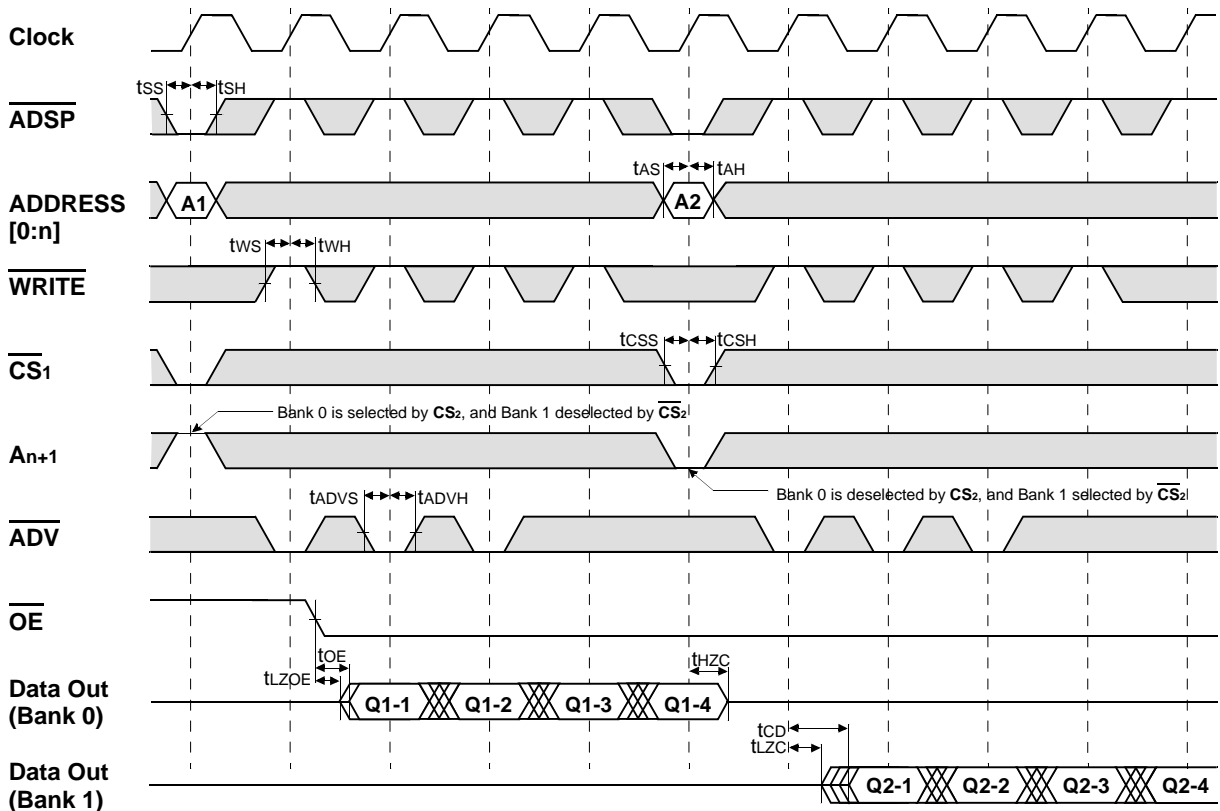
**DEPTH EXPANSION**

The Samsung 64Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



**INTERLEAVE READ TIMING** (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)



\*NOTES n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

□ Don't Care    ⊗ Undefined

**PACKAGE DIMENSIONS**

100-TQFP-1420A

Units: millimeters/inches

