Am7996 IEEE-802.3 (Ethernet/Cheapernet) Transceiver Application Note

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INTRODUCTION

The Am7996 IEEE-802.3 (Ethernet/Cheapernet) Transceiver integrates all the transceiver functions required for 10 Mbps CSMA/CD (Carrier Sense Multiple Access with Collision Detection) LANs. These functions include transmit receiver, collision detect, iptional signal Quality Error (SQE) test, Jabber timer (including the hooks for an external redundant jabber) and noise rejection filters (see Figure 1.) It highly integrates the Ethernet/Cheapernet systems when used with the AM7990 LANCE (data link controller) and Am7992B Serial Interface Adapter (SIA) (Manchester encoder/decoder).

The Am7996 is a CSMA/CD transceiver whose main structure consists of three functional blocks; transmit including jabber control, receiver, and collision detection. Each section op-

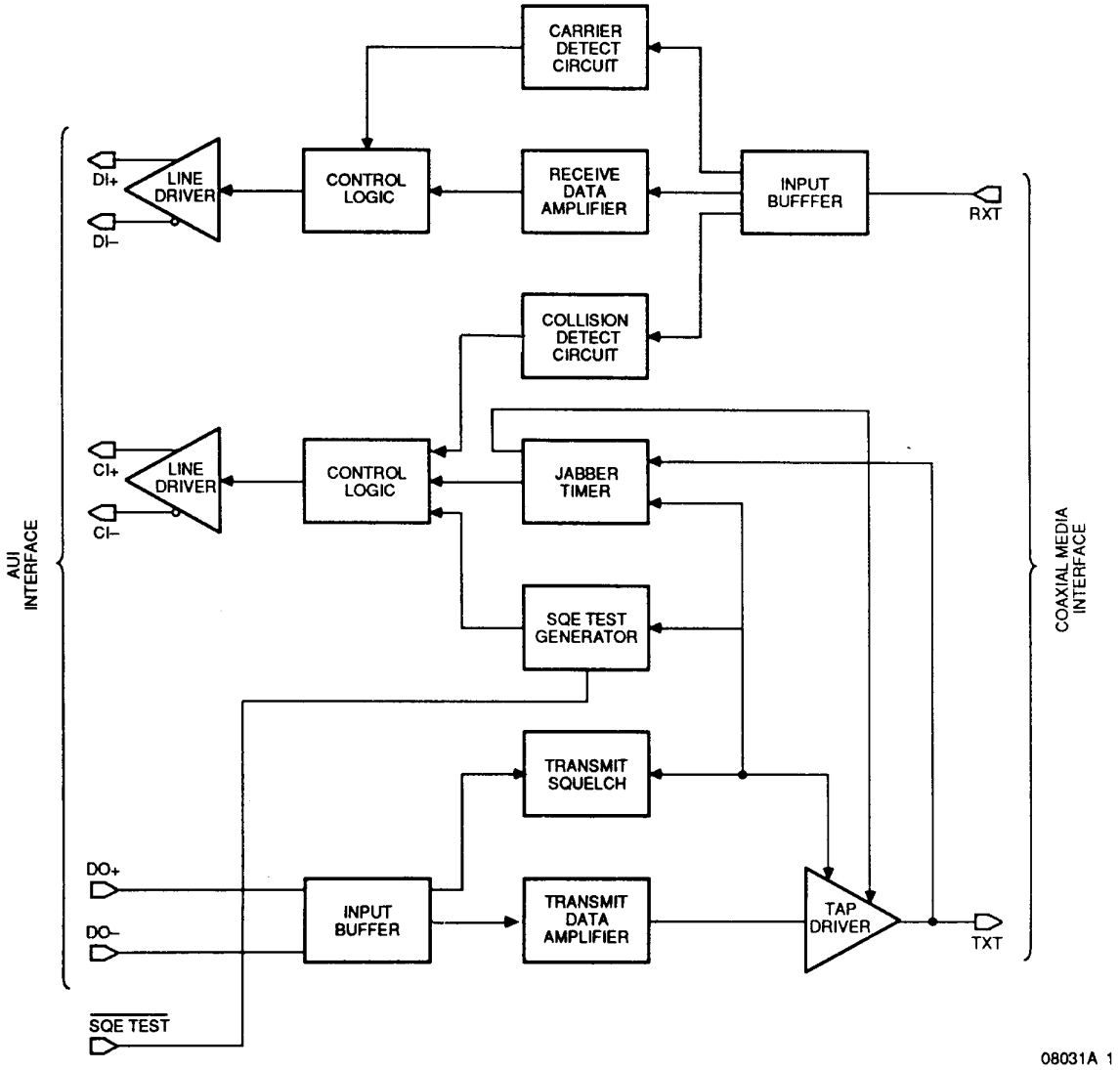


Figure 1. Am7996 Block Diagram

erates independently. In the transmit section, data is received differently from the Data Terminal Equipment (DTE) and transmitted out, single ended, to the medium (coax cable). The Jabber function guards the medium from node transmissions that are excessive in length. The receive section listens to data differentially to the DTE. The collision detection section monitors the medium for simultaneous transmissions, and when that occurs it reports it to the DTE via a 10 MHz differential signal.

This application note first describes briefly the Ethernet/Cheapernet standards. The use of Am7996 with extended cable lengths is then explained. The three functional blocks (transmit, receive, and collision detection) mentioned above are then discussed in detail. This is followed by practical guidelines regarding the external components required. Measurement techniques are also discussed. Finally, application examples are given.

IEEE-802.3 Standard (Ethernet/Cheapernet)

The IEEE-802.3 is the existing standard for the bottom two layers of the 7 layer Open System Interconnection (OSI) which was formulated and adopted by the International Standards Organizations (ISO). The main structure of the specification comes from Ethernet which was jointly developed by XEROX, Digital Equipment Corporation and Intel.

Another standard, known in the industry as "Cheapernet", was developed by the same committee at a faster pace than the 802.3 Ethernet standard. Cheapernet is an extension to the existing and proven standard, IEEE-802.3 Ethernet. It is a CSMA/CD network at 10 Mbps. Its network architecture is the same as Ethernet except it incorporates cheaper cable, connectors, and maintenance. Its installation consists of simply connecting an RG-58 cable to a BNC connector.

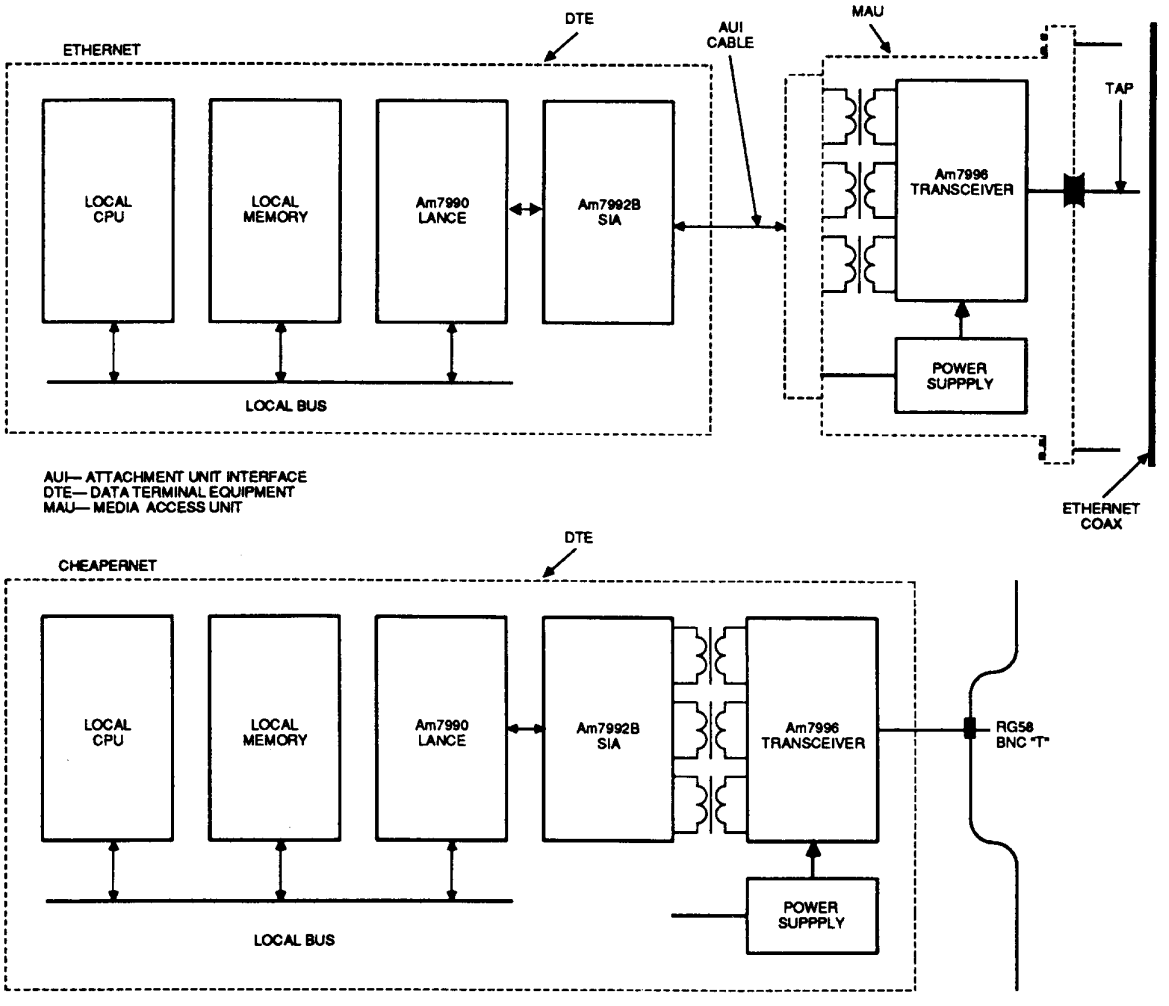


Figure 2. Ethernet and Cheapernet Configurations

Figure 2 shows a block diagram of an Ethernet and a Cheapernet configuration.

IEEE-802.3 refers to the original standard, Ethernet, as 10BASE5 or Type A applications, and refers to the second one, Cheapernet, as 10BASE2 or Type B applications. In the IEEE-802.3 terminology, 10BASE refers to 10 MHz baseband and the suffix 5 or 2 refers to 500 or 200 meter cable segment, respectively. Note that the actual length of the cable segment is 185 meters in the Cheapernet specification.

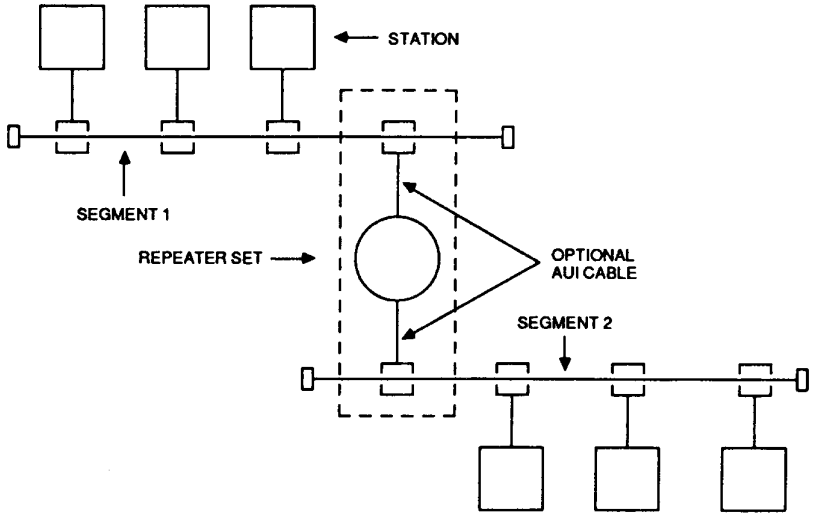
In an Ethernet installation, up to 100 Media Access Units (MAU) may be connected to one cable segment of 500 meters. In a Cheapernet installation, up to 30 MAUs may be connected to one cable segment of 185 meters. In either Ethernet or Cheapernet, repeaters may be used to connect up to five segments together into one network. Refer to Figure 3.

The Am7996 has been targeted for both applications, Ethernet and Cheapernet. It offers the flexibility and the engineering hooks for some of the tight parameters, and for network protection which is required in Ethernet applications. This gives the user the flexibilty of applying the same chip for both applications. Most OEM boards are now designed to include both options, an onboard transceiver for cheapernet application, and an optional 15 pin D connector for the AUI cable to access the Ethernet transceiver box.

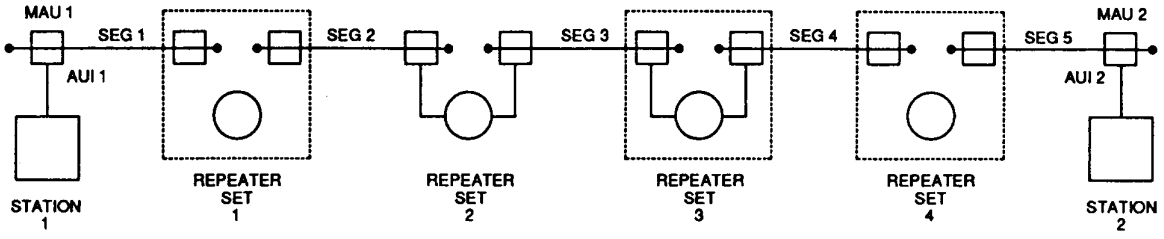
The salient features of Ethernet and Cheapernet are shown in Table 1.

Am7996 Application in Extended Cable Lengths

The Am7996 has been designed for Transmit Mode collision detection. (Collision detection methods are discussed later in this manual.) As a result, the Am7996 can be used in longer cable segments than specified in the IEEE-802.3. Table 2 below shows the extended cable length feature of the Am7996.



MINIMAL SYSTEM CONFIGURATION REQUIRING A REPEATER SET



MAXIMUM IEEE-802.3 TRANSMISSION PATH

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Figure 3. Ethernet/Cheapernet Network Configuration

The extended cable segment feature can eliminate the need for repeaters. This reduces the cost and adds flexibility in installing more nodes. Note that the extended cable segment support does not violate the IEEE-802.3 standard. It is the Transmit Mode collision detection scheme, in Am7996, which allows this extended feature.

TRANSMIT FUNCTION

The Am7996 receives differential signals from the DTE (in the case of Am7990 family applications, from the Am7992B–Serial Interface Adapter–SIA). For IEEE-802.3 Type A (Ethernet) applications, this signal is received through the AUI cable and isolation transformer. In IEEE-802.3 Type B (Cheapernet) applications, the AUI cable (but not the isolation transformer) is optional.

Data is received through an internal noise rejection filter that rejects signals with pulse widths less than 7 ns (negative going), or greater than 160 ns (positive going) with levels less than –175 mV peak. Only signals greater than –275 mV peak from the DTE are accepted. This minimizes false starts due to noise and ensures no valid packets are missed.

The Am7996's Tap driver provides the driving capability to ensure adequate signal level at the end of the maximum length network segment (500

Table 1. IEEE-802.3 10BASE5 (Ethernet) and 10BASE2 (Cheapernet) Comparison

Parameter	IEEE-802.3 10BASE5 (Ethernet)	IEEE-802.3 10BASE2 (Cheapernet)
Data Rate	10 Mbps	10 Mbps
Segment Length	500 meter	185 meter
Network Length	2500 meter	925 meter
Nodes Per Segment	100	30
Node Spacing (Min)	2.5 meter	0.5 meter
Cable/Connector	0.4 in diameter, 50 Ohm Double shielded shielded N-series connectors Rugged	0.2 diameter, 50 Ohm (RG-58 A/U type) Single BNC connectors Flexible (thin)
Transceiver Cable (AUI interface)	0.38 in. diameter multiway cable with 15 pin D connectors (Length up to 50 meter)	Optional
Capacitance/Node	4 pF	8 pF
Installation	Installer required (costly)	Mainly by user (low cost)

Table 2. Extended Cable Lengths with Am7996

Applications	CABLE LENGTH	
	IEEE-802.3	*Am7996
10BASE5, Ethernet (Ethernet Thick cable)	500 meter	1000 meter
10BASE2, Cheapernet (RG58 Thin cable)	185 meter	300 meter

* Transmit mode collision implementation

meters Ethernet, or 185 meters Cheapernet) under the worst case number of connections (100 nodes Ethernet, or 30 nodes Cheapernet). Required rise and fall times of data transmitted on the network are maintained by the Am7996 Tap driver. The Tap driver's output is connected to the media through external isolating diodes. To safeguard network integrity, the driver is disabled whenever the operating voltage falls below the minimum.

Signal Quality Error (SQE) Test (Heartbeat)

A diagnostic feature has been specified for the MAU in the IEEE-802.3. The Signal Quality Error (SQE) Test is a self test feature in the MAU which is invoked after the end of each transmission by the DTE. The SQE test starts eight bit times after the last transition of the transmitted signal and lasts for a duration of eight bit times. The Am7996 sends a 10 MHz differential signal through $CI_{\pm}$ to the DTE when $\overline{SQE\ TEST}$ pin (pin 7) is tied to V_{EE}. This test is an indication to the DTE that the MAU has recognized the end of the transmission and the collision pair, $CI_{\pm}$, is intact and operational.

Pin-strappable SQE Test Option: The SQE test is selectable via the $\overline{SQE\ TEST}$ pin (pin 7). It can be tied to V_{EE} for SQE test or to ground (V_{CC1} or V_{CC2}) for a non-SQE test MAU. The optional feature allows the use of the Am7996 in both repeater and non-repeater applications.

Jabber Function

Another means of protecting the network (medium) is to ensure that no node, under any circumstances, hangs the network. In an IEEE-802.3 network, the maximum packet size is limited to 1518 octets which is equivalent to about 1.2 ms (including the 64 bit preamble). The Jabber timer monitors the activity on the DO pair and senses TXT (pin 12) faults for excessive continuous transmission. The Jabber goes active and inhibits transmission if the Tap driver is active for longer than the Jab time. The Jab time specified by IEEE-802.3 is from 20 to 150 ms. In the Am7996, it is from 20 to 35 ms. When the Jabber goes active, it isolates the output drivers at the Tap from the coax and enables an SQE message (10 MHz differential collision signal) on the CI pair for the fault duration.

IEEE 802.3 states that in a self-powered MAU, the Jabber timer and collision presence on the CI pair are cleared after the fault condition goes away for a period of 500 ms ± 50% (250 to 750 ms). The Jabber reset time in the Am7996 is between 340 and 500 ms.

Redundant Jabber: The hooks for optional redundant protection specified by the IEEE-802.3 have been implemented in the Am7996. A redundant Jabber sits outside the Am7996 and typically duplicates the Jabber internal to the Am7996. When the external Jabber is implemented, the VTX-pin is directly controlled by the external Jabber circuitry. To externally disable TXT (and enable an SQE message on CI pair), the voltage at VTX-pin should be brought to a value more positive than V_{EE} + 2V.

Jabber Recovery Time: One of the parameters in the Jabber function is the Jabber recovery time which is significant in terms of the correct operation of the Jabber timer. The Jabber timer always starts counting from the start of each transmission and is reset at the end of the transmission. The time required for the timer to reset is called the Jabber recovery time. This parameter is 1 µs (max) in the Am7996. It is important that this time be as short as possible.

Consider an IEEE-802.3 network in maximum configuration. There are four repeaters in such a configuration. Because of the nature of such regenerative repeaters, the InterPacket Gap time (IPG) can shrink from 9.6 µsec (9.6 µsec is the IPG spec in IEEE-802.3 for the gap between two consecutive transmissions) to about 5.0 µsec in a normal packet transfer. The IPG can even shrink to less than 5.0 µsec under excessive collisions. Therefore, if the Jabber recovery is not short enough, the Jabber timer will not be cleared and will continue to count after the start of the next packet. Under the worst case condition, when back-to-back packets are in progress with short IPG, the Jabber goes falsely active. The Jabber recovery time is 1 µsec (max) in the Am7996 insuring proper operation under the worst case conditions.

Inhibit Internal Jabber: It may be desired in some non IEEE-802.3 applications to disable the Jabber function. Consider a point-to-point application where a continuous transmission of more than 20 ms is desired. For such applications, the internal Jabber can be disabled by removing the external collision oscillator circuitry (R_4, C_1) and connecting COLL OSC (pin 19) to V_{CC2} (pin 20). Note that this will also inhibit the SQE test and any CI pair message for collision presence.

RECEIVE AND CARRIER DETECT

The signal is acquired from the Tap through a high impedance (100 kOhm) resistive divider. A high input-impedance (low capacitance, high bandwidth, low noise) DC-coupled input amplifier in the Am7996 receives the signal. The received signal passes through a high-pass filter to minimize intersymbol distortion, and then through a data slicer. The Am7996 carrier detect compares received sig-

nals to a reference. Signals meeting carrier squelch criteria enable data to the differential line driver within five bit times from the start of the packet.

Received data is transmitted from the DI pair through an isolation transformer to the Ethernet AUI cable (IEEE-802.3–Type A). In IEEE-802.3 Type B (Cheapernet), the AUI cable is optional. Following the last transition of the packet, the DI pair is held high for two bit times and then decreases to idle level within twenty bit times.

COLLISION

Collision occurs when two or more transceivers attempt simultaneous transmissions on the medium. In a CSMA/CD network, a mechanism is needed to resolve the contention. All the intelligence for collision back-offs, and the retry process resides in the controller (Am7990). The Am7996 detects a collision when the DC average of the signals on the coax crosses the collision detect threshold. The collision threshold window has been based on the worst case conditions in the IEEE-802.3 cable segment (500 meter Ethernet cable, or 185 meters of RG-58 cable) when two nodes transmit at the same time.

Collision Reporting

When the Am7996 detects a collision, it generates a 10 MHz differential signal at CI± which continues as long as there is a collision in progress. The 10 MHz differential signal is normally detected by the Manchester Encoder/Decoder at the DTE (SIA, Am7992B) which translates to a TTL signal for the LAN controller (LANCE, Am7990).

Collision Detection Methods

There are two types of collision detection specified by the IEEE-802.3 standard: Transmit Mode and Receive Mode collision detection. The Am7996 has been designed to support Transmit Mode collision detection. The collision threshold window for Transmit Mode collision allows longer cable segment applications than what IEEE-802.3 has specified. For the Am7996 in repeater applications, Receive Mode collision detection can also be accomplished by adding two resistors, R_9 and R_{10}, external to the chip. Receive Mode collision detection is optional when the Media Access Unit (MAU) is used in non-repeater applications.

Transmit Mode Collision Detection: While transmitting, the MAU must detect a collision if one or more other nodes are also transmitting, and may detect collision, while not transmitting, if two other nodes are transmitting. This is called Transmit Mode collision detection. As a result of this type of collision detection, longer cable segments than what IEEE-802.3 has specified can be used. This type of collision detection is normally used in non-repeater applications.

Receive Mode Collision Detection: Regardless of whether a MAU is transmitting or not transmitting, the MAU must detect collision if two or more modes (perhaps including itself) are transmitting. This scheme requires a tighter threshold than Transmit Mode collsion detection. The Receive Mode collision detection limits the cable length to what the IEEE-802.3 has specified whereas transmit mode collision detection, due to its wider threshold window, allows for the extended cable segment.

Receive Mode collision detection is not necessary in non-repeater applications, but, it is a must in repeater applications since the carrier has to be sensed by both sides of the repeater. Figure 4 shows the external component configuration for Cheapernet Receive Mode collision detection.

The Am7996 meets the IEEE-802.3 collision detect requirements (see Table 3).

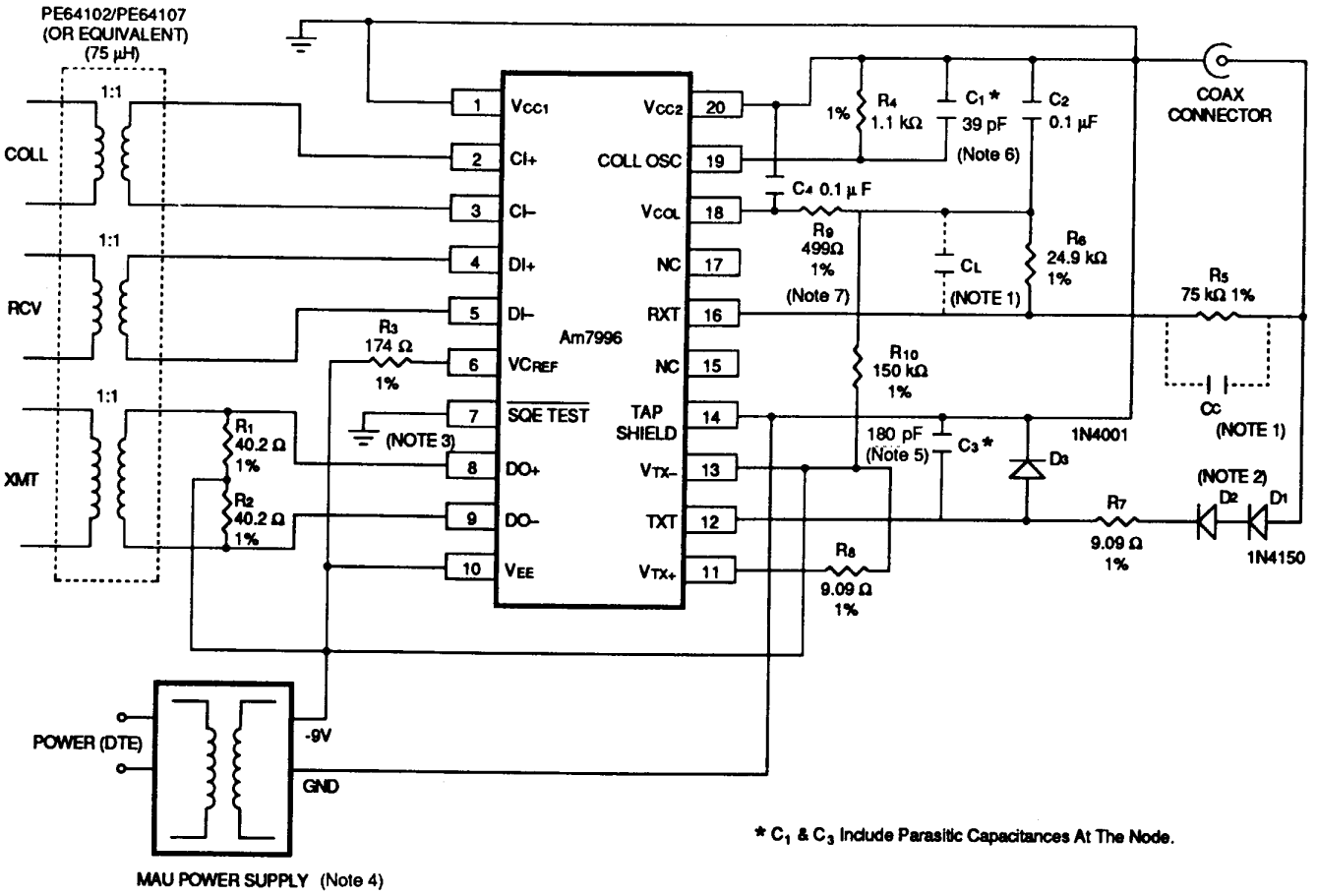
Collision Detection in Non-Repeater Applications: Receive Mode collision detection is normally not necessary when designing a MAU in a non-repeater application. This is because the received packet, the packet participating in collision, usually ends up as a runt packet (a packet less than 64 bytes long) which is normally discarded by Data Link layer controllers. In other cases such as late collision (collision occurring after 64 bytes), CRC error can be an indication that there might have been a collision in progress while receiving the packet.

Collision Detection in Repeater Applications: Receive Mode collision detect is strictly required in Repeater design applications. A repeater must report all the activities of either side of the network to the other side. In the case of a collision at one side of the network, the repeater must create the collision environment on the other side. The repeater must detect a collision caused by two nodes that occur from the far end of a segment. Since cable attenuation results in a lower level seen by the repeater, the Receive Mode Collision Detection specs must be tighter. If a collision occurs on one segment, the repeater sends a collision jam signal to the other segment to report such activity.

The Am7996 meets the Receive Mode collision detect as well, when R_9, R_{10}, and C_4 are integrated into the Am7996 external component diagram (see Figure 4).

EXTERNAL COMPONENT DESIGN GUIDELINES

The design and layout choices of the compo-



Notes: 1. C_L is the effective load capacitance across R_6; C_C is the compensation capacitance ($C_C = 1/3\ C_L$).

2. D_2 can eliminated in Cheapernet (IEEE-802.3, 10Base2) applications.

3. Shown with SQE Test disabled.

4. Discrete Power Supply or Hybrid – Hybrid DC-DC Converter Manufacturers include:

Ethernet (IEEE 802.3, 10BASE5)	**Cheapernet (IEEE 802.3,10BASE2)**
Reliability Inc. 2E12R9	Reliability Inc: 2VP5U9
Valor Electronics: PM1001	Valor Electronics: PM7102

5. The capacitance of C_3, Am7996 package, D_3 and the printed circuit board should add up to 180 pF ± 20%.

6. The capacitance of C_1, Am7996 package and the printed circuit board should add up to 39 pF.

7. R_9, R_{10}, and C_4 are for Receive Mode Collision detection only.

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Figure 4. Am7996 External Component Diagram for Receive Mode Collision Detection

nents external to the chip in the Am7996 adds flexibility, network protection, and hooks for achieving the tight parameters specified in the IEEE-802.3 and Ethernet specifications. The following describes the design considerations to be aware of in choosing those external components around the Am7996. Figure 5, the external components diagram, should be used in reference to the discussion below.

Layout Considerations

The Am7996 should be mounted as close as possible to the Tap for minimum capacitive loading. To minimize the capacitance at RXT (pin 16) between its adjacent pins (pins 15 and 17) and the capacitance introduced by TXT (pin12) to the Tap through external components, package, and PC trace, carefully layout the PC board as follows:

1. It is recommended that metal feed-throughs are not used at pins 15 and 17. These pins are No Connect pins.

2. Generally, all the PC traces between the chip and external components should be as short as possible. Additional effort should be made to place R_5, R_6, RXT (pin 16) and D_1, D_2, R_7, TXT (pin 12), and Am7996 close to the Tap.

3. To achieve the minimum capacitive loading at the Tap connection, there should be no power, ground, or signal planes in the area of Tap interconnections to 7996 pins (pins 11–18). (See also ground requirements discussed later.

4. The 7996 should be directly soldered to the PC board without a socket to reduce capacitive loading at the Tap connection.

5. Grounding:

   V_{CC1} and V_{CC2} (pin 1 and 20 respectively) must be connected together to the positive return (positive polarity of power to 7996).

   The Tap shield pin (pin 14) should be connected directly, via a single trace, to the shield of the coax connector. There should not be any ground plane connection to the Tap shield which will add to Tap capacitive loading.

   The DTE ground plane should not be extended beyond the pulse transformer (the one at the Am7996 side).

In IEEE-802.3 applications, using the AUI (Attachment Unit Interface) cable, the DTE logic ground can be extracted from any of pins 1, 4, 6, 8, 11, or 14 of the 15 pin D connector. In Ethernet Version 2 applications, Pins 4, 8, 11, and 14 are No Connect (NC) pins. The DTE logic ground can be extracted from Pin 6 only. See appendices A and C for pinout details and PC board layout considerations.

Tap Capacitance Loading Considerations

The goal is to minimize the capacitive loading at the Tap from both the receive path (RXT, pin16) and the transmit path (TXT, pin 12) to achieve the input impedance requirements of IEEE-802.3 specification.

A properly compensated external 4:1 attenuator (75K and 25K in series) reduces any parasitic capacitive loading in the receive path by a factor of 4 and ensures that the resistance presented to the coaxial cable will be at least 100K Ohms.

When the chip is not transmitting, the transmit path

Table 3. IEEE-802.3 Transmit Mode and Receive Mode Collision Detection.

	TRANSMIT MODE			*RECEIVE MODE		
MAU	Number of transmitters			Number of transmitters		
	<2	=2	>2	<2	=2	>2
Transmitting	NO	YES	YES	NO	YES	YES
Not transmitting	NO	MAY	YES	NO	YES	YES

NO: Will not generate SQE message
YES: Will generate SQE message
MAY: May generate SQE message

* Receive Mode collision detection is optional per IEEE-802.3 in non-repeater applications

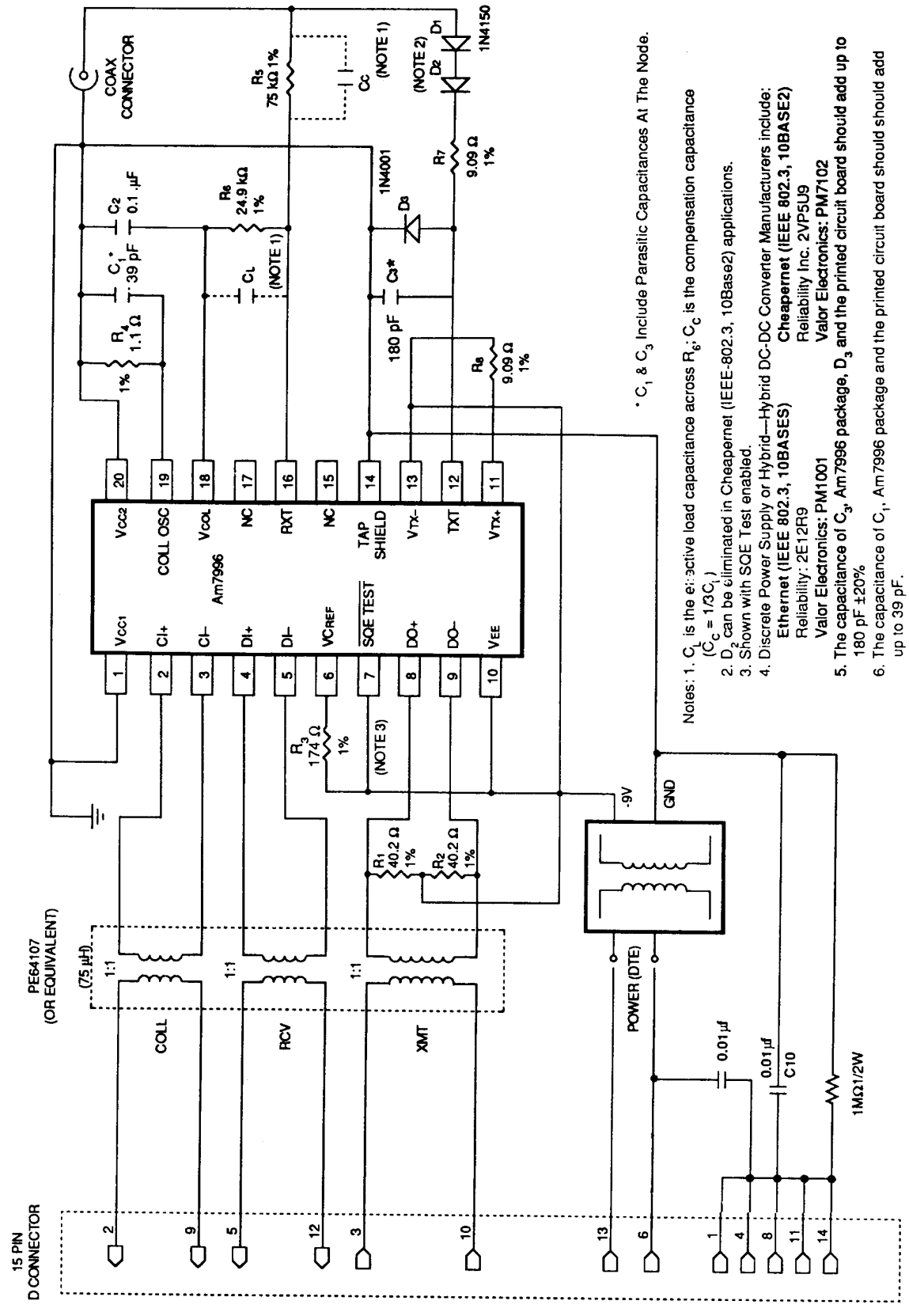


Figure 5. Am7996 External Component Diagram for Transmit Mode Collision Detection

is isolated from the Tap through a low capacitance switching diode. When transmitting, the additional diode in series reduces the capacitance loading at the Tap. IEEE-802.3 10BASE5 (Ethernet) has specified a limit of 2 pF for capacitive loading due to the MAU (Medium Attachment Unit) circuitry (total of 4 pF including the Tap connection). This tight limit is quite difficult to meet without additional circuitry such as the 4:1 attenuator, external to the Am7996.

In the IEEE-802.3 10BASE2, (Cheapernet) applications, the capacitive loading specification, due to the MAU circuitry, has been relaxed to 6 pF. Therefore, it is not as difficult to meet the capacitive loading requirement in Cheapernet applications. The external 4:1 attenuator also isolates the receive input of the integrated circuit from the Tap for safety and protection.

Attachment Unit Interface (AUI) Cable Terminator (R_1, R_2)

The DO± line receiver inputs should be terminated with R_1 and R_2, as shown in the external component diagram, equivalent to AUI cable impedance of 78.0 Ohms nominal. The effective parallel combination of the 80.4 Ohms (R_1 + R_2) and the DO± input impedance meets the IEEE-802.3 requirement of 78.0 ± 5 Ohms.

Although AUI cable is not normally used in Cheapernet applications, R_1, R_2, and the terminating resistors at the SIA (Am7992B) side must remain in. The terminating resistors are part of the load seen by the output drivers of the Am7996, DI±, and Transmit± of the Am7992B. Therefore, the removal of the terminating resistors will affect the differential level signals at DI± and Transmit±. Refer to the Cheapernet application example in the application section appearing later in this manual.

Timing Reference Resistor (R_3)

When the resistor, R_3, is connected between VC_{REF} (VC_{REF} is a compensated voltage reference input with respect to V_{EE}) and V_{EE}, the internal transmit and receive squelch timing and SQE oscillator frequency are set. SQE frequency is also determined by components connected between V_{CC2} (pin 20) and COLL OSC (pin 19).

SQE Oscillator Control (R_4, C_1)

In the Am7996, the collision oscillator frequency control is external to the chip. For a 10 MHz nominal SQE oscillator frequency, R_4 should be 1.1K 1%, and C1, 39pF ±5%, (including any parasitic capacitance). This will generate an SQE message with frequency of 10 MHz ± 15% for the following three cases:

1. SQE test
2. Collision for multinode transmission
3. Active Jabber

When VC_{REF} (pin 6) is properly set (it is set by placing R_3 = 174Ω between VC_{REF} and V_{EE} pin 10), the SQE oscillator period is set at $2.331R_4C_1$.

4:1 Attenuator (R5 and R6, CL and CC)

The chip acquires the signal from the Tap through a high impedance (100K Ohms) 4 to 1 attenuator. For proper reception of 10.0 MHz Manchester bit streams, the input attenuator at the RXT pin should be compensated to maintain the 4:1 ratio. Compensation is acieved by making 75 x C_C = 25 x C_L (C_C = 1/3 C_L). C_L is the total effective capacitance between RXT (pin16) and V_{COL} due to the package, external components, and PC trace. C_C is the compensation capacitance across the 75 kOhm resistor.

C_C is typically less than 2.0 pF when short PC traces are used around RXT's (pin 16) external components. A possible way of achieving the compensation is by placing a PC trace at one end of R_5 to obtain the equivalent C_C. A properly compensated attenuator will reduce the effective capacitive loading seen at the Tap to 1/4 of that seen at RXT (pin 16).

The ratio of the attenuator does not affect the collision detection threshold (V_{COT} specification in data sheet); it only affects the carrier threshold (V_{CAT} specification in data sheet) at the coax.

Figure 6 shows the attenuator section of the Am7996. At low frequencies (e.g., DC) with R_6 = 24.9K and R_5 = 75K, a 4:1 attenuator is achieved (1/4 V_{COAX} is added to V_{RXT}). With high input impedance at RXT, the series combination of R_5 and R_6 ensures that the resistance to the coaxial cable is at least 100 kOhms as specified by the IEEE 802.3.

At high frequencies (5 or 10 MHz), the parasitic capacitance across R_5 and R_6 determines the attenuator ratio. Therefore, R_5 must have a capacitance (C_C) to compensate for the effective capacitance (C_L) across R_6. For a 4:1 attenuator, C_C = 1/3 C_L (see appendix C for detail PC board layout considerations).

$$V_{RXT} - V_{COL} = \frac{(V_{COAX} - V_{COL})(1/C_L)}{(1/C_C) + (1/C_L)}$$

$$(V_{RXT} - V_{COL})(1 + C_L/C_C) = V_{COAX} - V_{COL}$$

Let: $y = C_L/C_C$

Then:

Equation 1: $V_{COAX} = V_{RXT}(1 + y) - y(V_{COL})$

For a 4:1 attenuator, y = 3

Note: All voltages are referenced to the Tap shield.

Example: (4:1 attenuator, y = 3)

For: $V_{COAX} = 0$

$V_{COL} = -1600$ mVDC (nominal)

Using Equation 1:

$0 = 4V_{RXT} - 3V_{COL}$

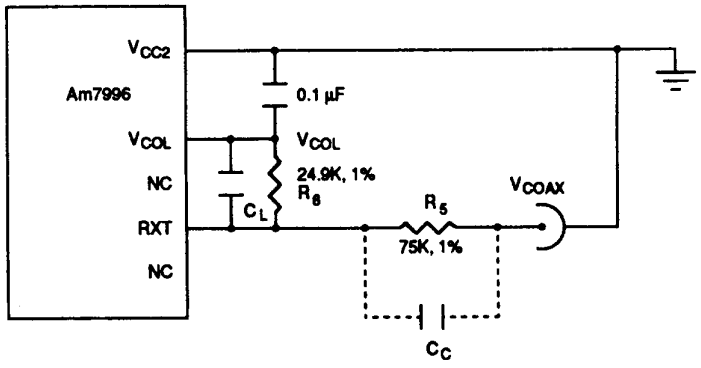
$V_{RXT} = -1200$ mVDC

For: $V_{COAX} = V_{CAT} = -600$ mVDC

Using Equation 1:

$-600 = 4V_{RXT} - 3(-1600)$

$V_{RXT} = -1350$ mVDC



$C_C = (1/y)\,C_L$

FOR A 4:1 ATTENUATOR, y = 3

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Figure 6. Am7996 External Attenuator

Attenuator Tolerance

Any deviation from the ideal compensation value for capacitor (C_C) will change the ratio of the attenuator. The attenuator ratio can deviate from the 4:1 ratio as long as the minimum signal level at the coax allowed by the standard can be recognized (see Table 4). Using Ohm's law for Figure 6, the voltage at coax (V_{COAX}) is obtained from equation 1.

The minimum average DC signal at coax can be obtained when two nodes are attached to a maximum length cable segment (500 meters of Ethernet cable or 185 meters of Cheapernet, RG58A/U or RG58C/U). While on node is transmitting from one end of the cable with minimum transmit current, the other node is measuring the attenuated signal received at the other end of the cable.

The external attenuator scheme serves the following two purposes:

1. Reduces the capacitive loading, seen at the coax, by the attenuator ratio (by 1/4 in a 4:1 attenuator). This helps to achieve the tight Tap capacitive loading specification of 2 pF, due to MAU circuitry, per IEEE 802.3, 10BASE5 (Ethernet).

2. Isolates the receive section of the chip (RXT pin) from the medium. It protects the chip which is part of the circuitry of the MAU.

Isolation Diodes D_1, D_2

Another part of the Tap capacitive loading is introduced by the transmit path. The diode D_1, external to the Am7996, is used to isolate the transmit path from the receive path when the chip is not transmitting. The second diode, D_2, protects the first diode, and it further reduces the capacitive loading introduced by the first diode, D_1. D_1 and D_2 are forward biased only when the chip is transmitting. The insertion of the second diode serves two purposes:

1. The capacitance seen at the Tap is reduced to the effective capacitance of the two diodes in series.

2. It provides redundancy in isolating the Tap from TXT pin should one diode get shorted. In Cheapernet applications, the 2nd diode, D_2, may be removed. Cheapernet does not require the redundancy for protection, and the limit for the Tap capacitance loading is not as tight as Ethernet (6 pF versus 2 pF).

   The capacitance introduced by the diode should be as low as possible. Low capacitance switching diodes with adequate current handling capability (80.0 mA nominal) such as the 1N4150 should be used for D_1 and D_2. Am7996 did not integrate the diodes into the chip because of power consideration.

Transmit Signal Wave Shaping (C_3)

C_3 provides wave-shaping for the transmitted signal at TXT (pin12). This 180 pF capacitance between the TXT and TAP SHIELD (pin 12 and 14 includes any parasitic capacitance at the node. A physical capacitor of 150 pF is a nominal value in a typical PC board which takes all the parasitic capacitance into consideration.

The low pass filter at the output stage of the Am7996 is one of the three poles which have been implemented to meet the harmonic content specification of IEEE-802.3 (two poles are internal to the Am7996). The RC components of the low pass filter are outside the Am7996. C_3, the combined resistance of D_1 and D_2, the 25 Ohm load presented by the coax line, and R_7 form the third pole of the TXT output filter.

The time constant for the low pass filter is: T = R x C where:

R is the total resistance seen between the Tap and the shield.

R = Current limiting resistor, (R_7 = 9.09) + Forward biased resistance of the diodes (about 2 Ohms) + 25 Ohms load

C = C_3 = 180 pF (including any parasitic capacitance)

T = 8 ns; Fundamental frequency of the filter is 20 MHz.

C_3 will have some effect on the rise and fall time of the transmit signals at the coax. The rise and fall time values can be improved (reduced) by reducing C_3. There is a limit to how much the capacitor value can be reduced without violating the harmonic content specification. A 150 pF capacitor used for C_3 in the Am7996 evaluation board meets the rise/fall time, and harmonic content specification.

Some attenuation of 10 MHz signals, relative to the 5 MHz signals, is due to the low pass filter implementation. The attenuation does not cause a problem and transmit level signals meet the IEEE-802.3 specifications.

Table 4. IEEE 802.3 Receive Mode Collision Detect Threshold

Application	No Detect (Average DC)	Must Detect (Average DC)
10BASE5 (Ethernet)	−1.492 V	−1.629 V
10BASE2 (Cheapernet)	−1.404 V	−1.581 V

The harmonic content specified by IEEE-802.3 is as follows:

2nd and 3rd harmonics:	at least 20 db below fundamental
4th and 5th harmonics:	at least 30 db below fundamental
6th and 7th harmonics:	at least 40 db below fundamental
All higher harmonics:	at least 50 db below fundamental

Network Protection (D_3 and R_7)

Am7996 offers a solution for network protection (see also the jabber function for protection). It is protected against high voltage surges when the clamp diode (D_3) and the resistor (R_7) are placed external to the chip. The diode protects the chip and the resistor limits the current to protect the diode.

If the Tap is at a positive voltage due to a fault condition, D_3 protects the TXT (pin 12) from sinking high currents from the Tap by shunting high current into ground. Under this condition, R7 (9.09 Ohms, 1/4W) helps limit the current through D_3. D_3 should have a rating of at least 50.0 Volts. A diode such as the 1N4001 can be used for D_3. The capacitive effect of diode D_3 should be taken into consideration as part of the total capacitance (180 pF) between TXT (pin 12) and TAP SHIELD (pin 14).

Set Transmit Current (R_8 = 9.09 Ohm)

This resistor is used to set the transmit output current at TXT (pin 12) nominally at 80.0 mA peak. If a redundant jabber controller is used externally, the supply to the current source comes from the jabber controller. This resistor should be placed as close to the chip as possible, to minimize any parasitic inductance.

Coax Collision Reference Threshold (C_2=0.1 μF)

V_{COL} is a DC reference for incoming signals from the Tap at RXT (pin 16). It is required that Vcol be a good analog signal ground in the presence of 10 Mbps Manchester data streams. In order to achieve that, C_2 is used to by-pass all the RF signals to Tap ground.

Additional Pins

Pins 17 and 15 on the Am7996 have been purposely allocated as No Connect pins on either side of the RXT Pin to give a minimum adjacent pin capacitance. The low RXT input capacitance, combined with any parasitic capacitance due to the resistor and PC trace, is reduced to 1/4 when measured at the Tap. This feature makes it feasible to meet the low input Tap capacitance required by the Ethernet specification. The input Tap capacitance in the Am7996 at RXT (pin 16) is 1.1 pF (typical) for plastic packages, and 1.7 pF (typical) for ceramic packages. Note that the input capacitance at RXT seen at the coax Tap is reduced to 1/4 th through the 4:1 attenuater, external to the chip.

Power (V_{EE}) Requirements

The Am7996 requires a single power supply at –9 ± 10% V. The IEEE-802.3 requires that the power to the MAU must be isolated from DTE. This indicates either the use of a dedicated power supply or isolating the power from DTE through a discrete or commercially available DC–DC converter. In summary, the power requirements are as follows:

- Power to the chip must be isolated from DTE to meet the high voltage isolation required by IEEE-802.3, 10Base5 (2000 VRMS) and 10Base2 (500 VRMS).
- V_{EE} = –9.0 V ± 10%
- Not more than 100 mV (P–P) ripple.
- Ripple frequency less than 100 KHz.

DC–DC Converter Recommendations: Refer to Table 5 for the DC–DC converters (or equivalents) that can be used with the Am7996.)

Isolation Transformers

The AUI transmit, receive, and collision signal pairs

Table 5. DC-DC Converters for Am7996

	APPLICATION	
Manufacturer	IEEE-802.3, 10BASE2 (Cheapernet)	IEEE-802.3, 10BASE5 (Ethernet)
Reliability Inc.	2VP5U9	2E12R9
Pulse Engineering Inc.	PE64381	PE64430

(DO±, DI±, and CI±) must be isolated through transformer coupling from the AUI cable. The isolation at the MAU side is required for two reasons:

1. To eliminate the common mode difference between the signals from the Am7996 and the DTE.

2. To protect the MAU from the fault conditions at the AUI cable.

In the Am7996, the inductance of the transformers for the AUI differential pairs DI±, DO±, and CI± should not be less than 75 µH.

The pin assignments for the transceiver cable are given in Appendix A.

Pulse Transformer Recommendations:

PE64102 (75 µH with 500 VRMS, IEEE-802.3, 10BASE2).
PE64107 (75 µH with 2000 VRMS, IEEE-802.3, 10BASE5) or equivalent.

MEASUREMENT TECHNIQUES

The following are guidelines for measuring some of the key parameters. For the actual test measurements and conditions, refer to the Am7996 data sheet and pertinent test documentation.

4:1 Attenuator Compensation

There are two ways to compensate for the parasitic capacitance across the 24.9 kOhm resistor:

1. By directly measuring the capacitance across the 24.9K resistor (with all the components mounted) and inserting a capacitor whose value is 1/3 of that capacitance across the 75K resistor. The compensation capacitance may also be achieved through the parallel PC traces. The 2nd technique eliminates the need for an additional capacitor across the 75K resistor.

2. Using a *high input impedance (low capacitance)* scope probe. This technique is accomplished through the observation of the signal at the coax Tap and at RXT pin (pin 16) as follows: Apply a square wave signal (0 to –2 Volts) to the coax Tap and observe the signal at the RXT pin. The signal at the RXT pin should be 1/4 of the signal at the coax. The signal at RXT should be somewhat underdamped to compensate for the scope probe 1–2 pF capacitance loading (see Figure 7).

   If a high input impedance (low capacitance) scope probe is not available, compensate for the capacitance of the available probe (the probe used for the RXT pin, pin 16) by adding a capacitor across the 75 kOhm resistor. For example, if the scope probe capacitance is 12 pF, place a 4 pF capacitance across the 75 kOhm resistor. The compensation for the scope probe capacitance ensures that any capacitance added across the 75 kOhm resistor for compensation is independent of scope probe loading.

   Once the scope observation shows the correct 4:1 ratio for the attenuator (see Figure 7), the added capacitance across the 75 kOhm (excluding the 4 pF added capacitance in the above example) is the compensation capacitance that can be added by a physical capacitor or through PC layout.

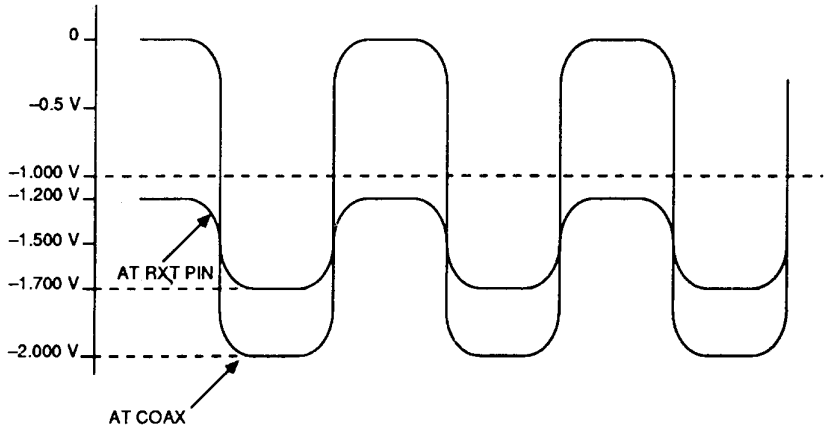

Figure 7. Attenuator Compensation Technique

NOTE.

Once the correct compensation capacitance has been determined for the prototype PC board, no more tuning should be required on the PC board when in production. The RXT input capacitance stays at what has been typically specified (1.7 pF ceramic, 1.1 pF plastic).

Coax Rise and Fall Time Measurements

The rise and fall times are specified at 25 ± 5 ns in the IEEE-802.3 standard, as well as in the Am7996 data sheet. The 10 Mbps Manchester encoded signals carry 10 MHz (all 1's or 0's) and 5 MHz (alternative 1's and 0's) signals due to the nature of the Manchester encoding. Therefore, the rise and fall time measurements should be performed at both 10 and 5 MHz as follows:

Using an IEEE-802.3 controller (e.g., Am7990, an IEEE-802.3 packet generator), send a packet which contains a series of 1's or 0's. Measure the rise and fall time in the data portion (all 1's, or 0's) for 10 MHz signals, and use the preamble portion (1010...) for 5 MHz signals. Adjust the maximum and the minimum peaks of the signal, using the vertical calibrator vernier of the oscilloscope, to form a vertical 0 to 100 grid. Using a small scale time base (e.g., 5 ns/div), measure the rise time from 10% to 90% of the signal. Note that the Am7996 transmit 10 MHz signals are attenuated somewhat relative to the 5 MHz signals due to the output stage low pass filter (the third pole) which is designed to meet the harmonic content specification of the IEEE-802.3 standard. Before measuring the 10 MHz signals, the 0 to 100% levels must be readjusted from the 0 to 100% levels of the 5 MHz signals.

The output characteristic of the low pass filter is such that an improvement can be accomplished in the rise and fall time and the rise/fall time mismatch by reducing the margin for harmonic content specification. The rise and fall time and mismatch can be reduced (improved) in value by reducing the value of C_3. C_3 can also be totally removed if the harmonic content specification is not a concern. In general, the rise and fall time mismatch directly affects the coax transmit jitter budget. The more mismatch, the more jitter will be induced on coax transmit signals.

Transmit Jitter Measurements

Jitter is the displacement of a signal transition relative to where it would ideally be placed as defined by the clock of the encoder. This displacement can be in either direction of the signal transition. The jitter can be measured for two cases:

Bit Cell Center (BCC)
Bit Cell Boundary (BCB)

BCC designates where ideally a clock transition takes place in a Manchester bit cell. The direction of the clock transition represents the value of the data. BCB designates where ideally a signal transition takes place to indicate an end of a bit cell and start of the second bit cell whose value is the complement of the previous one. The transmit jitter is the amount of the jitter which can be introduced to the coaxial cable by the MAU circuitry when transmitting. The IEEE-802.3 and the Am7996 data sheet call for 2 ns (max) (the data sheet parameter is Tskew).

One way of measuring the jitter is to produce an "eye pattern" for a bit cell center and bit cell boundary. An eye pattern can be produced (using the scope trigger control) by transmitting a packet which contains random data. As shown in Figure 8, the jitter can be measured by measuring the time between the 50% crossings of the signals which overlap each other.

Receive Jitter Measurements

The Receive jitter is the amount of jitter introduced differentially at the AUI side of the MAU at the DI± pins. The same method of jitter measurements used for measuring transmit jitter, by producing an "eye pattern" differentially at DI±, can be used for receive jitter measurements.

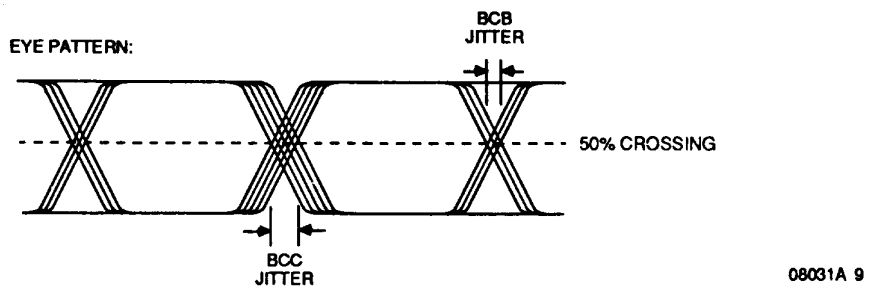

Figure 8. Jitter Measurement

The jitter measurements can be performed under 2 cases: jitter at near end and the jitter at far end. The jitter at near end is the amount of jitter which the MAU under test can produce differentially at DI± when an adjacent MAU (at a distance of 0.5 meter of RG-58, or 2.5 meter of Ethernet cable) is transmitting. The jitter at far end is when a MAU at the far end of the cable (185 meter of RG-58, or 500 meter of Ethernet cable) is transmitting. The latter case is the jitter measurement under the worst case conditions.

Collision Oscillator Frequency

The collision oscillator frequency can be measured at COLL OSC pin (pin 19). R_4 and C_1 are the RC components of the oscillator. C_1 can be adjusted for a 10 MHz nominal frequency. In the Am7996 evaluation board, a 39 pF capacitor was used to obtain a 10 MHz frequency.

APPLICATION EXAMPLES

Ethernet (IEEE-802.3, 10BASE5)

In an Ethernet application, the transceiver module (MAU) resides outside the DTE. The Ethernet coax cables run through the ceiling where the transceiver module is tapped on to it. The transceiver is linked to the DTE through a relatively flexible cable. This cable is a bundle of twisted pair wires, shielded individually, which carry the differential signals to and from the DTE and MAU. The power to the MAU is also carried through this cable. In the standard, this cable is known as Attachment Unit Interface (AUI) cable, and commercially is known as transceiver (or drop) cable. The AUI cable can be up to 50 meters long. In an Ethernet application, the Am7996 resides in the MAU, and Am7990/7992B reside in the DTE.

In Ethernet implementations, where the transceiver section resides outside the board with up to 50 meter AUI cable, there are two pulse transformers: One at the SIA side to protect the SIA, and one at the transceiver side to protect the transceiver against high voltage surges.

Cheapernet (IEEE-802.3, 10BASE2)

In the Cheapernet application, the MAU normally resides within the DTE, and the AUI cable is optional. In a typical Cheapernet controller board, the chip-set (Am7990, Am7992B, and Am7996) resides on the same board within the DTE.

Figure 9 shows a typical Cheapernet implementation using Am7990, Am7992B, and Am7996 (also refer to AMD stand alone Ethernet/Cheapernet evaluation board). For a detailed discussion of the external Ethernet/Cheapernet components to the Am7996, refer to the External Component Design Guidelines presented earlier in this application note. Most of the Cheapernet implementations also make provision for supporting the Ethernet connection. This is done by routing the ECL differential signals to the Ethernet D connector, bypassing the transceiver (Am7996), as shown in Figure 9. Note that only one pulse transformer per twisted pair is required between the Am7992B and Am7996 in Cheapernet implementations. The pulse transformer is needed to isolate the positive common mode levels of the SIA (Am7992B) from the Am7996 (which has negative common mode levels).

The SIA external components at pin 5 should be configured as shown in Figure 6 for half-step signaling when used in IEEE-802.3 applications. Ethernet Version II specification makes it optional, allowing either half-step or full-step signaling for connection with transceivers. Most of the current transceiver modules support the half-step signaling which is recommended by the IEEE-802.3 standard.

The Am7992B SIA generates negative narrow spikes (less than 10 ns, within 200 mV) every time RCLK (pin 4) is running. The spikes are due to the RC circuitry around TSEL (pin 5). The TSEL pin is an open collector output and a sense amplifier input. The gain of the amplifier is about four. The RC circuit controls the decay of the last positive transition (end of the packet) at Transmit± when half-step signaling is used (TSEL is grounded for full-step signaling).

The positive transitions on RCLK couple capacitively with the adjacent pin having the 510 Ohm pull up to V_{CC}. This noise is then amplified and appears as spikes at Transmit±. The problem is significant only when the SIA is receiving a packet (RCLK active) or when TEST is grounded (continuous RCLK). Any false signals at Transmit± meeting the amplitude and pulse width requirement can wake up the transceiver causing a collision to occur. Usually, the spikes are too narrow to wake up the transmitter section of the transceiver. As an extra precaution, a 20 pF or higher (50 pF if spikes are more than 200mV) capacitor across 510 Ohms can reduce the spikes significantly.

Consider the 40.2 Ohm resistors at the SIA side receive± and collision±, and at the transceiver side DO±, (see Figure 9). One may think that there is no need for the terminating resistors since no AUI cable is normally used in Cheapernet applications. True, there is no AUI cable; however, the resistors at DO± also form part of the output load when the SIA is driving transmit±,

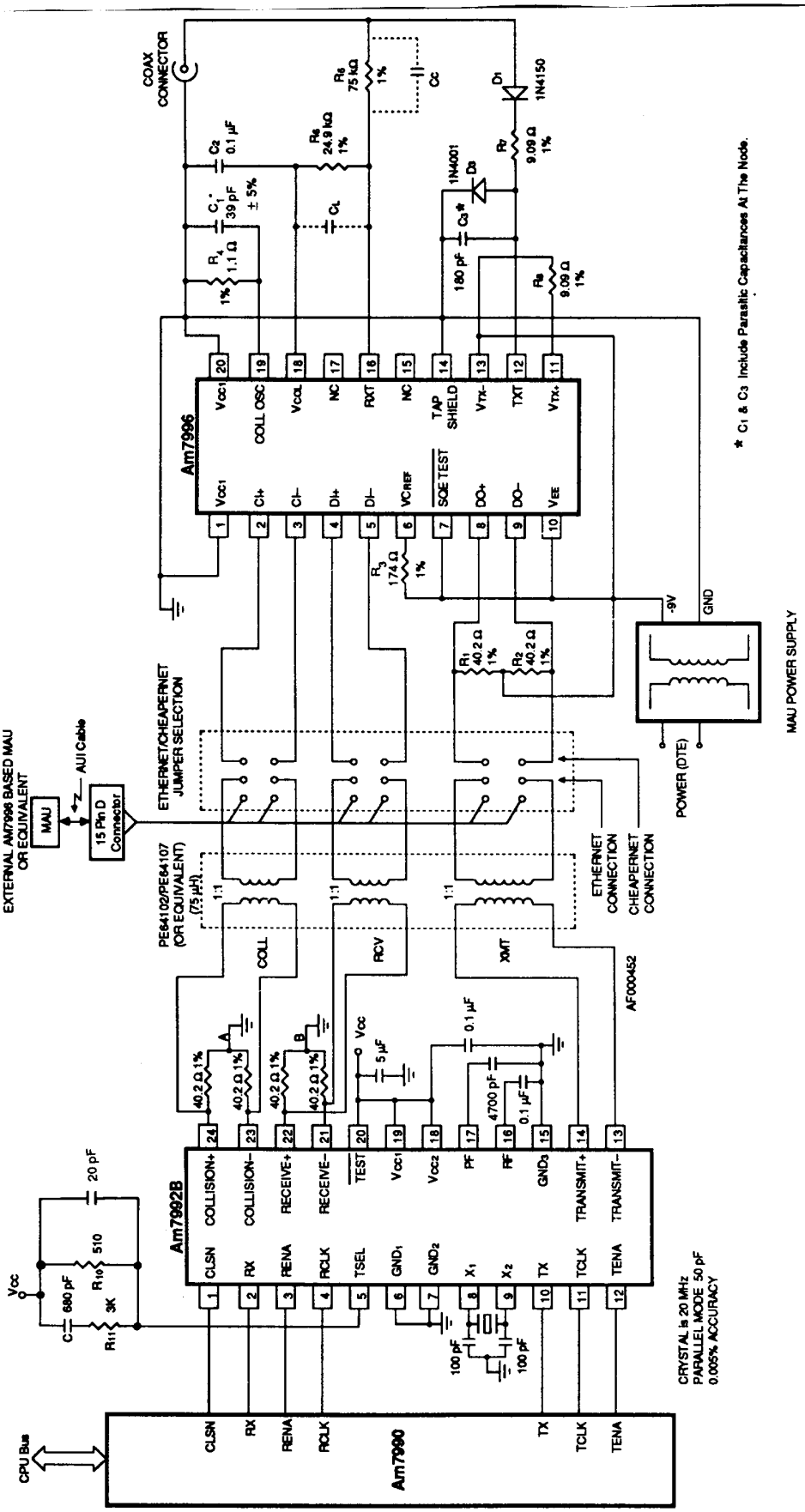

Figure 9. Am7996 Cheapernet Chip-set (Am7990, Am7992B, and Am7996) Interconnection Diagram

and the resistors at collision± and receive± form part of the output load when the transceiver is driving its CI± and DI± outputs. If these resistors are removed, the SIA and transceiver will still be functional; however, distortion on SIA/transceiver interface is more likely to occur. It is recommended that the 40.2Ω resistors be used as specified.

Repeater Design

A transceiver module is designed to drive either one Ethernet or one Cheapernet cable segment. There can be up to five cable segments as specified by the standard. Repeaters are used to link the cable segments together so that all the nodes attached to different cable segments can communicate with each other. The main function of the repeater is make all the isolated cable segments appear as one single cable. The repeater restores the energy of the signal to permit driving another cable segment. Refer to Figure 10 for a block diagram of a repeater and also to Figure 3 for a network configuration using repeaters.

There are two sides to the repeater: One side of the repeater is attached to one cable segment; the other side is attached to another cable segment. A repeater should transfer the messages across regardless of the address or the data contents of the packet. When a collision is detected on any side to which the repeater is transmitting, the repeater transmits a Jam (1010 pattern) to both sides of its connection. This mechanism ensures that the collision is recognized by all the nodes on both cable segments connected via the repeater.

When using the Am7996 in a repeater application, the external component diagram, Figure 4, should be used. In this configuration, the collision detection threshold is adjusted for receive mode collision detection, and the SQE test is inhibited.

Re-Generative Repeaters: There are two types of repeaters: re-generative and non-generative. The re-generative repeaters re-generate the 64 preamble bits (including the sync bits) normally within the frame. When a packet arrives (data carrier is detected), the repeater starts sending preamble bits to the other side while searching for the sync bits from the receiving end. When it finds the sync bits, it stores the data (the bits following the sync bits) until it is finished sending the preamble bits. Then it immediately starts sending the data. The preamble duplication mechanism ensures that any lost preamble bits, within the receiving packet, are restored before the data reaches the other cable segment.

Non-Generative Repeaters: The non-generative repeaters just repeat the signals without adding any preamble bits to the frame. The drawback with this type of repeater is that the lost preamble bits (due to the cables, transceivers, and other repeaters along the path) are not restored. Fewer preamble bits will leave less margin for the PLL decoders to lock into the Manchester data. It may take as many as 12 preamble bits for the PLL to acquire the clock in some of the VLSI decoders. The Am7992B (SIA) PLL acquires the clock in only 4 bit times.

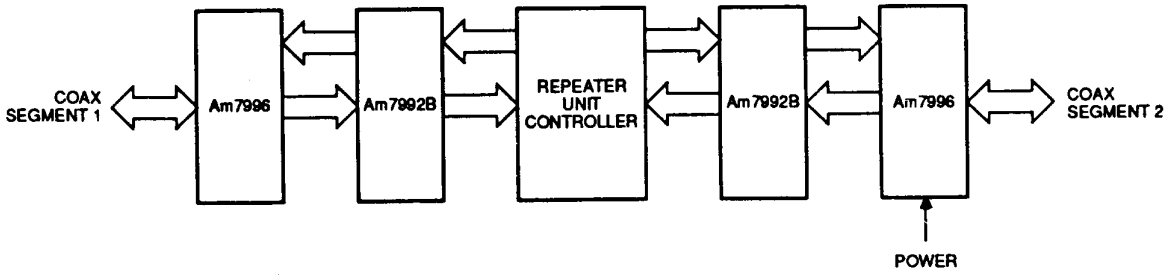

Figure 10. Typical Repeater Unit Block Diagram

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APPENDIX A

TRANSCEIVER CABLE PIN ASSIGNMENTS (IEEE 802.3)

Pin	Circuit	Description	Use
1	CI-S	Control In circuit Shield	Coll shield
2	CI-A	Control In circuit A	Coll –
3	DO-A	Data Out circuit A	Xmit (DO) +
4	DI-S	Data In circuit Shield	Rx Shield
5	DI-A	Data In circuit A	Rx (DI) +
6	Vc	Voltage Common	12 V ground
7	CO-A	Control Out circuit A	–option–
8	CO-S	Control Out circuit Shield	–option–
9	CI-B	Control In circuit B	Coll +
10	DO-B	Data Out circuit B	Xmit (DO) –
11	DO-S	Data Out circuit Shield	Xmit shield
12	DI-B	Data In circuit B	Rx (DI) –
13	VP	Voltage Plus	+ 12 V
14	VS	Voltage Shield	DTE ground
15	CO-B	Control Out circuit B	–option–
Shell	PG	Protective Ground	Chassis

ETHERNET AUI CABLE

Pin	Description	Use
1	Shield	Chassis
2	Collision Presence	Coll +
3	Transmit +	Xmit (DO) +
4	Reserved	NC
5	Receive +	Rx (DI) +
6	Power Return	12 V ground
7	Reserved	NC
8	Reserved	NC
9	Collision Presence	Coll –
10	Transmit –	Xmit (DO) –
11	Reserved	NC
12	Receive	Rx (DI) –
13	Power	+ 12 V
14	Reserved	NC
15	Reserved	NC
Shell		Chassis

APPENDIX B

RELATED HARDWARE SUPPORT

There are two different types of evaluation boards which integrate the Am7996. They are:

- Am7996 evaluation board (PN Am7996EVAL)
- Ethernet-Cheapernet Low Lost AT Board (PN ETHNEVAL5)

RELATED DOCUMENTATION

- Am7990 Family Reference Guide #03394
- Local Area Network Controller Am7990 (LANCE) Technical Manual #06363
- Interfacing the Am7990 to 7422 8-bit Microprocessors
- Am7990 (LANCE) Data Sheet #05698
- Am7992B (SIA) Data Sheet #03378
- Am7996 (Tranceiver) Data Sheet #07506

APPENDIX C

PC BOARD LAYOUT CONSIDERATIONS

To protect the transceiver from the environment and to achieve optimum performance, the Am7996 is designed to be used with two sets of external components: the transmitter circuit consisting of components D1, D2, D3, R7, R8, and C3, and the receiver circuit consisting of components R5, R6, C_L, and C_C (C_L is a parasitic capacitance rather than a discrete component). These two circuits are shown in both Figure 4 and in Figure 5. The resistor tolerances for these circuits are specified as 1% for temperature stability.

The only layout restriction for the transmitter circuit is that the longest current path from the TXT pin (pin 12) to the coaxial cable's center conductor must be no longer than 4 inches.

The layout of the receiver circuit, however, is critical. to minimize parasitic capacitance that can degrade the received signal, the external receiver circuit should be isolated from power and ground planes. There must be no power or ground plane under the area of the PC board that includes pins 15 through 20, R5, R6, and the connector for the coaxial cable. If a power or ground plane extends under this area, the receiver will not function properly due to excessive crosstalk and under- or over-compensation of the R5–R6 attenuator. Also, the RXT pin (Pin 16) should be as close to the coaxial cable connector as possible.

Since there are no severe layout restrictions on the transmitter circuit, the layout can be simplified by omittiing power and ground planes from the whole area on the right side of the Am7996 as shown in Figure11.

If the above layout rules are followed, the parasitic capacitance in parallel with R6 will be about 6 pF. This parasitic capacitance is shown in the schematics as C_L. (Note that C_L is a parasitic capacitance. Do not add a discrete capacitor in parallel with R6.) The capacitor labelled C_C in the schematics is the total capacitance in parallel with R5 including parasitic capacitance. The parasitic component of C_C will be about 1 pF. For optimum performance, the ratio of C_L to C_C should be the same as the ratio of R5 to R6, which is 3 to 1. This means that an additional 1 pF of capacitance must be added in parallel with R5.

This extra 1 pF of capacitance can easily be added by building a parallel-plate capacitor from PC traces right under resistor R5. This capacitor can consist of a 0.200 inch by 0.200 inch square of conductor on each side of the board as shown in Figure 12. (These dimensions assume that the PC board is made from 0.060 inch thick G-10 material.) The top plate of the capacitor should be connected to the one lead of R5, and the bottom plate should be connected to the other lead. Figure 13 shows an example of the suggested layout for a 4-layer printed circuit board. Note that the component labeling used in Figure 13 is not intended to correspond with the component labeling used in Figure 4 and Figure 5.

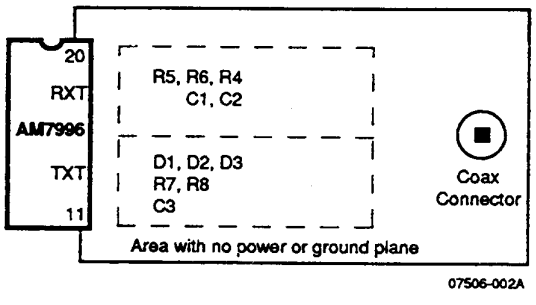


Figure 11. PC Board Outline

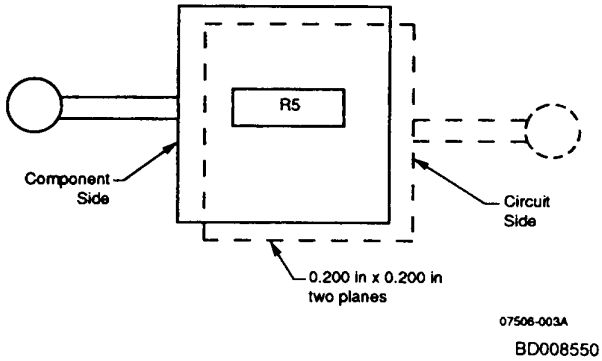
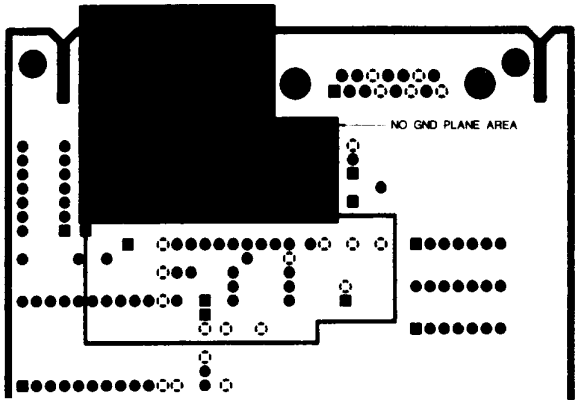


Figure 12 PC Board Trace Capacitor



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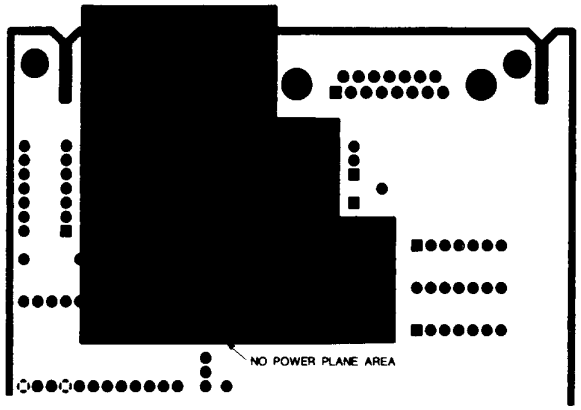
GND PLANE



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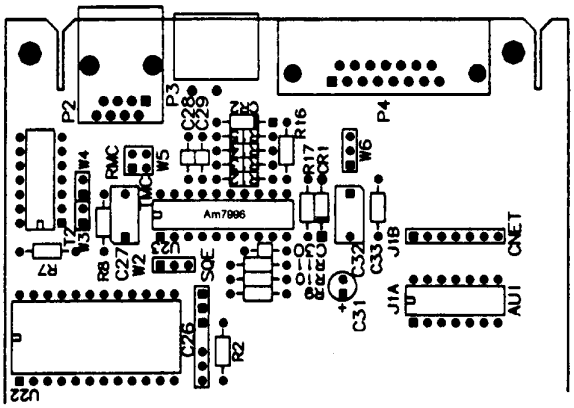
POWER PLANE



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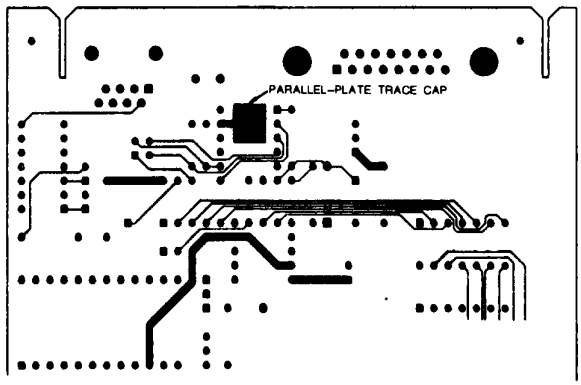

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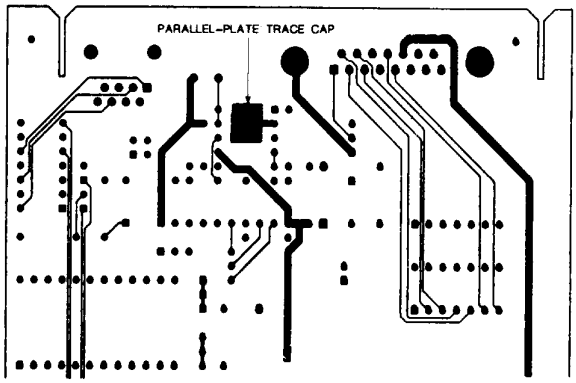

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C26	CAP-0.01UF
C27,28,29,30	CAP-0.1UF
C31	CAP-4.7UF
C32	CAP-150PF
C33	GAP CAP-0.001UF
CR1	DIODE-1N4150
CR2	DIODE-1N4001
P3	BNC
P4	15-PIN D SHELL
R2	RES-1M
R8	RES-1.1K
R9	RES-40.2
R10	RES-40.2
R11	RES-174
R12	RES-499
R13	RES-150K
R14	RES-24.9K
R15	RES-75K WITH TRACE CAP
R16	RES-9.09
R17	RES-9.09

Figure 13. Suggested Printed Circuit Board Layout for a 4 Layer PCB Application