GigaBit Logic

16G044
16G044M

T-50-17

Phase/Frequency Comparator
1 GHz Input Frequency

FEATURES

- Rising edge-triggered design
- Continuous duty cycle output response vs. input phase difference for $\pi < \theta < \pi$
- Constant duty cycle output indicating direction of error for unequal frequency inputs
- High reference frequency rejection
- Improved reference suppression compared with MC12040
- -122 dBc/Hz phase noise @ 1 KHz offset
- High speed, adjustable threshold comparator inputs for low level analog inputs
- AC - coupled or ECL/10G PicoLogic™ input compatibility
- Available in C - leaded or leadless chip carriers or in die form
- -55°C to +125°C operation (16G044M)

APPLICATIONS

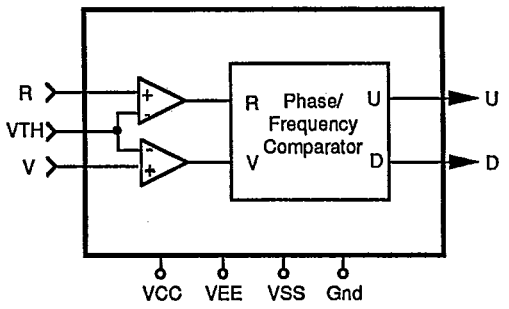
- Stable acquisition phase locked loops
- Frequency synthesizers (with 10G070 Variable Modulus Divider and 10G061 prog. counter)
- Frequency discriminators
- High speed PSK and FSK demodulators
- High resolution time delay measurement

FUNCTIONAL DESCRIPTION

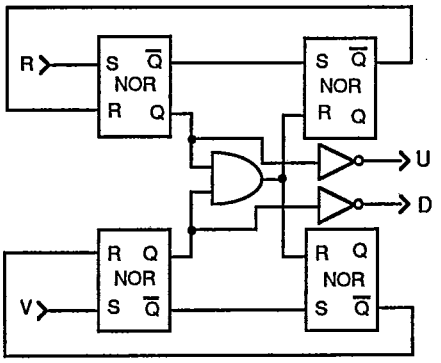
The 16G044/16G044M is a rising edge-triggered phase/frequency comparator with sensitive differential amplifier inputs capable of accepting input signals up to 1GHz in frequency. Functionally, it is similar in operation to the MC4044 or 11C44 although much faster and with much greater reference frequency rejection. When the R (Reference) and V (VCO) inputs are unequal in frequency and/or phase, the differential outputs U (Up) and D (Down) are pulse streams which when subtracted and integrated provide an error voltage for control of a VCO. This contrasts with an analog mixer or exclusive - OR based phase detector which does not produce explicit frequency error information. Use of the 16G044/16G044M in a PLL makes frequency acquisition more stable by comparison.

The 16G044/16G044M is fabricated using GigaBit's high volume, production proven GaAs MESFET process technology.

BLOCK DIAGRAM



EQUIVALENT LOGIC DIAGRAM



16G044/16G044M ORDERING INFORMATION

Package Type	16G044 (0°C to 85°C)		16G044M (-55°C to +125°C)	
	1GHz	750 MHz	1GHz	750 MHz
40-pin "C" 40-pin "L" Dice	16G044-2C 16G044-2L	16G044-3C 16G044-3L 16G044-3X	16G044M-2C 16G044M-2L	16G044M-3C 16G044M-3L 16G044M-3X

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16G044 Operation

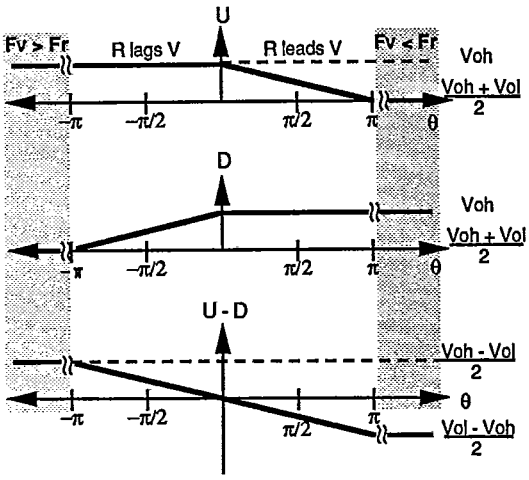


Figure 1: 16G044 Operation

The operation of the 16G044 is best explained with reference to Figure 1 which plots the average value of U, D, and U - D versus the phase or frequency difference between the R and V inputs.

Four relationships between R and V are possible: R lags or leads V in phase and Fr is less than or greater than Fv.

1. R lags V in phase

When the R and V inputs are equal in frequency but R lags V in phase, the U output is pegged high (at VOH) and the D output pulses low with a duty cycle that is proportional to the phase difference between R and V, reaching a minimum of 50% for 180° phase difference. Therefore, the average value of D varies between VOH (0° phase difference) and (VOH + VOL)/2 (180° phase difference). The signal on D indicates that the VCO frequency should be decreased to bring the loop into lock.

2. Fv > Fr

When the V input frequency exceeds that of the R input, the behavior of the 16G044 is the same as described in 1. above except that the D output duty cycle is constant at approximately 50%. The average value of D is constant at (VOH + VOL)/2 as shown in Figure 1. As above, the signal on D indicates that the VCO frequency should be decreased to establish lock.

3. R Leads V in Phase

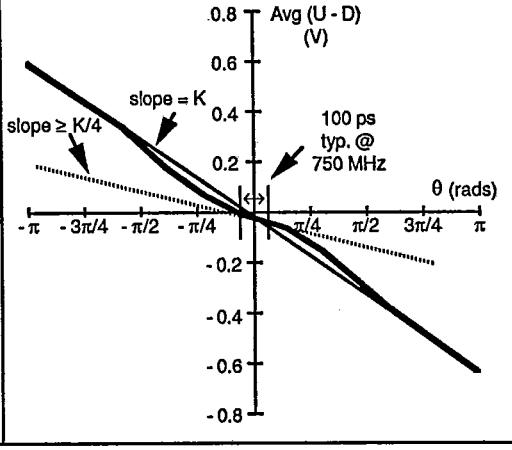
When the R and V inputs are equal in frequency but R leads V in phase, the D output is held high (at VOH) and the U output pulses low with a duty cycle that is proportional to the phase angle between R and V, reaching a minimum of 50% for 180° phase difference. The average value of U varies between VOH (0° phase difference and (VOH + VOL)/2 (180° difference). The signal on U indicates that the VCO frequency should be increased to establish lock.

4. Fv < Fr

When the V input frequency is less than the R input signal frequency, the 16G044 operates as described in 3. above except that the U output duty cycle does not vary, but is constant at approximately 50%. Therefore the average value of U is constant at (VOH + VOL)/2 as shown in Figure 1. Again, the signal on U provides information used to increase the VCO frequency to establish loop lock.

Note that when R and V are equal in frequency and phase, i.e. when the loop is locked, the average value of U - D is zero, meaning that the action of the 16G044 is to maintain the loop in lock status.

Figure 2: 16G044 Transfer Characteristic at 750 MHz (see Fig. 4)



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16G044 Operation (continued)

Figure 2 plots the transfer characteristic of the 16G044 with equal frequency R and V inputs at 750 MHz. The slope of the curve drawn as the solid straight line is the comparator gain constant, K, and is typically 600 mV/π radians or 0.19 V/rad. The reduction in K in the vicinity of zero phase difference is of particular interest to PLL system designers. The 16G044 is designed to minimize this decrease in gain to ≥ K/4 and to limit the range of flattening to less than 100ps or 27° (± 13.5°) of phase at 750 MHz.

Figure 3 describes the logical I/O characteristics of the 16G044 which is useful for purposes of testing the device at low speed.

Figure 3: 16G044 State Table

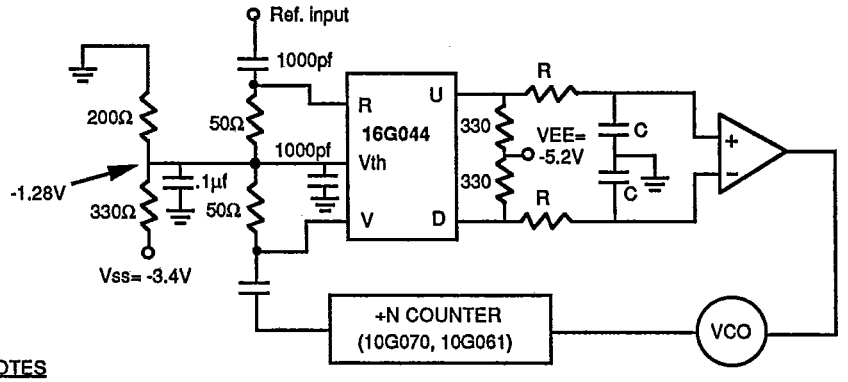
	Inputs		Outputs		Notes
	R	V	U	D	
R leads V	0	0	1	1	A
	↓	0	0	1	
	X	↓	1	1	
R lags V	0	0	1	1	A
	0	↓	1	0	
	↓	X	1	1	

Note A: This table assumes that the 0, 0 input state shown was preceded at some time with a falling edge (1—> 0) transition in both R and V.

PIN DESCRIPTIONS

R	Reference signal input
V	VCO signal input
U	The "Up" (R leads V) output
D	The "Down" (R lags V) output
VTH	Threshold voltage input for the input comparators. Must be in the range - 1.8V ≤ Vth ≤ - 0.8V
VCC	+ 5.0V supply pin
Gnd	Ground connection
VSS	- 3.4V supply pin
VEE	- 5.2V supply pin

16G044 Application in a Simple Phase Locked Loop



NOTES

1. The transfer characteristic of the simple loop filter shown is 1/(1 + sT) whereT = RC. Typically R should be chosen to be >1KΩ. The connections to the op-amp assume a negative VCO gain constant. These connections should be reversed if a VCO with a positive transfer characteristic is used.

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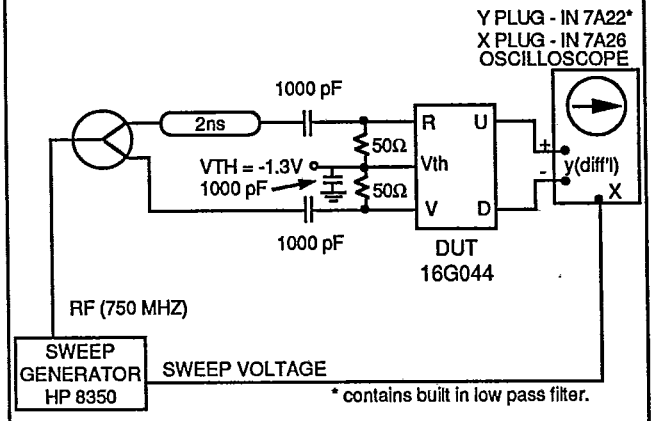
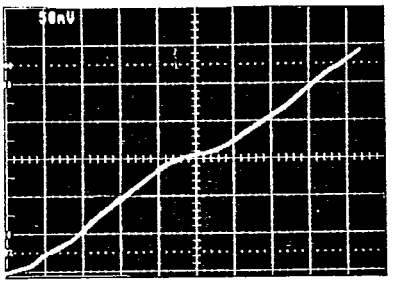
Figure 4. Test setup for high speed measurement of phase detector transfer characteristic.

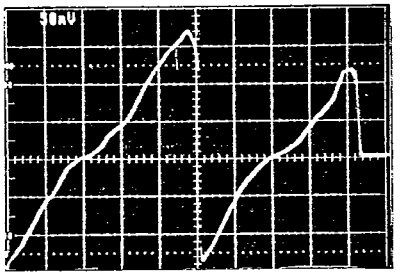


This test setup creates a delay line frequency discriminator which enables accurate linearity measurements of the phase detector. The resulting discriminator has zero output voltage at 500MHz and 1 GHz.

Figure 4 Oscillographs (0 dBm Input)



(Y = 250 mV/div., X = 250 to 750 MHz)



(Y = 250 mV/div., X = 300 to 1300 MHz)

ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	-65°C to + 150 °C	
TJ	Junction Temperature	-55°C to + 150 °C	
TC	Case Temperature Under Bias	-55°C to + 125 °C	2
VCC	Supply Voltage	0V to + 7.0V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	- 6.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = - 3.4 V, VEE = - 5.2 V	- 4.0 V to + 0.5 V	
I IN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to +0.5 V	3
IOUT	Current From Any Output; Continuous	-40 mA	
PD	Power Dissipation Per Output POUT = (-VOUT) x IOUT	50 mW	

Notes:
1. All voltages specified relative to Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and PD limitations.
4. Power supply sequencing is not necessary. However, sustained (>5 secs.) application of VSS in the absence of VEE could result in excessive power dissipation and damage to the device.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Operating Temperature		+25		°C	1
Gnd	Ground connection		0		V	
VCC	Supply Voltage	4.75	5.0	5.25	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	

Notes: 1. TC measured at case top. User attention to device thermal management is recommended. See GigaBit Application Note 3 for a detailed treatment of thermal management considerations.

DC CHARACTERISTICS (1,2)

VCC = 4.75V to 5.25V, VSS = -3.3V to -3.5V, VEE = -5.1V to -5.5V

		16G044 (0°C to 85°C)			16G044M (-55°C to +125°C)				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	NOTES
CMR	Input common mode range	-1.8		-0.8	-1.8		-0.8	V	
VIH	Input voltage high	-1.0		Gnd	-0.8		Gnd	V	
VIL	Input voltage low	VTT		-1.6	VTT		-1.8	V	
IIN	Input current	-300		300	-300		300	µA	3
VOH	Output voltage high	-0.8	-0.6	-0.3	-1.0	-0.6	-0.3	V	4
VOL	Output voltage low	VSS	-2.6	-1.8	VSS	-2.6	-1.8	V	4
IOH	Output high current		-25	-20		-25	-20	mA	5
ICC	VCC supply current		45	70		45	75	mA	
ISS	VSS supply current		75	120		75	130	mA	
IEE	VEE supply current		50	80		50	85	mA	
PD	Power dissipation		750	1170		750	1260	mW	6

Notes:
1. These characteristics are applicable from DC to ~ 500 MHz.
2. VTH = -1.3V
3. Vin = -1.0V to -1.6V
4. Outputs terminated 100Ω to VTT = -2.0V.
5. IOH is the available output current at VOH = -0.8V.
6. At nominal power supply voltages and 50% output duty cycle.

AC CHARACTERISTICS

VTH = -1.3V, VCC = 4.75V to 5.25V, VSS = -3.3V to -3.5V, VEE = -5.1V to -5.5V, outputs terminated in 100Ω to VTT = -2.0V

		16G044 (0°C to 85°C)			16G044M (-55°C to +125°C)				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input voltage high	-1.0		-0.3	-1.0		-0.3	V	
VIL	Input voltage low	VTT		-1.7	VTT		-1.7	V	
Kd2	Large signal gain constant (-2 version)	500/π	600/π	900/π	500/π	600/π	900/π	mV/rad	f = 1GHz
Kd3	Large signal gain constant (-3 version)	500/π	600/π	900/π	500/π	600/π	900/π	mV/rad	f = 750 MHz
kd2	Small signal gain constant (- 2 version)	125/π	300/π	450/π	125/π	300/π	450/π	mV/rad	f = 1GHz
kd3	Small signal gain constant (- 3 version)	125/π	300/π	450/π	125/π	300/π	450/π	mV/rad	f = 750 MHz

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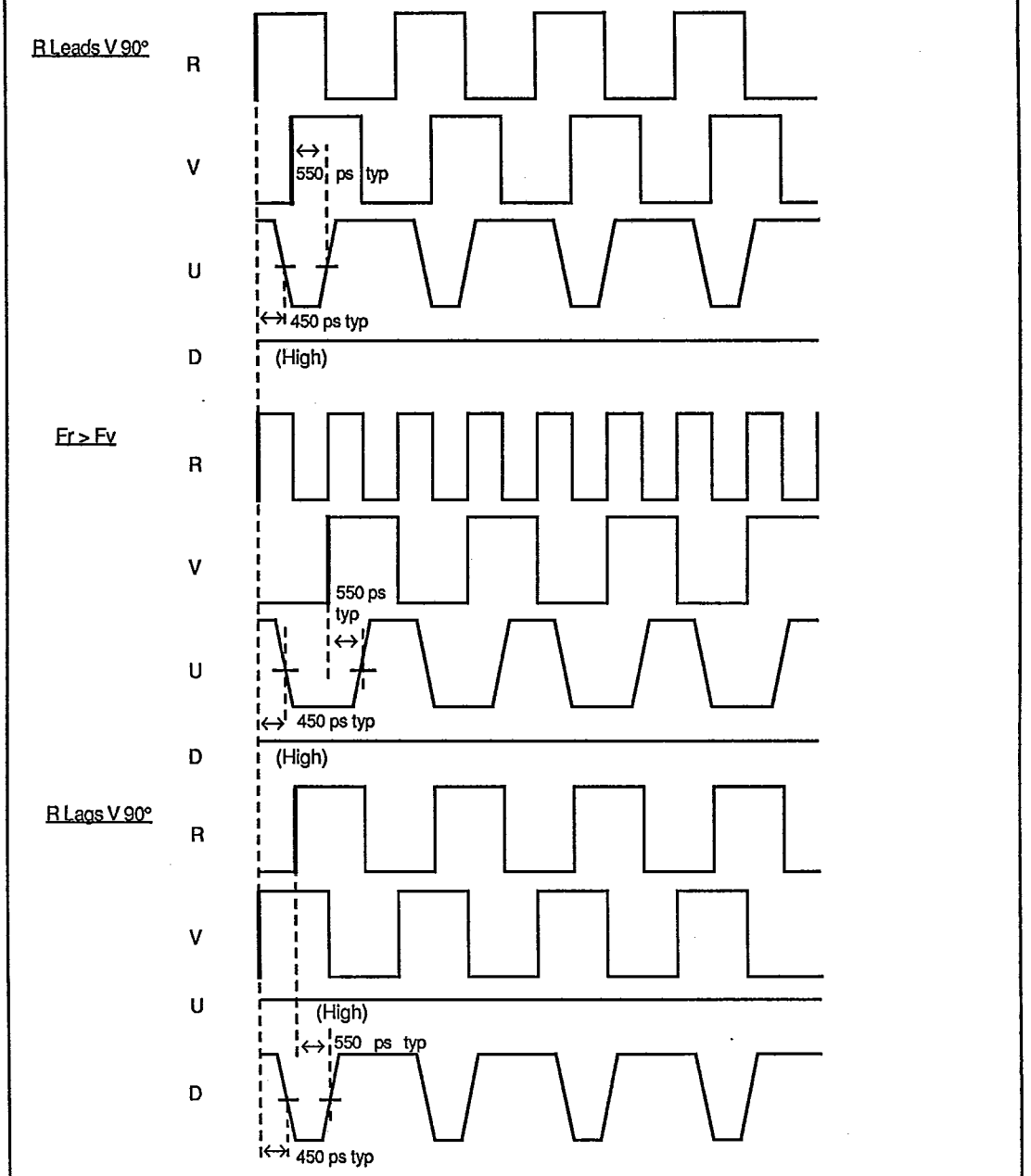
AC WAVEFORMS



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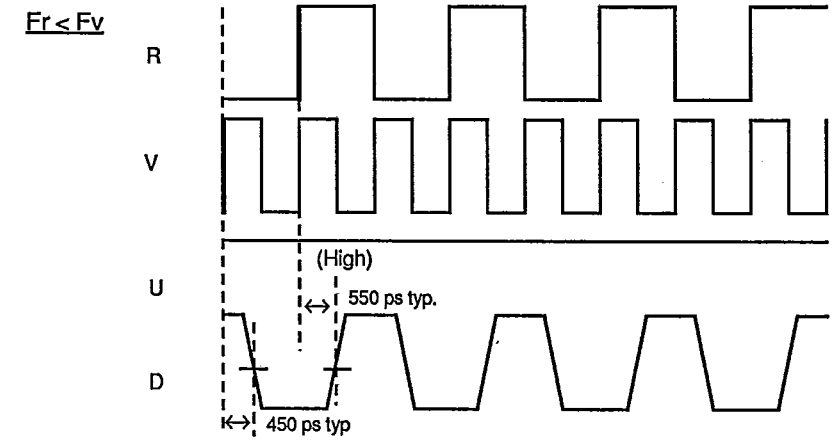
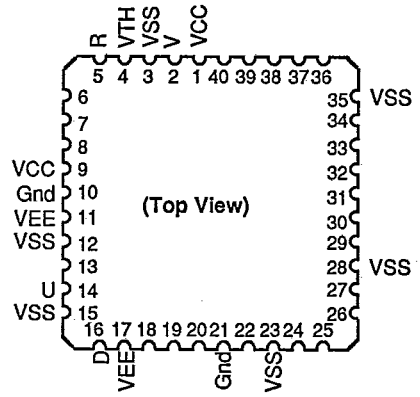
AC WAVEFORMS (cont.)



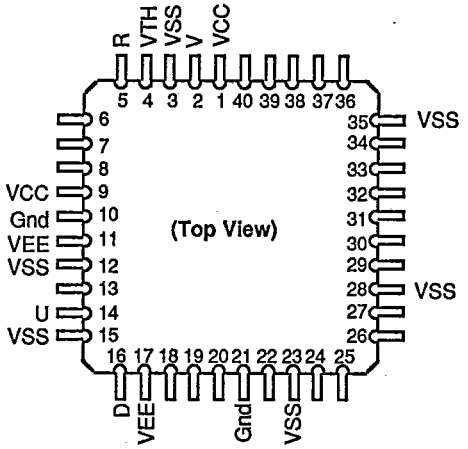
PACKAGE PINOUT DIAGRAMS

PACKAGE TYPE "L"



NOTES: Pin 1 is marked for orientation; all unmarked pins are unused.

PACKAGE TYPE "C"



NOTES: Pin 1 is marked for orientation; all unmarked pins are unused.

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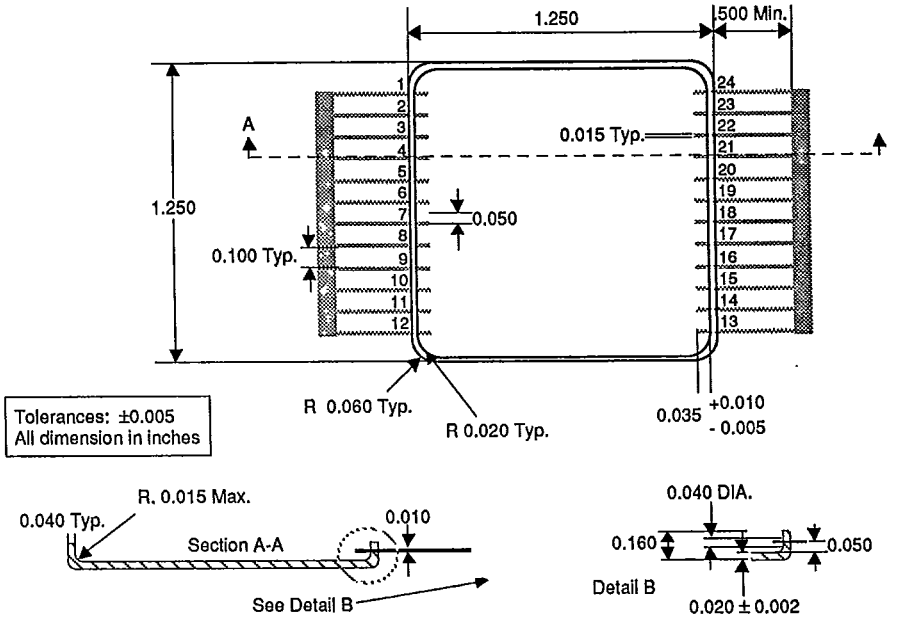
24 PIN HYBRID 18 PIN PACKAGE

T-90-20

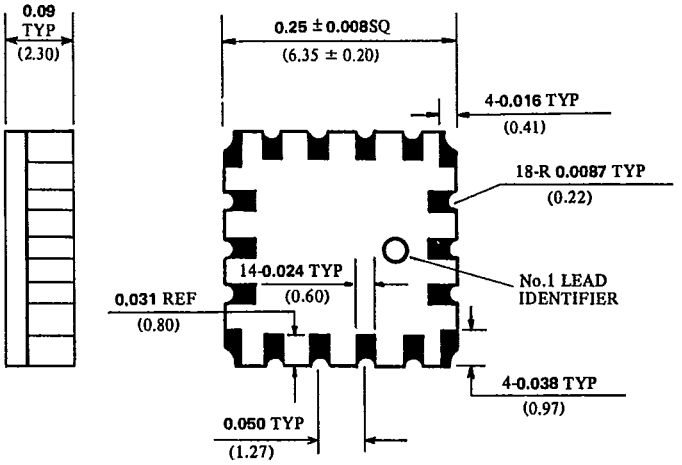
24 PIN HYBRID PACKAGE

Type H



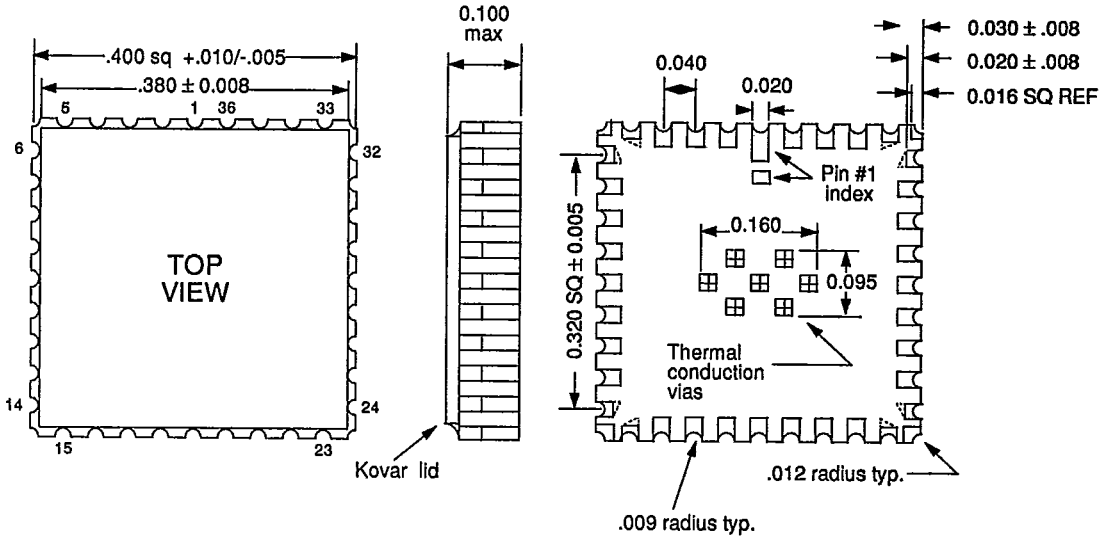
18 PIN LEADLESS CHIP CARRIER

TYPE L1



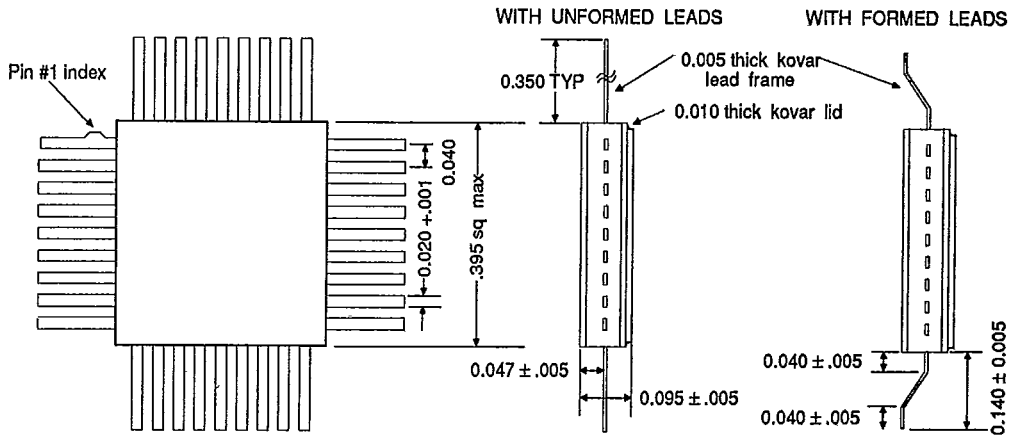
All dimensions shown in **inches** and (millimeters)

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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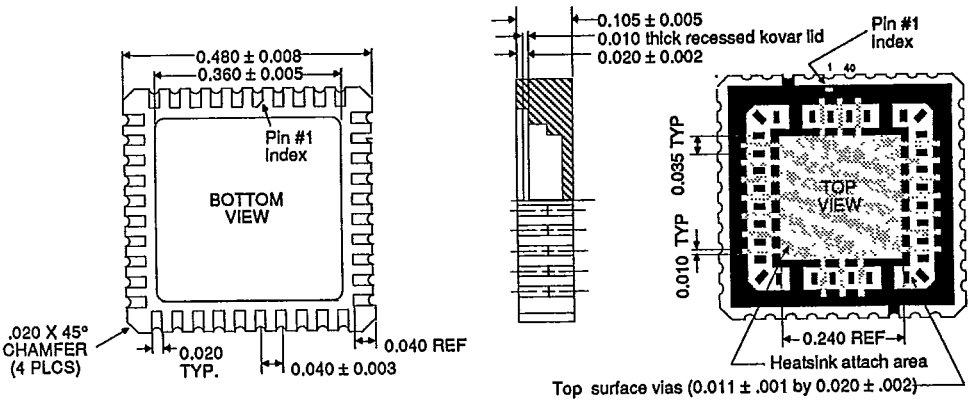
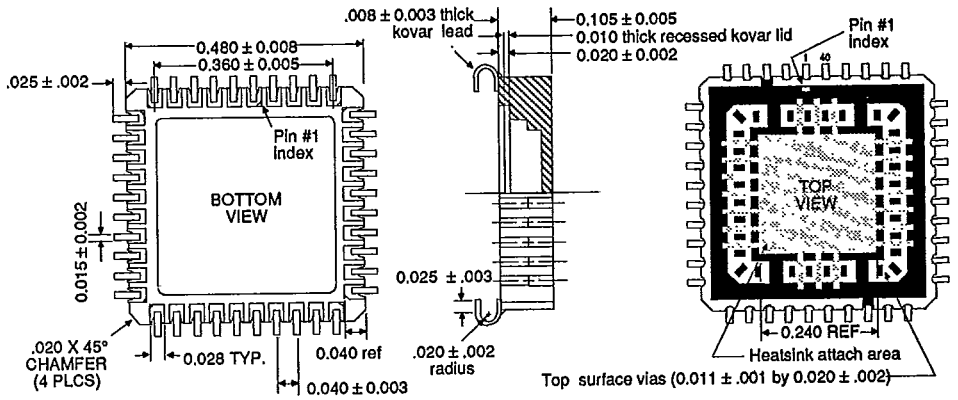
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

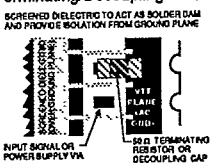


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail



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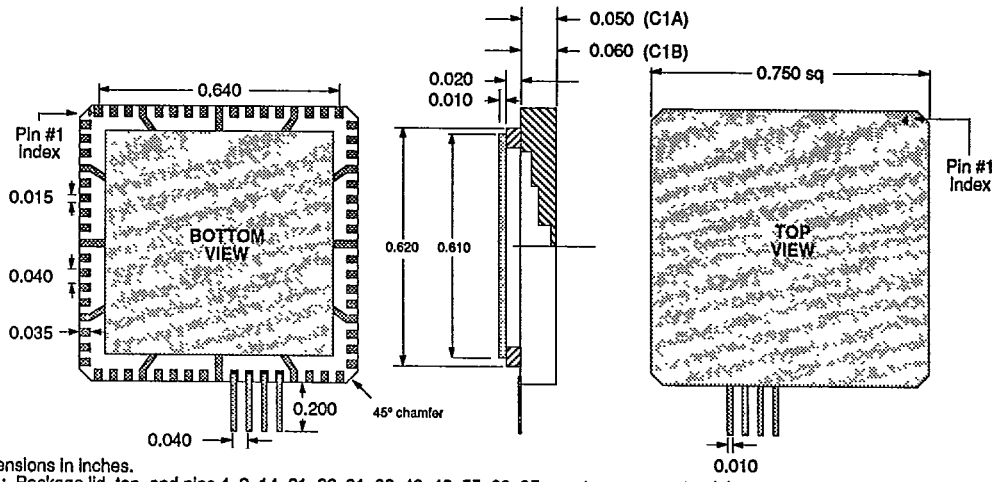
68 & 132 PIN PACKAGES

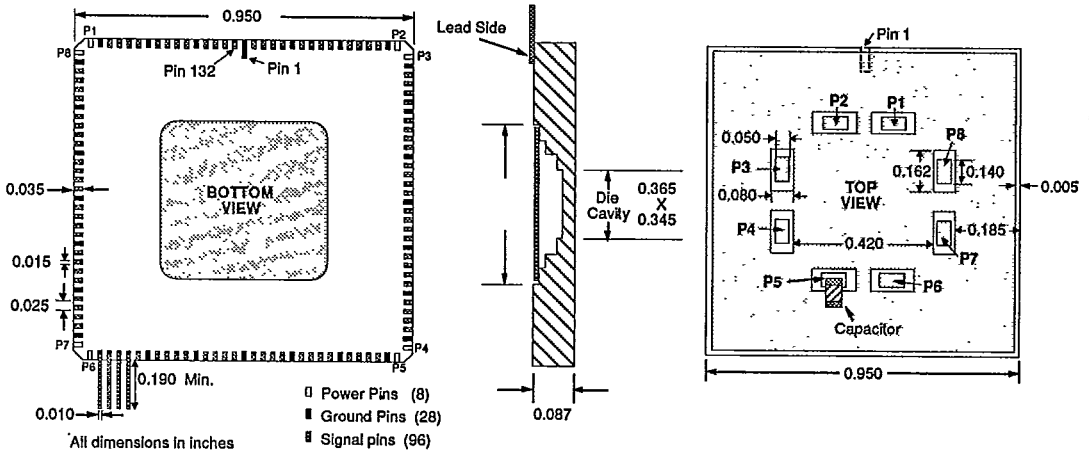
T-90-20

68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



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