UM0044
User manual

FlashLINK JTAG programming cable for PSD and uPSD

Features

- Allows PC or Notebook parallel port to program uPSD and PSD devices using PSDsoft Express software development tool.
- Supports IEEE 1149.1 JTAG signals (TCK, TMS, TDI, TDO).
- Supports additional signals (TSTAT and $\overline{\text{TERR}}$) to reduce programming time.
- Single FlashLINK Cable assembly supports both 3.3V and 5V target devices with no manual configuration. Target device may operate from 2.7V to 5.5V.
- “Flying Lead” cable included to adapt to any target connector using 0.025” square posts.
- “LoopTest” cable included to validate PC parallel port operation.

Overview

The family of Flash PSD and uPSD devices offer In-System Programming (ISP) allowing a completely blank device to be programmed while soldered to a circuit board. This simplifies manufacturing and provides an effective way to update products after they are in use.

Flash PSD and uPSD devices comply to the core requirements of the IEEE 1149.1 JTAG specification. However, these devices do not support boundary scan functions. Instead, they support ISP, and some uPSD devices support emulation through JTAG.

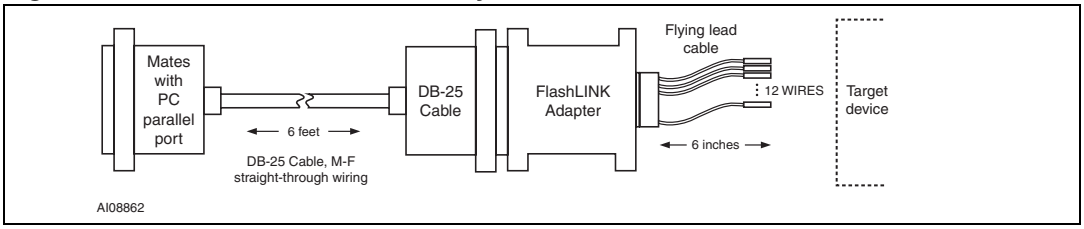
The FlashLINK cable assembly shown in *Figure 1* will perform ISP only on uPSD and PSD devices, not memory or logic devices from other vendors. The software development tool PSDsoft Express is a Windows based program which operates the FlashLINK cable assembly (PSDsoft Express may be downloaded at no charge from www.st.com/psm). PSDsoft Express supports device chaining, meaning more than one uPSD or PSD device can reside in a single JTAG chain. Also, other devices (memory, logic from other vendors) may reside in the JTAG chain, but these devices will stay in BYPASS Mode.

PSDsoft Express will generate BSDL, JAM STAPL, and SVF files for use with 3rd party JTAG programming equipment.

The four basic JTAG pins (TCK, TMS, TDI, TDO) on uPSD devices are dedicated to operate as JTAG pin at all times. However, the four JTAG pins on PSD devices may also be used for general I/O functions.

ST has created two optional JTAG signals (TSTAT and $\overline{\text{TERR}}$) to reduce programming times. These pins supply programing status on signal pins rather than having to scan out the status serially for each byte programmed in Flash memory. Program times using this method (6-pin JTAG) can be as much as 30% less than the standard method (4-pin JTAG).

Figure 1. FlashLINK cable assembly



1. 14-pin ribbon cable may also be used. *Not supplied in FL-101 Kit.*

Contents

1 Pin definition on FlashLINK adaptor

Table 1. Pin description for 14-pin FlashLINK adaptor connector

Pin #	Signal Name	Description	Type(1)	FlashLINK is Signal:
1	JEN	JTAG Enable - active-low when JTAG traffic is present	OC	Source
2	$\overline{\text{TRST}}$(2)	JTAG Reset on target, active-low, optional per IEEE 1149.1	OC	Source
3	GND(3)	Signal Ground		
4	CNTL(2)	Generic Control signal	OC	Source
5	TDI	JTAG IEEE 1149.1 Serial Data Input		Source
6	TSTAT	JTAG-ISP Programming Status to speed programming, optional		Destination
7	V_{CC}(4)	DC source from target, 2.7V to 5.5V		
8	RST	Target system reset, recommended	OC	Source
9	TMS	JTAG IEEE 1149.1 Mode Select		Source
10	GND	Signal Ground		
11	TCK	JTAG IEEE 1149.1 Clock		Source
12	GND	Signal Ground		
13	TDO	JTAG IEEE 1149.1 Serial Data Out		Destination
14	TERR	JTAG-ISP Programming Error Status to speed programming, optional		Destination

Note: 1 OC = Open Collector, pulled-up to V_{CC} inside FlashLINK Adaptor.

2 Not supported by PSDsoft Express, signals remain inactive.

3 All signal grounds are tied together inside FlashLINK Adaptor.

4 The target must supply V_{CC} to the FlashLINK Adaptor (2.7V to 5.5VDC, 15mA max at 5.5V).

Not all 14 signals are required for all applications. Here is how they are used:

- (6) Core signals that must be connected: TDI, TDO, TMS, TCK, V_{CC}, GND
- (2) Optional signals that reduce programming time as much as 30%: TSTAT and $\overline{\text{TERR}}$
- (1) Optional signal to control multiplexing of JTAG signals (PSD only) or to indicate JTAG activity: $\overline{\text{JEN}}$
- (1) Optional IEEE-1149.1 signal for JTAG chain reset: $\overline{\text{TRST}}$
- (1) Optional (but recommended) signal to allow FlashLINK to reset target system after ISP: $\overline{\text{RST}}$
- (1) Optional generic control signal to target system from FlashLINK: CNTL
- (2) Two additional ground lines to help reduce EMI if a ribbon cable is used. These ground lines “sandwich” the TCK signal in the ribbon cable. These two ground signals are not present on the flying lead cable.

2 Connector definition

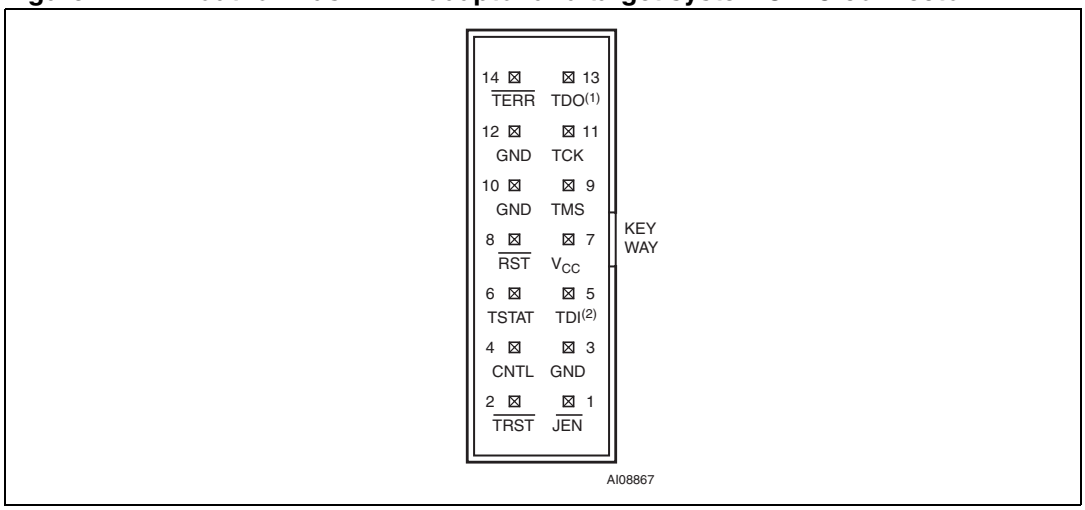
There is no industry standard JTAG connector. Each device manufacturer differs. ST has a specific connector and pinout for the FlashLINK Adaptor. The connector scheme on the FlashLINK connector can accept a standard 14-pin ribbon cable connector (2 rows of 7 pins on 0.1” centers, standard keying) or any other user specific connector that can slide onto 0.025” square posts. The pinout for the FlashLINK Adaptor connector is shown in *Figure 2*.

A standard ribbon cable is a good way to quickly connect to the target circuit board. If a ribbon cable is used, then the receiving connector on the target system should be the same connector type with the same pinout as the FlashLINK Adaptor shown in *Figure 2*.

Note: The JTAG signal TDI is sourced from the FlashLINK Adaptor and should be routed on the target circuit board so that it connects to the TDI input pin of the PSD or uPSD device.

The JTAG signal TDO is an input received by the FlashLINK Adaptor and is sourced by the PSD or uPSD device on its TDO output pin. See Figure 3 on page 8, Figure 4 on page 9, and Figure 5 on page 10 for more information.

Figure 2. Pinout for FlashLINK adaptor and target system JTAG connector



Note: This diagram perspective is looking into the face of the shrouded male connector on the FlashLINK Adaptor, 0.025-inch (0.635mm) posts on 0.100-inch (2.54mm) centers. Connector reference: Molex 70247-1401.

Recommended ribbon cables for quick connection of the FlashLINK Adaptor to the end-product: Samtec HCSD-07-D-06.00-01-S-N; Digikey M3CCD-14065-ND.

Note: 1 TDO is a signal destination on the FlashLINK and a signal source on the target board.

2 TDI is a signal source on the FlashLINK and a signal destination on the target board.

3 Software

The FlashLINK cable assembly is driven by the software development tool PSDsoft Express (available at no charge from www.st.com/psm). With this tool you define the pin functions, memory map, and PLD configuration of PSD or uPSD devices, add microcontroller firmware to be programmed into Flash memory, then generate a single file to program into the device (an object file with the filename extension *.obj). PSDsoft Express will then use the FlashLINK cable assembly to program this object file into the PSD or uPSD device. Other operations include erase, verify, upload, and blank check. See the PSDsoft Express User Manual for more detail.

Note: Be sure to use the latest version of PSDsoft Express. Updates are available from www.st.com/psm.

3.1 Diagnostic tests

PSDsoft Express also performs some diagnostic tests for the PC parallel port and FlashLINK cable assembly.

3.1.1 Loop test

Should be run first to test basic operation of the PC parallel port and the FlashLINK cable assembly. “LoopTest” will wrap FlashLINK signal outputs back into FlashLINK signal inputs for signal path verification.

3.1.2 Connect test

Is optional to test system performance and check the JTAG signal path all the way through the target circuit board including PSD or uPSD device.

To run these tests, install and run PSDsoft Express on your PC or laptop:

1. Connect the six foot long DB-25 cable to your PC parallel port on one side, and to the FlashLINK Adaptor on the other side.
2. Click mouse on the JTAG ISP programmer box at the bottom-left of the PSDsoft Express main flow diagram.
3. Select single or multiple JTAG devices depending on your target configuration (single is most common), then click on the Hardware Setup (“HW Setup”) box at the lower part of the JTAG Operations window.

For “LoopTest”:

1. Connect the small loop test adaptor cable (not the flying lead cable) to the 14-pin connector on the FlashLINK Adaptor.
2. Connect the red lead of the loop test connector to a V_{CC} source (5V or 3.3V), and connect the black lead of the loop test connector to ground.
3. In the “HW Setup” box click the “Loop Test” box to run the test. If it fails, be sure that your are supplying V_{CC} and ground, and also make sure that the PC’s parallel port is enabled.

For “Connect Test”:

1. Connect the “Flying Lead” cable, or a ribbon cable to the FlashLINK Adaptor, and also connect it to your target circuit board just as if you are ready to program the device.
2. Turn on the power on the target device, and then click the “Connect Test” button in the “HW Setup” box.

This test involves the circuit traces on your circuit board. If there is a failure, it is likely due to signal routing or signal integrity on the target circuit board, or the PC may have compatibility problems with the parallel port driver used by PSDsoft Express.

Note: If either test fails, you will see a window pop-up that allows you to email in the problem. Please do so and we will assist you.

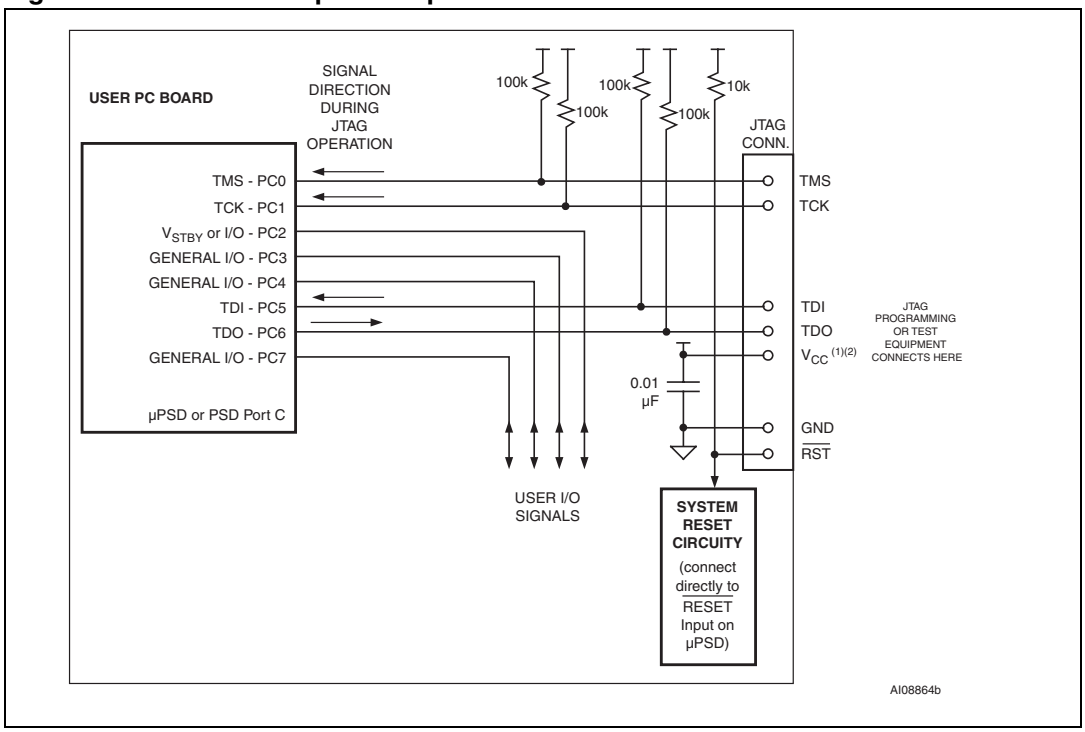
4 Circuit examples

4.1 4-pin JTAG

The first example shown in *Figure 3* uses the standard JTAG signals (4-pin JTAG). This is the default configuration in PSDsoft Express (4-pin JTAG).

Note: The recommended pull-up resistors and decoupling capacitor are near the JTAG connector.

Figure 3. Circuit example for 4-pin JTAG



Note: 1 For 5V uPSD3xxx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 5V system V_{DD}.

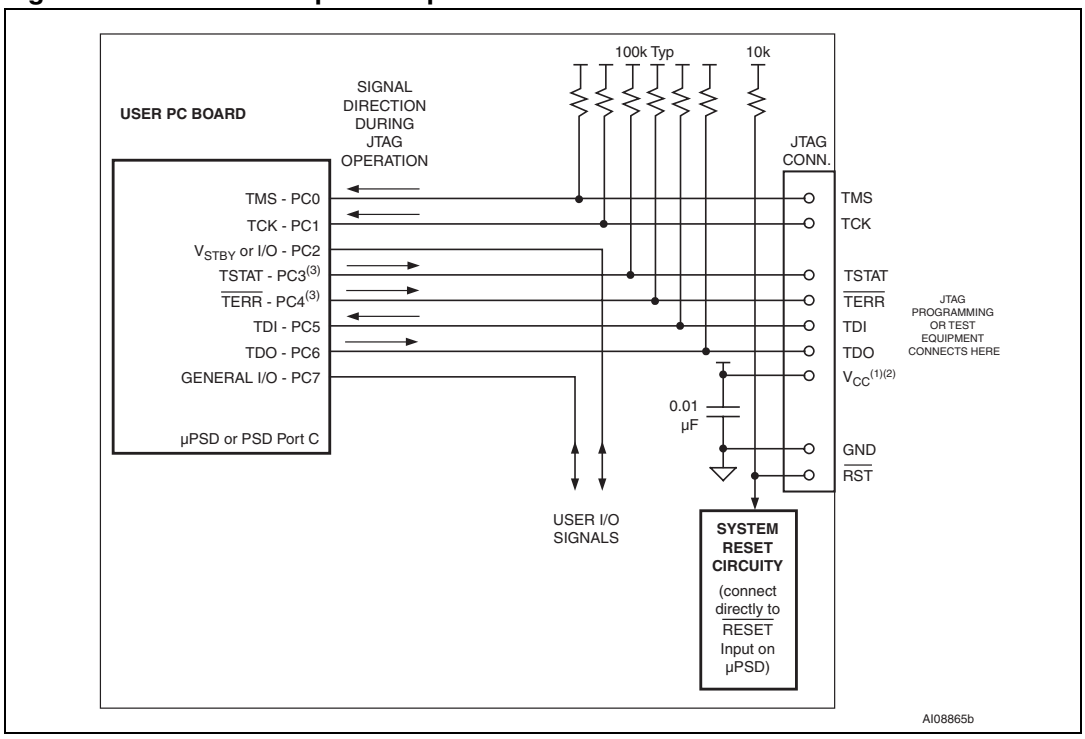
2 For 3.3V uPSD3xxx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 3.3V system V_{CC}.

4.2 6-pin JTAG

The second example in *Figure 4* uses the two additional (and optional) JTAG signals TSTAT and $\overline{\text{TERR}}$ to reduce programming time.

To configure this in PSDsoft Express, just click on pin PC3 or pin PC4 and choose “Dedicated JTAG” function. These two signals must be used as a pair, so choosing either one for JTAG will assign both to dedicated JTAG function.

Figure 4. Circuit example for 6-pin JTAG



Note: 1 For 5V uPSD3xxx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 5V system V_{DD}.

2 For 3.3V uPSD3xxx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 3.3V system V_{CC}.

3 TSTAT and $\overline{TERR}$ are not part of the IEEE 1149.1 Specification.

4.3 Multiplexed JTAG (PSD only)

The third example in *Figure 5* illustrates one method to multiplex JTAG signals with general I/O functions (PSD only, not available on uPSD). In this example, the PLD input pin at PC7 was chosen (this could be any PLD input pin) to control how the JTAG pins operate. The signal $\overline{JEN}$ from the FlashLINK Adaptor drives PC7. When $\overline{JEN}$ is active (logic low), the JTAG pins operate as JTAG. When $\overline{JEN}$ is inactive (logic high), the JTAG pins operate as general I/O. You must configure this in PSDsoft Express by declaring the JTAG pins as general I/O (not dedicated JTAG pins), then configure one PLD input pin (PC7 in this example), then you must define an equation which will toggle the JTAG pin operation between JTAG and general I/O.

To define this equation in PSDsoft Express:

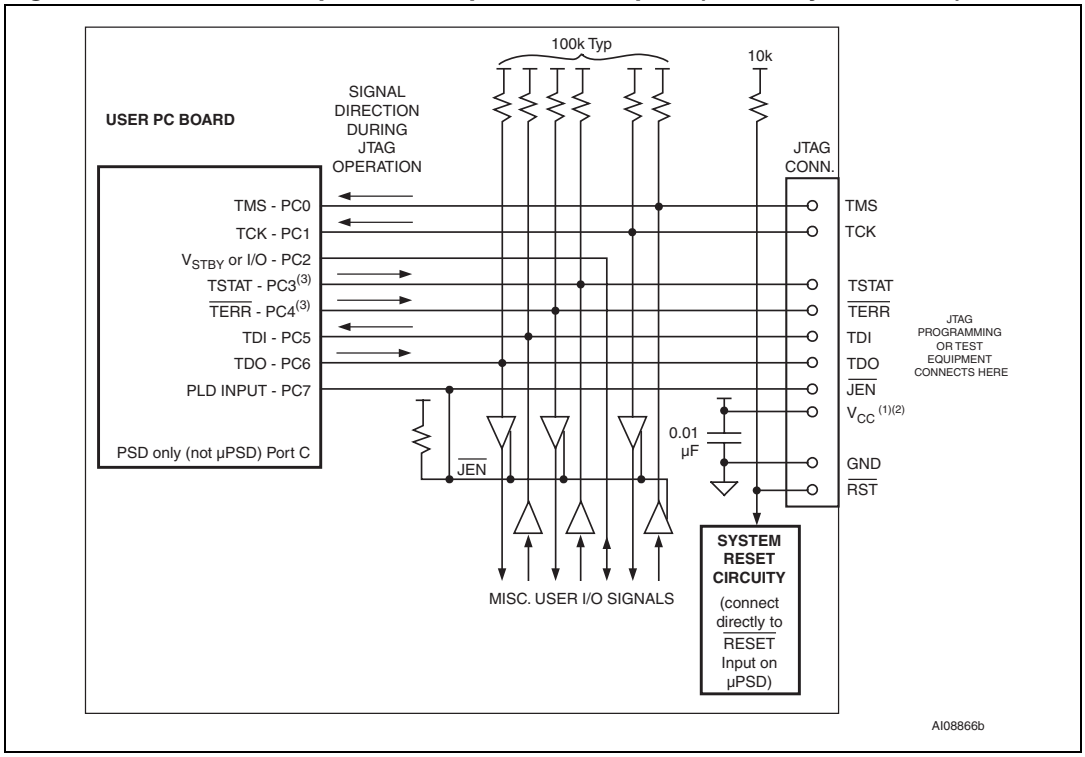
1. Click on the “JTAG Enable Tab” in the Design Assistant window.
2. Write the equation for the internal node “jtagsel”, which controls the function of JTAG pins (jtagsel logic high is JTAG, logic low is I/O).

For the example in *Figure 5*, the equation should be jtagsel = !PC7, so you would just have to type !PC7 in the equations box and PSDsoft Express will do the rest.

Note: You can click on the “Show Eq” button to see the resultant equation.

Note: $\overline{JEN}$ controls the tri-state buffers on the general I/O pins to avoid signal conflict when operating in JTAG Mode or General I/O Mode.

Figure 5. Circuit Example for Multiplexed JTAG pins (PSD only, not uPSD)



Note: 1 For 5V uPSD3xxx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 5V system V_{DD}.

2 For 3.3V uPSD3xxx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 3.3V system V_{CC}.

3 TSTAT and $\overline{TERR}$ are not part of the IEEE 1149.1 Specification.

5 Chaining JTAG devices

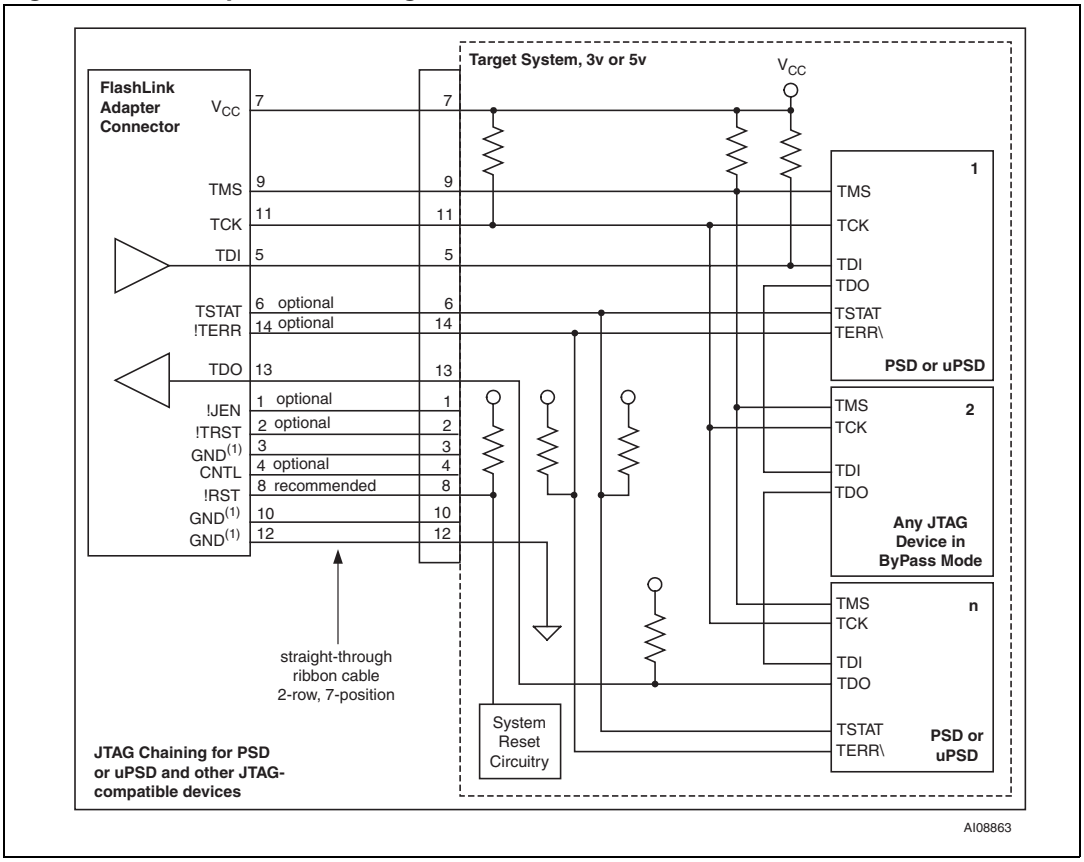
The IEEE-1149.1 specification allows chaining more than one device in a JTAG chain. uPSD and PSD devices may be included in this JTAG chain. However, PSDsoft Express will place devices from other vendors into BYPASS Mode, keeping them passive in the chain when programming uPSD and PSD devices. Conversely, when other vendors' JTAG control software is operating the JTAG chain, uPSD and PSD devices may be placed into BYPASS Mode. *Figure 6* shows an example of a JTAG chain with three devices, including a device from another manufacturer. This example also shows how to use 6-pin JTAG in a chaining situation.

Chaining must be configured in PSDsoft Express:

1. Click on the JTAG ISP box in the lower-left corner of the PSDsoft Express main flow diagram.
2. A pop-up dialog box will appear and ask how many devices are in the JTAG chain. If you click "More than one," you will go to the JTAG Operations window that allows you to define the number of devices in the chain as well as their position.

Note: If you do not see this dialog box (that asks how many devices are in the JTAG chain), pull down the "Preferences" menu of the main PSDsoft Express window and re-enable this option (question).

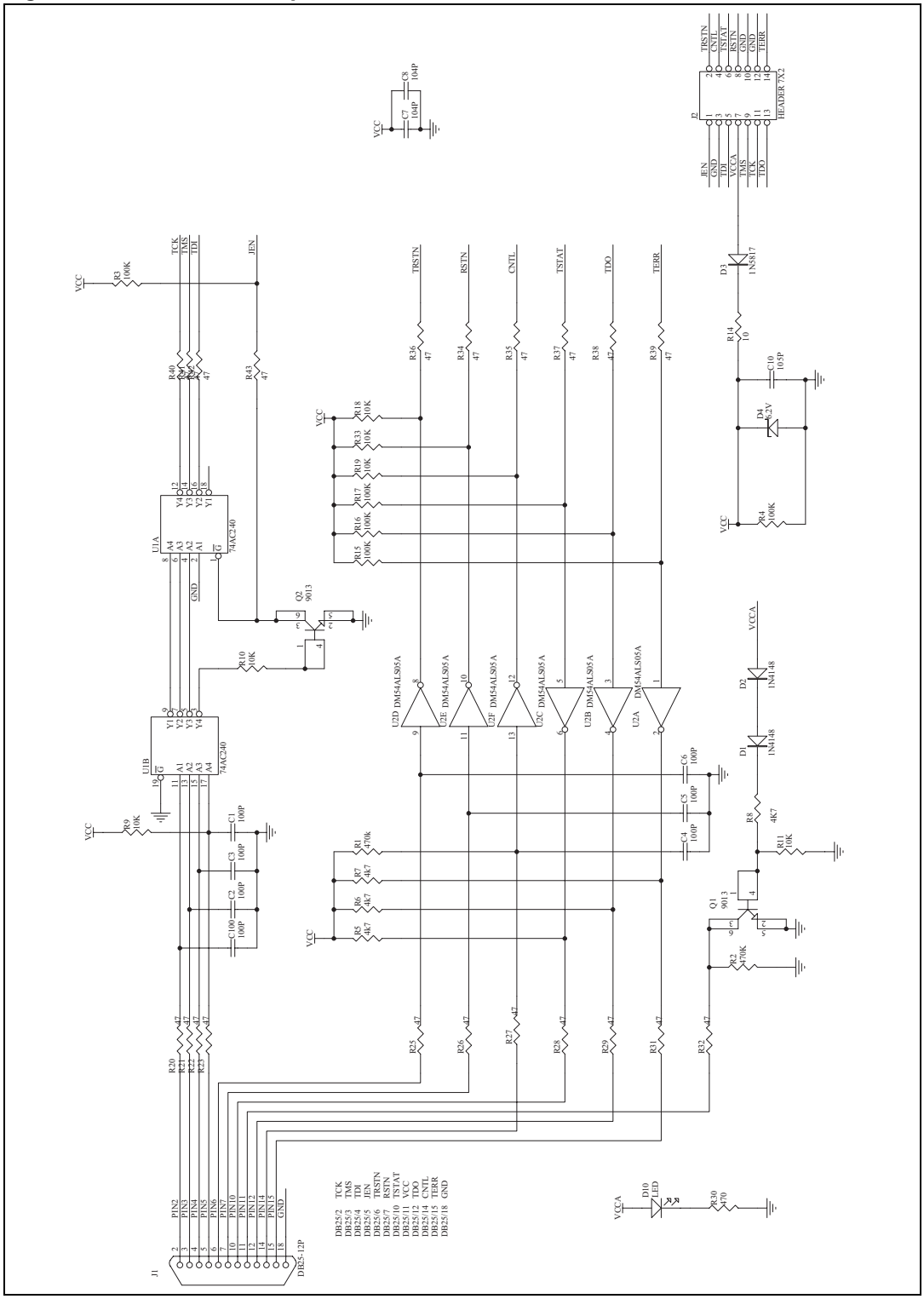
Figure 6. Example of Chaining JTAG Devices



Note: 1 All Ground pins are connected together inside the FlashLINK assembly.

Appendix A FlashLINK schematic

Figure 7. FlashLINK adaptor schematic



6 Contact information

For current information on ST Flash PSD and uPSD products, please consult our pages on the world wide web at www.st.com/psm

If you have questions or comments concerning the matters raised in this document, please send them to: the following email address:

apps.psd@st.com

Please include your name, company, location, and phone number.

7 Revision history

Table 2. Document revision history

Date	Revision	Changes
	1.0	First issue, written in WSI format
30-Jan-2002	1.1	Front page, and back two pages, in ST format, added to the PDF file Any references to Waferscale, WSI, EasyFLASH and PSDsoft 2000 updated to ST, ST, Flash+PSD and PSDsoft Express
13-Nov-2003	2.0	Reformatted
09-Mar-2004	3.0	Republished
06-Sep-2005	4.0	*Figure 3*, *Figure 4*, *Figure 5* updated by adding clearer JTAG connection labeling Notes associated with the above Figures renumbered *Figure 7* updated, connecting pin 13 to pin 8 for the DB25 connector
26-Jan-2007	5.0	Document reformatted *Figure 7* updated