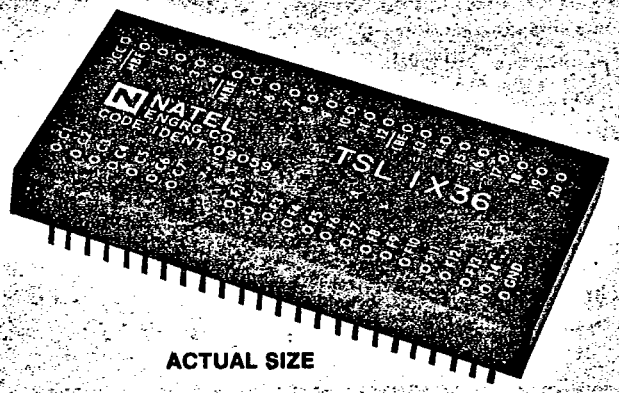
NATEL TSL 1X36

TWO Speed Synchro Data Processor 3-State 20-bit Data Output

Features

- **Small size**
  (1.3 x 2.6 x 0.35 inch)
- **High resolution**
  (20 bits)
- **High accuracy**
  (21 bits or ±½ LSB)
- **3-state output**
  (8 and 16-bit data-bus compatible)
- **36:1, 36:2, 18:1, 9:1 Ratios**
  (With same module)
- **No ambiguous output readings**
- **Fast parallel operation (250 ns)**
- **Automatic correction of misalignment between synchros**
  (up to ±90° of fine synchro)
- **Priced at $235/USA price**
  (TSL 1X36-1S)



ACTUAL SIZE

Applications

Ordnance control
Radar tracking
Navigation
High accuracy industrial control systems

Description

Model TSL 1X36 accepts 2 binary word inputs from two synchro (or resolver)-to-digital converters in a mechanically or electrically geared coarse/fine system and provides a single unambiguous 20-bit binary output representing the coarse shaft angle. A new feature provided in the TSL 1X36 is its 3-state output, available in three bytes, which allows it to be compatible with an 8-bit data-bus. With a resolution of 20 bits, the TSL 1X36 processor provides an accuracy of ± ½ LSB . . . a factor of 4 improvement over existing units such as Natel's TSL1036.

In addition to high accuracy and 3-state output, the processor is less than half the size of existing designs. In spite of its size, the processor is not a hybrid, rather it employs a different design approach that allows it to cut size without increasing cost.

Although the unit described in this data sheet provides for ratios of 36:1 and its binary multiples, processors for speed ratios of 2:1 thru 72:1 are available on special order.

The inputs to the TSL 1X36 are up to 14 bits from the fine converter and 7 bits from the coarse converter. The two-speed processor may be used with any synchro (or resolver)-to-digital converters that produce a parallel binary output.

When used with Natel Hybrid converters of the 1000 series, a complete 2-speed converter occupies less space than the original processor . . . (3.1 x 2.6 x .42"), while providing a 20-bit, 3-state output.

Two-speed System

A two-speed synchro (or resolver) system consists of two synchros geared electrically or mechanically to a single shaft. One synchro provides coarse positioning of the angle and the second synchro, through gearings, provides fine positioning of the angle and improves the resolution and accuracy of the system by a multiple equal to the gear ratio (less gearing errors).

In order to convert the shaft angle information into a single unambiguous digital word, the two-speed processor TSL 1X36, together with two synchro (or resolver)-to-digital converters is used. A coarse converter of very low accuracy and a fine converter of moderate accuracy together with the TSL 1X36 logic combiner provide a very high accuracy 2-speed conversion system. The TSL 1X36 processor can accept data from any type of synchro converter that provides parallel binary outputs. This includes all tracking, sampling types or multiplexed . . . hybrid or discrete converters (for information on synchro converters request the Natel Synchro Conversion catalog).

Correction for Misalignment error

In a 2-speed synchro system it is almost impossible to mechanically align the two synchros exactly. In addition there is a backlash error in the mechanical gearing of two synchros. These errors, called misalignment errors, are automatically corrected in the two-speed processor. The TSL 1X36 corrects misalignments of up to ± 90° of fine synchro shaft angle (±2.5° of coarse shaft angle for 36:1 system) by using the fine synchro converter input as the reference and continuously adjusting the data of the coarse synchro converter as required.

Theory of Operation

The operation of Model TSL 1X36 is illustrated in the block diagram of figure 1. The 7-bits of coarse digital word are multiplied by 36 to obtain coarse data rescaled to a binary multiple of the fine speed digital word. The 3 MSBs of fine speed data are compared with the corresponding bits of rescaled coarse data. If the two do not match the coarse data is modified to align it with the information contained in the fine data. The corrected coarse data together with 14-bits of fine data represent true angle free of any ambiguity or misalignment error. This data is divided by 36 to obtain the 20-bit digital word whose MSB is 180° and represents angular position of the coarse shaft of the two-speed system. This data is then supplied to three, independently controlled, 3-state buffers organized as a high byte of 4 MSBs, a middle byte of the next 8 bits and a low byte of 8 LSBs. Simultaneous parallel output of all 3 bytes is obtained by applying logic "0" (Ground) to the three enable control lines, $\overline{HBE}$, $\overline{MBE}$ and $\overline{LBE}$.

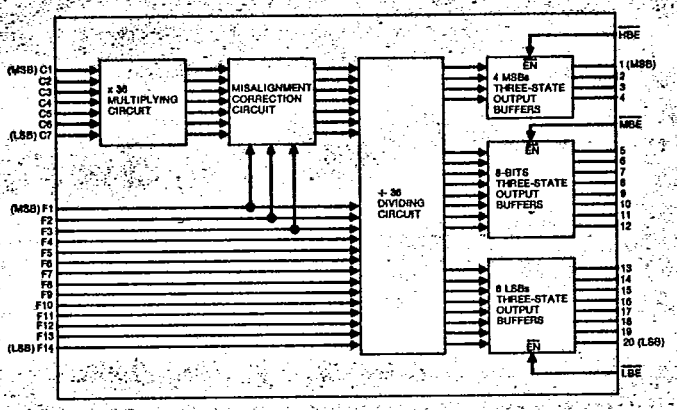


FIGURE 1 Block Diagram TSL 1X36

Specifications

PARAMETER	VALUE
Inputs	
Speed ratios	36:1, 16:1, 9:1
Fine speed input	Up to 14-bits parallel binary angle
Coarse speed input	Up to 7-bits parallel binary angle
Logic levels	DTL/TTL compatible (positive logic)
Loading	1 TTL load
Outputs	
Resolution	Up to 20-bits parallel Binary Angle
Accuracy	± ½ LSB
Logic levels	DTL/TTL compatible (positive logic)
Drive Capability	5 TTL loads
Three State Outputs	
Low level OFF state current (I_{LZ})	-100 μA MAX (V_O=0.5 V)
High level OFF state current (I_{HZ})	100 μA MAX (V_O=2.4 V)
Output short circuit current (I_{OS})	-50 mA typical
ENABLE CONTROLS ($\overline{HBE}$, $\overline{MBE}$, $\overline{LBE}$) Logic levels	DTL/TTL compatible
Loading	1 TTL load
Maximum mechanical misalignment between coarse and fine synchro	±90° of fine speed input (e.g., ±2.5° of coarse shaft for 36:1 System)
Conversion Time	250 ns typical, 320 ns max
Power Supply	
Voltage	5 V-dc ± 10%
Current	500 mA typical, 650 mA max
Physical Characteristics	
Size	2.625 x 1.325 x 0.35 inch (66.7 x 33.7 x 8.9 mm)
Weight	2 oz (56 gms) max

Absolute Maximum Ratings

Supply voltage ..... -0.5 V-dc to 7.0 V-dc
Input voltage ..... -1.0 V-dc to 5.5 V-dc
Input current ..... -10 mA to 5mA
Output current ..... -50 mA to 50 mA
Storage temperature ..... -55°C to +135°C

Pin Designations

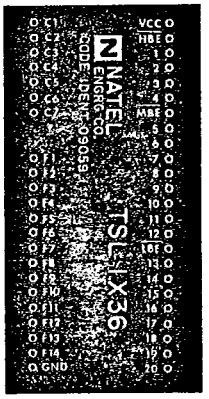


FIGURE 2 TSL 1X36 Pin Assignment

C1-C7	Coarse Angle Binary Input C1 is MSB, C7 is LSB
F1-F14	Fine Angle Binary Input F1 is MSB, F14 is LSB
GND	Power supply ground digital ground
5 V	Power supply voltage +5 V-dc
1-20	Combined Angle Binary Output 1=MSB, 20=LSB
$\overline{HBE}$	High Byte Enable ---- Output bits 1 through 4 are enabled (low impedance of 3-state output) when $\overline{HBE}$ is set to a logic "low." When $\overline{HBE}$ is set to a logic "high," the output bits 1 through 4 are disabled (high impedance state of 3-state output)
$\overline{MBE}$	Middle Byte Enable ---- A logic low on $\overline{MBE}$ enables output bits 5 through 12
$\overline{LBE}$	Low Byte Enable ---- A logic low on $\overline{LBE}$ enables output bits 13 through 20

Note: For simultaneous 20-bit parallel output $\overline{HBE}$, $\overline{MBE}$, and $\overline{LBE}$ should be connected to ground.

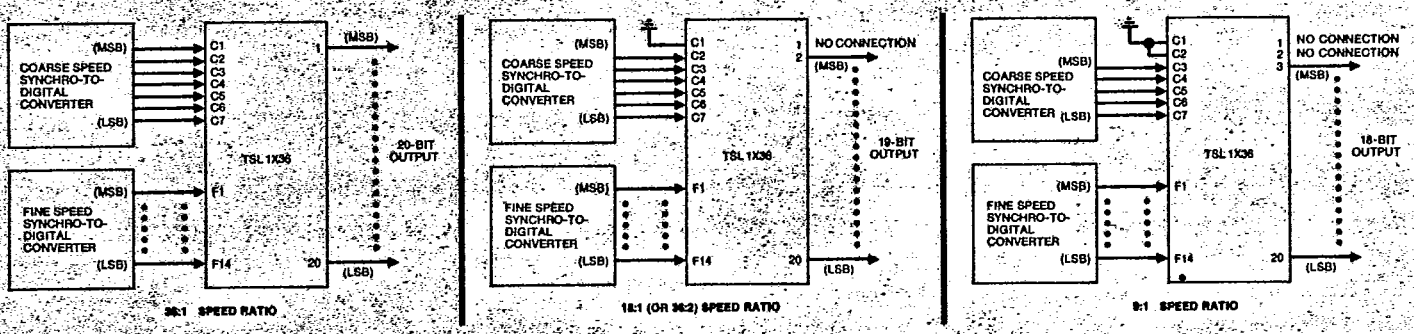


FIGURE 3 Connections for Different Speed Ratios

Input, Output Interface

Figure 3 shows input connections for different speed ratios. Note that for a speed ratio of 18:1 coarse input C1 is grounded and output MSB (180°) is the output labeled 2. For a speed ratio of 36:2, although input and output connections are same as that for 18:1, the MSB output (2) represents 90°. For a speed ratio of 9:1 inputs C1 and C2 are connected to ground and output bit 3 is the MSB (180°). For fine speed digital input of less than 14-bits unused LSB inputs must be connected to ground.

Depending upon the type of converters used -- sampling or tracking -- there are different methods of transferring data. The input data must be stable for the duration of conversion by the TSL 1X36.

The recommended method for data transfer from tracking converters is to combine converter busy outputs of both fine and coarse synchro converters with an OR gate to monitor when neither converter is updating. Apply an inhibit pulse to both converters simultaneously and when the data output from both converters is stable (as indicated by the combined busy output) transfer output data. The conversion time for the TSL 1X36 is 320 ns maximum.

Data transfer from sampling converters is accomplished by combining the DATA READY outputs of both fine and coarse synchro converters with an AND gate. When data is ready for both converters the input data may be transferred. If, instead of DATA READY, a CB (converter busy) signal is available, then an OR gate would be required to determine if the data is stable. For multiplexed systems storage registers would be required for fine and coarse data. Contact one of our applications engineers if you need assistance for your design.

OUTPUT DATA TRANSFER on an 8-bit data-bus is shown in figure 4. The timing diagram for data transfer is shown in figure 6. Access time and recovery time for enable controls is shown in the timing diagram of figure 5. The output data is available 320 ns after the input data is applied. When a logic low is applied to the enable controls, the corresponding data-bits are loaded on the 8-bit data bus. Enable control $\overline{LBE}$ transfers 8 LSBs, $\overline{MBE}$ transfers 8 middle data bits and $\overline{HBE}$ transfers 4 MSBs on the data bus.

Note that user should avoid having more than one register enabled on the bus at one time since the enabled outputs will deliver short circuit current into other enabled outputs wired together. While physical damage to the converter is unlikely, long-range affects of short circuit currents are unpredictable.

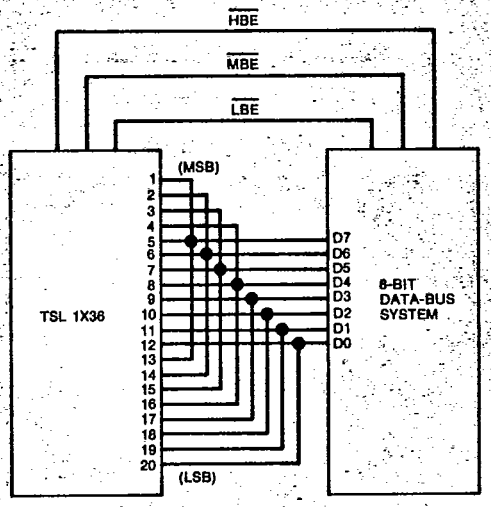


FIGURE 4 Output Connections for 8-Bit Data Bus

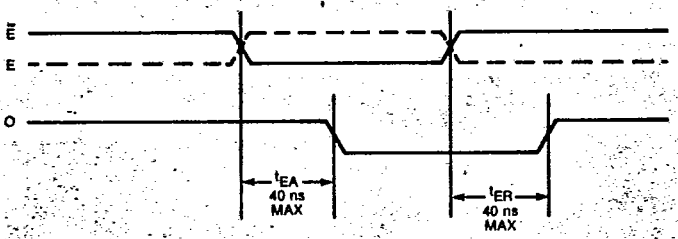


FIGURE 5 Enable Access Time and Recovery Time

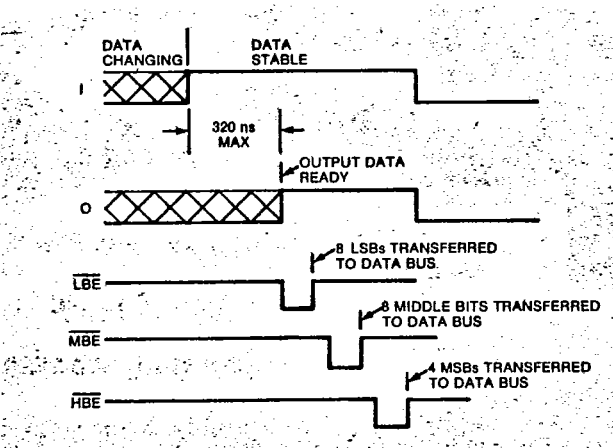
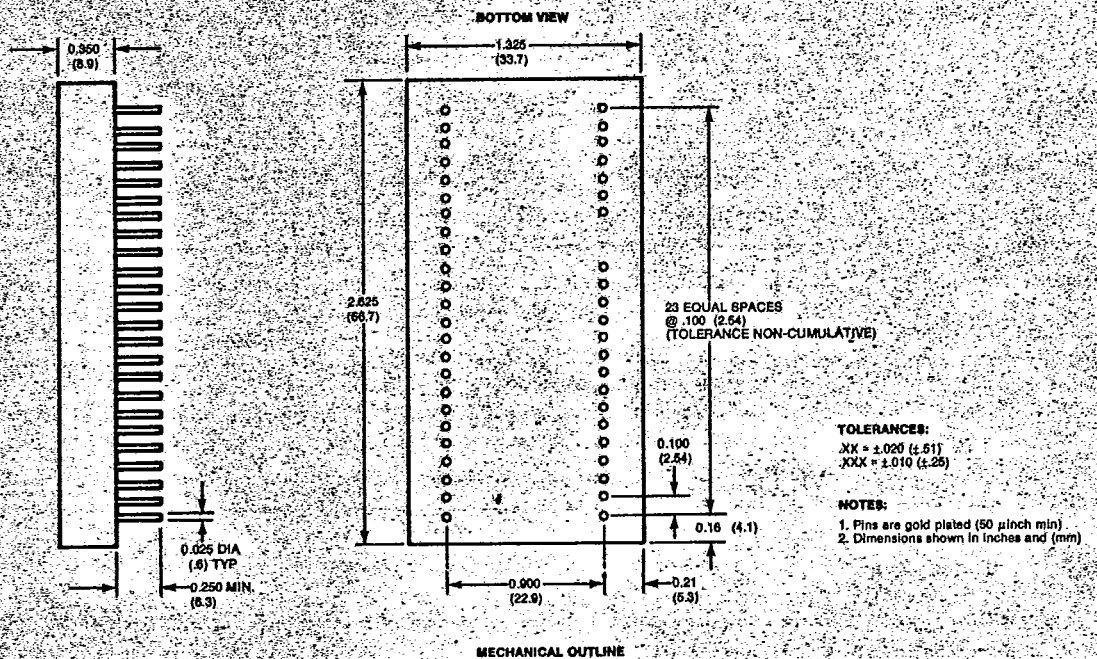


FIGURE 6 Data Transfer Timing Diagram



MECHANICAL OUTLINE

Ordering Information

TSL 1X36---T M

Temperature Range

1=0°C to 70°C
3=-55°C to +105°C

Mil - specification

S=standard
B=MIL-STD-883B
C=MIL-STD-883C

For speed ratios other than 36:1, contact factory for part number.

Other products available from NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10 to 16-bit resolutions (1000 series)
- Hybrid (36-pin DDIP size) Digital-to-Synchro (Resolver) converter with 14 and 16-bit resolutions (2000 series)
- Two-speed Synchro (Resolver)-to-Digital converters with 16 and 20-bit resolutions in a single package. (Models 2SD402 and 2SD412).
- Multiplexed Synchro (Resolver)-to-Digital converters.
- Solid State control transformers (SSCT) and differential transmitters (SCDX).
- Angle position indicators and synchro instrumentation for one-speed and multi-speed applications.
- High Power synchro/resolver drivers
- Code-converters.

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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Specifications subject to change without notice.