DRAM dual-ported controllers | 74F764-1/74F765-1

FEATURES

- Allows two microprocessors to access the same bank of dynamic RAM
- Performs arbitration, signal timing, address multiplexing and refresh
- 9 Address output pins allow direct control of up to 256K dynamic RAMs
- External address multiplexing enables control of 1Mbit (or greater) dynamic RAMs
- Separate refresh clock allows adjustable refresh timing
- 74F764-1 has an on-chip 18-bit address input latch
- 74F764-1/765-1 allow control of dynamic RAMs with row access times down to 40ns
- 74F764-1/765-1 output drivers designed for first reflected wave switching

DESCRIPTION

The 74F764-1/765-1 DRAM Dual-ported Controller is a high-speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F764-1 vs. 74F765-1

The 74F764-1, though functionally and pin-to-pin compatible with the 74F765-1, differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

The specialized outputs eliminate the need for signal terminations in essentially all applications.

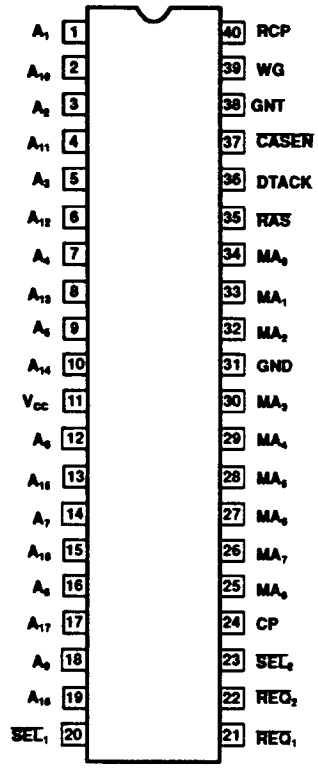
Both devices are available in 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

ORDERING INFORMATION

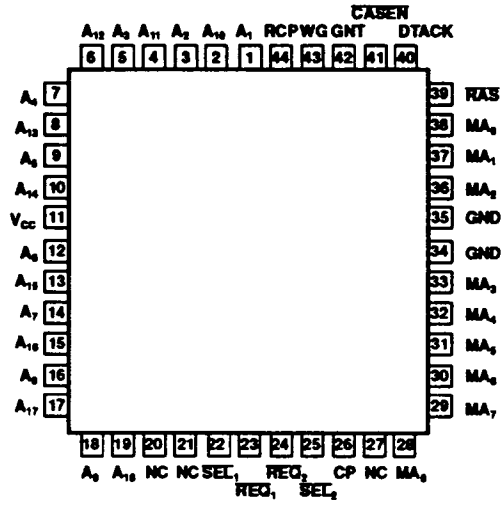
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%, T_A = 0°C to 70°C
Plastic Dip	74F764-1N, 74F765-1N
PLCC–44	74F764-1A, 74F765-1A

PIN CONFIGURATION

N Package

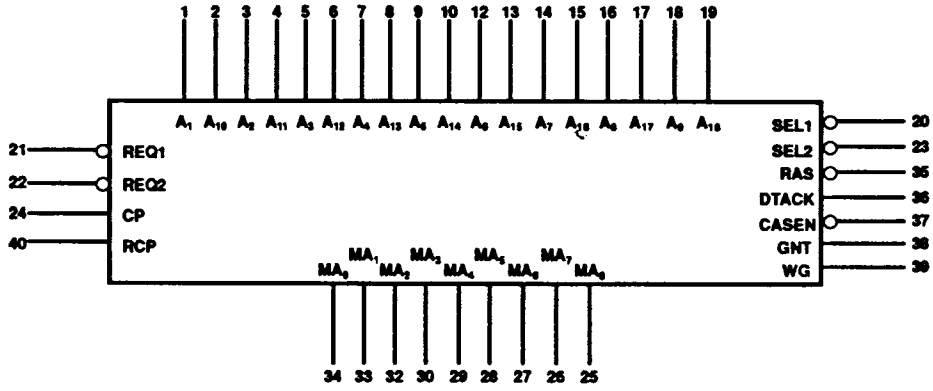


A Package



LOGIC SYMBOL

N Package



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A_1	1	1	I	Address inputs used to generate memory row address
A_2	3	3	I	
A_3	5	5	I	
A_4	7	7	I	
A_5	9	9	I	
A_6	12	12	I	
A_7	14	14	I	
A_8	16	16	I	
A_9	18	18	I	
A_{10}	2	2	I	Address inputs used to generate memory column address
A_{11}	4	4	I	
A_{12}	6	6	I	
A_{13}	8	8	I	
A_{14}	10	10	I	
A_{15}	13	13	I	
A_{16}	15	15	I	
A_{17}	17	17	I	
A_{18}	19	19	I	
$\overline{REQ}_1$	21	23	I	Memory access request from Microprocessor 1
$\overline{REQ}_2$	22	24	I	Memory access request from Microprocessor 2
CP	24	26	I	Clock input which determines the master timing
RCP	40	44	I	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	20	22	O	Select signal is activated in response to active $\overline{REQ}_1$ input, indicating selection of Microprocessor 1
V_{CC}	11	11		Power supply +5V ±10%
GND	31	34 35		Ground
$\overline{SEL}_2$	23	25	O	Select signal is activated in response to active $\overline{REQ}_2$ input, indicating selection of Microprocessor 2
MA_0	34	38	O	Memory address output pins, designed to drive address lines of the DRAM
MA_1	33	37	O	
MA_2	32	36	O	
MA_3	30	33	O	
MA_4	29	32	O	
MA_5	28	31	O	
MA_6	27	30	O	
MA_7	26	29	O	
MA_8	25	28	O	
GNT	38	42	O	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	35	39	O	Row Address Strobe, used to latch the row address into the bank of DRAM (to be connected directly to the $\overline{RAS}$ inputs of the DRAMs)
WG	39	43	O	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has been met

DRAM dual-ported controllers 74F764-1/74F765-1

ARCHITECTURE

The 74F764-1/765-1 DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 74F764-1/765-1 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on different edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figures 1 and 2).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock for the 74F764-1/765-1 should be equal to:

(Tras(of the DRAM) + 22 – 10)/4ns plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until after the completion of the refresh cycle (see Figures 8 and 9).

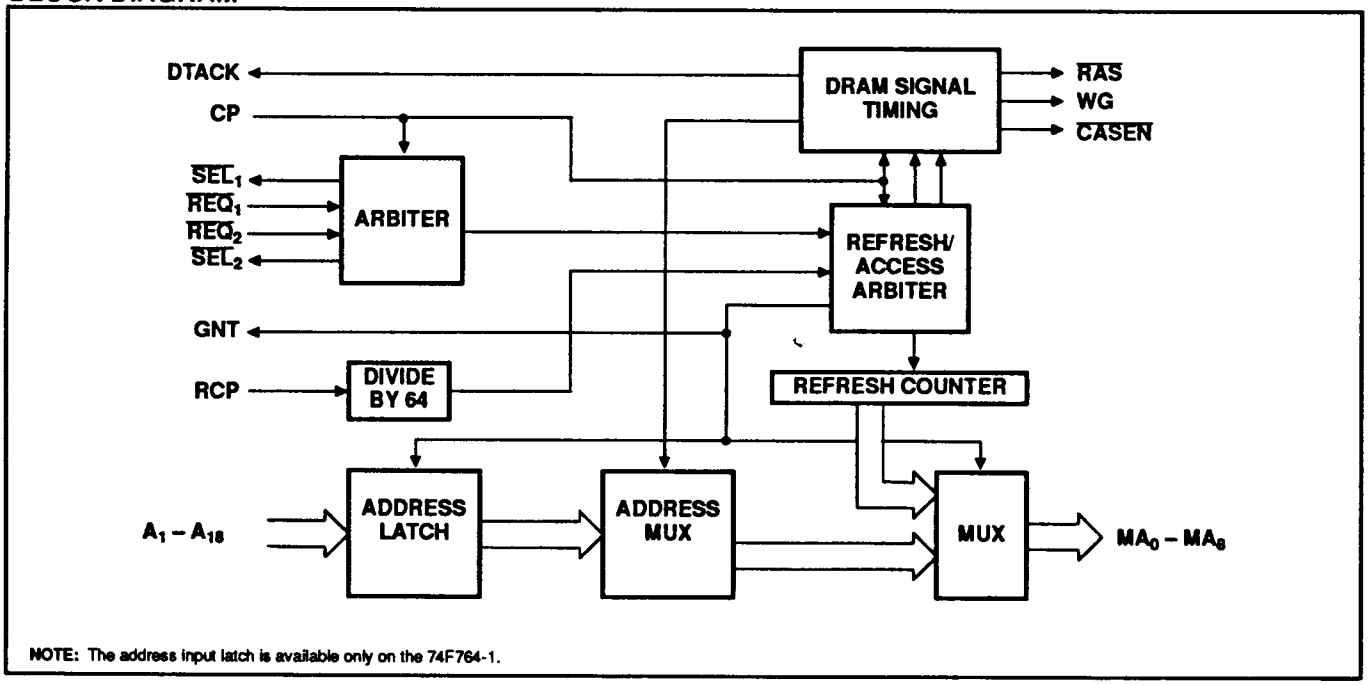
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the toher processor is performing an access cycle. This will ensure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If however, there were any pending refresh requests, assertion of the GNT output will be held OFF until the refresh request has been serviced.

When GNT goes High, the A_1–A_{18} address inputs to the 74F764-1/765-1 are latched internally and the A_1–A_9 signals are propagated to the MA0–MA8 outputs. The address inputs are not latched by the 74F765-1 and therefore, A_1–A_9 inputs propagate directly to the MA_0–MA_8 outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



NOTE: The address input latch is available only on the 74F764-1.

One half-clock cycle later, the A10–A18 latch outputs on the 74F764/764A or A10–A18 inputs to the 74F765/765A are selected and propagated to the MA0–MA8 outputs (refer to Figures 1 and 2). The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the A_{10}–A_{18} signals to propagate and stablize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with Higher-order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$ is valid, the controller will wait for 2 $^1/_2$ clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycels. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

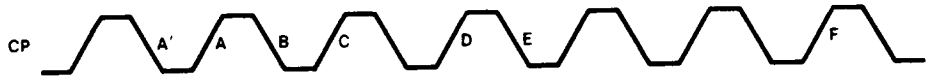
All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input High. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 9 refresh counter address signals to the MA0–MA8 outputs. After a half-clock cycle the RAS output is asserted for four cycles and then negated for three clock cycles to meet the RAS precharge requirements of the DRAMS (see Figures 4 and 5).

A' $\overline{REQ}_2$ sampled
A $\overline{REQ}_1$ sampled ($\overline{REQ}_2$ disabled by $\overline{SEL}_1$ circuitry)
$\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry)
B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs
C $\overline{RAS}$ triggered
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on the F764-1

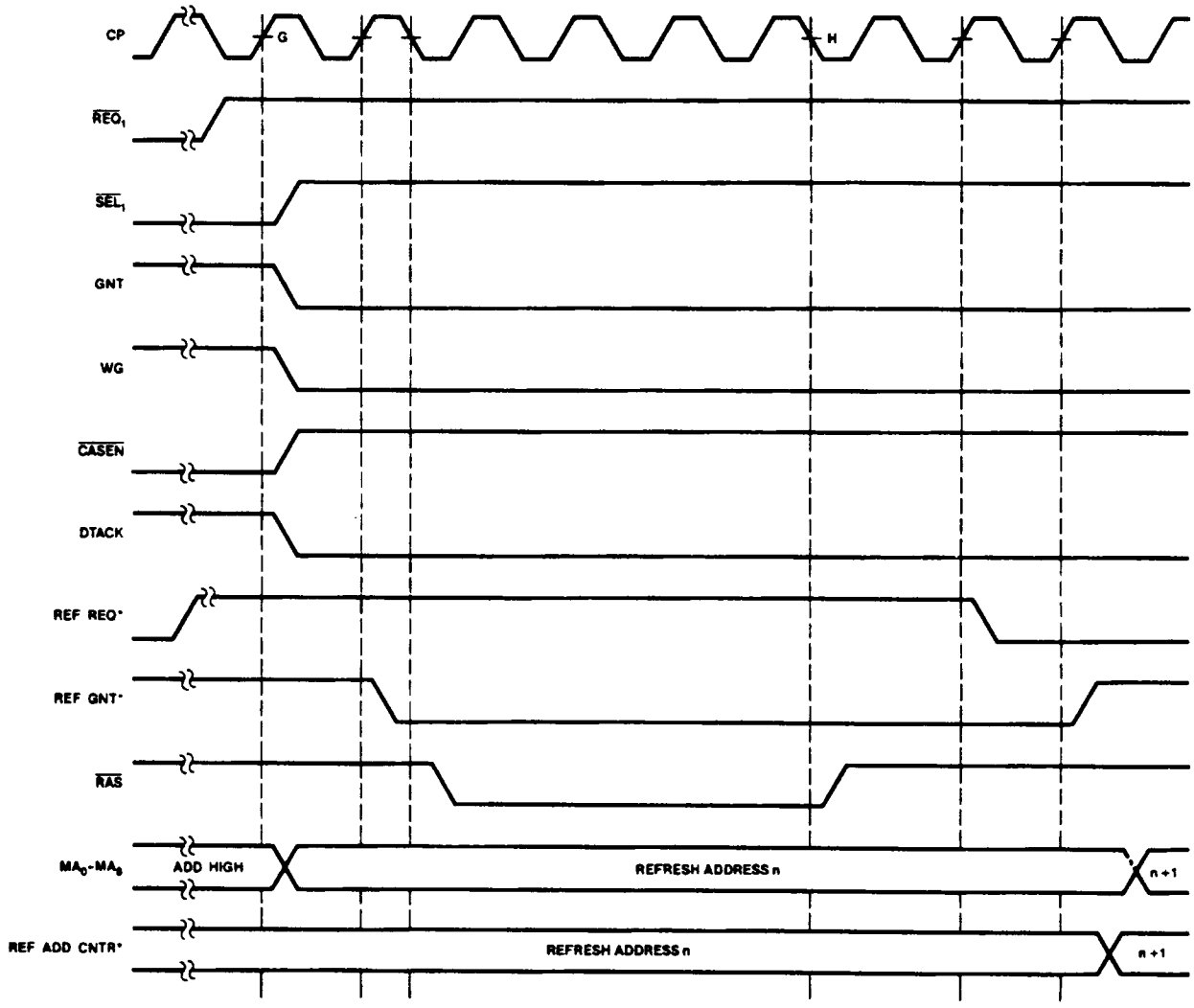
Figure 1. Sequence of Events for $\overline{REQ}_1$ Memory Access Cycle for 74F764-1/765-1



A' $\overline{REQ}_2$ sampled
$\overline{SEL}_2$ triggered ($\overline{SEL}_2$ triggered by $\overline{REQ}_2$ sampling circuitry)
A $\overline{REQ}_1$ is not sampled (disabled by $\overline{SEL}_2$ circuitry)
B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs
C $\overline{RAS}$ triggered
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on the F764-1

Figure 2. Sequence of Events for $\overline{REQ}_2$ Memory Access Cycle for 74F764-1/765-1



NOTE:
* These are internal signals only.

Figure 3. Refresh Cycle Timing following a $\overline{REQ}_1$ Memory Access Cycle for All Devices

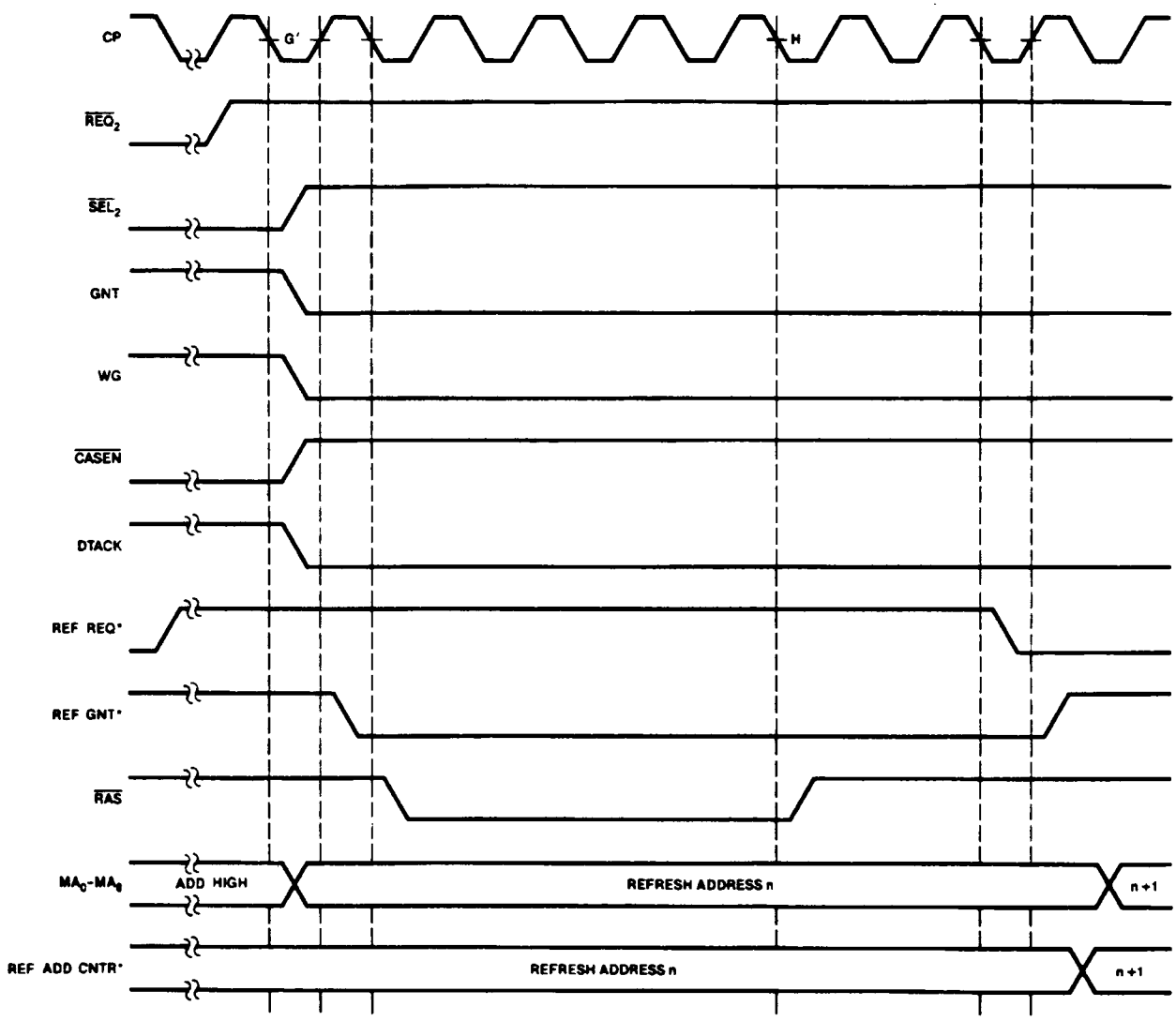


Figure 4. Refresh Cycle Timing following a $\overline{REQ_2}$ Memory Access Cycle for All Devices

USING THE 74F764-1/765-1 TO ADDRESS 1MBIT DRAMs

The addressing capabilites of the DRAM dual-ported controllers can be extedned to address 1Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 5 shows an application, using an external 2-to-1 multiplexer to address 1Mbit dynamic RAMs. The 9-bit internal refresh counter of the controller provides 512 row addresses which more than meet the refreshing needs for most industry standard 1Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 512 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 512 row addresses.

The WG output of the controller should be used to multiplex between the external row and column address bits. However, it is important that the propagation delay through the external mulitplexer does not cause column address setup violations on the dynamic RAM.

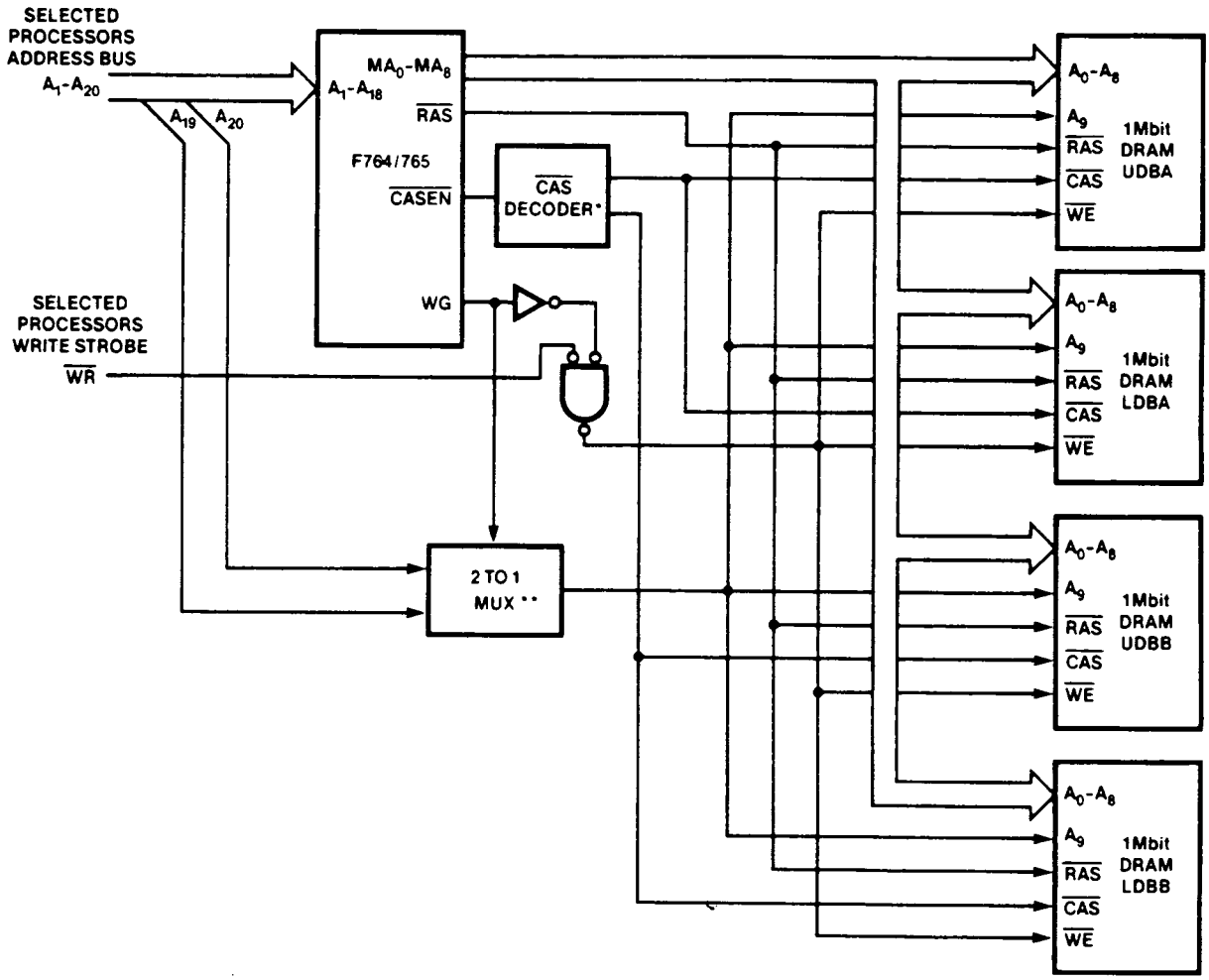


Figure 5. Using the Controller to Address 1Mbit DRAMs

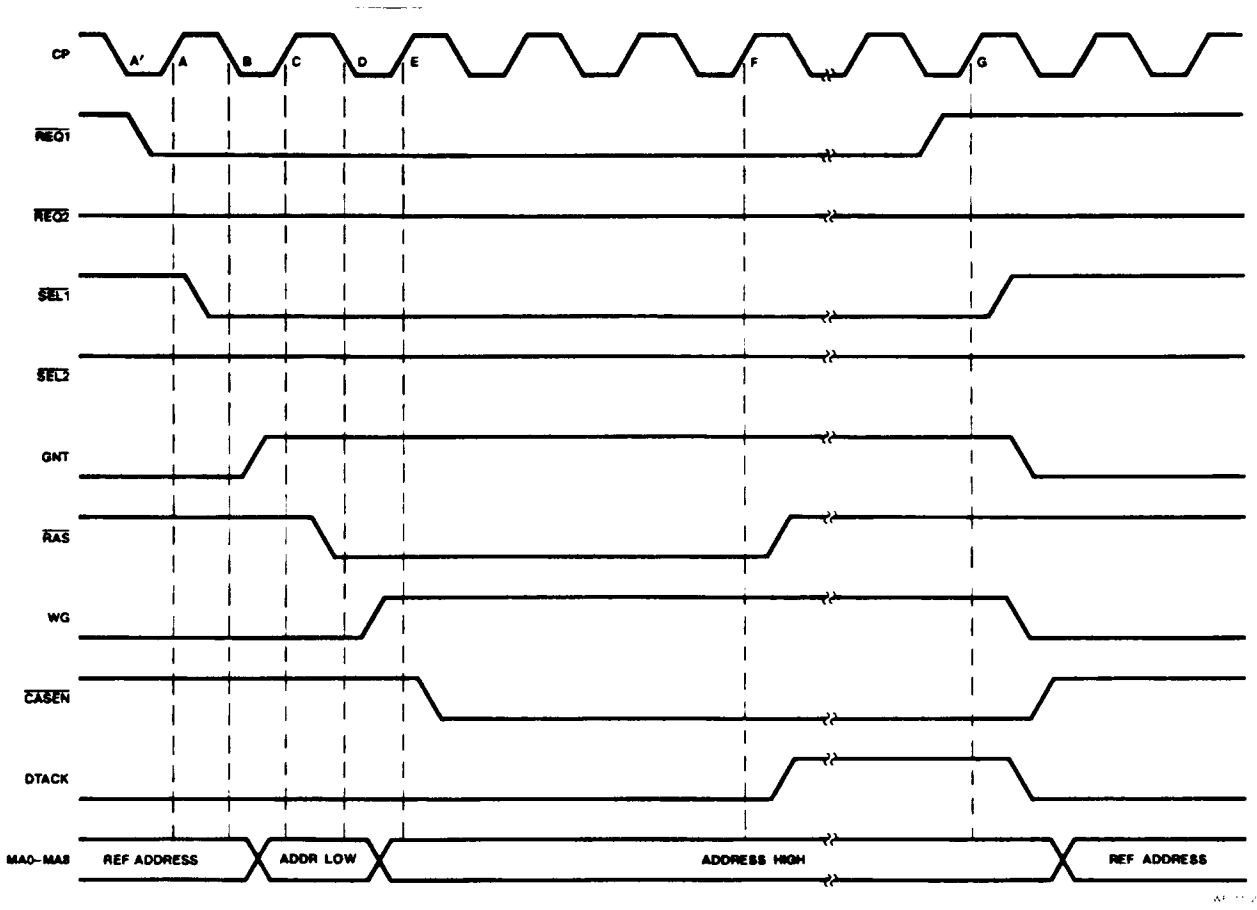


Figure 6. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for 74F764-1/765-1

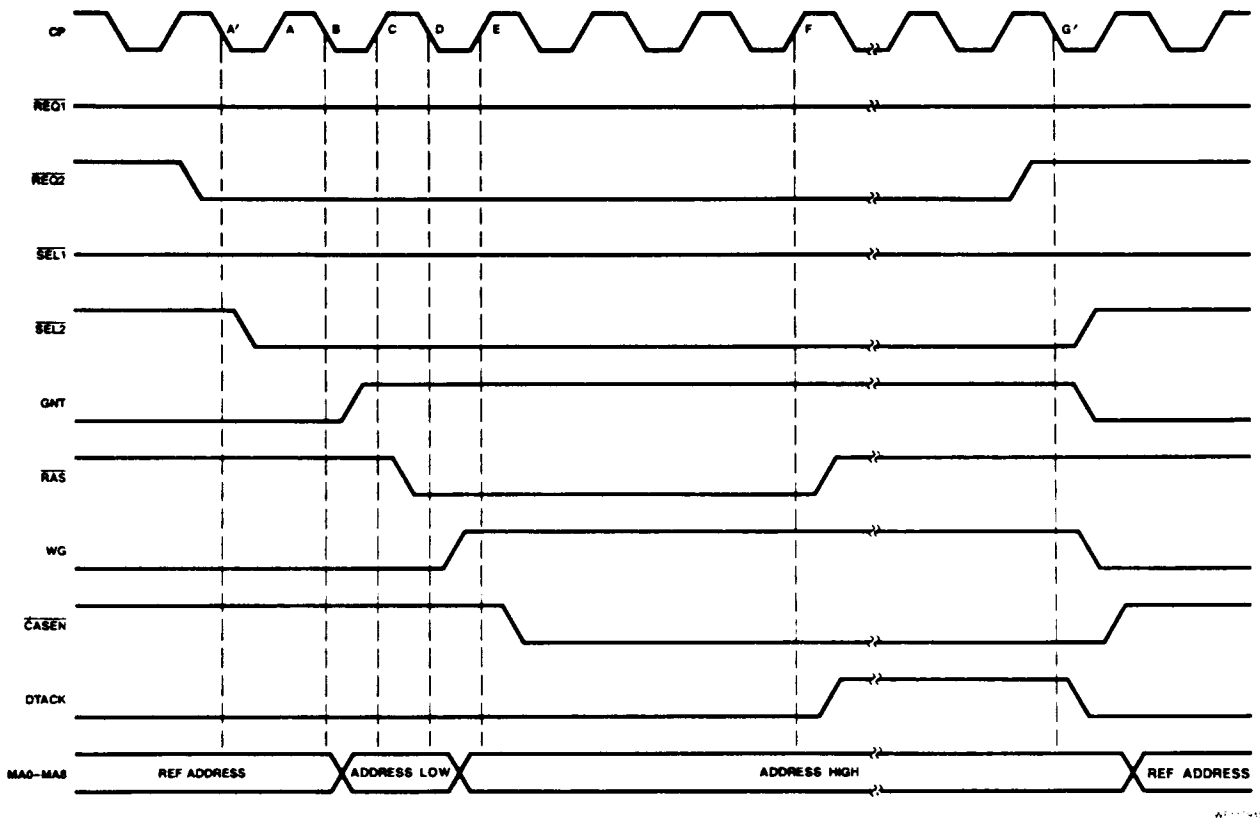


Figure 7. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing for 74F764-1/765-1

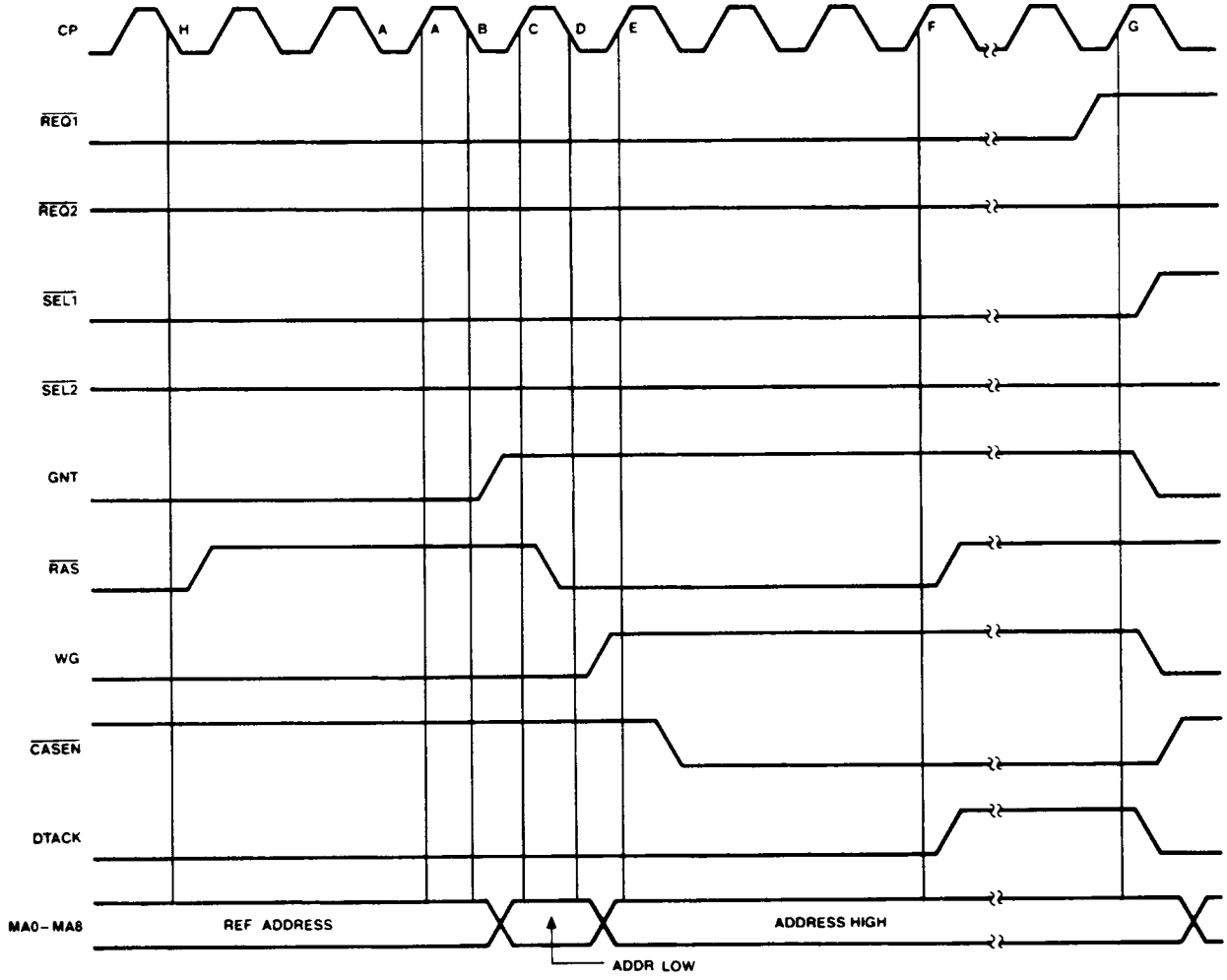


Figure 8. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing following a Refresh Cycle for 74F764-1/765-1

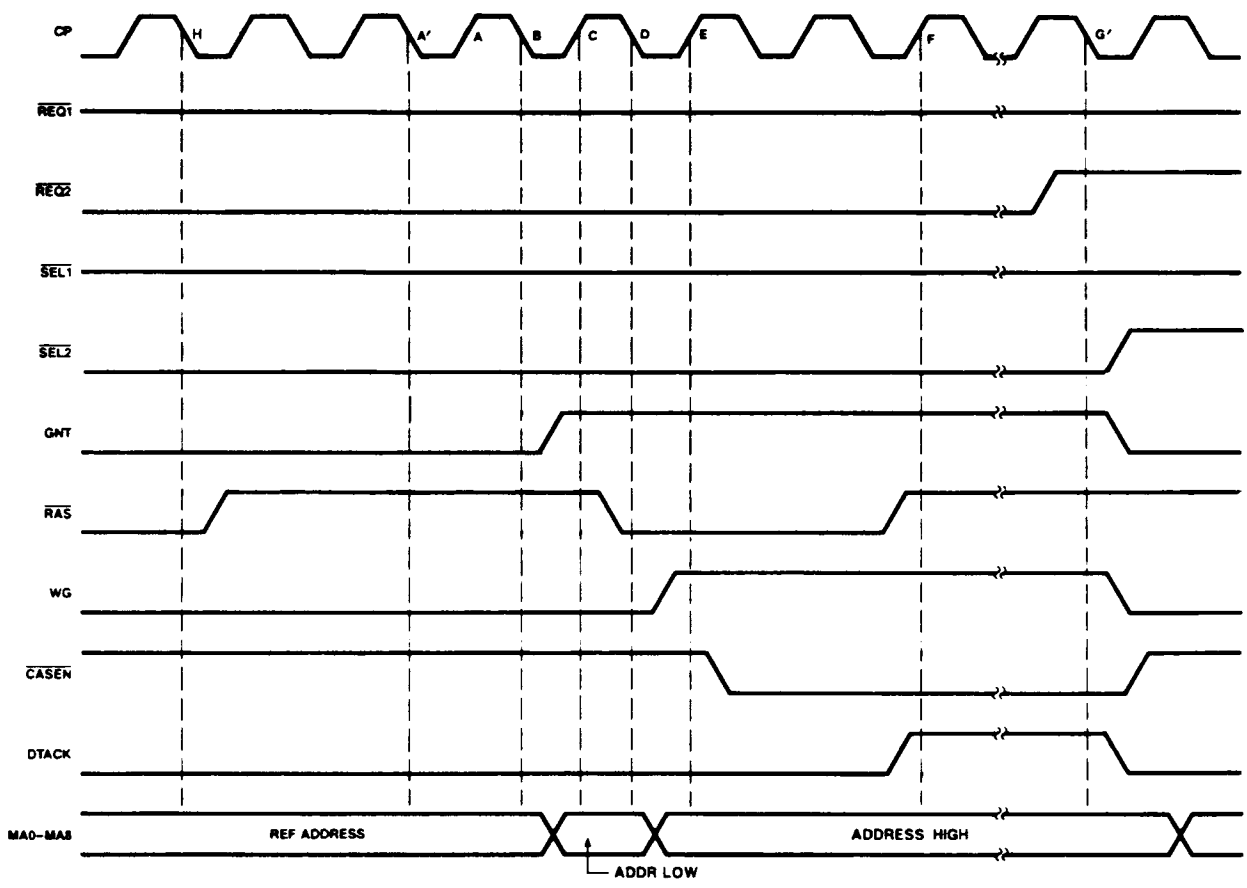


Figure 9. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing following a Refresh Cycle for 74F764-1/765-1

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the oprating free-air temperature range.)

SYMBOL	PARAMETER	74F764-1/765-1	UNIT
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_{IN}	Input Voltage	-0.5 to +7.0	V
I_{IN}	Input Current	-30 to +5	mA
V_{OUT}	Voltage applied to Output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to Output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764-1/765-1			UNIT
		MIN	NORM	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	High-level Input Voltage	2.0			V
V_{IL}	Low-level Input Voltage			0.8	V
I_{IK}	Input Clamp Current			-18	mA
I_{OH}	High-level Output Current[3]			-20	mA
I_{OL}	Low-level Output Current[3]			8	mA
T_A	Operating free-air temperature range				°C

NOTE:
3. Transient currents will exceed these values in actual operation.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F764-1/765-1			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -20mA	±10% V_{CC}	2.4	2.70		V
					±5% V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 8mA	±10% V_{CC}		0.30	0.50	V
					±5% V_{CC}		0.30	0.50	V
V_{OL2}[3]	Low-level output voltage			I_{OL2}[3] =75mA	±5% V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.7	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.2	-0.6	mA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX			-80	-150	-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	165	mA
		I_{CCL}					125	170	mA

NOTES:
1. For the conditions shown as MIN or MAX, use the appropriate value under the recommended oprating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of hihg-speed test appartus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		T_A = +25°C, V_{CC} = +5.0V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 300pF, R_L = 70Ω		
		MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	100	150		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL_1}$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL_1}$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(G') to $\overline{SEL_2}$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A') to $\overline{SEL_2}$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(B) to GNT	9	12	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to GNT	20	23	26	17	28	ns
t_{PLH}	Propagation delay CP(B) to MA(row address)	11	14	17	10	19	ns
t_{PHL}		14	18	22	13	24	
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	11	14	16	10	18	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	13	17	20	12	22	ns
t_{PLH}	Propagation delay CP(D) to WG	9	11	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to WG	20	23	26	19	26	ns
t_{PLH}	Propagation delay CP(D) to MA(column address)	12	14	17	11	19	ns
t_{PHL}		14	18	21	13	23	
t_{PLH}	Propagation delay CP(G or G') to $\overline{CASEN}$	14	17	20	12	22	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	14	16	19	13	21	ns
t_{PLH}	Propagation delay CP(F) to DTACK	10	12	15	9	17	ns
t_{PHL}	Propagation delay CP(G or G') to DTACK	20	23	26	19	28	ns
	74F765-1 Only						
t_{PLH}	Propagation delay $A_1 - A_{18}$ to $MA_0 - MA_8$	9	11	14	8	16	ns
t_{PHL}		9	12	15	8	17	

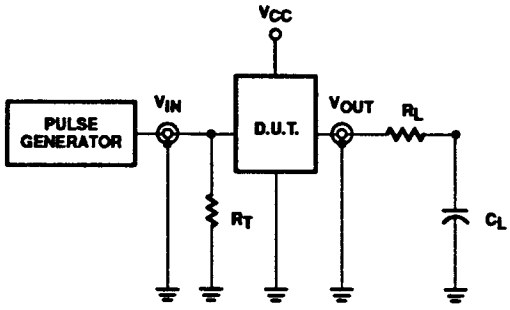
AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		T_A = +25°C, V_{CC} = +5.0V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 300pF, R_L = 70Ω		
		MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ_1}$, $\overline{REQ_2}$ to CP	3	1		4		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ_1}$, $\overline{REQ_2}$	2	0		3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5	3		5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	5			5		ns
	74F764-1 Only						
$t_s(H)$ $t_s(L)$	Setup time, High or Low $A_1 - A_{18}$ to CP (↓)	0	-1[1]		1		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP (↓) to $A_1 - A_{18}$	5	3		6		ns

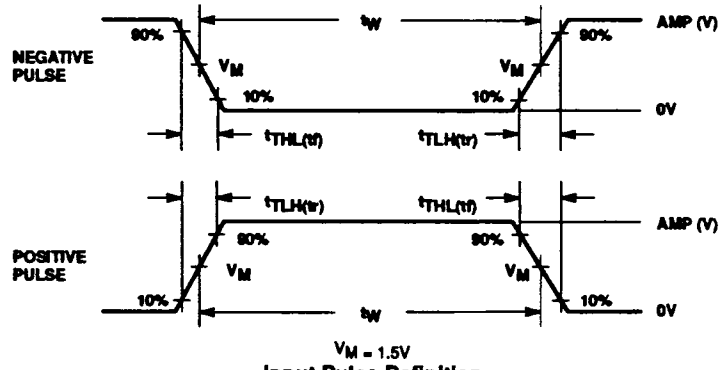
NOTE:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 1ns after the falling edge of the CP clock. It is suggested that $\overline{SEL_2}$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL_1}$ to enable Address Bus 1. This will ensure that setup time for Address Bus 1 is not violated.

TEST CIRCUIT AND WAVEFORMS FOR ALL DEVICES



Test Circuit for Simulating RAM Boards



Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	T_W	T_{TLH}	T_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:
R_L = Load resistor to GND, see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

APPLICATIONS

The DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 10 shows a 68000 processor sharing a 64K × 8 (two banks each consisting of sixteen 16K × 1 devices) memory with a Z-80 processor. Since neither Z-80 nor 68000 have multiplexed address and data bus, the 74F765-1 is appropriate.

Since the Z-80 has an 8-bit wide data bus, data buffers are used to convert the 16-bit memory data bus to an 8-bit wide processor bus. Address bit (A_0) from the Z-80 serves as an enable to one of the two data buffers at a given time. Address bit (A15) from either the Z-80 or the 68000 distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

When the Z-80 is selected and A_{15} is a zero, all even bytes will be accessed from UDBA and all odd bytes from LDBA. Similarly, when A_{15} is a one, UDBB will contain all even bytes and LDBB all odd bytes.

For 68000, Upper and Lower Data Strobes ($\overline{UDS}$ and $\overline{LDS}$) determine whether a byte or word transfer will take place. The $\overline{WAIT}$ input on the Z-80 is asserted when $\overline{REQ}_1$ is generated, and is negated when the GNT output is asserted by the controller. The additional gating circuitry is to ensure that $\overline{DTACK}$ to the 68000 is asserted only when it is selected.

Figure 11 shows two 8086 processors sharing 1MByte (two banks each consisting of sixteen 256K × 1 devices) of dynamic RAM. Using 74F764 in this application may eliminate the need for an external address latch.

Similarly, Figure 12 shows two 68020 processors sharing the same amount of memory.

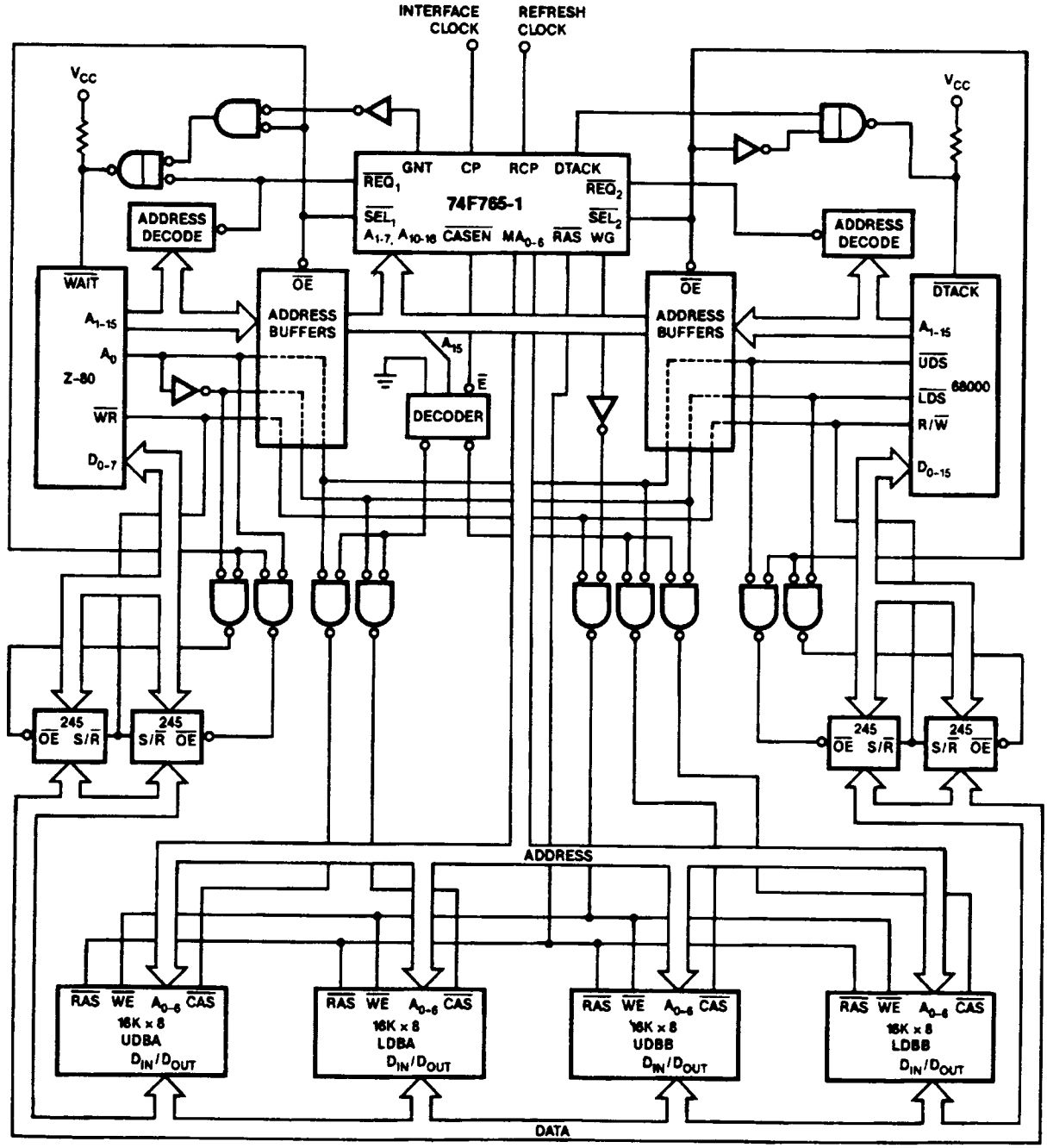
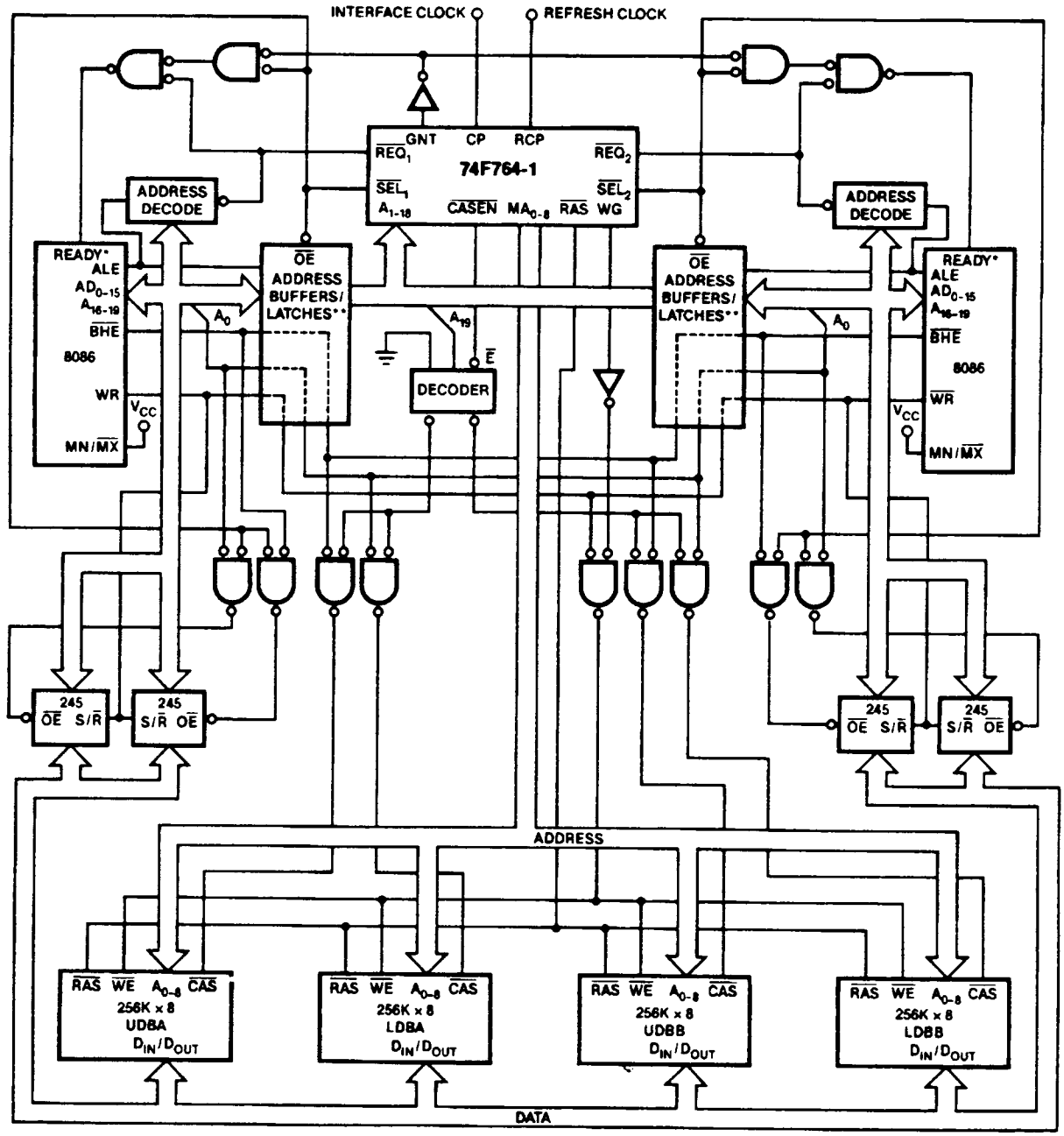


Figure 10. A 68000 Processor sharing 64K × 8 DRAM with a Z-80



* It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet
** Whether or not the 8086 address bus needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller

Figure 11. Two 8086 Processors sharing 1MByte of DRAM

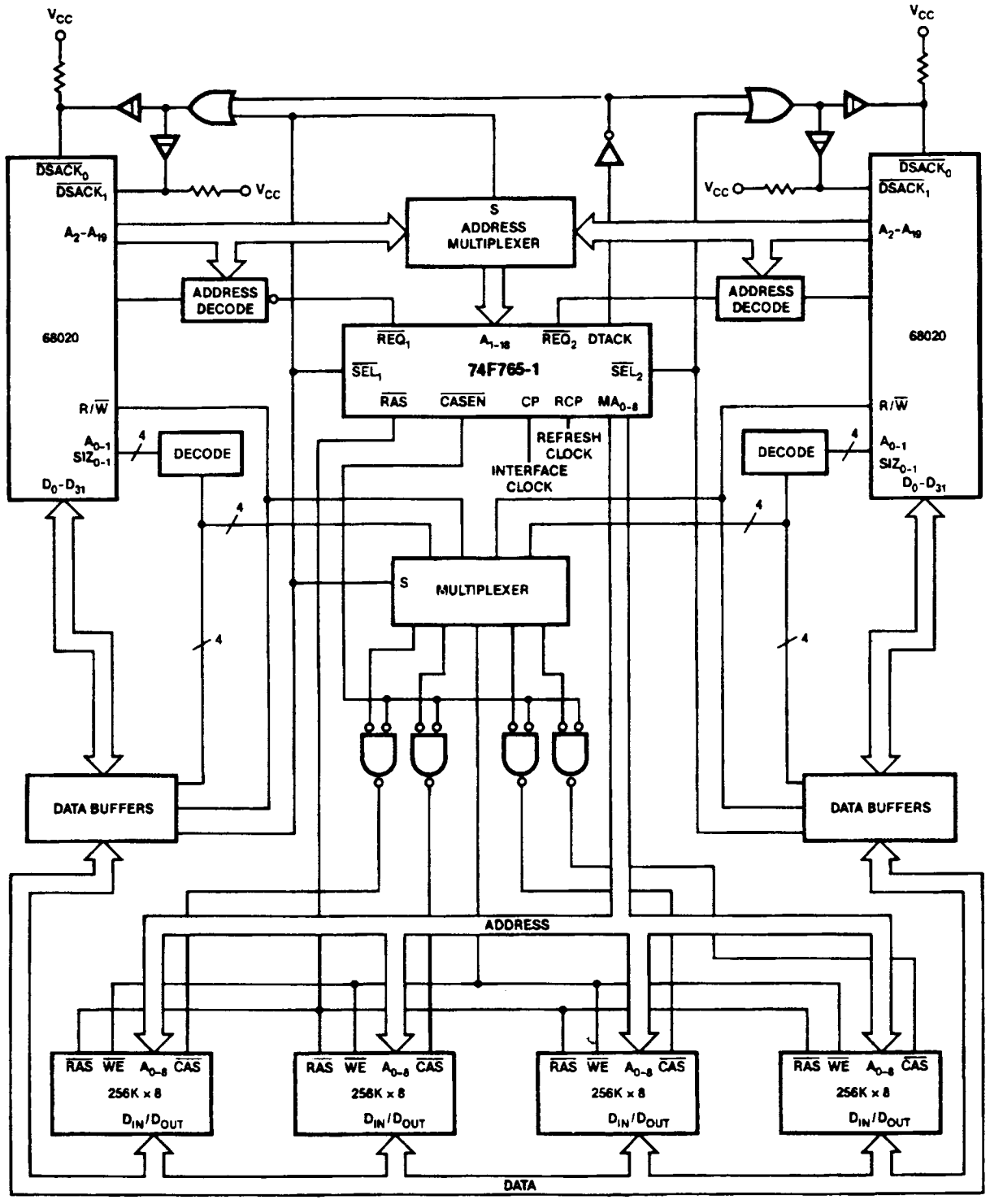


Figure 12. Two 68020 Processors sharing 1MByte of DRAM

74F764-1 FAMILY LINE DRIVING CHARACTERISTICS

The 74F764-1/765-1 are designed to provide first reflected wave switching with as wide a range of characteristic impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP-housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4 volts and must be pulled down to 0.8 volts or less on the incident wave, the DRAM controller output must sink (4-0.8)/70A or 46mA at 0.8 volts. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady state operation at these currents may result in electromigration).

Figures 13 and 14 show the output I/V characteristics of the DRAM controller family of devices. These figures also demonstrate a graphical method for determining the first reflected wave characteristics of the devices.

When driving any type of memory arrays with the 74F764-1/765-1, the schottky diode termination shown in Figure 15 can be used (most of these will need no termination at all).

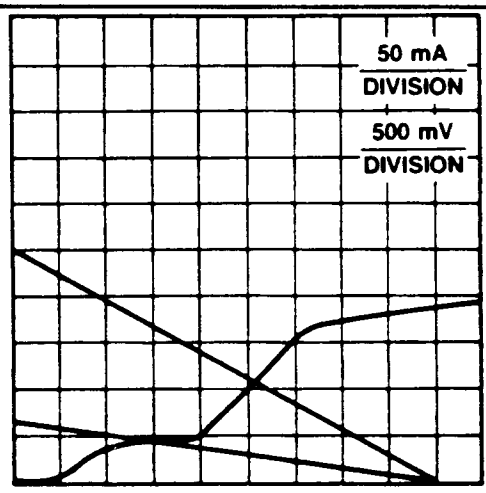


Figure 13. I-V Output characteristics of the 74F764-1 and 765-1 in the Low State. Any unterminated line impedance between 18Ω and 70Ω (both shown) will typically switch on the first reflected wave without violating the -1V minimum input voltage specification typical of DRAMs.

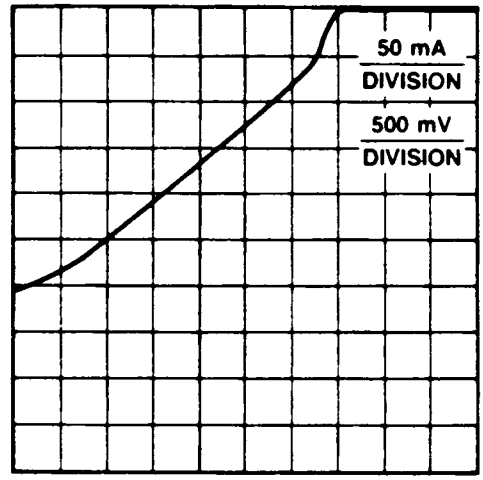


Figure 14. I-V Output characteristics of the 74F764-1 and 765-1 while in the High state.

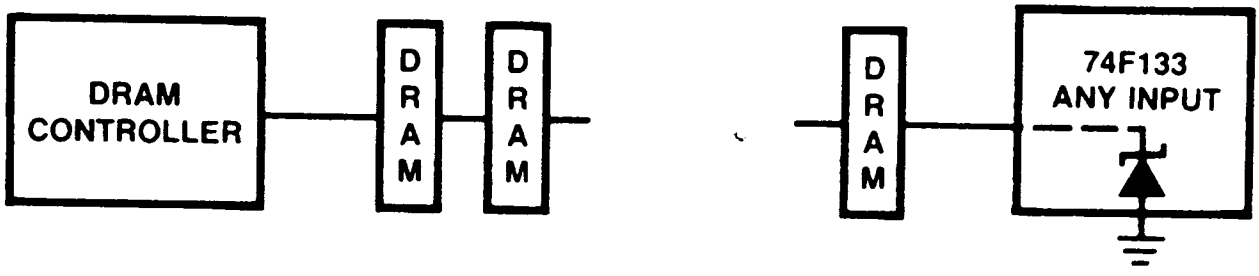


Figure 15.